

LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

FEATURES

DIRECT REPLACEMENT FOR SILICONIX PAD SERIES

REVERSE BREAKDOWN VOLTAGE $BV_R \geq -30V$

REVERSE CAPACITANCE $C_{RSS} \leq 2.0pF$

ABSOLUTE MAXIMUM RATINGS¹

@ 25 °C (unless otherwise stated)

Maximum Temperatures

Storage Temperature -55 to +150 °C

Operating Junction Temperature -55 to +150 °C

Maximum Power Dissipation

Continuous Power Dissipation (PAD) 300mW

Continuous Power Dissipation (J/SSTPAD) 350mW

Maximum Currents

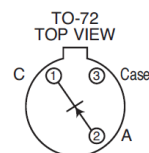
Forward Current (PAD) 50mA

Forward Current (J/SSTPAD) 10mA

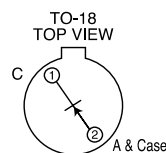
PAD SERIES

PICO AMPERE DIODES

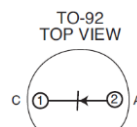
PAD1,2,5



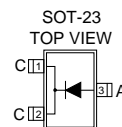
PAD50



JPAD



SSTPAD



COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	ALL PAD	-45			V	$I_R = -1\mu A$
		ALL SSTPAD	-30				
		ALL JPAD	-35				
V_F	Forward Voltage			0.8	1.5		$I_F = 5mA$
C_{RSS}	Total Reverse Capacitance	PAD1,5		0.5	0.8	pF	$V_R = -5V, f = 1MHz$
		All Others		1.5	2		

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		PAD	JPAD	SSTPAD	UNITS	CONDITIONS
I_R	Maximum Reverse Leakage Current	PAD1	-1			pA	$V_R = -20V$
		PAD2	-2				
		(SST/J)PAD5	-5	-5	-5		
		(SST/J)PAD10	-10	-10	-10		
		(SST/J)PAD20	-20	-20	-20		
		(SST/J)PAD50	-50	-50	-50		
		(SST/J)PAD100	-100	-100			
		(SST/J)PAD200		-200			
		(SST/J)PAD500		-500			

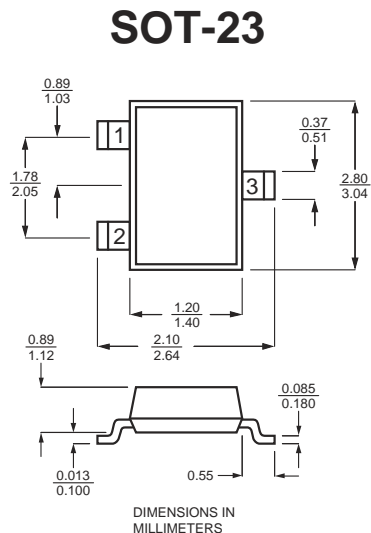
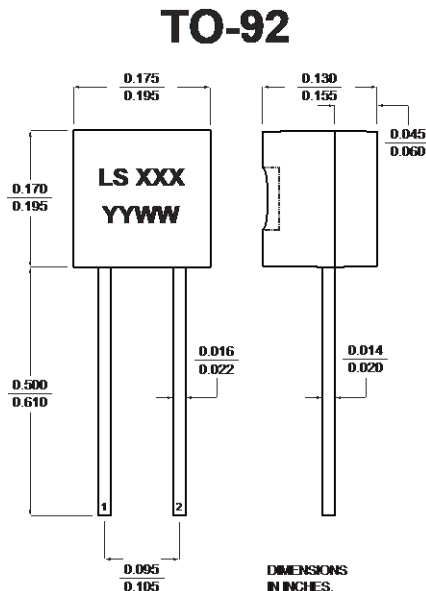
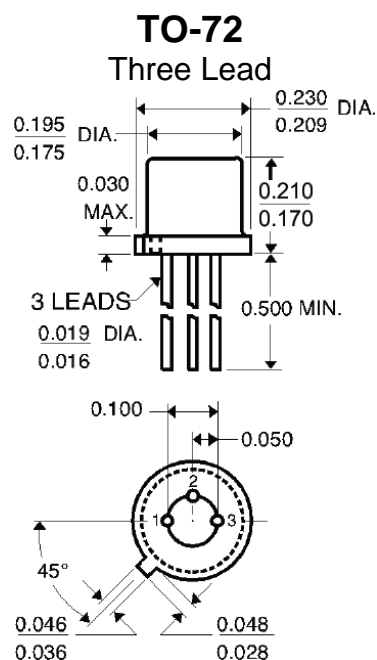
1. Derate 2mW/°C above 25°C

2. Derate 2.8mW/°C above 25°C

Input Differential Voltage limited to 0.8V (typ) by JPADs D₁ and D₂. Common Mode Input voltage limited by JPADs D₃ and D₄ to ± 15 V.

Typical Sample and Hold circuit with clipping. JPAD diodes reduce offset voltages fed capacitively from the JFET switch gate.

The circuit diagram shows a two-stage op-amp precision rectifier. The first stage is a voltage follower where the input e_{in} is connected to the non-inverting input of an op-amp. The op-amp's output is connected to the gate of a 2N4393 JFET, whose source is grounded and drain is connected back to the op-amp output. The JFET's drain is also connected to the non-inverting input of a second op-amp. The second op-amp's inverting input is connected to a network of two diodes (JPAD5 D1 and D2) and a capacitor C. D1 is anode-to-output, cathode-to-inverting input. D2 is anode-to-inverting input, cathode-to-output. The output of the second op-amp is connected to the base of a 2N4117A BJT. The BJT's emitter is grounded, and its collector is connected to a load resistor R, with the output voltage V_{OUT} taken across R. The BJT is biased by a +V supply.



1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The PAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.

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Mouser Electronics

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