iND83212
Datasheet
Rev 0.97

1 REVISION HISTORY

Table 1 Revision History

Rev #	Date	Action
0.1	12/30/2021	Initial Release
0.2	01/17/2022	Updated PINOUT
0.3	05/20/2022	Updated pinout/diagram/package
0.4	09/13/2022	Updated register map
0.5	09/19/2022	Add section “IO Capture”
0.6	10/13/2022	1. Updated the power mode descriptions. 2. Added sections for individual registers in Register Descriptions.
0.7	10/26/2022	1. Updated Current Ranges of Deepsleep and Hibernate modes 2. Added 9.1.1 Power on sequence
0.8	11/16/2022	1. Added DFN14 Package Outline in 6.2.1 2. Added DFN14 Pin description in 6.3
0.9	12/05/2022	Modify Computational Formula of PWM period and pulse width in 9.2.6
0.91	02/09/2023	1. Updated DFN14 package’s pins description by replacing 1V5 with NC 2. Added the GPIO3/GPIO4 to table of ABSOLUTE MAXIMUM RATINGS
0.92	02/17/2023	1. Add description section of auxiliary PWM 2. Add description section of GPIO 3. Fix wrong pin name on Pin 17 of QFN-20 package
0.93	04/24/2023	1. Add dimension brief description in 6.2.1.2 2. Split pin descriptions of QFN20 package and DFN14 package 3. Fix wrong LED pin number on DFN-14 package 4. Apply new part number rule, enable ordering code iND83212-D14 5. Add ordering information for iND83212-D14
0.94	06/16/2023	1. Update clock electrical characteristics 2. Update ADC electrical characteristics
0.95	09/18/2023	Add MSL level of package
0.96	09/26/2023	1. Add notes for the GPIO count for iND83212-Q20 and iND83212-D14 2. Remove LIN switch related content which is not available for iND83212
0.97	10/27/2023	Updated the description of 8.2.18.11 TRIM

2 TABLE OF CONTENTS

3 LIST OF TABLES

4 LIST OF FIGURES

Figure of Contents

5 ORDERING INFORMATION

Part number	Ordering Code	Package	MSL	Shipping
iND83212	iND83212-Q20	QFN20	Level 1	4000pcs/Tape&Reel
	iND83212-D14	DFN14	Level 1	4000pcs/Tape&Reel

Table 2 Ordering Information

6 SYSTEM OVERVIEW

"iND83212" IC is an automotive LED lighting integrated device that combines together a 32bit MCU (Cortex M0) with a power management unit capable of handling 45V Load dump from the car battery, 3 high voltage constant current open drain IO with PWM, a LIN slave, an integrated 12 bit ADC for monitoring, aging and temperature compensation purpose.

- Full automotive qualification AEC-Q100 Grade1
- Functional Safety Enhancements:
  - Hardware LIN TX monitor to prevent a dominant bus caused by internal malfunction
  - LIN Bus Idle timeout monitor
    - Always active, even the chip is in hibernate mode
    - For preventing a fast discharge of the car battery, if a short to ground is detected, the following options are available
      - Automatically switch off LIN slave's pullup.
    - Auto-recovery if the failure condition disappears
- CPU architecture:
  - ARM Cortex-M0 processor
  - SysTick Timer (24bits, interruptible)
  - Serial Wire Debug port (SWD)
  - Built-in Nested Vectored Interrupt Controller (NVIC)
  - Programmable Watch-Dog Timer
  - 3 programmable timers
- Memory:
  - 64kBytes of Flash Program Memory, 10 years retention in automotive environment
  - 16kBytes of SRAM
- Peripherals/Digital Features
  - Clock and Reset Manager
    - Two internal clock resources:
      - Trimmable 256KHz Auxiliary ROSC mode supports more flexible/accurate LIN wakeup filtering. Auxiliary system clock frequency is 256KHz/16.

- Trimmable 16MHz ROSC with SSC support
- Reset Sources:
  - POR and BOR (no external reset)
  - SW Triggers: Hard/Soft

- Power Management
  - Active Mode
  - CPU Sleep Mode
    - Triggered by Cortex-M0 WFI instruction
    - Wakeup Resources: Interrupts/Exceptions
  - DeepSleep Mode
    - ASIC power-on
    - MCU power-off
    - Wakeup Resources: GPIOs/LINS/Wakeup Timer
  - Hibernate Mode
    - ASIC 5V domain power-on
    - ASIC 1.5V domain power-off
    - MCU power-off
    - Wakeup Resources: Only LINS
- One SAE J2602/LIN2.2 LIN Slave Controller and Transceiver
- Watch dog timer (ASIC side) with window mode support
- 3x16bits PWM required to control LED current driver:
  - Common prescaler and 16bit timer
  - Support power balance with independent rise/fall timing configuration
- Up to 4 General Purpose IOs*
  - Dual edges detection interrupt supported
  - PWM mode supported
  - Input capture supported

- Peripherals/Analog Features
  - 3 Programmable 60mA max constant current / high voltage IO open drain
  - PN voltage measurement for temp compensation

        - Integrated a dedicated 2.5mA current source
        - Fully differential measurement
    - Temperature Sensor/Monitor with ADC
    - Battery voltage detection and monitoring
    - Hardware over temperature protection
    - 12-bit SAR ADC with 16channels
        - Bandgap Reference
        - Accurate VBAT Channel
        - Junction Temperature
        - Analog Input from GPIO x 4*
        - Analog Input from LED x 3
        - Forward Voltage of External LED x 3
        - VDD1V5/VDD3V3/VDDPRE5V
    - Integrated voltage regulators
        - LDO 3.3V
            - Output
            - ASIC Core and IO supply
            - MCU I/O
        - LDO 1.5V
            - Output
            - MCU core

Note:
1. GPIO4 is not available for iND83212-D14

6.1 BLOCK DIAGRAM

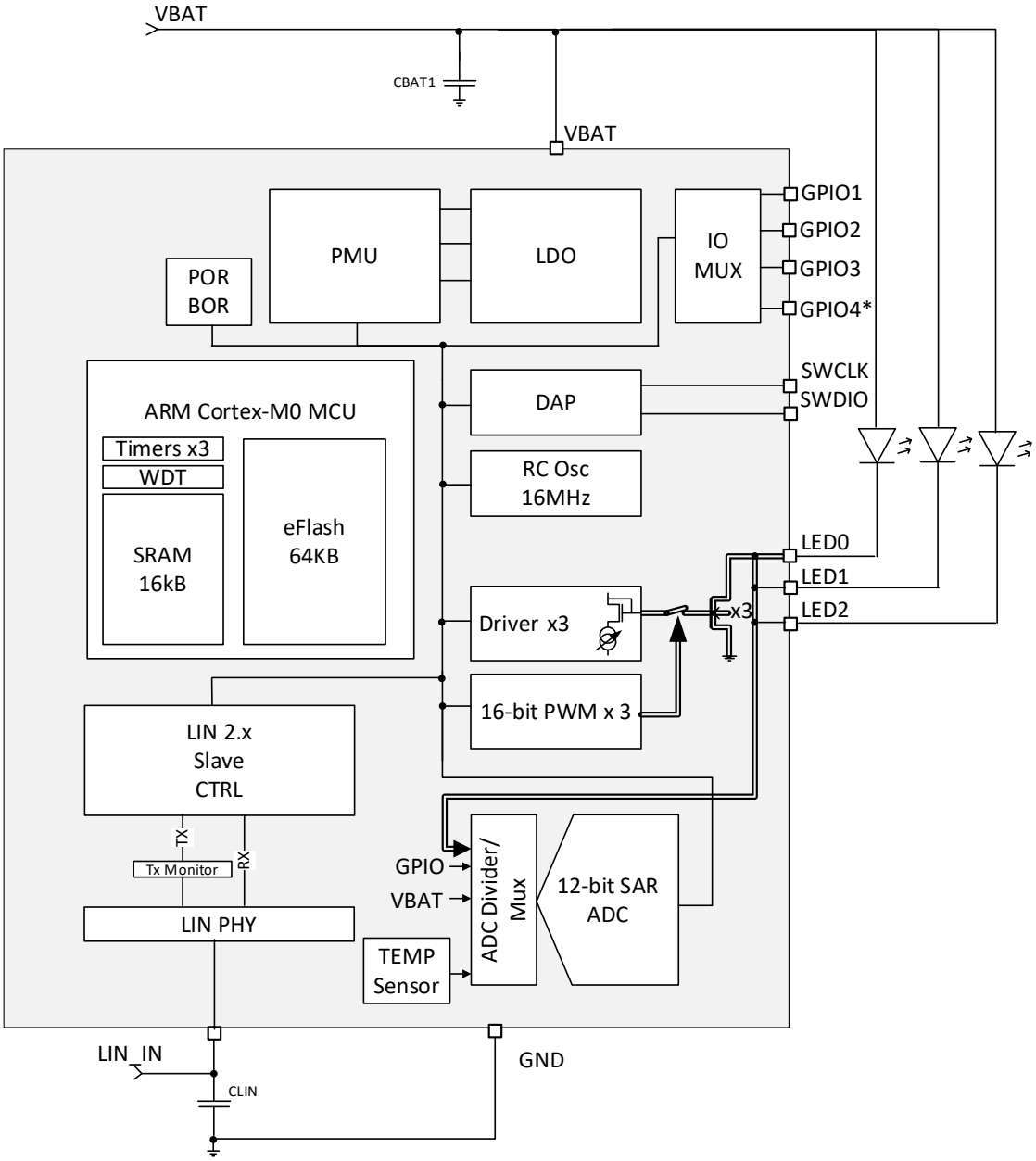

Figure 1 IC block diagram

Note:

1. The application block diagram does not include components used to qualify the system against ISO7637-2/-3
2. Only 3 GPIOs are available on iND83212-D14 device without GPIO4

6.2 Package Overview and Pin Description

6.2.1 Package Outline

6.2.1.1 iND83212-Q20

iND83212-Q20, QFN20, 4x4 mm body size, 0.5 mm lead pitch.

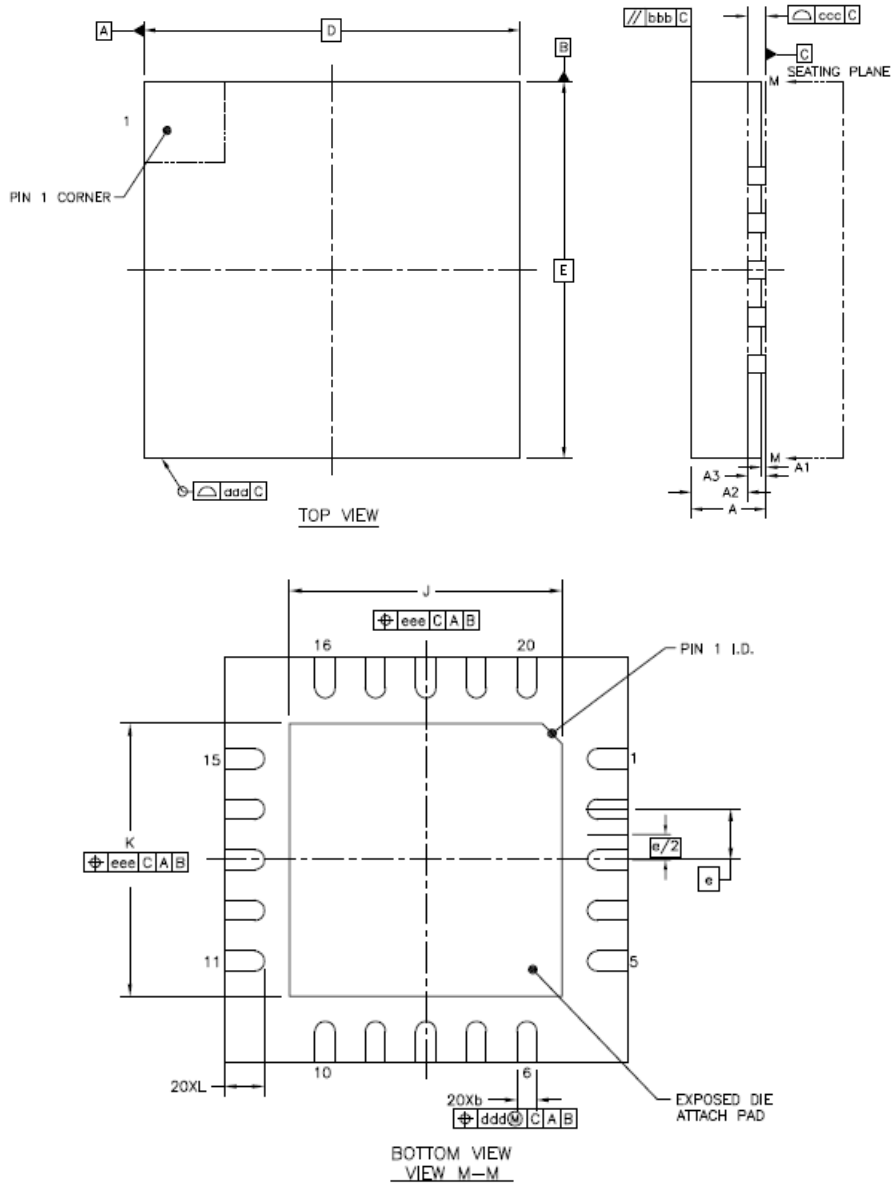

Figure 2 Package Outline

DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	—	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.20	0.25	0.30
BODY SIZE	X	D	3.95	4.00	4.05
	Y	E	3.95	4.00	4.05
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D1	2.65	2.70	2.75
	Y	E1	2.65	2.70	2.75
LEAD LENGTH		L	0.35	0.40	0.45
LEAD EDGE TO PKG EDGE		Z	0.875 REF		
Tolerance of form and position					
PACKAGE EDGE TOLERANCE	aaa	0.1			
MOLD FLATNESS	bbb	0.1			
COPLANARITY	ccc	0.08			
LEAD OFFSET	ddd	0.1			
EXPOSED PAD OFFSET	eee	0.1			

Table 3 QFN20 package dimension

6.2.1.2 iND83212-D14

iND83212-D14, DFN14, 3x3 mm body size, 0.4 mm lead pitch.

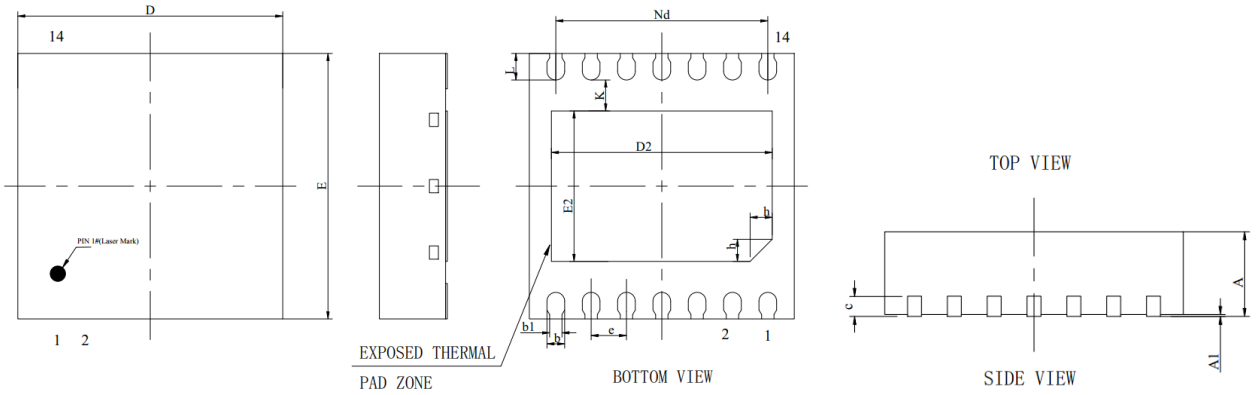

Figure 3 Package Outline

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0. 05
b	0. 15	0.20	0.25
b1	0.14REF		
c	0.203REF		
D	2. 90	3. 00	3. 10
D2	2. 40	2. 50	2. 60
e	0. 40BSC		
Nd	2. 40BSC		
E	2. 90	3. 00	3. 10
E2	1. 60	1. 70	1. 80
L	0. 25	0.30	0. 35
h	0. 20	0. 25	0. 30
K	0.35REF		

Table 4 DFN14 package dimension

6.2.2 Package Branding

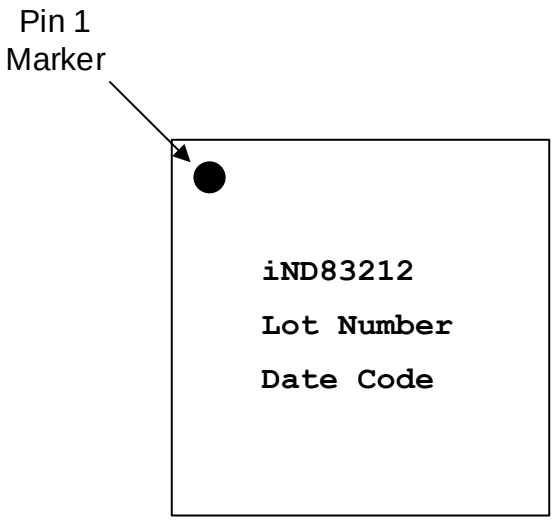

Figure 4 Package Branding

6.3 IO PIN DESCRIPTIONS

6.3.1 iND83212-Q20

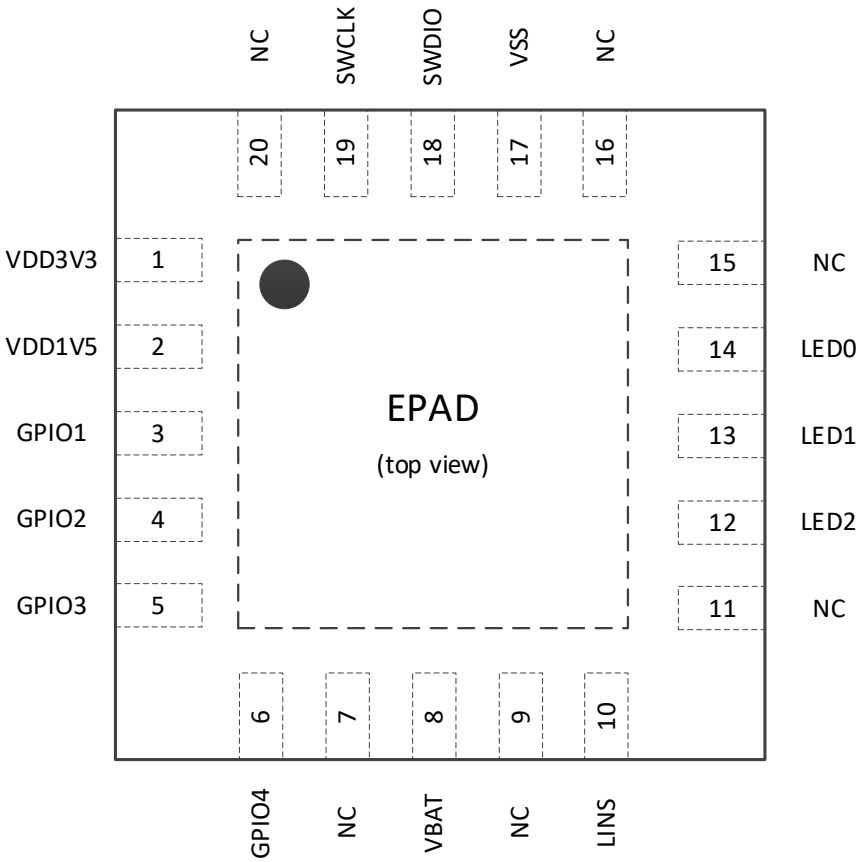

Figure 5 Pin Configuration (iND83212-Q20, QFN20)

Table 5 Pin description (iND83212-Q20, QFN20)

Pin #	Pin Name	Type	Voltage	Direction	Description
1	VDD3V3	Supply	VDD3V3	n/a	Connect to an external 2.2uF or large capacitor(1)
2	VDD1V5	Supply	VDD1V5	n/a	Connect to an external 2.2uF or large capacitor(1)
3	GPIO1	GPIO	VDD3V3	I/O	General purpose IO/LIN RXD

Pin #	Pin Name	Type	Voltage	Direction	Description
4	GPIO2	GPIO	VDD3V3	I/O	General purpose IO/LIN TXD
5	GPIO3	GPIO	VDD3V3	I/O	General purpose IO/LIN RXD
6	GPIO4	GPIO	VDD3V3	I/O	General purpose IO
7	NC				
8	VBAT	Supply	Vehicle Power	n/a	
9	NC				
10	LINS	IO	Pulled up to Vehicle Power	I/O	J2602 LIN 2.x
11	NC				
12	LED2	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink
13	LED1	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink
14	LED0	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink
15	NC				
16	NC				
17	VSS	Supply	GND	Analog	Bonding with ground plane
18	SWDIO	GPIO	VDD3V3	I/O	ARM debugger data. Integrated weak pull up. (2)
19	SWCLK	GPIO	VDD3V3	Input	ARM debugger clock. Integrated weak pull down. (2)
20	NC				

Pin #	Pin Name	Type	Voltage	Direction	Description
*	EPAD	Supply	GND	n/a	Ground(3)

Note:

1. VDD3V3 and VDD1V5 has only very limited load capacity, the peak current of external load should not exceed 10mA in total, and should never apply any external power on these pins
2. SWD debugging/flashing port must keep disconnected before the IC start-up sequence finished, preventing the reversed current from the SWD pins damages the IC
3. GND pin is the thermally significant pin

6.3.2 iND83212-D14

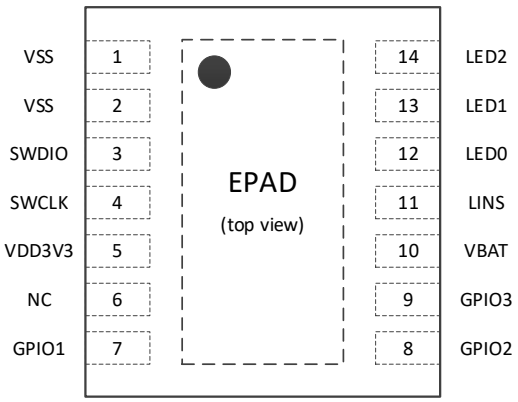

Figure 6 Pin Configuration (iND83212-D14, DFN14)

Table 6 Pin description (iND83212-D14, DFN14)

Pin #	Pin Name	Type	Voltage	Direction	Description
1	VSS	Supply	GND	Analog	Bonding with ground plane
2	VSS	Supply	GND	Analog	Bonding with ground plane
3	SWDIO	GPIO	VDD3V3	I/O	ARM debugger data. Integrated weak pull up. (2)
4	SWCLK	GPIO	VDD3V3	Input	ARM debugger clock. Integrated weak pull down.

Pin #	Pin Name	Type	Voltage	Direction	Description
					(2)
5	VDD3V3	Supply	VDD3V3	n/a	Connect to an external 2.2uF or large capacitor(1)
6	NC				
7	GPIO1	GPIO	VDD3V3	I/O	General purpose IO/LIN RXD
8	GPIO2	GPIO	VDD3V3	I/O	General purpose IO/LIN TXD
9	GPIO3	GPIO	VDD3V3	I/O	General purpose IO/LIN RXD
10	VBAT	Supply	Vehicle Power	n/a	
11	LINS	IO	Pulled up to Vehicle Power	I/O	J2602 LIN 2.x
12	LED0	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink
13	LED1	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink
14	LED2	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink
*	EPAD	Supply	GND	n/a	Ground(3)

Note:

4. VDD3V3 and VDD1V5 has only very limited load capacity, the peak current of external load should not exceed 10mA in total, and should never apply any external power on these pins
5. SWD debugging/flashing port must keep disconnected before the IC start-up sequence finished, preventing the reversed current from the SWD pins damages the IC
6. GND pin is the thermally significant pin

6.3.3 Pin state upon Power-on Reset

- Unless otherwise noted, all pins default to tristate/Isolation mode (Hi-Z) upon power-on reset.

7 ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

Table Absolute Maximum Ratings, Voltages Referenced to ground

Names	Conditions	Min.	Max.	Unit
VBAT	No damage, t<500ms	-0.3	+45	V
VBAT	No damage, t<5min	-0.3	+28	V
VBAT	No damage, t<5ms	-1.1		V
VBAT	No damage, t<20ns	-4.0		V
VBAT	No damage, ISO 7637-2 pulse 1, VBAT=13.5V, TA=23°+/-5C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor	-100		V
VBAT	No damage, ISO 7637-2 pulse 2 VBAT=13.5V, TA=23°+/-5C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor		+50	V
VBAT	No damage, accept ISO 7637-2 pulses 3A, 3B, VBAT=13.5V, TA=(23+/-5)°C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor	-150	+100	V
VBAT	No damage, ISO 7637-2 pulses 5b VBAT=13.5V, TA=(23+/-5)°C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor		+45	V
LIN	No damage, t<500ms	-40	+40	V
LIN	No damage, ISO 7637-3 pulse 1 VBAT=13.5V, TA=23°+/-5C, test pulse applied to LIN via 1nF capacitor	-100		V

LIN	No damage, ISO 7637-2 pulse 2 VBAT=13.5V, TA=23°+/-5C, test pulse applied via 1nF capacitor		+50	V
LIN	No damage, ISO 7637-2 pulses 3A, 3B VBAT=13.5V, TA= (23+/-5) °C, test pulse applied via 1nF capacitor	-150	+100	V
HVIO	No damage, t<500ms	-0.3	+45	V
HVIO	No damage, t<5min	-0.3	+28	V
HVIO	No damage, t<5ms, voltage applied on the anode side of the LED, current sink open (LED Off)	-1.1		V
HVIO	No damage, t<20ns, voltage applied on the anode side of the LED, current sink open (LED Off)	-4		V
GPIO1, GPIO2, GPIO3, GPIO4, SWCLK, SWDIO		-0.3	3.6	V
VBAT/LIN_IN to GND	ESD HBM	-4	+4	kV
All pins except VBAT and LIN	ESD HBM	-2	+2	kV
All pins	ESD CDM	-750	+750	V
Storage Temp		-55	+150	°C

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. The absolute maximum ratings provided in the table above are limiting values that do not lead to a permanent damage of the part. But functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ELECTRICAL CHARACTERISTICS

Table 7 Electrical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Operation Conditions					
Operating ambient Temperature		-40	25	125	°C
Operating Junction Temperature		-40	25	125	°C
Package Thermal Resistance	Junction to Ambient (ThetaJA)		30		K/W
VBAT		6	13.5	18	V
IO Supply (VDD3P3)		3.0	3.3	3.6	V
ASIC Core Supply (VDD3P3)		3.0	3.3	3.6	V
ASIC Core Supply (VDD1P5)		1.35	1.5	1.65	V
MCU Core Supply	MCU Core Supply including SRAM and Flash	1.35	1.5	1.65	V
Flash Memory					
Sector Endurance		20k			cycles
Data Retention	@25degC	100			Years
Data Retention	@85degC	25			Years
SRAM					
Min Retention Voltage	Minimum Retention Voltage below which SRAM data are not guaranteed.	1.08			V
Clocks					
System RC Oscillator Frequency			16		MHz
System RC Oscillator Accuracy		-4		4	%

Parameter	Conditions	Min.	Typ.	Max.	Unit
System RC Oscillator start up time			10		us
Auxiliary system clock	Used in hibernate/deep sleep mode		256		kHz
Auxiliary system clock Accuracy		-6		6	%
POR/BOR					
POR (VDD3P3)		1.8		2.1	V
BOR VDD3P3	200mV window, steps every 100mV (2.3 to 3.2V)	2.3		3.2	V
BOR VDD1P5	Max Value at which system resume operation			1.6	V
Battery Monitor					
Under Voltage Threshold	Analog Comparator Generates interrupt to MCU except in Hibernate mode (disabled feature)	4.5	5.0	5.5	V
		5.5	6.0	6.5	V
		6.5	7.0	7.5	V
		7.5	8.0	8.5	V
		8.5	9.0	9.5	V
Under Voltage hysteresis	Programmable, UVHYS=0	2.5	4.0	6.0	%
	Programmable, UVHYS=1	4.0	6.0	9.5	%
	Programmable, UVHYS=2	5.0	8.5	14.0	%
	Programmable, UVHYS=3	6.0	10.5	19.0	%
Under Voltage Digital debounce time	Programmable for signal rise and fall, 62.5ns or 62.5us steps			16	ms
Over Voltage Threshold	Analog Comparator, generates interrupt to MCU except in Hibernate mode (disabled feature)	14		19	V
Over Voltage Hysteresis	Programmable, OVHYS=0	1.5	2.5	3.0	%
	Programmable, OVHYS=1	3.0	5.5	8.0	%

Parameter	Conditions	Min.	Typ.	Max.	Unit
	Programmable, OVHYS=2	5.0	9.0	13.0	%
	Programmable, OVHYS=3	8.0	12.0	16.0	%
Over Voltage Digital debounce time	Programmable for signal rise and fall, 62.5ns or 62.5us steps			16	ms
Current Source HVIO(LED)					
HVIO voltage	minimum voltage to ensure current regulation			1.6	V
Sink Current	VBAT>6V	0.12		60	mA
Sink Current step size			120		uA
Sink Current Error	Ta=25degC	-7		+7	%
Temperature Drift			-0.025		%/K
HVIO switch resistance	Guaranteed by design	53			Ω
Over Temperature Monitor					
Overtemp Threshold	Analog Comparator, generates interrupt or reset to MCU.	90		165	degC
Overtemp hysteresis		-10			degC
Temperature Sensor					
Temperature range	The MCU is in charge to pull the ADC related data from temperature sensor.	-40		150	degC
Temperature Accuracy		-10		+10	degC
Active current			20		uA
Differential Amplifier for LED VFW measurement					
Input Voltage Range (Vin)	>4V @Gain=1/4	VBAT-4		VBAT	V
	>4V @Gain=1/8	VBAT-8		VBAT	V
Output Voltage Range	Internal output range of LED Sense	0	Vin*Gain	Vref (ADC)	ms
Output Voltage Relative Error				1	%
Gain	1-bit Programmable	0.533/2		0.533	

Parameter	Conditions	Min.	Typ.	Max.	Unit
Wake Up					
TWAKEUP	LIN_IN/LIN_OUT, programmable	30	150	200	us
Wake Up Timer	Wakeup Time = 2^(WUT_TAPSEL)/10kHz clock WUT_SEL=0 to 15, default 0	0.1		3276.8	ms
ASIC Watchdog timer					
Timeout	Programmable (See Register Description)	0.128		16	s
SAR ADC					
Resolution			12		bits
Conversion Speed	17 cycles per conversion (4 cycles for S/H and 13 cycles for conversion)			250	kS/s
ADC Clock				4	MHz
INL	Guaranteed by design	-1		1	LSB
DNL	Guaranteed by design	-1		1	LSB
Reference voltage	Post Calibration		2.4		V
LIN EC specified with VBAT=8V to 16V – refer to LIN 2.x specification, VBUS=LIN pin/line					
Supply Voltage	Supply voltage range	6	13.5	18	V
IBUS_LIM	Current Limitation for Driver dominant state driver on VBUS = VBAT=16V	40		200	mA
Rslave	Lin Slave Pullup	20	30	60	kΩ
IBUS_PAS_dom	Input Leakage Current at the Receiver including Pull-Up Resistor driver off VBUS = 0V VBAT= 12V	-1			mA
IBUS_PAS_rec	Driver off, VBUS>VBAT 8V<VBAT<16V			20	uA

Parameter	Conditions	Min.	Typ.	Max.	Unit
	8V<VBUS<16V				
IBUS_no_GND	Control unit disconnected from ground GND Device = VSUP 0V<VBUS<16V VBAT = 12V Loss of local ground must not affect communication in the residual network. **LIN 2.2A**	-1		+1	mA
Device Bus Leakage Current Ground Disconnected	VBAT= VGND=12V, 0V<VBUS<18V **J2602**	-100		100	uA
IBUS_no_BAT	VBAT disconnected 0<VBUS<16V, VBAT=0V **LIN 2.2A** Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.			100	uA
Device Bus Leakage current VBAT disconnected	0V<VBUS<18V, VBAT=VGND=0V **J2602**	-23		23	uA
BUS_VOL Transmitter dominant voltage	Load 500Ohms, driver open drain active	0.0		0.2	VSUP
BUS_VOH Transmitter recessive voltage	Driver open drain high impedance	0.8		1.0	VSUP
CSLAVE	LIN pin input capacitance Note that LIN 2.2A spec 220pF typ, 250pF max as total node capacitance at the connector including the physical bus driver and all other components including C_{LIN}			35	pF
VBUSdom	Receiver dominant state			0.4	VSUP
VBUSrec	Receiver recessive state	0.6			VSUP

Parameter	Conditions	Min.	Typ.	Max.	Unit
VBUS_CNT	Center point Receiver VBUS_CNT =(Vth_dom+ Vth_rec)/2	0.475	0.5	0.525	VSUP
Vhys	Receiver hysteresis VHYS = Vth_rec -Vth_dom			0.175	VSUP
Trx_pd	propagation delay of receiver C_{RXD} load 20pF (RX output of transceiver, internal node, access in test mode) minimum slew rate for the LIN rising and falling edges is 50V/us			6	us
Trx_sym	symmetry of receiver propagation delay rising edge w.r.t. falling edge C_{RXD} load 20pF C_{RXD} load 20pF (RX output of transceiver, internal node, access in test mode)	-2		+2	us
LIN Timing parameters (CBUS ; RBUS): (1nF; 1kΩ) / (6.8nF;660Ω) / (10nF;500Ω)					
D1 Duty Cycle (20kbits/s)	THRec(max) = 0.744 x VSUP; THDom(max) = 0.581 x VSUP; VSUP = 7.0V...16V; tBit = 50µs; D1 = tBus_rec(min) / (2 x tBit)	0.396			-
D2 Duty Cycle (20kbits/s)	THRec(min) = 0.422 x VSUP; THDom(min) = 0.284 x VSUP; VSUP = 7.6V...16V; tBit = 50µs; D2 = tBus_rec(max) / (2 x tBit)			0.581	-
D3 Duty Cycle (10.4kbits/s)	THRec(max) = 0.778 x VSUP; THDom(max) = 0.616 x VSUP; VSUP = 7.0V...16V; tBit = 96µs; D3 = tBus_rec(min) / (2 x tBit)	0.417			-
D4 Duty Cycle (10.4kbits/s)	THRec(min) = 0.389 x VSUP; THDom(min) = 0.251 x VSUP; VSUP = 7.6V...16V; tBit = 96µs; D4 = tBus_rec(max) / (2 x tBit)			0.590	-

Parameter	Conditions	Min.	Typ.	Max.	Unit
tBus_rec(max)-tBus_dom(min)	Δt3, 10.4kbs operation, low speed mode, **J2602**			15.9	us
tBus_dom(max)-tBus_rec(min)	Δt4, 10.4kbs operation, low speed mode, **J2602**			17.28	us
GPIOs					
GPIOVIL	Input Low Voltage			0.3*VDD3P3	V
GPIOVIH	Input High Voltage	0.7*VDDD3P3			V
GPIOIOL	Max load current with output voltage=VOL			10	mA
GPIOIOH	Max load current with output voltage=VOLH			10	mA
GPIOVOL	Output Low Voltage			0.4	V
GPIOVOH	Output High Voltage	2.4			V
GPIOPU	Pull Up Resistance			110	kOhm
GPIOPD	Pull Down Resistance			110	kOhm
SWD					
SWDVIL	SWDIO, SWCLK			0.8	V
SWDVIH	SWDIO, SWCLK	2			V
SWCLKIOL	SWCLK, Max load current with output voltage=VOL			4	mA
SWCLKIOH	SWCLK, Max load current with output voltage=VOH			4	mA
SWDIOIOL	SWDIO, Max load current with output voltage=VOL			8	mA
SWDIOIOH	SWDIO, Max load current with output voltage=VOH			8	mA
SWDVOL	SWDIO			0.4	V

Parameter	Conditions	Min.	Typ.	Max.	Unit
SWDVOH	SWDIO	2.4			V
SWDIOPU	SWDIO, Pull-up resistance	22		110	kOhm
SWCLKPD	SWCLK, Pull-down resistance	22		110	kOhm

Electrical Characteristics are valid over the full temperature range of Tj = -40°C to +125°C and a supply range of 6V ≤ VBAT ≤ 18V unless otherwise noted.

The figure below shows the relation between the propagation delay, the TX thresholds and associated receiver duty cycles. Refer to D1 to D4 duty cycles in the table above for THRec and THDom threshold levels.

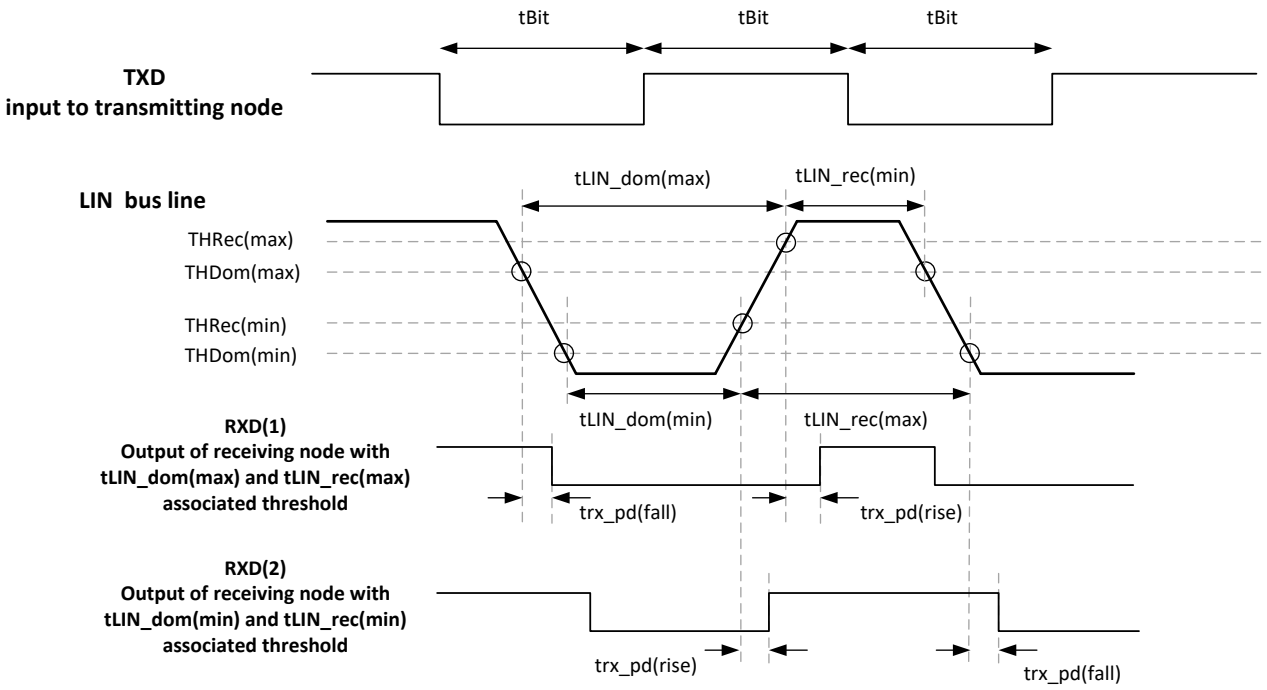

Figure 7 LIN timing Diagram

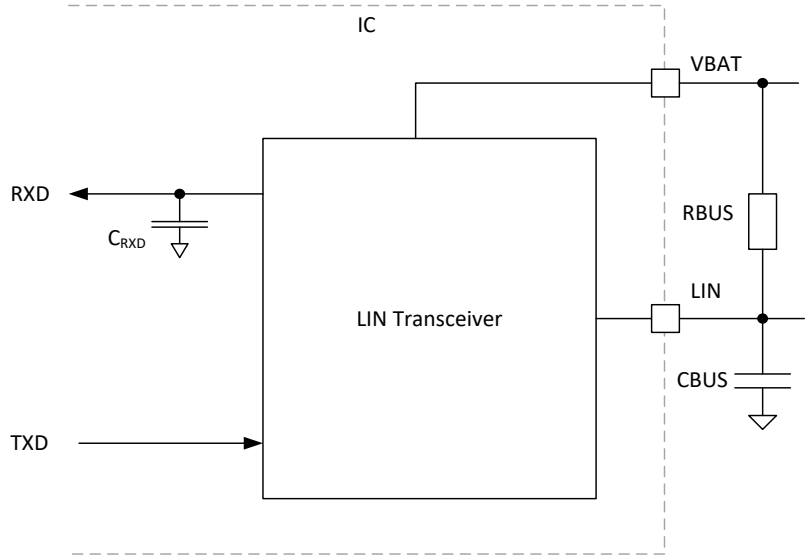

Figure 8 LIN AC Test Circuit

7.3 CURRENT CONSUMPTION

Table 8 Current Consumption

Mode	Conditions	Min.	Typ.	Max.	Unit
Normal	Ta=85C, VBAT=18V, RCO=16MHz, full functionality: MCU running, no flash write, LED OFF, ADC ON, VBAT and TEMP monitor ON, WDT ON.			10	mA
DeepSleep	All regulators (5V, 3.3V,1.5V) ON, 1.5V regulator is in low power mode, MCU OFF, Load dump protection active. Ta=85degC max, VBAT=13.5V Overvoltage/Undervoltage detection, PWM, LED driver, Tempsensor and ADC are OFF except one LIN RX on and GPIO toggling and wake up timer.	35	50	60	uA

Table 8 Current Consumption					
Mode	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Hibernate	Main regulator (5V) ON, 3.3V/1.5V regulators OFF, IO Voltage regulator & Core Voltage regulater off, Load dump protection active. Ta=85degC max, VBAT=13.5V VBAT Overvoltage/Undervoltage detection, Only LIN Wakeup monitor active.	15	22	30	uA

8 MEMORY DESCRIPTION

8.1 TOP LEVEL MEMORY MAP

The chip uses a unified memory model with a linear address space (Von Neumann architecture) including Flash and RAM memories as well as registers address space. The implementation of the Cortex M0 core uses a high density 64KB Flash cell along with 16KB of SRAM.

Table 9 Top Level Memory Map

Address	Memory	Description
0x00000000 – 0x0000FFFF	Flash	64Kbytes of Flash Memory, user programmable.
0x00010000 – 0x0003FFFF	N/A	Reserved
0x00040000 – 0x000400FF	N/A	Reserved
0x00040100 – 0x000401FF	N/A	Reserved
0x00040200 – 0x1FFFFFFF	N/A	Reserved
0x20000000 – 0x20003FFF	SRAM	16Kbytes of SRAM
0x20004000 – 0x4FFFFFFF	N/A	Reserved
0x50000000 - 0x5000003F	CRGA	Clock & Reset Generator
0x50000040 - 0x5000005F	PMUA	Power Management Unit
0x50000060 - 0x5000007F	EVTHOLD	Event Hold Control
0x50000080 - 0x500000FF	BTE	Block Transfer Engine registers
0x50010100 - 0x500101FF	WICA	WakeUp Interrupt Controller
0x50010300 - 0x500103FF	WDTA	Watchdog Timer Registers
0x50010600 - 0x500106FF	PWM	Control (and status) registers for the pulse width modulation waveform generator.

Address	Memory	Description
0x50010700 - 0x500107FF	LINS	LIN slave interface registers
0x50010900 - 0x500109FF	PWM_AUX	Control (and status) registers for the pulse width modulation waveform generator.
0x50010D00 - 0x50010DFF	SAR_CTRL	SAR ADC Interface registers
0x50011000 - 0x50011FFF	IOCTRLA	I/O configuration and DFT pin control
0x50012000 - 0x50013FFF	SYSCTRLA	System configuration and retention memory
0x50018000 - 0x5001FFFF	GPIO	GPIO bit control and configuration
0x50020000 - 0x50020007	TIMER0	General purpose timer 0 registers
0x50020008 - 0x5002000F	TIMER1	General purpose timer 1 registers
0x50020010 - 0x50020017	TIMER2	General purpose timer 2 registers
0x50020018 - 0x5002001F	WDT1	The watchdog timer that is local to VERNE MCU
0x50020020 - 0x5002005F	FLASH	FLASH Memory registers
0x50020048 – 0xDFFFFFFF	N/A	Reserved
0xE0000000 – 0xE00FFFFF	Private peripheral bus	ARM peripherals
0xE0100000 – 0xEFFFFFFF	N/A	Reserved
0xF0000000 – 0xF0001FFF	System ROM tables	ARM core IDs
0xF0002000 – 0xFFFFFFFF	N/A	Reserved

8.2 REGISTER DESCRIPTIONS

Peach MCM Map		
Address	**Peripheral Name**	**Description**
0x50000000 - 0x5000003F	CRGA	Clock & Reset Generator
0x50000040 - 0x5000005F	PMUA	Power Management Unit
0x50000060 - 0x5000007F	EVTHOLD	Event Hold Control
0x50000080 - 0x500000FF	BTE	Block Transfer Engine registers
0x50010100 - 0x500101FF	WICA	WakeUp Interrupt Controller
0x50010300 - 0x500103FF	WDTA	Watchdog Timer Registers
0x50010600 - 0x500106FF	PWM	Control (and status) registers for the pulse width modulation waveform generator.
0x50010700 - 0x500107FF	LINS	LIN slave interface registers
0x50010900 - 0x500109FF	PWM_AUX	Control (and status) registers for the pulse width modulation waveform generator.
0x50010D00 - 0x50010DFF	SAR_CTRL	SAR ADC Interface registers
0x50011000 - 0x50011FFF	IOCTRLA	I/O configuration and DFT pin control
0x50012000 - 0x50013FFF	SYSCTRLA	System configuration and retention memory
0x50018000 - 0x5001FFFF	GPIO	GPIO bit control and configuration
0x50020000 - 0x50020007	TIMER0	General purpose timer 0 registers
0x50020008 - 0x5002000F	TIMER1	General purpose timer 1 registers
0x50020010 - 0x50020017	TIMER2	General purpose timer 2 registers
0x50020018 - 0x5002001F	WDT1	The watchdog timer that is local to VERNE MCU
0x50020020 - 0x5002005F	FLASH	FLASH Memory registers

8.2.1 CRGA

CRGA		
Address	**Register Name**	**Description**
0x50000000	LFCLKCTRL	Low frequency clock control
0x50000004	SYSCLKCTRL	System clock control
0x50000008	RESETCTRL	Reset control
0x5000000C	MODULERST	Module Reset control
0x50000010	BORACTION	BOR action
0x50000014	BORCONFIG	BOR configuration
0x50000018	BORDEGLITCH	BOR Deglitch, NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE and write trim key
0x5000001C	WDTACTION	Watchdog action
0x50000020	LFCLKKILL	Low frequency clock kill
0x50000024	OVTEMPACTION	OVTEMP action
0x50000028	OVTEMPCONFIG	OVTEMP configuration
0x5000002C	OVUVACTION	OVUV action

8.2.1.1 LFCLKCTRL

0x50000000 **LFCLKCTRL** ^

Low frequency clock control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F8	CLKLFSEL	LF Clock Source select. Used to select If osc mode between 0x0: CLK_LF(LF OSC out) is 256KHz, slow system clock freq is Freq_CLK_LF/2 = 128KHz. 0x1: CLK_LF(LF OSC out) is 256KHz, slow system clock freq is Freq_CLK_LF/16= 16KHz.	1	rw	0x1
F0	LFRCSTS	Slow oscillator status. Will be high when the Low Frequency oscillator is selected	1	ro	0x0

8.2.1.2 SYSCLKCTRL

0x50000004	SYSCLKCTRL	^

System clock control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	F20		-	F16			-	-	-	-	-	-	-	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F20	HF_RC_LDO_VSEL	16MHz RC OSC LDO output select. 0x0: 1V45 Selected 0x1: 1V50 Selected 0x2: 1V55 Selected 0x3: 1V65 Selected	2	rw	0x1
F16	DIVSYSCLK	Clock div select. Select the divider ratio on the system clock when using fast oscillator 0x0: No Division. Full Clock speed. 0x1: Div by 2. 0x2: Div by 3. 0x3: Div by 4. 0x4: Div by 5. 0x5: Div by 6. 0x6: Div by 7. 0x7: Div by 8.	3	rw	0x0
F8	SYSCLKSEL	Clock select. Used to switch between the fast and slow system clocks 0x0: Slow clock 0x1: Fast clock	1	rw	0x0
F1	HFRCSTS	Fast oscillator status. Will be high when High Frequency oscillator is enabled	1	ro	0x0
F0	HFRCENA	Fast oscillator enable. Setting this bit when the High Frequency oscillator is not running will cause the oscillator to start (the PMU may have already started it). Even though the fast oscillator is running, its output is only used when selected via the clock mux - see CLKSEL. This bit is cleared automatically on entering SLEEP mode	1	rw	0x0

8.2.1.3 RESETCTRL

0x50000008	RESETCTRL	^

Reset control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	F20	-	-	F17	F16	-	F14	F13	F12	F11	F10	F9	F8	-	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	SOFTRSTREQ	Soft reset request. Set to trigger a soft reset of chip Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F20	SAFEMODEENA	Safe Mode enable. Set to enable safe Mode.Configure with writting debug key of SYSCTRL_SFRS->DEBUG_ACCESS_KEY.	1	rw	0x0
F17	SAFEMODEREQ	Safe Mode request. Set to force chip into Safe Mode, in which Chip can only be wakeup by POR.Configure with writting debug key of SYSCTRL_SFRS->DEBUG_ACCESS_KEY. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F16	HARDRSTREQ	Hard reset request. Set to trigger a hard reset of chip	1	wo	0x0
F14	OVTEMPFLAGCLR	OVTEMP flag clear. Set to clear the OVTEMP flag	1	wo	0x0
F13	WDTFLAGCLR	WDT flag clear. Set to clear the WDT flag	1	wo	0x0
F12	BOR1V5FLAGCLR	BOR 1v5 clear. Set to clear the 1.5V brownout detected flag	1	wo	0x0
F11	UVFLAGCLR	UV flag clear. Set to clear the UV flag	1	wo	0x0
F10	BOR3V3FLAGCLR	BOR 3v3 clear. Set to clear the 3.3V brownout detected flag	1	wo	0x0
F9	OVFLAGCLR	OV flag clear. Set to clear the OV flag	1	wo	0x0
F8	PORFLAGCLR	POR flag clear. Set to clear the POR flag	1	wo	0x0
F6	OVTEMPFLAG	Over Temp Violation flag. Set by the hardware when the over temp condition is detected.	1	ro	N/A
F5	WDTFLAG	Watchdog bark flag. Set by the hardware when the watchdog barks.	1	ro	N/A
F4	BOR1V5FLAG	BOR 1v5 flag. Set by the hardware when a brownout of the 1.5V supply is detected.	1	ro	0x0
F3	UVFLAG	Under Voltage Monitor flag. Set by the hardware when the under voltage monitor.	1	ro	N/A
F2	BOR3V3FLAG	BOR 3v3 flag. Set by the hardware when a brownout of the 3.3V supply is detected.	1	ro	0x0
F1	OVFLAG	Over Voltage Monitor flag. Set by the hardware when the over voltage monitor.	1	ro	N/A
F0	PORFLAG	Power on reset flag. Set by the hardware during power-on reset	1	ro	N/A

8.2.1.4 MODULERST

0x5000000C	MODULERST	^

Module Reset control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	MODULERSTREQ	Module Soft reset request. Set to trigger a soft reset of module below. 0x1: ADC Soft reset request 0x2: LINS Soft reset request 0x4: PWM soft reset request 0x8: PWM AUX soft reset request Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	4	wo	0x0

8.2.1.5 BORACTION

0x50000010	BORACTION	^

BOR action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	F23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F31	BOR_1V5_LOCK	Set Only bit. Set this bit to lock BOR_1V5_ACTION & S_BOR_1V5 bits.	1	rw	0x0
F23	BOR 3V3 LOCK	Set Only bit. Set this bit to lock BOR 3V3 ACTION & S BOR 3V3 bits.	1	rw	0x0
F4	VDD1V5	BOR 1v5 action. Defines the consequences of brown-out condition on the 1v5 supply being detected by the hardware. Configure with writting trim key 0x1: IRQ generated 0x0: Hard reset generated	1	rw	0x0
F0	VDD3V3	BOR 3v3 action. Defines the consequences of brown-out condition on the 3v3 supply being detected by the hardware. Configure with writting trim key 0x1: IRQ generated 0x0: Hard reset generated	1	rw	0x0

8.2.1.6 BORCONFIG

0x50000014	BORCONFIG	^

BOR configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	F16				-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F16	S_BOR_1P5V	BOR 1v5 threshold. Select the BOR threshold voltage level for the 1v5 regulator. Following typical value can be used as reference: NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE and write trim key 0x0: Vr: 1.243 V, Vf: 1.218 V, 0x1: Vr: 1.273 V, Vf: 1.243 V, 0x2: Vr: 1.298 V, Vf: 1.273 V, 0x3: Vr: 1.328 V, Vf: 1.298 V, 0x4: Vr: 1.358 V, Vf: 1.328 V, 0x5: Vr: 1.393 V, Vf: 1.363 V, 0x6: Vr: 1.428 V, Vf: 1.393 V, 0x7: Vr: 1.463 V, Vf: 1.428 V, 0x8: Vr: 1.498 V, Vf: 1.468 V, 0x9: Vr: 1.538 V, Vf: 1.503 V, 0xa: Vr: 1.583 V, Vf: 1.548 V, 0xb: Vr: 1.623 V, Vf: 1.588 V, 0xc: Vr: 1.673 V, Vf: 1.633 V, 0xd: Vr: 1.718 V, Vf: 1.683 V, 0xe: Vr: 1.773 V, Vf: 1.733 V, 0xf: Vr: 1.828 V, Vf: 1.788 V,	4	rw	0x3
F0	S_BOR_3P3V	BOR 3v3 threshold. Select the BOR threshold voltage level for the 3v3 regulator, Following typical value can be used as reference: NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE and write trim key 0x0: Vr: 2.223 V, Vf: 2.163 V, 0x1: Vr: 2.288 V, Vf: 2.228 V,	4	rw	0xA

		0x2: Vr: 2.358 V, Vf: 2.293 V, 0x3: Vr: 2.428 V, Vf: 2.363 V, 0x4: Vr: 2.503 V, Vf: 2.433 V, 0x5: Vr: 2.583 V, Vf: 2.513 V, 0x6: Vr: 2.668 V, Vf: 2.598 V, 0x7: Vr: 2.763 V, Vf: 2.688 V, 0x8: Vr: 2.858 V, Vf: 2.783 V, 0x9: Vr: 2.968 V, Vf: 2.883 V, 0xa: Vr: 3.078 V, Vf: 2.998 V, 0xb: Vr: 3.203 V, Vf: 3.118 V, 0xc: Vr: 3.338 V, Vf: 3.248 V, 0xd: Vr: 3.483 V, Vf: 3.388 V, 0xe: Vr: 3.638 V, Vf: 3.543 V, 0xf: Vr: 3.813 V, Vf: 3.708 V,			

8.2.1.7 BORDEGLITCH

0x50000018 **BORDEGLITCH** ^

BOR Deglitch, NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE and write trim key.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F14		F12		-	-	-	F8	F6		F4		-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F14	SEL_BOR3V3_POS_DEGLITCH	select the deglitch width of BOR3V3 posedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x3
F12	SEL_BOR3V3_NEG_DEGLITCH	select the deglitch width of BOR3V3 negedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x0
F8	ENA_BOR3V3_DEGLITCH	enable of BOR3V3 deglitch.	1	rw	0x0
F6	SEL_BOR1V5_POS_DEGLITCH	select the deglitch width of BOR1V5 posedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x3
F4	SEL_BOR1V5_NEG_DEGLITCH	select the deglitch width of BOR1V5 negedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x0
F0	ENA_BOR1V5_DEGLITCH	enable of BOR1V5 deglitch.	1	rw	0x0

8.2.1.8 WDTACTION

0x5000001C **WDTACTION** ^

Watchdog action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F16	-	-	-	-	F8				-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F16	WDTBARKCNTCLR	WatchDog Bark Counter Clear. Set to clear watchdog bark counter.	1	wo	0x0
F8	WDTBARKCNT	WatchDog Bark Counter. Read to reflect the WDT bark counter value.	4	ro	0x0
F0	WDTACTION	Watchdog action. Defines the consequences of watchdog bark being detected by the hardware. 0x0: IRQ generated 0x1: Hard reset generated	1	rw	0x1

8.2.1.9 LFCLKKILL

0x50000020 **LFCLKKILL** ^

Low frequency clock kill.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	KILLLFRC	Kill slow RC oscillator. Setting this bit gates the low frequency RC oscillator input.Configure with writting debug key of SYSCTRL_SFRS->DEBUG_ACCESS_KEY.	1	rw	0x0

8.2.1.10 OVTEMPACTION

0x50000024 OVTEMPACTION ^

OVTEMP action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F31	OVTEMP_LOCK	Set Only bit. Set this bit to lock OVTEMP related bits.	1	rw	0x0
F0	OVTEMP	Over Temperature action. Defines the consequences of over temp condition detected by the hardware. 0x2: No action 0x1: IRQ generated 0x0: Hard reset generated	2	rw	0x2

8.2.1.11 OVTEMPCONFIG

0x50000028 OVTEMPCONFIG ^

OVTEMP configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F25	TEMPSENSE_EN	enable Temp Sensor Analog Part. Set to enable Temperature Sensor analog circuit. NOTE: The write operation of this register takes effect by IOCTRL_SFRS->LIN.UPDATE	1	rw	0x1
F24	OVERTEMP_EN	OverTemp Monitor Enable bit.	1	rw	0x0
F0	VTEMP_SEL	Over Temp protect threshold temp trim. Select the OVTEMP threshold level for the monitor.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE . 0x0: Rising: 93.13-Deg; Falling: 79.13-Deg 0x1: Rising: 98.13-Deg; Falling: 84.13-Deg 0x2: Rising: 103.6-Deg; Falling: 89.13-Deg 0x3: Rising: 109.1-Deg; Falling: 94.13-Deg 0x4: Rising: 115.1-Deg; Falling: 99.63-Deg 0x5: Rising: 121.1-Deg; Falling: 105.1-Deg 0x6: Rising: 127.1-Deg; Falling: 111.1-Deg 0x7: Rising: 133.1-Deg; Falling: 117.1-Deg 0x8: Rising: 139.6-Deg; Falling: 123.1-Deg 0x9: Rising: 146.6-Deg; Falling: 129.6-Deg 0xa: Rising: 153.6-Deg; Falling: 136.1-Deg 0xb: Rising: 160.6-Deg; Falling: 142.6-Deg 0xc: Rising: 168.1-Deg; Falling: 149.6-Deg 0xd: Rising: 176.6-Deg; Falling: 157.1-Deg 0xe: Rising: 185.1-Deg; Falling: 164.6-Deg 0xf: Rising: 195.6-Deg; Falling: 172.6-Deg	4	rw	0x6

8.2.1.12 OVUVACTION

0x5000002C OVUVACTION ^

OVUV action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	F27	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F31	UV_LOCK	Set Only bit. Set this bit to lock UV ACTION related bits.	1	rw	0x0
F27	OV_LOCK	Set Only bit. Set this bit to lock OV ACTION related bits.	1	rw	0x0
F4	UV_ACTION	Under Voltage action. Defines the consequences of under voltage condition detected by the hardware. 0x1: No action 0x0: Hard reset generated	1	rw	0x1

F0	OV_ACTION	Over Voltage action. Defines the consequences of over voltage condition detected by the hardware. 0x1: No action 0x0: Hard reset generated	1	rw	0x1

8.2.2 PMUA

PMUA		
Address	**Register Name**	**Description**
0x50000040	CTRL	Control
0x50000044	PMUTRIM	PMU Trim Register
0x50000048	DWELL	Dwell
0x5000004C	VBATCTRL	VBAT Monitor Register
0x50000050	VBATTRIM	VBAT Monitor Trim Register
0x50000054	VBATDBNC	VBAT Debounce Register
0x50000058	VBATDBNCTHRES	VBAT Monitor Threshold Register
0x5000005C	PMUIRQ	Voltage Monitor interrupts

8.2.2.1 CTRL

0x50000040 **CTRL** ^

Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	F29	F28	F27	F26	F25	F24	-	-	F21	F20	F19	-	F17	F16	-	-	F13	F12	F11	F10	F9	F8	-	-	-	F4	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	UPDATE	PMUA Configure Update. Set to update the Configurations to PRE5V domains. NOTE: DO NOT change the CTRL register when it is high, which indicates there is an update in progress, It gets cleared by the core when the current update is done	1	dual	0x0
F29	DBG_ISO	NOTE:Don't use. Debug Contrl of isolation of domain 1V5 to domain PRE5V at PMU debug mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F28	DBG_DIS_BOR_1V5	Debug Contrl of dis_bor_1v5 at PMU debug mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F27	DBG_DIS_BOR_3V3	Debug Contrl of dis_bor_3v3 at PMU debug mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F26	DBG_DIS_LDO_1V5	Debug Contrl of dis_ldo_1v5 at PMU debug mode.(Not Use) NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F25	DBG_DIS_LDO_3V3	NOTE:Don't use.Debug Contrl of dis_ldo_3v3 at PMU debug mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F24	DBG_DIS_CP	Set 1, Shut down PRE5V ChargePump, PRE5V=Vzener-Vgs. Only take effect at Debug mode(DBG_TEST = 1) at PMU debug mode	1	rw	0x0
F21	PD1V5_ENA_HIBERNATE	enable of 1V5 Power Domain at Hibernate mode. set to enable the 1V5 Power Domain at Hibernate mode, this mode is defined as DEEPSLEEP mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F20	DBG_DISCHARGE_3V3	3V3 LDO Debug Mode: a. Set '0' to test 3V3-LDO function; b. Set '1' to test 3V3-LDO Discharge Circuit. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F19	DBG_DISCHARGE_1V5	1V5 LDO Debug Mode: a. Set '0' to test 1V5-LDO function; b. Set '1' to test 1V5-LDO Discharge Circuit. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F17	DBG_TEST	PRE5V DBG mode enable. Set 1, Pre5V voltage can output through 3P3V LDO pin(DBG_DIS_LDO_3V3 = 1'b0 for enable 3v3-LDO).	1	rw	0x0

F16	IGNORE_CIFS	Ignore QACKs. Setting a bit in this register prevents PMUA from waiting for the assertion of the corresponding 'Quiescent State Acknowlege' signal when before transitioning towards the Hibernate state.	1	rw	0x0
F13	OPT_EN_LP_CAPLESS	1.5V ldo low power mode, set 1 to enter low power at Deepsleep mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at Trim mode	1	rw	0x1
F12	OPT_EN_LOWIQ	Set to enable of low power mode for BG_TOP at Deepsleep Mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at Trim mode	1	rw	0x1
F11	VDD1V5_LDO_CHOOSE	1.5V LDO Mode selection. NOTE: This register is not used by Analog PMU 0x0: choose Capless LDO 0x1: choose Caps LDO	1	rw	0x0
F10	DBG_EN_LP_CAPLESS	1.5V ldo low power mode, set 1 to enter low power at PMU debug mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F9	DBG_DIS_BG_UVLO	Set to disable of low power mode for UVLO in BG_TOP at PMU debug mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F8	DBG_EN_LOWIQ	Set to enable of low power mode for BG_TOP at PMU debug mode. NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	1	rw	0x0
F4	BG_OK	the flag of bandgap OK. the flag of bandgap OK	1	ro	N/A
F1	FASTBOOT	Fast boot. Set to enable used of the fast clock during subsequent power-up sequences (including the portion consumed by the chip boot sequence). The set value brings the system up with the slow clock to make the initial boot and any boot after a hard reset (e.g. after a brownout) as safe as possible.	1	rw	0x1
F0	HIBERNATE	Hibernate. Set to put the chip into HIBERATE mode. Before setting this bit, ensure that wake interrupt controller HOLD bit has been set (and that a corresponding Lullaby interrupt has been received).	1	wo	0x0

8.2.2.2 PMUTRIM

0x50000044 **PMUTRIM** ^

PMU Trim Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	-	F24		-	-	F16						-	-	-	F8					F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F28	VDD3V3_LDO_TRIM	3.3V LDO output trim.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode 0x0: 3.40V 0x1: 3.00V 0x2: 3.09V 0x3: 3.18V 0x4: 3.28V 0x5: 3.52V 0x6: 3.65V 0x7: 3.80V	3	rw	0x0
F24	VDD1V5_LDO_TRIM	1.5V LDO output trim. The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode 0x0: 1.55V 0x1: 1.61V 0x2: 1.65V 0x3: 1.69V	2	rw	0x0
F16	TRIM_BG	Trim BandGap. (1) The voltage range before trimming is 1.16797V ~ 1.26337V. (2) The trim ratio 1/1.4811. (3) The voltage is 1.21455V while TRIM_BG == 0x0. The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	6	rw	0x0
F8	TRIM_VREF_BUF	Trim the buffer refernce voltage include VREF_1/VREF_1P1/VREF_0P75/VREF_0P6. (1) The voltage range before trimming is 1.19825V ~ 1.237V. (2) The step is 1.25mV, and the precision of trimming is +- 0.625mV. (3) The voltage is 1.217V while TRIM_VREF_BUF == 0x0. The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode	5	rw	0x0
F4	OCP_CTRL_3V3	OCP trim for 3P3V LDO(default 30mA) .The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode. 0x0: 10.0 mA 0x1: 12.5 mA 0x2: 15.0 mA 0x3: 17.5 mA 0x4: 20.0 mA 0x5: 22.5 mA	4	rw	0x8

		0x6: 25.0 mA 0x7: 27.5 mA 0x8: 30.0 mA 0x9: 32.5 mA 0xa: 35.0 mA 0xb: 37.5 mA 0xc: 40.0 mA 0xd: 42.5 mA 0xe: 45.0 mA 0xf: 47.5 mA			
F0	OCP_CTRL_1V5	OCP trim for 1.5V LDO(default 30mA) .The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE at PMU debug mode. 0x0: 20.0 mA 0x1: 22.5 mA 0x2: 25.0 mA 0x3: 27.5 mA 0x4: 30.0 mA 0x5: 32.5 mA 0x6: 35.0 mA 0x7: 37.5 mA 0x8: 40.0 mA 0x9: 42.5 mA 0xa: 45.0 mA 0xb: 47.5 mA 0xc: 50.0 mA 0xd: 52.5 mA 0xe: 55.0 mA 0xf: 57.5 mA	4	rw	0x4

8.2.2.3 DWELL

0x50000048 **DWELL** ^

Dwell. Minimum times spent in various PMUA states. Please Note- The STARTUP_BIAS_DWELL state timeout is hardcoded to a value of 0xC. A value of 0xC in the STARTUP_BIAS_DWELL state @ 16KHz yields a delay of 1.5 milliseconds

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F12				F8				F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F12	POWER_DOWN_MCU	Power down MCU dwell time. Defines the amount of time spent in the 'Power down MCU' state. Pausing here allows the MCU supplies to discharge (to guarantee subsequent POR).at PMU debug mode	4	rw	0x4
F8	ATTACH_3V3	Attach 3.3V dwell time. Defines the amount of time spent in the 'Attach 3V3' state. State Attaches 3.3V to MCU.at PMU debug mode	4	rw	0x4
F4	ATTACH_1V5	Attach 1.5V dwell time. Defines the amount of time spent in the 'Attach 1V5' state. State Attaches 1.5V to MCU.at PMU debug mode	4	rw	0x4
F0	ENABLE_1V5	Enable 1.5V dwell time. Defines the amount of time spent in the 'Enable 1V5' state. Allows 3v3 and 1v5 regs to settle.at PMU debug mode	4	rw	0x4

8.2.2.4 VBATCTRL

0x5000004C **VBATCTRL** ^

VBAT Monitor Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F27	F26	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F27	HIGH_DBNC	Battery Voltage High Status after deboucing. Battery monitor over voltage event signal coming from the debouncer of analog comparator circuit.	1	ro	0x0
F26	LOW_DBNC	Battery Voltage Low Status after debouncing. Battery monitor under voltage event signal coming from the debouncer of analog comparator circuit.	1	ro	0x0
F25	HIGH	Battery Voltage High Status. RAW battery monitor over voltage event signal coming from the analog comparator circuit.	1	ro	0x0
F24	LOW	Battery Voltage Low Status. RAW battery monitor under voltage event signal coming from the analog comparator circuit.	1	ro	0x0
F3	OV_POL	Battery Voltage Monitor Over Voltage Interrupt Event Polarity. Flips the over voltage event signal coming from the analog comparator circuit which feeds into the interrupt generator. 0x0: Native Polarity 0x1: Flip Polarity	1	rw	0x0
F2	UV_POL	Battery Voltage Monitor Under Voltage Interrupt Event Polarity. Flips the under voltage event signal coming from the analog comparator circuit which feeds into the interrupt generator.	1	rw	0x0

		0x0: Native Polarity 0x1: Flip Polarity			
F1	BAT_OV_EN	Battery Over Voltage Monitor Enable. Set to enable the vbat over voltage monitor analog comparator circuit.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE	1	rw	0x0
F0	BAT_UV_EN	Battery Under Voltage Monitor Enable. Set to enable the vbat under voltage monitor analog comparator circuit.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE	1	rw	0x0

8.2.2.5 VBATTRIM

0x50000050 **VBATTRIM** ^

VBAT Monitor Trim Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F24		-	-	-	-	F16				-	-	-	-	-	-	F8		-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F24	OVHYS	Battery Voltage Monitor Over Voltage Hysterisis Select. Selects the hysterisis level for the Over Voltage monitor.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE 0x0: 0.359V 0x1: 0.720V 0x2: 1.080V 0x3: 1.440V	2	rw	0x1
F16	OVLEVEL	Battery Voltage Monitor Over Voltage Select. Selects the reference level for the Over Voltage monitor to output one-hot Configuration to Analog Module.(If OVLEVEL>9, the actual analog trim value is the same as default value:OVLEVEL=0x07).The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE 0x0: Over Voltage Threshold- 10'h001: 14.75V 0x1: Over Voltage Threshold- 10'h002: 15.18V 0x2: Over Voltage Threshold- 10'h004: 15.65V 0x3: Over Voltage Threshold- 10'h008: 16.37V 0x4: Over Voltage Threshold- 10'h010: 16.85V 0x5: Over Voltage Threshold- 10'h020: 17.57V 0x6: Over Voltage Threshold- 10'h040: 18.30V 0x7: Over Voltage Threshold- 10'h080: 19.00V 0x8: Over Voltage Threshold- 10'h100: 19.97V 0x9: Over Voltage Threshold- 10'h200: 20.70V	4	rw	0x7
F8	UVHYS	Battery Voltage Monitor Under Voltage Hysterisis Select. Selects the hysterisis level for the Under Voltage monitor.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE 0x0: 0.475V 0x1: 0.835V 0x2: 1.225V 0x3: 1.635V	2	rw	0x1
F0	UVLEVEL	Battery Voltage Monitor Under Voltage Select. Selects the reference level for the Under Voltage monitor. If UVLEVEL[5:3]>0x04, the actual analog trim value is the same as UVLEVEL=0x0A. The UVLEVEL threshold is mononically increased with the setting.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE 0x0: Vf: 4.615V 0x1: Vf: 4.685V 0x7: Vf: 5.135V 0x8: Vf: 5.225V 0x9: Vf: 5.135V 0xa: Vf: 5.405V 0xf: Vf: 5.895V 0x10: Vf: 6.015V 0x11: Vf: 6.125V 0x17: Vf: 6.925V 0x18: Vf: 7.075V 0x19: Vf: 7.235V 0x1f: Vf: 8.385V 0x20: Vf: 8.605V 0x21: Vf: 8.845V 0x27: Vf:10.610V	6	rw	0xA

8.2.2.6 VBATDBNC

0x50000054 **VBATDBNC** ^

VBAT Debounce Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset

F5	OVSTRB1SEL	Low frequency strobing select for debouncing. Enables strobing 1 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 0 for quick acknowledgement of OV event.	1	rw	0x0
F4	OVSTRB0SEL	Low frequency strobing select for debouncing. Enables strobing 0 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 1 for debouncing of OV.	1	rw	0x1
F3	UVSTRB1SEL	Low frequency strobing select for debouncing. Enables strobing 1 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 0 for quick acknowledgement of UV event.	1	rw	0x0
F2	UVSTRB0SEL	Low frequency strobing select for debouncing. Enables strobing 0 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 1 for debouncing of UV.	1	rw	0x1
F1	OV	over voltage signal debounce enable. if set to '1, debounces the over voltage signal before going to over voltage interrupt generation else the signal bypass the debouncer	1	rw	0x1
F0	UV	under voltage signal debounce enable. if set to '1, debounces the under voltage signal before going to under voltage interrupt generation else the signal bypass the debouncer	1	rw	0x1

8.2.2.7 VBATDBNCTHRES

0x50000058 **VBATDBNCTHRES** ^

VBAT Monitor Threshold Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	OVTHRES0	Over Voltage debouncing threshold for 1to0 Transition. Sets the threshold for debouncing the over voltage event going from 1 to 0. It will require the ov event to stay high for the (OVTHRES0+1) number of LF/HF clocks to transit from a 1 to 0.	8	rw	0xFF
F16	UVTHRES0	Under Voltage debouncing threshold for 1to0 Transition. Sets the threshold for debouncing the under voltage event going from 1 to 0. It will require the uv event to stay high for the (UVTHRES0+1) number of LF/HF clocks to transit from a 1 to 0.	8	rw	0xFF
F8	OVTHRES1	Over Voltage debouncing threshold for 0to1 Transition. Sets the threshold for debouncing the over voltage event going from 0 to 1. It will require the ov event to stay high for the (OVTHRES1+1) number of LF/HF clocks to transit from a 0 to 1.	8	rw	0x1
F0	UVTHRES1	Under Voltage debouncing threshold for 0to1 Transition. Sets the threshold for debouncing the under voltage event going from 0 to 1. It will require the uv event to stay high for the (UVTHRES1+1) number of LF/HF clocks to transit from a 0 to 1.	8	rw	0x1

8.2.2.8 PMUIRQ

0x5000005C **PMUIRQ** ^

Voltage Monitor interrupts. Contains the the enable, clear, status and active flag for the Battery Voltage interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	OV	over voltage interrupt active.	1	ro	0x0
F24	UV	under voltage interrupt active.	1	ro	0x0
F17	OV	over voltage interrupt status.	1	ro	0x0
F16	UV	under voltage interrupt status.	1	ro	0x0
F9	OV	over voltage interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	UV	under voltage interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	OV	over voltage interrupt enable.	1	rw	0x0
F0	UV	under voltage interrupt enable.	1	rw	0x0

8.2.3 EVTHOLD

EVTHOLD		
Address	**Register Name**	**Description**
0x50000060	HOLD	Hold

8.2.3.1 HOLD

0x50000060 HOLD ^

Hold.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	HOLD	Hold. Set to prevent serialisation of new non-wakeup events in prepartion for hibernate mode. At the point of becoming set, a request to send the lullaby interrupt is automatically generated. The lullaby handler can then safely assert the PMUA->CTRL.HIBERNATE bit in order to put the device into hibernate mode.	1	wo	0x0

8.2.4 BTE

BTE		
Address	**Register Name**	**Description**
0x50000080	BTE_CTRL	BTE Control Register
0x50000084	BTE_SRAM_ADDR	BTE SRAM Address Register

8.2.4.1 BTE_CTRL

0x50000080 BTE_CTRL ^

BTE Control Register. This register can only be written if there is no ongoing transfer. If the BTE is transferring data, any writes to this register will be ignore

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F27	F26	F25	F24	F16								F0															

#	Field Name	Field Description	Width	Access	Reset
F27	START	An operation is initiated when this bit is set. The bit auto-clears when the block is complete.	1	rw	0x0
F26	BLOCKING	If set then the block transfer has priority over the MCU. If the MCU tries to use the bus, it will stall until the block transfer is complete. If not set, then the MCU waits only until the remainder of the current word completes and then waits until the bus is idle again before continuing.	1	rw	0x0
F25	TX_DIR	Transfer direction. If set then SRAM->ASIC otherwise ASIC->SRAM	1	rw	0x0
F24	INC_ADDR	if set then ASIC die address increments at the end of each transfer. Set to zero if the peripheral is a FIFO.	1	rw	0x0
F16	BXNUM	Number of 32-bit words to transfer.	8	rw	0x0
F0	BXADD	Address of the ASIC die (LSB). This is the lower 16 bits of the ASIC die address. The MSBs are 0x5001.	16	rw	0x0

8.2.4.2 BTE_SRAM_ADDR

0x50000084 BTE_SRAM_ADDR ^

BTE SRAM Address Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	BXSRAMADDR	Address of the SRAM (LSB). This is the lower 16 bits of the SRAM address. The MSBs are 0x2000.	16	rw	0x0

8.2.5 WICA

WICA		
Address	**Register Name**	**Description**
0x50010100	CTRL	Wakeup Control Register
0x50010104	STATUS	Wakeup Status Register

8.2.5.1 CTRL

0x50010100 **CTRL** ^

Wakeup Control Register. This is the control register for wakeup via gpio or lin or wut

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F14	-	F12	-	F10	F9	F5				-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F14	TIMER_IRQCLR	clear the wutimer_irq. writting a '1 to this register will clear the wutimer_irq	1	wo	0x0
F12	LINS_IRQCLR	clear the wulin_irq. writting a '1 to this register will clear the wulins_irq	1	wo	0x0
F10	TIMER_IRQENA	Timer Wakeup Interrupt Enable. if set, wutimer_irq is asserted if wakeup timer matches the tapsel	1	rw	0x1
F9	LINS_IRQENA	LIN Slave Wakeup Interrupt Enable. if set, wulin_irq is asserted if a wakeup signal is detected on the LIN_IN bus	1	rw	0x1
F5	TIMER_TAPSEL	WakeUp Timer Tap Select. Wakeup Time = 2^(WUT_TAPSEL) x Tlfclk(62.5us)	4	rw	0x4
F2	TIMER ENA	Wakeup Timer Enable. it enables the wakeup timer	1	rw	0x0
F1	LINS_WICA_SEL	LIN Slave Wakeup Source Select at Deepsleep mode. '1' select the source from LIN Slave Control. '0' select the source from pmu_pre5v(Default)	1	rw	0x0
F0	LINS_ENA	LIN Slave Wakeup Enable. it enables the detect of a wakeup signal on the LIN_IN bus	1	rw	0x0

8.2.5.2 STATUS

0x50010104 **STATUS** ^

Wakeup Status Register. This is the status register for wakeup via gpio or lin or wut

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	-	-	-	-	-	-	-	-	F2	-	F0

#	Field Name	Field Description	Width	Access	Reset
F16	TIMERCNT	Wakeup Timer Counter Value. Counter Value of the Wakeup Timer	16	ro	0x0
F2	TIMER	Wakeup Timer Status. This gets set if a wakeup timer is enabled and the count matches the tapsel setting during hibernate, CLRIRQ clears this Register	1	ro	0x0
F0	LINS	LIN Slave Wakeup Status. This gets set if a wakeup signal is detected on the LIN_IN bus when LINS SLEEP bit is set. CLRIRQ clears this Register	1	ro	0x0

8.2.6 WDTA

WDTA		
Address	**Register Name**	**Description**
0x50010300	CTRL	Control
0x50010304	STOP	Stop

0x50010308	CLEAR	Clear
0x5001030C	CNTVAL	Counter value
0x50010310	INT	WDTA Interrupts

8.2.6.1 CTRL

0x50010300 CTRL ^

Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F14	F12		F11	F8			-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F14	WINOPENFLAG	Window open flag. A flag that indicates when the watchdog window is open. It only can be cleared by Reg CLEAR! 0x0: Window is Closed 0x1: Window is Open	1	ro	0x0
F12	WINOPENSEL	Window Mode open select. Defines the watchdog window open time (the time between the watchdog start and the window open). 0x0: 1/2 * WDT timeout 0x1: 1/4 * WDT timeout 0x2: 1/8 * WDT timeout 0x3: 1/16* WDT timeout	2	rw	0x0
F11	WINOPENENA	Window Mode Enable. Enables Window Mode. 1'b1: Enable the Window mode of Watchdog, if the WDT is cleared before the time window opens, the WDT will issue a system reset. 1'b0: Disable the Window mode of Watchdog.	1	rw	0x0
F8	TIMEOUTSEL	Timeout select. Defines the watchdog timeout period (the time between a clear operation and the next timeout). 0x0: 2^10 * 62.5us ~= 128 ms 0x1: 2^11 * 62.5us ~= 256 ms 0x2: 2^12 * 62.5us ~= 512 ms 0x3: 2^13 * 62.5us ~= 1.0 s 0x4: 2^14 * 62.5us ~= 2.0 s 0x5: 2^15 * 62.5us ~= 4.0 s 0x6: 2^16 * 62.5us ~= 8.0 s 0x7: 2^17 * 62.5us ~= 16.0 s	3	rw	0x7
F1	RUNNING	Running status. A flag that indicates when the watchdog timer is enabled. 0x0: Watchdog timer is stopped and cleared 0x1: Watchdog timer is running	1	ro	0x0
F0	UPDATE	Window Mode Enable. Set to update Analog-Watchdog Configurations. NOTE: DO NOT change the CTRL register when it is high, which indicates there is an update in progress, It gets cleared by the core when the current update is done	1	dual	0x0

8.2.6.2 STOP

0x50010304 STOP ^

Stop.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F31	STOP_LOCK	Set Only bit. Set this bit to lock STOP bits.	1	rw	0x0
F0	STOP	Stop. Write the *stop* code (0xc3) to this register to reset the timer and disable the watchdog (e.g. during debug). If any other value is written to this register the watchdog will be enabled.	8	rw	0x55

8.2.6.3 CLEAR

0x50010308 CLEAR ^

Clear.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset

F0	CLEAR	Clear. Write the value 0x3c574ad6 (as a single word access) to reset the watchdog timer. Periodically performing this action is the expected method of preventing the watchdog from timing out (and resetting the MCU).	32	wo	0x0

8.2.6.4 CNTVAL

0x5001030C	CNTVAL	^

Counter value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	CNTVAL	Counter value. The instantaneous value of watchdog timeout counter	32	ro	0x0

8.2.6.5 INT

0x50010310	INT	^

WDTA Interrupts. Contains the ENABLE, CLEAR, STATUS and IRQ for the UART interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	WINOPEN	Window Open Interrupt. Set by WDTA timeout	1	ro	0x0
F24	WDTA	WDTA timeout Interrupt. Set by WDTA timeout	1	ro	0x0
F17	WINOPEN	Window Open Status. Set by WDTA timeout	1	ro	0x0
F16	WDTA	WDTA timeout Status. Set by WDTA timeout	1	ro	0x0
F9	WINOPEN	Window Open Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	WDTA	WDTA timeout Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	WINOPEN	Window Open Interrupt Enable.	1	rw	0x0
F0	WDTA	WDTA timeout Interrupt Enable.	1	rw	0x0

8.2.7 PWM

PWM		
Address	**Register Name**	**Description**
0x50010600	BASE	Base functions
0x50010604	PWMCNT	PWM Count Value
0x50010608	ENAREQ	Enable request
0x5001060C	ENASTS	Enable status
0x50010610	INIT	Intial State of Outputs
0x50010614	INV	Invert
0x50010618	UPDATE	Update
0x5001061C	PULSE0	PWM0 pulse setup
0x50010620	PULSE1	PWM1 pulse setup
0x50010624	PULSE2	PWM2 pulse setup
0x50010628	INTPOSEDGENA	PWM posedge interrupt enable
0x5001062C	INTNEGEDGENA	PWM negedge interrupt enable
0x50010630	INTPOSEDGCLR	PWM posedge interrupt control
0x50010634	INTNEGEDGCLR	PWM negedge interrupt control
0x50010638	INTPOSEDGSTS	PWM posedge interrupt status
0x5001063C	INTNEGEDGSTS	PWM negedge interrupt status
0x50010640	INTPOSEDGIRQ	PWM posedge interrupt active

0x50010644	INTNEGEDGIRQ	PWM negedge interrupt active
0x50010648	INTPWM	PWM interrupt control

8.2.7.1 BASE

0x50010600 **BASE** ^

Base functions.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	F8			-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

8.2.7.2 PWMCNT

0x50010604 **PWMCNT** ^

PWM Count Value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT	PWM counter value to give a sense about the current period	16	dual	0x0

8.2.7.3 ENAREQ

0x50010608 **ENAREQ** ^

Enable request.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F26	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F26	FORCEINACTIVE	Set to force PWM signals return to initial value immediately.	1	rw	0x0
F25	CLRREQALL	Write 1 to clear all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F24	ENAREQALL	Write 1 to enable all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F0	ENAREQ	Set to enable the waveform generator.	3	rw	0x0

8.2.7.4 ENASTS

0x5001060C **ENASTS** ^

Enable status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	ENASTS	Status of enable in the waveform generator.	3	ro	0x0

8.2.7.5 INIT

0x50010610	INIT	^

Intial State of Outputs.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INIT	Set to initialise the output waveform.	3	rw	0x0

8.2.7.6 INV

0x50010614	INV	^

Invert.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INVERT	Set to invert the output waveform.	3	rw	0x0

8.2.7.7 UPDATE

0x50010618	UPDATE	^

Update.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	UPDATE	Set to trigger consumption of new PULSE parameters (invert,prescale_sel,period,pulse start & stop). The flag is automatically cleared by the hardware when the settings are consumed, so reading a high value indicates that an update is still pending.	1	dual	0x0

8.2.7.8 PULSE0

0x5001061C	PULSE0	^

PWM0 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE0	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL0	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.7.9 PULSE1

0x50010620	PULSE1	^

PWM1 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE1	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL1	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.7.10 PULSE2

0x50010624	PULSE2	^

PWM2 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE2	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL2	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.7.11 INTPOSEDGENA

0x50010628	INTPOSEDGENA	^

PWM posedge interrupt enable. Contains the enable for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGENA	Interrupt enable. bit[2:0]: posedge interrupt enable.	3	rw	0x0

8.2.7.12 INTNEGEDGENA

0x5001062C	INTNEGEDGENA	^

PWM negedge interrupt enable. Contains the enable for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGENA	Interrupt enable. bit[2:0]: negedge interrupt enable.	3	rw	0x0

8.2.7.13 INTPOSEDGCLR

0x50010630	INTPOSEDGCLR	^

PWM posedge interrupt control. Contains the clear for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGCLR	Interrupt clear. bit[2:0] : posedge interrupt clear.	3	wo	0x0

8.2.7.14 INTNEGEDGCLR

0x50010634	INTNEGEDGCLR	^

PWM negedge interrupt control. Contains the clear for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGCLR	Interrupt clear. bit[2:0] : negedge interrupt clear.	3	wo	0x0

8.2.7.15 INTPOSEDGSTS

0x50010638	INTPOSEDGSTS	^

PWM posedge interrupt status. Contains the status for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGSTS	Interrupt status. bit[2:0] : posedge interrupt status.	3	ro	N/A

8.2.7.16 INTNEGEDGSTS

0x5001063C	INTNEGEDGSTS	^

PWM negedge interrupt status. Contains the status for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGSTS	Interrupt status. bit[2:0] : negedge interrupt status.	3	ro	N/A

8.2.7.17 INTPOSEDGIRQ

0x50010640	INTPOSEDGIRQ	^

PWM posedge interrupt active. Contains the active for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGIRQ	Interrupt active. bit[2:0] : posedge interrupt active.	3	ro	N/A

8.2.7.18 INTNEGEDGIRQ

0x50010644	INTNEGEDGIRQ	^

PWM negedge interrupt active. Contains the active for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGIRQ	Interrupt active. bit[2:0] : negedge interrupt active.	3	ro	N/A

8.2.7.19 INTPWM

0x50010648	INTPWM	^

PWM interrupt control. Contains the enable, clear, status and active for the PWM period & updated interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	UPD	Updated Interrupt active.	1	ro	N/A
F24	PERIOD	Period Interrupt active.	1	ro	N/A
F17	UPD	Updated Interrupt status.	1	ro	N/A
F16	PERIOD	Period Interrupt status.	1	ro	N/A
F9	UPD	Updated Interrupt clear.	1	wo	0x0
F8	PERIOD	Period Interrupt clear.	1	wo	0x0

F1	UPD	Updated Interrupt enable.	1	rw	0x0
F0	PERIOD	Period Interrupt enable.	1	rw	0x0

8.2.8 LINS

LINS		
Address	**Register Name**	**Description**
0x50010700	DATABYTE1	Data Byte 1
0x50010704	DATABYTE2	Data Byte 2
0x50010708	DATABYTE3	Data Byte 3
0x5001070C	DATABYTE4	Data Byte 4
0x50010710	DATABYTE5	Data Byte 5
0x50010714	DATABYTE6	Data Byte 6
0x50010718	DATABYTE7	Data Byte 7
0x5001071C	DATABYTE8	Data Byte 8
0x50010720	CTRL	Control Register
0x50010724	STATUS	Status
0x50010728	ERROR	Error Register
0x5001072C	DL	DATA Length Register
0x50010730	BTDIV07	Bit time Divider Register
0x50010734	BITTIME	Control Settings
0x50010738	ID	ID Register
0x5001073C	BUSTIME	Lin Bus Timing Register
0x50010740	STATUSEXT	Extended Status
0x50010744	WUPDETECTTHRES	Wakeup Detection Threshold
0x50010748	CONF	Extended Configuration Register for compatibility issue

8.2.8.1 DATABYTE1

0x50010700 **DATABYTE1** ^

Data Byte 1. DATA_BUF1~4 could be read/written through one word access to this register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	DATABUF4SHADOW	Data Buffer 2 Shadow. Shadow register of 4th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F16	DATABUF3SHADOW	Data Buffer 2 Shadow. Shadow register of 3rd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F8	DATABUF2SHADOW	Data Buffer 2 Shadow. Shadow register of 2nd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F0	DATABUF1	Data Buffer 1. 1st byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.8.2 DATABYTE2

0x50010704 **DATABYTE2** ^

Data Byte 2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF2	Data Buffer 2. 2nd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.8.3 DATABYTE3

0x50010708 **DATABYTE3** ^

Data Byte 3.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF3	Data Buffer 3. 3rd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.8.4 DATABYTE4

0x5001070C **DATABYTE4** ^

Data Byte 4.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF4	Data Buffer 4. 4th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.8.5 DATABYTE5

0x50010710 **DATABYTE5** ^

Data Byte 5.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	DATABUF8SHADOW	Data Buffer 8 Shadow. Shadow register of 8th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F16	DATABUF7SHADOW	Data Buffer 7 Shadow. Shadow register of 7th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F8	DATABUF6SHADOW	Data Buffer 6 Shadow. Shadow register of 6th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F0	DATABUF5	Data Buffer 5. 5th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.8.6 DATABYTE6

0x50010714 **DATABYTE6** ^

Data Byte 6.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF6	Data Buffer 6. 6th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.8.7 DATABYTE7

0x50010718 **DATABYTE7** ^

Data Byte 7.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF7	Data Buffer 7. 7th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.8.8 DATABYTE8

0x5001071C **DATABYTE8** ^

Data Byte 8.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF8	Data Buffer 8. 8th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.8.9 CTRL

0x50010720 **CTRL** ^

Control Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	-

#	Field Name	Field Description	Width	Access	Reset
F7	STOP	Stop Register. The host controller of the LIN slave has set this register if it handles a data request interrupt and can not make use of the frame content with the received identifier(e.g. extended identifiers). For that case the LIN slave stops the processing of the LIN communication until the next SYNC BREAK is detected. A read access to this bit delivers always the value 0 Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F6	SLEEP	Sleep Request. The bit is used by the LIN core to determine whether the LIN bus is in Sleep Mode or not. The host controller has to set the bit after sending or receiving a Sleep Mode frame. If DIS_AUTOSLEEP = 0, the bit will be set automatically by the LIN core if a bus idle timeout is detected. The host controller has to clear the bit after a wakeup signal is detected. NOTE: When the chip uses the LINs wakeup logic in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	1	rw	0x0
F5	TRANSMIT	Transmit Operation. The bit determines whether the current frame is a transmit frame or a receive frame for the LIN node. It has to be set by the host controller. 0x0: receive operation 0x1: transmit operation	1	rw	0x0
F4	DATAACK	Data Acknowledgement. The bit has to be set by the host controller of a LIN slave after handling a data request interrupt (compare STATUS.DATA_REQ register). The bit will be reset by the LIN core.	1	rw	0x0
F3	RSTINT	Reset interrupt. The host controller has to set this bit to reset the STATUS.INTR register and the interrupt request output of the LIN core. A read access to this bit delivers always the value 0.	1	wo	0x0
F2	RSTERR	Reset Error. The host controller has to set this bit to reset the error bits in status register and error register. A read access to this bit delivers always the value 0.	1	wo	0x0
F1	WAKEUPREQ	WakeUp Request. The bit has to be set by the host controller to terminate the Sleep Mode of the LIN bus by sending a Wakeup signal. The bit will be reset by the LIN core.	1	rw	0x0

8.2.8.10 STATUS

0x50010724 **STATUS** ^

Status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	ACTIVE	Lin Bus Active. The bit indicates whether the LIN bus is active or not. Note: For the LIN slave, this bit is set after the detection of a correct SYNC BREAK / SYNC FIELD sequence and it is reset at the end of the transmission or if the processing of the current frame is stopped by the host controller 0x0: no Lin bus activity 0x1: transmission on the LIN bus is active	1	ro	0x0
F6	BUSIDLETIMEOUT	BUS Idle Timeout. This bit is set by the LIN core if LIN is in hardware mode and no bus activity is detected for 4s~10s. In addition, an interrupt request to the host controller is generated in that case. After that, It is assumed that the LIN bus is in sleep mode and CTRL.SLEEP register will be set by the LIN core. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0

F5	ABORTED	Aborted. The bit is set if the processing of the current frame has been stopped by setting CTRL.STOP register. The bit is cleared by the LIN core after receiving a correct SYNC BREAK / SYNC FIELD sequence	1	ro	0x0
F4	DATAREQ	Data Request. The LIN core slave sets the bit after receiving the Identifier and requests an interrupt to the host controller. The host controller has to decode the Identifier to decide whether the current frame is a transmit or a receive operation. It has to adjust CTRL.TRANSMIT register and to load the data length. For transmit operations it has to load the data buffer too. After that the host controller has to set CTRL.DATA_ACK register	1	ro	0x0
F3	INTR	Interupt Request. The LIN core sets the bit when it requests an interrupt to the host controller. It has the same value as the interrupt output INTR. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register	1	ro	0x0
F2	ERROR	Lin Error. The LIN core sets the bit if an error has been detected (compare error register). The bit has to be reset by the host controller by setting the bit CTRL.RST_ERR register	1	ro	0x0
F1	WAKEUP	WakeUp. The bit is set when the LIN core is transmitting a Wakeup signal.	1	ro	0x0
F0	COMPLETE	Complete. The LIN core will set the bit after a transmission has been successfully finished and it will reset it at the start of a transmission	1	ro	0x0

8.2.8.11 ERROR

0x50010728 — **ERROR** — ^

Error Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F8	BITMONDATA	Bit Monitor Error occurred in Start or Data Bits. The Bit value monitored on the bus is different from the sent bit value and the error occurrs on the start or data bits.	1	ro	0x0
F7	BITMONSTOP	Bit Monitor Error occurred in Stop Bit. The Bit value monitored on the bus is different from the sent bit value and the error occurrs on the stop bit. In SAE2602, the error belongs to framing error.	1	ro	0x0
F6	FRAMEERR	Byte Field Framing Error. This bit is set by the LIN core slave if a transmission is aborted after the beginning of the data field due to a timeout or an incomplete frame	1	ro	0x0
F5	SBITERR	Start Bit Error in Byte field. Start Bit Error in Byte field, i.e., invalid start bit.	1	ro	0x0
F4	BITMON	Bit Monitor Error. The Bit value monitored on the bus is different from the sent bit value, bit monitor error will trigger an interrupt	1	ro	0x0
F3	PARITY	Parity Error. Identifier parity error	1	ro	0x0
F2	TIMEOUT	Timeout Error. There are several reason that can cause a timeout error: The master detects a timeout error if it is expecting data from the bus but no slave does respond. If the slave responds to late and the frame is not finished within the maximum frame length TFRAME_MAX a timeout error will be detected too. The slave detects a timeout error if it is requesting a data acknowledge to the host controller (for selecting receive or transmit, data length and loading data), and the host controller does not set CTRL.DATA_ACK or CTRL.STOP register until the end of the reception of the first byte after the identifier. The slave detects a timeout error if it has transmitted a wakeup signal and it detects no sync field (from the master) within 150 ms. Note: The slave does not perform an exact check of the frame length TFRAME_MAX but a timeout is detected after 200 bit times, if the slave is in receive mode and there are missing data fields or a missing ID field from the master.	1	ro	0x0
F1	CHK	Checksum Error. Checksum Error	1	ro	0x0
F0	BITERR	Bit Error in Byte field. Bit Error in Byte field, i.e., invalid stop bit.	1	ro	0x0

8.2.8.12 DL

0x5001072C — **DL** — ^

DATA Length Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F7	ENHCHK	Enhancement Check. The host controller has to set the checksum type used in the current frame by adjusting this register. 0x0: for classic checksum 0x1: for enhanced checksum	1	rw	0x0
F6	DISBITMON	Disable Bit Monitor. Set to disable the bit monitor during transmission. The bit must be set in case that RXD/TXD are separated.	1	rw	0x0
F5	DISAUTOSLEEP	Disable Auto Sleep. Set to Disable auto sleep.	1	rw	0x0

F0	LENGTH	Data Length. The host controller has to define the length of the data field of the current LIN frame by adjusting the data length register. If the data length is loaded with the value 1111b the length of the data field is decoded from Bit 5 and 4 of the identifier register id according to the Table below (e.g. compatibility to LIN specification 1.1). Otherwise the amount of data bytes can be written directly to the data length register (supported values are 0..8). **ID (Bit 5) ID (Bit 4) Number of Bytes in the data field** 0 0 2 0 1 2 1 0 4 1 1 8	4	rw	0x0

8.2.8.13 BTDIV07

0x50010730 **BTDIV07**

Bit time Divider Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	BTDIV07	Bt Div LSBs. Bit time divider [7:0]	8	rw	0xFF

8.2.8.14 BITTIME

0x50010734 **BITTIME**

Control Settings.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6		-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F6	PRESCL	Prescaler Register. Prescaler Setting	2	rw	0x3
F0	BTDIV8	Bt Div Most Significant bit. Bit time divider [8]	1	rw	0x1

8.2.8.15 ID

0x50010738 **ID**

ID Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	ID	ID. ID register	6	rw	0x0

8.2.8.16 BUSTIME

0x5001073C **BUSTIME**

Lin Bus Timing Register. Table 2-9 Control of time settings for wup_repeat_time and bus_inactivity_time

Bit 3	Bit 2	Bit 1	Bit 0	Time
0	0	0	0	Reset value
0	0			4 s (bus_inactivity_time)

0	1			6 s (bus_inactivity_time)
1	0			8 s (bus_inactivity_time)
1	1			10 s (bus_inactivity_time)
		0	0	180 ms (wup_repeat_time)
		0	1	200 ms (wup_repeat_time)
		1	0	220 ms (wup_repeat_time)
		1	1	240 ms (wup_repeat_time)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4	F2		F0	

#	Field Name	Field Description	Width	Access	Reset
F4	BUSDOMINANTRELEASEWUPENA	Bus Dominant Release Wakeup Enable. NOTE: When the chip uses the LINs bus idle detection in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	1	rw	0x0
F2	BUSINACTIVE	Bus Inactivity Time. NOTE: When the chip uses the LINs bus idle detection in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	2	rw	0x0
F0	WUPREPEAT	wakeup repeat time.	2	rw	0x0

8.2.8.17 STATUSEXT

0x50010740 **STATUSEXT** ^

Extended Status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2		F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	BUSIDLEMONITOR	Bus Idle Monitor Status. If LIN is in hardware mode, BIT[0] is set by the lin core if the bus has no activity for 4s~10s and BIT[1] is set by the lin core if LIN is stuck at dominant inactivity state for 4s~10s. Any bus transition will clear these two bits. LIN Slave's pullup will be disabled & LIN Master's pullup will be reduced to 30K when BIT[1] is set.	2	ro	0x0
F1	BUSIDLETIMEOUTDOMINANT	Dominant Bus Idle Timeout. The bit is set by the lin core if LIN is in hardware mode & the bus is stuck at dominant inactivity state for 4s~10s. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F0	COMPLETETX	Complete TX. The LIN core will set the bit after a TX transmission has been successfully finished and it will reset it at the start of a transmission.	1	ro	0x0

8.2.8.18 WUPDETECTTHRES

0x50010744 **WUPDETECTTHRES** ^

Wakeup Detection Threshold.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	WUPDETECTTHRES	Wakeup Detection Threshold. Threshold setting(LF_CLK_PREDIV clock cycls) of lin wakeup signal. For instace, if target threshold is 150us@LF_CLK_PREDIV=250KHz, WUP_DETECT_THRES = 150/(1000/250)-1. NOTE: When the chip uses the LINs wakeup logic in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	6	rw	0x24

8.2.8.19 CONF

0x50010748 **CONF** ^

Extended Configuration Register for compatibility issue.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset

F8	BITMONMODE	BIT Monitor Mode. Control the exit timing when bit monitor error occured. Only writable when the transaction is idle. 0x0: Default. The transmission finished immediately if bit_mon is detected. 0x1: Even bit_mon is detected, the transmission will not be finished until the byte transfer is completed.	1	rw	0x0
F0	INTERBYTECNT	Inter-Byte Space Bit Count. Bit count of inter-byte space. >= 1bit inter-byte space is required by some legacy LIN devices. Only writable when the transaction is idle.	2	rw	0x1

8.2.9 PWM_AUX

PWM_AUX		
Address	**Register Name**	**Description**
0x50010900	BASE0	Base 0 functions
0x50010904	PWMCNT0	PWM Count Value
0x50010908	BASE1	Base 1 functions
0x5001090C	PWMCNT1	PWM Count Value
0x50010910	BASESEL	Base Timer Select for individual Channels
0x50010914	ENAREQ	Enable request
0x50010918	ENASTS	Enable status
0x5001091C	INIT	Intial State of Outputs
0x50010920	INV	Invert
0x50010924	UPDATE	Update
0x50010928	PULSE0	PWM0 pulse setup
0x5001092C	PULSE1	PWM1 pulse setup
0x50010930	PULSE2	PWM2 pulse setup
0x50010934	PULSE3	PWM3 pulse setup
0x50010938	INTPOSEDGENA	PWM posedge interrupt enable
0x5001093C	INTNEGEDGENA	PWM negedge interrupt enable
0x50010940	INTPOSEDGCLR	PWM posedge interrupt control
0x50010944	INTNEGEDGCLR	PWM negedge interrupt control
0x50010948	INTPOSEDGSTS	PWM posedge interrupt status
0x5001094C	INTNEGEDGSTS	PWM negedge interrupt status
0x50010950	INTPOSEDGIRQ	PWM posedge interrupt active
0x50010954	INTNEGEDGIRQ	PWM negedge interrupt active
0x50010958	INTPERIOD	PWM Period interrupt control
0x5001095C	INTUPDATED	PWM Updated interrupt control

8.2.9.1 BASE0

0x50010900 **BASE0** ^

Base 0 functions.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	F8			-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD0	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL0	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

8.2.9.2 PWMCNT0

0x50010904 — **PWMCNT0**

PWM Count Value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT0	PWM counter value to give a sense about the current period	16	ro	0x0

8.2.9.3 BASE1

0x50010908 — **BASE1**

Base 1 functions.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	F8			-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD1	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL1	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

8.2.9.4 PWMCNT1

0x5001090C — **PWMCNT1**

PWM Count Value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT1	PWM counter value to give a sense about the current period	16	ro	0x0

8.2.9.5 BASESEL

0x50010910 — **BASESEL**

Base Timer Select for individual Channels.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	BASE_SEL	Base Selects: bit0:1=PWM0 Select BASE1, 0=PWM0 Select BASE0. bit1:1=PWM1 Select BASE1, 0=PWM1 Select BASE0.	4	rw	0x0

8.2.9.6 ENAREQ

0x50010914 — **ENAREQ**

Enable request.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	F26	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		
#	**Field Name**								**Field Description**																	**Width**	**Access**	**Reset**
F26	FORCEINACTIVE								Set to force PWM signals return to initial value immediately.																	1	rw	0x0
F25	CLRREQALL								Write 1 to clear all ENA_REQ bits; Write 0 has no effects.																	1	wo	0x0
F24	ENAREQALL								Write 1 to enable all ENA_REQ bits; Write 0 has no effects.																	1	wo	0x0
F0	ENAREQ								Set to enable the pwm channel.																	4	rw	0x0

8.2.9.7 ENASTS

0x50010918 — **ENASTS**

Enable status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	ENASTS	Status of enable in the pwm channel.	4	ro	0x0

8.2.9.8 INIT

0x5001091C — **INIT**

Intial State of Outputs.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INIT	Set to initialise the output waveform.	4	rw	0x0

8.2.9.9 INV

0x50010920 — **INV**

Invert.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INVERT	Set to invert the output waveform.	4	rw	0x0

8.2.9.10 UPDATE

0x50010924 — **UPDATE**

Update.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F0	UPDATE	Set to trigger consumption of new PULSE parameters (invert,prescale_sel,period,pulse start & stop). The flag is automatically cleared by the hardware when the settings are consumed, so reading a high value indicates that an update is still pending.	2	dual	0x0

8.2.9.11 PULSE0

0x50010928 — **PULSE0**

PWM0 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

F16		F0			
#	Field Name	Field Description	Width	Access	Reset
F16	PRISE0	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL0	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.9.12 PULSE1

0x5001092C	PULSE1	^

PWM1 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE1	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL1	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.9.13 PULSE2

0x50010930	PULSE2	^

PWM2 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE2	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL2	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.9.14 PULSE3

0x50010934	PULSE3	^

PWM3 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE3	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL3	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.9.15 INTPOSEDGENA

0x50010938	INTPOSEDGENA	^

PWM posedge interrupt enable. Contains the enable for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGENA	Interrupt enable. bit[3:0]: posedge interrupt enable.	4	rw	0x0

8.2.9.16 INTNEGEDGENA

0x5001093C	INTNEGEDGENA	^

PWM negedge interrupt enable. Contains the enable for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGENA	Interrupt enable. bit[3:0]: negedge interrupt enable.	4	rw	0x0

8.2.9.17 INTPOSEDGCLR

0x50010940	INTPOSEDGCLR	^

PWM posedge interrupt control. Contains the clear for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGCLR	Interrupt clear. bit[3:0] : posedge interrupt clear.	4	wo	0x0

8.2.9.18 INTNEGEDGCLR

0x50010944	INTNEGEDGCLR	^

PWM negedge interrupt control. Contains the clear for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGCLR	Interrupt clear. bit[3:0] : negedge interrupt clear.	4	wo	0x0

8.2.9.19 INTPOSEDGSTS

0x50010948	INTPOSEDGSTS	^

PWM posedge interrupt status. Contains the status for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGSTS	Interrupt status. bit[3:0] : posedge interrupt status.	4	ro	N/A

8.2.9.20 INTNEGEDGSTS

0x5001094C	INTNEGEDGSTS	^

PWM negedge interrupt status. Contains the status for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGSTS	Interrupt status. bit[3:0] : negedge interrupt status.	4	ro	N/A

8.2.9.21 INTPOSEDGIRQ

0x50010950	INTPOSEDGIRQ	^

PWM posedge interrupt active. Contains the active for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGIRQ	Interrupt active. bit[3:0] : posedge interrupt active.	4	ro	N/A

8.2.9.22 INTNEGEDGIRQ

0x50010954 **INTNEGEDGIRQ** ^

PWM negedge interrupt active. Contains the active for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGIRQ	Interrupt active. bit[3:0] : negedge interrupt active.	4	ro	N/A

8.2.9.23 INTPERIOD

0x50010958 **INTPERIOD** ^

PWM Period interrupt control. Contains the enable, clear, status and active for the PWM period interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F24		-	-	-	-	-	-	F16		-	-	-	-	-	-	F8		-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F24	PERIOD	Period Interrupt active.	2	ro	N/A
F16	PERIOD	Period Interrupt status.	2	ro	N/A
F8	PERIOD	Period Interrupt clear.	2	wo	0x0
F0	PERIOD	Period Interrupt enable.	2	rw	0x0

8.2.9.24 INTUPDATED

0x5001095C **INTUPDATED** ^

PWM Updated interrupt control. Contains the enable, clear, status and active for the PWM updated interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F24		-	-	-	-	-	-	F16		-	-	-	-	-	-	F8		-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F24	UPD	Updated Interrupt active.	2	ro	N/A
F16	UPD	Updated Interrupt status.	2	ro	N/A
F8	UPD	Updated Interrupt clear.	2	wo	0x0
F0	UPD	Updated Interrupt enable.	2	rw	0x0

8.2.10 SAR_CTRL

SAR_CTRL

Address	Register Name	Description
0x50010D00	DATA1	Data Out of CH1,
0x50010D04	DATA2	Data Out of CH2,
0x50010D08	DATA3	Data Out of CH3,
0x50010D0C	DATA4	Data Out of CH4,
0x50010D10	SARANACFG	SAR Analog Configuration Register
0x50010D14	SARCFG	SAR Configuration Register
0x50010D18	AFECTRL	SAR AFE Control

0x50010D1C	SARCTRL	SAR ADC Control
0x50010D20	ADCCHCONF	ADC Channel Configuration
0x50010D24	SARINT	SAR Interrupts
0x50010D28	SARCLKDIV	SAR CLOCK DIVIDE

8.2.10.1 DATA1

0x50010D00 **DATA1** ^

Data Out of CH1,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA1	The result of ADC conversion of CH1(in 2's-complement)	16	ro	0x0

8.2.10.2 DATA2

0x50010D04 **DATA2** ^

Data Out of CH2,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA2	The result of ADC conversion of CH2(in 2's-complement)	16	ro	0x0

8.2.10.3 DATA3

0x50010D08 **DATA3** ^

Data Out of CH3,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA3	The result of ADC conversion of CH3(in 2's-complement)	16	ro	0x0

8.2.10.4 DATA4

0x50010D0C **DATA4** ^

Data Out of CH4,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA4	The result of ADC conversion of CH4(in 2's-complement)	16	ro	0x0

8.2.10.5 SARANACFG

0x50010D10 **SARANACFG** ^

SAR Analog Configuration Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F7	SARPREAMPEN	adc pre-amp enable. 0:disable, 1:enable	1	rw	0x0

F0	ADCVREFSEL	adc vref select. 0x0: adc_vref = vbg when sar_ena_req=1 0x1: adc_vref = 2*vbg when sar_ena_req=1 0x2: adc_vref = VDD_3V3 when sar_ena_req=1 0x3: adc_vref = VDD_3V3 when sar_ena_req=1	2	rw	0x1

8.2.10.6 SARCFG

0x50010D14 — **SARCFG** ^

SAR Configuration Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	F16				-	-	F12		F8				F7	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F16	TRIGDLY	trigger delay. setting trigger delay time from 0 to 15 sar clock cycles. For PN-detect, trigger delay MUST >= 2us.	4	rw	0x8
F12	PWMSEL	PWM Trigger Signal Selects. Selects the source PWM channel.	2	rw	0x0
F8	TRIGSEL	SAR Converion Trigger Selects. Selects the trigger condition of SAR ADC. Don't change the bits during an ADC conversion sequence is ongoing. 0x1: Triggered through writing 1 to conversion bit. 0x2: Triggered by the PWM posedge. 0x4: Triggered by the PWM negedge. 0x8: Triggered by PWM period.	4	rw	0x0
F7	ROUND	ADC round enable. Enable ADC round. 0x0: No round. 0x1: Negative code+1	1	rw	0x1
F0	SAMPCYC	Sample cycle. setting sampling time from 1 to 16 sar clock cycles. 0x0: 1 Cycle 0x1: 2 Cycle 0x2: 3 Cycle 0xf: 16 Cycle	4	rw	0x7

8.2.10.7 AFECTRL

0x50010D18 — **AFECTRL** ^

SAR AFE Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F14		-	-	-	-	F8		F7	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F14	SARINPUTGAIN	choose ADC input gain. 0x0: 22/32 0x1: 31/32	2	rw	0x1
F8	SARINPUTMODE	ADC AFE Input Modes. Select ADC AFE Input Modes. 0x0: All external. 0x1: VINP buffered, VINN external. 0x2: VINN buffered, VINP external. 0x3: Both VINP & VINN buffered.	2	rw	0x3
F7	SARAFEEN	ADC AFE Enable. adc afe enable. If vinp, vinn and vin vcm all choose external, adc afe should be disabled: adc_adc_en=0, otherwise, adc afe must be enabled: adc_afe_en=1.	1	rw	0x0
F0	ADCSELVINVCMEXT	Select External Inputs to ADC. choose ADC input common voltage. 0: choose internal vin_vcm, equals to (vinp+vinn)/2; 1: choose external vin_vcm, for PN detect.	1	rw	0x0

8.2.10.8 SARCTRL

0x50010D1C — **SARCTRL** ^

SAR ADC Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	F18	-	F16	-	-	-	-	-	F10	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F18	CONT	Continuous Conversion Enable. If this bit has been set before an ADC conversion sequence trigged by CONVERT bit or PWM signals, the sequence will be treated as a sequential conversion, rather than a single conversion.	1	rw	0x0

F16	CONVERT	ADC START/STATUS Register. If SOFTWARE trigger source is selected, set to start a conversion, If SARBAUD trigger source is selected, set to activate the internal baud generator. The tick of the buad generator will trigger an ADC conversion. Read 1 indicates ADC conversion is active; Read 0 indicates ADC is in idle state.	1	dual	0x0
F10	DIGRESET	SAR Digital Part Reset. Resets SAR digital parts. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F0	SARENAREQ	SAR ADC Enable. Set to enable the SAR analog & digital part	1	rw	0x0

8.2.10.9 ADCCHCONF

0x50010D20 **ADCCHCONF** ^

ADC Channel Configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	F24					-	-	-	F16					-	-	-	F8					F3				F0			

#	Field Name	Field Description	Width	Access	Reset
F31	TESTBATTERYGAINCHOOSE	VBAT Gain Select. 0: gain=1/14, vbat max 30V/14=2.14v, under ADC vref=2.4v 1: gain=1/28, vbat max 30V/28=1.07v, under ADC vref=1.2v	1	rw	0x0
F24	CH4SEL	Channel4 Selection. Refer to Channel1 Selects.	5	rw	0x0
F16	CH3SEL	Channel3 Selection. Refer to Channel1 Selects.	5	rw	0x0
F8	CH2SEL	Channel2 Selection. Refer to Channel1 Selects.	5	rw	0x0
F3	CH1SEL	Channel1 Selection. Channel1 Selects. 0x1: adc_vinp=adc_refp , adc_vinn=adc_refp (all shot to adc_ref(2.4V) for adc channel offset K) 0x2: adc_vinp=adc_refp , adc_vinn=vref_gnd (for adc channel +gain error K) 0x3: adc_vinp=vref_gnd , adc_vinn=adc_refp (for adc channel -gain error K) 0x4: adc_vinp=TempSensor , adc_vinn=vref_gnd 0x5: adc_vinp=VDD_1V5 , adc_vinn=vref_gnd 0x6: adc_vinp=VDD_3V3 , adc_vinn=vref_gnd 0x7: adc_vinp=VDD_PRE5V (1/4) , adc_vinn=vref_gnd 0x8: adc_vinp=VBAT ACCURATE (gain selected by TEST_BATTERY_GAIN_CHOOSE), adc_vinn=vref_gnd 0x9: adc_vinp=LED0 , adc_vinn=vref_gnd 0xa: adc_vinp=LED1 , adc_vinn=vref_gnd 0xb: adc_vinp=LED2 , adc_vinn=vref_gnd 0xc: adc_vinp=GPIO1 , adc_vinn=vref_gnd 0xd: adc_vinp=GPIO2 , adc_vinn=vref_gnd 0xe: adc_vinp=GPIO3 , adc_vinn=vref_gnd 0xf: adc_vinp=GPIO4 , adc_vinn=vref_gnd 0x10: adc_vinp=VBAT , adc_vinn=LED0 (with gain selected by ioctrla.LED.GAIN_SEL) 0x11: adc_vinp=VBAT , adc_vinn=LED1 (with gain selected by ioctrla.LED.GAIN_SEL) 0x12: adc_vinp=VBAT , adc_vinn=LED2 (with gain selected by ioctrla.LED.GAIN_SEL)	5	rw	0x0
F0	SEQCNT	Channel Sequence count. Selects the sequence of channels to be converted 0x1: CH1 only 0x2: CH1->CH2 0x3: CH1->CH2->CH3 0x4: CH1->CH2->CH3->CH4	3	rw	0x0

8.2.10.10 SARINT

0x50010D24 **SARINT** ^

SAR Interrupts. Contains the enable, status and clear for the SAR interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	F16	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F24	INT_CONV_DONE	Convert Done Interrupt. Set by the SAR when an convert done occurs	1	ro	0x0
F16	CONV_DONE	Convert Done. Set by the SAR when an conversion is done.	1	ro	0x0
F8	INT_CONV_DONE_CLR	Convert Done Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F0	INT_CONV_DONE_ENA	Convert Done Interrupt Enable.	1	rw	0x0

8.2.10.11 SARCLKDIV

0x50010D28	SARCLKDIV	^

SAR CLOCK DIVIDE. sar clock divider. sar_div_clk is divided from system clock, sar_div_clk maximum frequency is 4Mhz.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	SARCLKDIV	SAR CLOCK DIVIDE.	8	rw	0x5

8.2.11 IOCTRLA

IOCTRLA		
Address	**Register Name**	**Description**
0x50011000	GPIO1	GPIO Pin 1 Control
0x50011004	GPIO2	GPIO Pin 2 Control
0x50011008	GPIO3	GPIO Pin 3 Control
0x5001100C	GPIO4	GPIO Pin 4 Control
0x50011010	LIN	LIN Pin Control
0x50011014	LINSGFCONF	LINS Glitch Filter Configuration in active mode
0x50011018	LINTXDMONITOR	LIN TXD Dominant Timeout
0x5001101C	LED	LED Pin Control
0x50011020	ANALOGTESTMUXOVERRIDE	Analog Testmux Override
0x50011024	IRQ	IOCTRLA LINS TXD Dominant Monitor interrupts
0x50011028	LINSGFCONF1	LINS Glitch Filter Configuration in active mode
0x5001102C	FILT_ACCESS	Glitch Filter access key
0x50011030	IOCAPTURE	IO capture controller
0x50011034	IOCAPTUREPERIOD0	
0x50011038	IOCAPTUREPERIOD1	
0x5001103C	COUNTERGPIO0	
0x50011040	COUNTERGPIO1	
0x50011044	COUNTERGPIO2	
0x50011048	COUNTERGPIO3	
0x5001104C	IOGFCONF	IO capture Glitch Filter Configuration in active mode

8.2.11.1 GPIO1

0x50011000	GPIO1	^

GPIO Pin 1 Control. GPIO Pin 1 has 8 seperate drivers: GPIO Controller, PWM Controller, Testmux, LINS_RXD from GPIO, LINS signle wire mode, LINS_RX from PHY and outputs of 3 stages LINS_RXD Glitch filter.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F24						-	-	F16						-	-	-	-	-	-	-	-	-	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F24	MUXSEL	GPIO1_MUXSEL:Selects debug signal to be output on gpio1. 0x0: PMUA (Power Management Unit Asic) QACK 0x1: PMUA (Power Management Unit Asic) Wakeup signal 0x2: PMUA (Power Management Unit Asic) snowflake 0x3: LIN Slave Output of 1st Stage Glitch Filter 0x4: LIN Slave Output of 2nd Stage Glitch Filter 0x5: LIN Slave Output of 3rd Stage Glitch Filter 0x6: LIN Slave PHY Output Rxd 0x7: LIN Slave PHY Input Txd 0x8: CRGA (Clock Reset Generation Asic) (scan_test_mode | lf_rc_clk) 0x9: CRGA (Clock Reset Generation Asic) (scan_test_mode | hf_rc_clk) 0xa: CRGA (Clock Reset Generation Asic) (scan_test_mode | lf_rc_sts) 0xb: CRGA (Clock Reset Generation Asic) (scan_test_mode | hf_rc_sts) 0xc: CRGA (Clock Reset Generation Asic) (scan_test_mode | clk_sys_gated) 0xd: CRGA (Clock Reset Generation Asic) (a_por_n) 0xe: CRGA (Clock Reset Generation Asic) (bor_3v3_n) 0xf: CRGA (Clock Reset Generation Asic) (ovtemp_flag) 0x10: CRGA (Clock Reset Generation Asic) (bor_1v5_n)	6	rw	0x0

		0x11: CRGA (Clock Reset Generation Asic) (wdt_bark) 0x12: ADC controller clk adc_clk_in 0x22: LIN Slave Input of Core rxd 0x23: LIN Slave Output of Core txd 0x24: BOR CONTROL STATE MACHINE state[0] 0x25: BOR CONTROL STATE MACHINE state[1] 0x26: BOR CONTROL STATE MACHINE bor_bias_ena 0x27: BOR CONTROL STATE MACHINE bor_bias_ena_l 0x28: BOR CONTROL STATE MACHINE pmua_bor_bias_ena 0x29: BOR CONTROL STATE MACHINE hf_clk_allowed 0x2a: BOR CONTROL STATE MACHINE hf_active 0x2b: BOR CONTROL STATE MACHINE pmua_bor_arm_sync 0x2c: BATTERY VOLTAGE MONITOR vbat_low 0x2d: BATTERY VOLTAGE MONITOR vbat_high 0x2e: BATTERY VOLTAGE MONITOR vbat_low_flag 0x2f: BATTERY VOLTAGE MONITOR vbat_high_flag 0x30: BATTERY VOLTAGE MONITOR vbat_low_dbnc 0x31: BATTERY VOLTAGE MONITOR vbat_high_dbnc			
F16	GPIO2_MUXSEL	Selects debug signal to be output on gpio2. Refer to GPIO1_MUXSEL for signal selection	6	rw	0x0
F6	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F5	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F4	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F3	LINS_SEL	LINS Connection Select. 0x0: LINS RXD External input Mode. 0x1: Single wire mode, LINS RXD/LINS TXD, Open-drain output.	1	rw	0x0
F0	HWMODE	hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x3: GPIO1_LINS_SEL=0 : LINS RXD; GPIO1_LINS_SEL=1 : Single wire mode, LINS RXD/LINS TXD, Open-drain output. 0x4: Monitor 1st Stage input of LINS RX Glitch filter. 0x5: Monitor 1st Stage output of LINS RX Glitch filter. 0x6: Monitor 2nd Stage output of LINS RX Glitch filter. 0x7: Monitor 3rd Stage output of LINS RX Glitch filter.	3	rw	0x0

8.2.11.2 GPIO2

0x50011004 **GPIO2** ^

GPIO Pin 2 Control. GPIO Pin 2 has four seperate drivers: GPIO Controller, PWM Controller, Testmux, LINS_TXD and outputs of 3 stages LINS_RXD Glitch filter.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6	F5	F4	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F6	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F5	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F4	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: LINS PHY TXD Drive Mode. GPIO input connects to LINS PHY TXD. DEBUG Access must be enabled in the system control block to drive LINS PHY TXD outputs. 0x3: LINS Core TXD Monitor. 0x4: Testmux Mode. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x5: Monitor 1st Stage output of LINS RX Glitch filter. 0x6: Monitor 2nd Stage output of LINS RX Glitch filter. 0x7: Monitor 3rd Stage output of LINS RX Glitch filter.	3	rw	0x0

8.2.11.3 GPIO3

0x50011008	GPIO3	^

GPIO Pin 3 Control. GPIO Pin 3 has 8 seperate drivers: GPIO Controller, PWM Controller, LINS_RXD monitor, LINS_RXD from GPIO, LINS signle wire mode and outputs of 3 stages LINS_RXD Glitch filter.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F6	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F5	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F4	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F3	LINS_SEL	LINS Connection Select. 0x0: LINS RXD External input Mode. 0x1: Single wire mode, LINS RXD/LINS TXD, Open-drain output.	1	rw	0x0
F0	HWMODE	hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: LINS RXD which is input of lins_core connects to GPIO output. 0x3: LINS_SEL=0 : LINS RXD; LINS_SEL=1 : Single wire mode, LINS RXD/LINS TXD, Open-drain output. 0x4: Monitor 1st Stage input of LINS RX Glitch filter. 0x5: Monitor 1st Stage output of LINS RX Glitch filter. 0x6: Monitor 2nd Stage output of LINS RX Glitch filter. 0x7: Monitor 3rd Stage output of LINS RX Glitch filter.	3	rw	0x0

8.2.11.4 GPIO4

0x5001100C	GPIO4	^

GPIO Pin 4 Control. GPIO Pin 8 has four seperate drivers: GPIO Controller, PWM Controller ,LINS_TXD from GPIO, LINS_TXD Monitor and outputs of 3 stages LINS_RXD Glitch filter.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6	F5	F4	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F6	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F5	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F4	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. GPIO input connects to LINS TXD. 0x3: LINS CORE TXD Monitor 0x4: Monitor 1st Stage input of LINS RX Glitch filter. 0x5: Monitor 1st Stage output of LINS RX Glitch filter. 0x6: Monitor 2nd Stage output of LINS RX Glitch filter. 0x7: Monitor 3rd Stage output of LINS RX Glitch filter.	3	rw	0x0

8.2.11.5 LIN

0x50011010	LIN	^

LIN Pin Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	F24	-	-	-	-	-	F18	-	-	F12					F8				F7	F6	F5	-	F3	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F31	UPDATE	LIN Configure Update. Set to update the Configurations to PRE5V domains. NOTE: DO NOT change the CTRL register when it is high, which indicates there is an update in progress, It gets cleared by the core when the current update is done	1	dual	0x0
F24	PMODE	LIN Power Mode. Control LINS power state in hibernate mode. 0x0: Regardless of the related enable bits, LIN TX analog parts will be shut-down in hibernate mode, unless any LIN dominant signal is detected. 0x1: LIN TX analog parts are still controlled by theirs corresponding enable bits.	1	rw	0x0
F18	LINS_PUOFF_TIMEOUT	LINS Pullup Disable in dominant TimeOut condition. Set to disable LINS 30K pullup in case that lin bus is shorted to ground(Bus idle dominant timeout is detected) for saving power. LINS Pullup will be recovered automatically if bus idle dominant timeout is released by any bus activity. Only reset by power-on sequence. NOTE: The write operation of this register takes effect by PMUA_SFRS->CTRL.UPDATE	1	rw	0x1
F12	LINS_SLEEP_GF_THRES1	LINS RXD glitch filter threshold for 0 to 1, detect '1' width of (T_clk_lf*resetvalue = 4us*3 = 12[us], NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK and IOCTRLA_SFRS->LIN.UPDATE	4	rw	0x0
F8	LINS_SLEEP_GF_THRES0	LINS RXD glitch filter threshold for 1 to 0, detect '0' width of (T_clk_lf*resetvalue = 4us*3 = 12[us], NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK and IOCTRLA_SFRS->LIN.UPDATE	4	rw	0x1
F7	LINS_RXD_HIGH_RST_ENA	Enable signal that LINs RXD glitch filter at sleep mode is asynchronous reset by high of LINs_RXD. NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK and IOCTRLA_SFRS->LIN.UPDATE	1	rw	0x0
F6	LINS_RXENA	LIN receive enable. NOTE: The write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	1	rw	0x0
F5	LINS_TXENA	LIN transmit enable.	1	rw	0x0
F3	LINS_PU30K_ENA	LIN 30K pullup enable.	1	rw	0x1
F0	LINS_HWMODE	LIN Slave hardware mode. 0x0: Hardware Mode Disabled. GPIO2 writes/reads the LIN I/O pin. 0x1: Hardware Mode Enabled. LIN peripheral writes/reads the LIN I/O pin.	1	rw	0x0

8.2.11.6 LINSGFCONF

0x50011014 **LINSGFCONF** ^

LINS Glitch Filter Configuration in active mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	F16							-	F8							-	-	-	-	F3	F2	F0	

#	Field Name	Field Description	Width	Access	Reset
F16	LINSDBNCTHRES1	3rd Stage LINS Debounce Threshold for 0 to 1. 3rd Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*40 = 2.5[us]. NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	7	rw	0x49
F8	LINSDBNCTHRES0	3rd Stage LINS Debounce Threshold for 1 to 0. 3rd Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*40 = 2.5[us]. NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	7	rw	0x49
F3	LINS_RX_GF_ENA_2ND	LINS RXD 2nd Glitch Filter enables. Enable LINS Glitch Filter 2nd stage. NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	1	rw	0x1
F2	LINS_RX_GF_ENA_1ST	LINS RXD 1st Glitch Filter enables. Enable LINS Glitch Filter 1st stage. NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	1	rw	0x1
F0	LINSRXGFENA	LINS RXD Glitch Filter enables. Bit0: Enable LINS Glitch Filter 3rd stage; Bit1: Enable LINS Glitch Filter for Sleep Mode. NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	2	rw	0x3

8.2.11.7 LINTXDMONITOR

0x50011018	LINTXDMONITOR	^

LIN TXD Dominant Timeout.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F8	LINSTXDTIMEOUTDOMINANT	Tx Dominant Timeout. The bit is set by LINS TxD monitor if LINS's TxD is stuck at dominant output for 64ms. A dominant to recessive transition of the TxD will clear this bit. LIN's TX will be disabled automatically when this bit is set.	1	ro	0x0
F0	LINSTXDMONITORENA	LINS TxD Monitor enable.	1	rw	0x1

8.2.11.8 LED

0x5001101C	LED	^

LED Pin Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F24			F22		F19			F17		F16	F15	-	-	-	F9			F8	-	F4			-	F0		

#	Field Name	Field Description	Width	Access	Reset
F24	LED_PULLUP_EN	LED PULLUP ENABLE. LED PAD Pullup enable, ONE HOT code. 0x1: LED0 PAD pullup to PRE5V through a diode and a 50K resistor 0x2: LED1 PAD pullup to PRE5V through a diode and a 50K resistor 0x4: LED2 PAD pullup to PRE5V through a diode and a 50K resistor	3	rw	0x0
F22	OP_GBW_SEL	LED SENSE OP GBW SEL. PN detect fully differential Op GBW choose 00: 3M 01: 5M 10: 8M 11: 10M	2	rw	0x1
F19	OP_CHOOSE_R	LED SENSE OP CHOOSE R. choose nulling resistor to do frequency compensation. Which denpends on the bandwidth of the OP. R R GBW(CL=3pF) 000 0.5K 11(10M) 001 2.5K 10(8M) 01(5M) 010 4.5K 011 6.5K 11(3M) 100 8.5K 101 10.5K 110 12.5K 111 14.5K	3	rw	0x1
F17	PN_OP_START_BIAS_BOOST	PN OP START BIAS BOOST. PN diff OP start bias current 00: 250nA 01: 500nA 10: 750nA 11: 1uA	2	rw	0x0
F16	GAIN_SEL	LED Sense AFE gain select. V_ADC = (vbat-vled)*GAIN , where V_ADC is voltage to ADC LED channle, and GAIN is selected by GAIN_SEL as following: 0x0: GAIN = 0.533 0x1: GAIN = 0.533/2	1	rw	0x0
F15	VFW_ENA	LED Forward Voltage Current Enable. Set to enable the independent LED VFW current source(maximum=5mA). When ADC CH2 measurement is active, the LED channel selected by CH2 SEL will be driven by LED VFW current source.	1	rw	0x0
F9	SENSE_CTRL	LED. LED Sense Control bits for override control/debug.	3	rw	0x0
F8	SENSE_ENA	LED Forward Voltage Sense Enable. Set to enable LED forward voltage sense module. After setting this bit, it's recommended to wait ~40us before ADC conversion for LED_SENSE to settle down.	1	rw	0x1
F4	DATA	LED Data Out. When the LED hardware mode is disabled, then the data in this register bit is used to drive the LED driver. Each bit controls the corresonding LED Channel respectively.	3	rw	0x0
F0	HWMODE	LED hardware mode. LED Hardware Mode Enable. Each bit controls the corresponding LED Channel respectively. 0x0: Hardware Mode Disabled. LED_DATA register drives the LED Data Output pin. Read is not available on this pin. 0x1: Hardware Mode Enabled. PWM_BARIUM peripheral drives the LED Data Output pin. Read is not available on this pin.	3	rw	0x0

8.2.11.9 ANALOGTESTMUXOVERRIDE

0x50011020 **ANALOGTESTMUXOVERRIDE** ^

Analog Testmux Override. This register controls the multiplexers for analog signals.
The select bit allows firmware to control the corresponding select field (in other words, firmware control).
The following table is intended to be a helpful guide in what data should be written to this register in order to connect a source and target together.
Note- Care should be taken to write zero to this register between connection changes. This ensures a clean break between selections.

Data to write at ANALOG_TESTMUX_OVERRIDE to enable connection

Source Description Target Description Data to write to connect Source to Target

3.3V Digital Supply * 1/2	GPIO1	0x0000_0107
1.5V Digital Supply	GPIO1	0x0000_0207
VDD_PRE5v * 1/4	GPIO1	0x0000_0407
VBG_1P2V	GPIO2	0x0000_0807
VBG_BUF	GPIO2	0x0000_1007
VREF_1P1	GPIO2	0x0000_2007
Temperature Sensor	GPIO2	0x0000_4007
ADC_REFP	GPIO2	0x0000_8007
BOR_REF	GPIO2	0x0001_0007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			F24				-	F20			-	-	-	F8									-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	LEDSEL	Firmware Debug Value. 0x1: Enable LED0 analog connection for short to gnd detecting 0x2: Enable LED1 analog connection for short to gnd detecting 0x4: Enable LED2 analog connection for short to gnd detecting	3	rw	0x0
F24	ADCSELREG	Firmware Debug Value. need to be configured TOGETHER WITH GPIO_CON_REG to enable GPIO0/1 PAD output. (ADC_SEL_SEL also need to be set to 1) 0x1: Enable GPIO0 analog connection to ADC 0x2: Enable GPIO1 analog connection to ADC 0x4: Enable GPIO2 analog connection to ADC 0x8: Enable GPIO3 analog connection to ADC	4	rw	0x0
F20	ADCCONREG	Firmware Debug Value. Contains the output value when the ADC_CON_SEL firmware select bit is set 0x1: Select LED0 Forward Voltage for measurement 0x2: Select LED1 Forward Voltage for measurement 0x4: Select LED2 Forward Voltage for measurement	3	rw	0x0
F8	GPIOCONREG	Firmware Debug Value. GPIO test MUX select 0x1: Select VDD3V3*1/2 to GPIO1 0x2: Select VDD1V5 to GPIO1 0x4: Select VDD_PRE5V*1/4 to GPIO1 0x8: Select VBG_1P2V to GPIO2 0x10: Select VBG_BUF to GPIO2 0x20: Select VREF_1P1 to GPIO2 0x40: Select tempsensor to GPIO2 0x80: Select ADC_REFP to GPIO2 0x100: Select BOR_REF from GPIO2, for BOR trig point test	9	rw	0x0
F2	ADCSELSEL	Hardware/Firmware Select. 0x0: Hardware Controlled. 0x1: ADC_SEL_REG controls output.	1	rw	0x0
F1	ADCCONSEL	ADC CON SEL. 0x0: Hardware Controlled. 0x1: ADC_CON_REG controls output.	1	rw	0x0
F0	GPIOCONSEL	Hardware/Firmware Select. 0x0: Hardware Controlled. 0x1: GPIO_CON_REG controls output.	1	rw	0x0

8.2.11.10 IRQ

0x50011024 **IRQ** ^

IOCTRLA LINS TXD Dominant Monitor interrupts. Contains the the enable, clear, status and active flag for the LINS TXD Dominant Monitor interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	F16	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F24	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt active.	1	ro	0x0
F16	LINS TXD DOM	LINS TXD Dominant Monitor interrupt status.	1	ro	0x0
F8	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F0	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt enable.	1	rw	0x0

8.2.11.11 LINSGFCONF1

0x50011028 **LINSGFCONF1** ^

LINS Glitch Filter Configuration in active mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F24							-	F16							-	F8							-	F0						

#	Field Name	Field Description	Width	Access	Reset
F24	LINS_DBNC_THRES1_2ND	2nd Stage LINS Debounce Threshold for 0 to 1. 2nd Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*32 = 2[us]). NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	7	rw	0x18
F16	LINS_DBNC_THRES0_2ND	2nd Stage LINS Debounce Threshold for 1 to 0. 2nd Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*16 = 1[us]). NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	7	rw	0xC
F8	LINS_DBNC_THRES1_1ST	1st Stage LINS Debounce Threshold for 0 to 1. 1st Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*0 = 0[us]). NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	7	rw	0x0
F0	LINS_DBNC_THRES0_1ST	1st Stage LINS Debounce Threshold for 1 to 0. 1st Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*8 = 0.5[us]). NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	7	rw	0xC

8.2.11.12 FILT_ACCESS

0x5001102C **FILT_ACCESS** ^

Glitch Filter access key.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F31	FILT_UNLOCK	Set Only bit. Write 1 to this bit to un-lock FILT_CODE bits.	1	rw	0x0

8.2.11.13 IOCAPTURE

0x50011030 **IOCAPTURE** ^

IO capture controller.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	F17		F16	F12				F8				F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F17	PRESCALE	prescaler select. 0x0: Divide by 1. 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8	2	rw	0x0
F16	PRESCALE_EN	prescale enable. prescale enable.	1	rw	0x0

F12	IRQSTS	IO capture irq status. io capture irq status.	4	ro	0x0
F8	IRQCLR	IO capture irq clear. clear io capture irq. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	4	rw	0x0
F4	IRQENA	IO capture irq enable. enable io capture irq, gpio posedge or io capture counter exceeds the threshold will trigger interrupt.	4	rw	0x0
F0	CAPENA	IO capture enable. enable io capture.	4	rw	0x0

8.2.11.14 IOCAPTUREPERIOD0

0x50011034 **IOCAPTUREPERIOD0** ^

.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD_GPIO1	GPIO1 input signal period. GPIO1 input signal period.	16	rw	0xFFFF
F0	PERIOD_GPIO0	GPIO0 input signal period. GPIO0 input signal period.	16	rw	0xFFFF

8.2.11.15 IOCAPTUREPERIOD1

0x50011038 **IOCAPTUREPERIOD1** ^

.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD_GPIO3	GPIO3 input signal period. GPIO3 input signal period.	16	rw	0xFFFF
F0	PERIOD_GPIO2	GPIO2 input signal period. GPIO2 input signal period.	16	rw	0xFFFF

8.2.11.16 COUNTERGPIO0

0x5001103C **COUNTERGPIO0** ^

.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	COUNTER_LOW_GPIO0	GPIO0 input low level counter. GPIO0 input low level counter, the low level width is equal to the counter plus 1.	16	ro	0x0
F0	COUNTER_HIGH_GPIO0	GPIO0 input high level counter. GPIO0 input high level counter, the high level width is equal to the counter plus 1.	16	ro	0x0

8.2.11.17 COUNTERGPIO1

0x50011040 **COUNTERGPIO1** ^

.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	COUNTER_LOW_GPIO1	GPIO1 input low level counter. GPIO1 input low level counter, the low level width is equal to the counter plus 1.	16	ro	0x0
F0	COUNTER_HIGH_GPIO1	GPIO1 input high level counter. GPIO1 input high level counter, the high level width is equal to the counter plus 1.	16	ro	0x0

8.2.11.18 COUNTERGPIO2

0x50011044	COUNTERGPIO2	^

.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	COUNTER_LOW_GPIO2	GPIO2 input low level counter. GPIO0 input low level counter, the low level width is equal to the counter plus 1.	16	ro	0x0
F0	COUNTER_HIGH_GPIO2	GPIO2 input high level counter. GPIO2 input high level counter, the high level width is equal to the counter plus 1.	16	ro	0x0

8.2.11.19 COUNTERGPIO3

0x50011048	COUNTERGPIO3	^

.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	COUNTER_LOW_GPIO3	GPIO3 input low level counter. GPIO3 input low level counter.	16	ro	0x0
F0	COUNTER_HIGH_GPIO3	GPIO3 input high level counter. GPIO3 input high level counter.	16	ro	0x0

8.2.11.20 IOGFCONF

0x5001104C	IOGFCONF	^

IO capture Glitch Filter Configuration in active mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8							-	F0						

#	Field Name	Field Description	Width	Access	Reset
F8	IO_DBNC_THRES1	IO Debounce Threshold for 0 to 1. IO Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*8 = 0.5[us]). NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	7	rw	0x8
F0	IO_DBNC_THRES0	IO Debounce Threshold for 1 to 0. IO Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*8 = 0.5[us]). NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	7	rw	0x8

8.2.12 SYSCTRLA

SYSCTRLA		
Address	**Register Name**	**Description**
0x50012000	RETAIN0	Retained data 0
0x50012004	RETAIN1	Retained data 1
0x50012008	DEBUG_ACCESS_KEY	Debug access key
0x5001200C	DEBUG_ACCESS_ENABLED	Debug access enabled
0x50012010	TRIM_ACCESS_KEY	Trim access key
0x50012014	TRIM_ACCESS_ENABLED	Trim access enabled
0x50012018	PMU_ACCESS_KEY	PMU configure access key
0x5001201C	PMU_ACCESS_ENABLED	PMU configure access enabled
0x50012020	LF_OSC_TRIM	Trim controls for the low frequency (32k/250KHz) oscillators
0x50012024	HF_OSC_TRIM	Trim controls for the high frequency (16MHz) oscillator

0x50012028	BIAS	Bias Control
0x5001202C	TRIMLEDBIAS	LED bias current Trim
0x50012030	TRIMLED0	High Voltage LED trim
0x50012034	TRIMLED1	High Voltage LED trim
0x50012038	TRIMLED2	High Voltage LED trim
0x5001203C	TRIMVFW	VFW Current Trim
0x50012040	LIN	LIN IO Control (Trim access need to be enabled before Written)
0x50012044	DFTCODE	DFT Unlock Code
0x50012048	DFT_ACCESS_ENABLED	DFT access enabled
0x5001204C	DFTTESTMODESTART	DFT Mode Start
0x50012050	NAME	ASIC name
0x50012054	REV	Silicon Revision
0x50012058	BORTESTMODE	BOR Testmode Enable

8.2.12.1 RETAIN0

0x50012000 RETAIN0 ^

Retained data 0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	RETAIN0	Firmware scratch register 0. Only reset at power-on (e.g contents retained in Hibernate mode and retained despite any hard or soft resets). NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE	8	dual	0x0

8.2.12.2 RETAIN1

0x50012004 RETAIN1 ^

Retained data 1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	RETAIN1	Firmware scratch register 1 (0x1). Contents retained in Hibernate mode - but lost after any hard or soft reset.	8	rw	0x0

8.2.12.3 DEBUG_ACCESS_KEY

0x50012008 DEBUG_ACCESS_KEY ^

Debug access key.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F31	DEBUG_LOCK	Set Only bit. Set this bit to lock DEBUG_CODE bits.	1	rw	0x0
F0	DEBUG_ACCESS_KEY	Write the value 0x5 to this register to enable debug options. Write any other value to disable the debug options.	4	rw	0x0

8.2.12.4 DEBUG_ACCESS_ENABLED

0x5001200C DEBUG_ACCESS_ENABLED ^

Debug access enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	DEBUG_ACCESS_ENABLED	A status flag that is set when debug access is enabled	1	ro	0x0

8.2.12.5 TRIM_ACCESS_KEY

0x50012010 TRIM_ACCESS_KEY ^

Trim access key.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F31	TRIM_LOCK	Set Only bit. Write 1 to this bit to lock TRIM_CODE bits.	1	rw	0x0
F0	TRIM_ACCESS_KEY	Write the value 0xe to this register to enable 'trim access' (which allows write access to various trim settings and production test options). Write any other value to disable trim access.	4	rw	0x0

8.2.12.6 TRIM_ACCESS_ENABLED

0x50012014 TRIM_ACCESS_ENABLED ^

Trim access enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	TRIM_ACCESS_ENABLED	A status flag that is set when trim access is enabled	1	ro	0x0

8.2.12.7 PMU_ACCESS_KEY

0x50012018 PMU_ACCESS_KEY ^

PMU configure access key.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F31	PMU_LOCK	Set Only bit. Set this bit to lock PMU_CODE bits.	1	rw	0x0
F0	PMU_ACCESS_KEY	Write the value 0xA to this register to enable 1v5 domain at hibernate. Write any other value to disable the 1v5 domain at hibernate.	4	rw	0x0

8.2.12.8 PMU_ACCESS_ENABLED

0x5001201C PMU_ACCESS_ENABLED ^

PMU configure access enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	PMU_ACCESS_ENABLED	A status flag that is set when pmu access is enabled	1	ro	0x0

8.2.12.9 LF_OSC_TRIM

0x50012020 LF_OSC_TRIM ^

Trim controls for the low frequency (32k/250KHz) oscillators.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	TRIM_LF_RC	LF RC oscillator trim. Following value only used as a reference: NOTE: The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE and write trim key 0x0: freq=141.1KHz	8	rw	0xA0

		0x9b: freq=250.0KHz 0xa0: freq=256.0KHz 0xff: freq=441.7KHz			

8.2.12.10 HF_OSC_TRIM

0x50012024 HF_OSC_TRIM ^

Trim controls for the high frequency (16MHz) oscillator.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F16								-	-	-	-	F9			F8	F0								

#	Field Name	Field Description	Width	Access	Reset
F16	SSCDIV	SSC Clock Divider. SSC Freq = SYS_FREQ/[(SSC_DIV+1)*(SSC_DEEP+1)*4].	8	rw	0x28
F9	SSCDEEP	SSC Depth Configuration.	3	rw	0x0
F8	SSCENA	SSC Enable.	1	rw	0x0
F0	TRIM_HF_RC	High Frequency RC Oscillator trim. TRIM bits will be changed if SSC is enabled. Reload the trim bits from Flash if SSC is disabled while the change has happened.write trim key. Following value only used as a reference: 0x0: freq= 9MHz 0xa7: freq=16MHz 0xff: freq=35MHz	8	rw	0xA7

8.2.12.11 BIAS

0x50012028 BIAS ^

Bias Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F1	LEDBIASREG	High Voltage LED bias select register. If LED_BIAS_SEL is set, then LED_BIAS_REG allows override access to the LED BIAS signal.	1	rw	0x0
F0	LEDBIASSEL	High Voltage LED bias select. 0x0: The LED Bias is enabled and disabled by the pmu hardware state machine by default. 0x1: The value of the LED_BIAS_REG field is what is used to drive the LED_BIAS signal. (override mode)	1	rw	0x0

8.2.12.12 TRIMLEDBIAS

0x5001202C TRIMLEDBIAS ^

LED bias current Trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	LEDBIASTRIM	LED bias current trim. each code is about 50nA step.wirte trim key	8	rw	0x80

8.2.12.13 TRIMLED0

0x50012030 TRIMLED0 ^

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM0	LED trim (120uA step; max about 60mA).	9	rw	0x1F4

8.2.12.14 TRIMLED1

0x50012034	TRIMLED1	^

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM1	LED trim (120uA step; max about 60mA).	9	rw	0x1F4

8.2.12.15 TRIMLED2

0x50012038	TRIMLED2	^

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM2	LED trim (120uA step; max about 60mA).	9	rw	0x1F4

8.2.12.16 TRIMVFW

0x5001203C	TRIMVFW	^

VFW Current Trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	TRIMVFW	PN Forward Voltage Current trim (10uA step max about 2.56mA).	8	rw	0xC8

8.2.12.17 LIN

0x50012040	LIN	^

LIN IO Control (Trim access need to be enabled before Written).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F24			-	-	-	-	-	-	-	-	-	-	F12		-	F8			-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F24	LINS_TX_DUTY	LIN Slave IO Duty cycle adjust.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE and wirte trim key 0x0: duty cycle = 0.488 0x1: duty cycle = 0.492 0x2: duty cycle = 0.494 0x3: duty cycle = 0.495 0x0: duty cycle = 0.497 0x1: duty cycle = 0.500 0x2: duty cycle = 0.507 0x3: duty cycle = 0.529	3	rw	0x5
F12	LINS_RX_BIAS_BOOST	adjust rise delay from LIN_IN to Input of LINS Controller.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE and wirte trim key 0x0: 2.323 us 0x1: 1.344 us 0x2: 0.968 us 0x3: 0.767 us	2	rw	0x0
F8	LINS_TX_BIAS_BOOST	Select boost of LIN Slave TX IO Current, it should be within 40mA ~ 200mA.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE and wirte trim key 0x0: 31.4 mA 0x1: 48.6 mA 0x2: 66.2 mA 0x3: 88.2 mA 0x4: 101.2 mA 0x5: 117.9 mA 0x6: 135.2 mA 0x7: 151.5 mA	3	rw	0x4

F0	LINS_TX_SLOPE	boost TX driver slew rate of LIN_IN,Slew from 40%*Vbat to 60%*Vbat @Vbat=13V,Cbus=1nF.The write operation of this register takes effect by PMU_SFRS->CTRL.UPDATE and wirte trim key 0x0: slewRate_pos = 0.62V/us, slewRate_neg = 0.63V/us 0x1: slewRate_pos = 0.62V/us, slewRate_neg = 0.63V/us 0x2: slewRate_pos = 1.19V/us, slewRate_neg = 1.27V/us 0x3: slewRate_pos = 1.74V/us, slewRate_neg = 1.88V/us 0x4: slewRate_pos = 2.31V/us, slewRate_neg = 2.42V/us 0x5: slewRate_pos = 2.79V/us, slewRate_neg = 2.99V/us 0x6: slewRate_pos = 3.37V/us, slewRate_neg = 3.51V/us 0x7: slewRate_pos = 5.14V/us, slewRate_neg = 16.69V/us	3	rw	0x4

8.2.12.18 DFTCODE

0x50012044 DFTCODE ^

DFT Unlock Code.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F31	DFT_LOCK	Set Only bit. Write 1 to this bit to lock DFT related config bits.	1	rw	0x0
F0	DFTCODE	Test Mode Unlock Enable Code. 0x1C needs to be written to this register to unlock the DFT_TESTMODE_SEL and DFT_TESTMODE_START registers.	8	wo	0x0

8.2.12.19 DFT_ACCESS_ENABLED

0x50012048 DFT_ACCESS_ENABLED ^

DFT access enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	DFT_ACCESS_ENABLED	A status flag that is set when DFT access is enabled.	1	ro	0x0

8.2.12.20 DFTTESTMODESTART

0x5001204C DFTTESTMODESTART ^

DFT Mode Start.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	DFTTESTMODESTART	Puts the ASIC into DFT testmode. Once the start bit is set, the I/O configuration will switch from Application mode to DFT Test Mode. The General Purpose I/Os will be configured as a JTAG interface. Once Test Mode is enabled, the ASIC will be boundary terminated and the processor will lose the ability to communicate with any ASIC peripherals. A chip power cycle is required to get out of the DFT test mode. Test Mode Enable state.	1	wo	0x0

8.2.12.21 NAME

0x50012050 NAME ^

ASIC name.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	NAME	ASIC name. A read from this register will return the ASIC name	32	ro	N/A

8.2.12.22 REV

0x50012054	REV	^

Silicon Revision.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	REV	Silicon Revision. A read from this register will return the ASCII silicon revision (e.g. ASCII C0 is 0x4331)	16	ro	N/A

8.2.12.23 BORTESTMODE

0x50012058	BORTESTMODE	^

BOR Testmode Enable.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENABORTESTMODE	BOR Testmode Enable. 0x0: BOR Testmode Disabled: Reference Voltage for BOR is from Band Gap (Functional Mode) 0x1: BOR Testmode Enabled: Reference Voltage for BOR is from gpio1_anaOut (Test Mode	1	rw	0x0

8.2.13 GPIO

GPIO		
Address	**Register Name**	**Description**
0x50018000	GPADATA	GPIO Port A Data
0x50018800	GPENA	GPIO Port Enables
0x50019000	GPAP03	GPIO Port A Pin 0-3 Control
0x50019004	GPAP4	GPIO Port A Pin 4 Control

8.2.13.1 GPADATA

0x50018000	GPADATA	^

GPIO Port A Data. bit[0] GPIO1 PIN, bit[1] GPIO2 PIN, bit[2] LIN_IN PIN, bit[3] GPIO3 PIN, bit[4] GPIO4 PIN

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	GPADATA	Port A data. To aid in the efficiency of software, the GPIO ports allow for the modification of individual bits in the GPIO Data by using bits [7:0] of the address bus as a enable. In this manner, software drivers can modify individual GPIO pins in a single instruction without affecting the state of the other pins. This method is more efficient than the conventional method of performing a read-modify-write operation to set or clear an individual GPIO pin. To write all the bits at the same time use address offset of 0x03.	5	dual	0x4

8.2.13.2 GPENA

0x50018800	GPENA	^

GPIO Port Enables.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset

F0	GPAENA	Enables the Clock-Gate, can be cleared to save power, if none of the GPIO functionality is required	1	rw	0x1

8.2.13.3 GPAP03

0x50019000 **GPAP03** ^

GPIO Port A Pin 0-3 Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F29	F28	F27	F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	GPAACTDETFE[3]	GPIO3 PIN activity fall status.	1	ro	N/A
F30	GPAACTDETRE[3]	GPIO3 PIN activity rise status.	1	ro	N/A
F29	GPAACTDET[3]	GPIO3 PIN activity interrupt.	1	ro	N/A
F28	GPACLR[3]	GPIO3 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F27	GPAFE[3]	GPIO3 PIN falling edge enable.	1	rw	0x0
F26	GPARE[3]	GPIO3 PIN rising edge enable.	1	rw	0x0
F25	GPAIE[3]	GPIO3 PIN interrupt mask.	1	rw	0x0
F24	GPADIR[3]	GPIO3 PIN output enable.	1	rw	0x0
F23	GPAACTDETFE[2]	LIN_IN PIN activity fall status.	1	ro	N/A
F22	GPAACTDETRE[2]	LIN_IN PIN activity rise status.	1	ro	N/A
F21	GPAACTDET[2]	LIN_IN PIN activity interrupt.	1	ro	N/A
F20	GPACLR[2]	LIN_IN PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F19	GPAFE[2]	LIN_IN PIN falling edge enable.	1	rw	0x0
F18	GPARE[2]	LIN_IN PIN rising edge enable.	1	rw	0x0
F17	GPAIE[2]	LIN_IN PIN interrupt mask.	1	rw	0x0
F16	GPADIR[2]	NOT USED. SEE IOCTRL RxLIN_ena & TxLIN_ena.	1	rw	0x0
F15	GPAACTDETFE[1]	GPIO2 PIN activity fall status.	1	ro	N/A
F14	GPAACTDETRE[1]	GPIO2 PIN activity rise status.	1	ro	N/A
F13	GPAACTDET[1]	GPIO2 PIN activity interrupt.	1	ro	N/A
F12	GPACLR[1]	GPIO2 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPAFE[1]	GPIO2 PIN falling edge enable.	1	rw	0x0
F10	GPARE[1]	GPIO2 PIN rising edge enable.	1	rw	0x0
F9	GPAIE[1]	GPIO2 PIN interrupt mask.	1	rw	0x0
F8	GPADIR[1]	GPIO2 PIN output enable.	1	rw	0x0
F7	GPAACTDETFE[0]	GPIO1 PIN activity fall status.	1	ro	N/A
F6	GPAACTDETRE[0]	GPIO1 PIN activity rise status.	1	ro	N/A
F5	GPAACTDET[0]	GPIO1 PIN activity interrupt.	1	ro	N/A
F4	GPACLR[0]	GPIO1 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPAFE[0]	GPIO1 PIN falling edge enable.	1	rw	0x0
F2	GPARE[0]	GPIO1 PIN rising edge enable.	1	rw	0x0
F1	GPAIE[0]	GPIO1 PIN interrupt mask.	1	rw	0x0
F0	GPADIR[0]	GPIO1 PIN output enable.	1	rw	0x0

8.2.13.4 GPAP4

0x50019004 **GPAP4** ^

GPIO Port A Pin 4 Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	GPAACTDETFE[4]	GPIO4 PIN activity fall status.	1	ro	N/A
F6	GPAACTDETRE[4]	GPIO4 PIN activity rise status.	1	ro	N/A
F5	GPAACTDET[4]	GPIO4 PIN activity interrupt.	1	ro	N/A
F4	GPACLR[4]	GPIO4 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPAFE[4]	GPIO4 PIN falling edge enable.	1	rw	0x0
F2	GPARE[4]	GPIO4 PIN rising edge enable.	1	rw	0x0
F1	GPAIE[4]	GPIO4 PIN interrupt mask.	1	rw	0x0
F0	GPADIR[4]	GPIO4 PIN output enable.	1	rw	0x0

8.2.14 TIMER0

TIMER0		
Address	**Register Name**	**Description**
0x50020000	COUNT	Timer Counter Register
0x50020004	CFG	Timer Control Register

8.2.14.1 COUNT

0x50020000	COUNT	^

Timer Counter Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	COUNT	Count. Initial counter value. The timer will count from this value to 0xFFFFFFFF and roll over to 0x00000000. At this point it will generate an interrupt if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.	32	rw	0x0

8.2.14.2 CFG

0x50020004	CFG	^

Timer Control Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENA	Enable. This bit starts/stops the timer: < br> 1 = Timer Running < br> 0 = Timer Inactive	1	rw	0x0

8.2.15 TIMER1

TIMER1		
Address	**Register Name**	**Description**
0x50020008	COUNT	Timer Counter Register
0x5002000C	CFG	Timer Control Register

8.2.15.1 COUNT

0x50020008		COUNT			^
Timer Counter Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	COUNT	Count. Initial counter value. The timer will count from this value to 0xFFFFFFFF and roll over to 0x00000000. At this point it will generate an interrupt if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.	32	rw	0x0

8.2.15.2 CFG

0x5002000C		CFG			^
Timer Control Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	ENA	Enable. This bit starts/stops the timer: < br> 1 = Timer Running < br> 0 = Timer Inactive	1	rw	0x0

8.2.16 TIMER2

TIMER2		
Address	**Register Name**	**Description**
0x50020010	COUNT	Timer Counter Register
0x50020014	CFG	Timer Control Register

8.2.16.1 COUNT

0x50020010		COUNT			^
Timer Counter Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	COUNT	Count. Initial counter value. The timer will count from this value to 0xFFFFFFFF and roll over to 0x00000000. At this point it will generate an interrupt if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.	32	rw	0x0

8.2.16.2 CFG

0x50020014		CFG			^
Timer Control Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	ENA	Enable. This bit starts/stops the timer: < br> 1 = Timer Running < br> 0 = Timer Inactive	1	rw	0x0

8.2.17 WDT1

WDT1		
Address	**Register Name**	**Description**
0x50020018	CFG	Config
0x5002001C	KEY	Key

8.2.17.1 CFG

0x50020018 **CFG** ^

Config.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3		F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F3	PRESET	Preset. Defines the watchdog timeout period. It means that the WDT internal counter will count from 0 to the prescaler value at the system clock speed and trigger if not cleared. For instance, a system running from a 30MHz Crystal with WDTPRES[1I0] = 10 will trigger the WDT after approximately 0.14 seconds if not cleared properly and in time by the application. 0x0: 2^13 / System Clock 0x1: 2^19 / System Clock 0x2: 2^22 / System Clock 0x3: 2^32 / System Clock	2	rw	0x0
F2	RSTFLAG	Reset flag. This flag is set by the system at the initialization if the initialization was caused by a reset triggered by the WDT. The bit can be cleared by the application.	1	rw	0x0
F1	RSTEN	Reset enable. If enabled a WDT time-out will force the microcontroller to reset. This bit can be asserted but it cannot be de-asserted.	1	rw	0x0
F0	ENA	WDT Enable. This bit can be asserted but it cannot be de-asserted. It means that once the WDT is enabled it cannot be turned off until a Reset or Power-On Reset occurs.	1	rw	0x0

8.2.17.2 KEY

0x5002001C **KEY** ^

Key. Writing the sequence CLEAR, KEY0, KEY1 to this register will clear (pet) the watchdog - preventing it from timing out and resetting the system.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	KEY	Key. To clear the WDT counting the following words must be written in this order and without any other instruction between then: 0x3C570001 0x007F4AD6	32	rw	0x0

8.2.18 FLASH

FLASH		
Address	**Register Name**	**Description**
0x50020020	FLADDR	Destination address for flash write / erase operation
0x50020024	FLWRDT	Flash data to be written
0x50020028	UNLBWR	Flash data unlock register
0x5002002C	BWRSTRT	Flash write start register
0x50020030	UNLSER	Flash sector erase unlock register
0x50020034	SERSTRT	Flash sector erase start register
0x50020040	FLSCTRL	Flash control register
0x50020044	FLSCP	Flash code protection register
0x50020050	FLS_UNLOCK_CTRL_OP	Flash Unlock Control Operation Register

0x50020054	CTRL_OP	Flash Control Operation Register
0x50020058	TRIM	Flash Trim Register

8.2.18.1 FLADDR

0x50020020 **FLADDR** ^

Destination address for flash write / erase operation.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0																

#	Field Name	Field Description	Width	Access	Reset
F0	ADDR	Target address for write/erase operation. In byte writes, this is the read address of the flash to be written to. In erase modes, it is a read address inside the sector to be erased. This register must be written in the correct sequence or the operation will fail.	17	rw	0xFFFF

8.2.18.2 FLWRDT

0x50020024 **FLWRDT** ^

Flash data to be written.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA	Content to be written into the targeted address. This register must be written in the correct sequence or the operation will fail.	32	rw	0x0

8.2.18.3 UNLBWR

0x50020028 **UNLBWR** ^

Flash data unlock register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_WRITE	Control register to unlock write. A value of 0x55555555 must be written to this address at the correct point in the write sequence or the operation will fail.	32	rw	0x0

8.2.18.4 BWRSTRT

0x5002002C **BWRSTRT** ^

Flash write start register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	WRITE_START	Control register to start a write. A value of 0xAAAAAAAA must be written to this address at the correct point in the write sequence or the operation will fail.	32	rw	0x0

8.2.18.5 UNLSER

0x50020030 **UNLSER** ^

Flash sector erase unlock register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset

F0	UNLOCK_ERASE	Control register to unlock a sector erase. A value of 0x66666666 must be written to this address at the correct point in the sector erase sequence or the operation will fail.	32	rw	0x0

8.2.18.6 SERSTRT

0x50020034 **SERSTRT** ^

Flash sector erase start register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	ERASE_START	Control register to commit a sector erase. A value of 0x99999999 must be written to this address at the correct point in the sector erase sequence or the operation will fail.	32	rw	0x0

8.2.18.7 FLSCTRL

0x50020040 **FLSCTRL** ^

Flash control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F0	CTRL	Number of wait states used in the reading process. Each read from flash memory will take number of cycles equal to 1+RWC to complete.	2	rw	0x1

8.2.18.8 FLSCP

0x50020044 **FLSCP** ^

Flash code protection register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	CODE_PROT	Code Protection / SerialWire Lockout Control Code protection control register. Write a value of 0xF2E11047 to disable the SerialWire interface. Write 0x00000000 to enable it. This allows the user program to disable the SerialWire interface to prevent unauthorized debug access to the part. NOTE1: This register does not lock the Flash Memory against read/write/erase by the applications program. Instead what it does is to disable all communications with the debug interface, therefore preventing any external attack. The application code is still able to modify the flash content. NOTE2: Upon Power-On Reset or Normal Reset the system disables the communication for a small time interval (8192 clock cycles). If the application needs to be protected it is mandatory to set this register with the appropriate code in the beginning of the initialization process and before the internal hardware enable the debug communication.	32	rw	0x0

8.2.18.9 FLS_UNLOCK_CTRL_OP

0x50020050 **FLS_UNLOCK_CTRL_OP** ^

Flash Unlock Control Operation Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_CTRL_OP	Flash Control Operation Register Unlock value. 0xACDC_1972 needs to be written in this register to unlock the Control Operation Register access. When this register is read, it returns the state of the lock: 0: The Control Operation Register is locked. The Control Operation Register (FLASH_CTRL_OP) cannot be written. 1: The Control Operation Register is unlocked. The Control Operation Register (FLASH_CTRL_OP) can be written.	32	rw	0x0

		Note: After each write to the FLASH_CTRL_OP register, the state of the lock is cleared and the pattern needs to be written again to allow a new configuration of the register.			

8.2.18.10 CTRL_OP

0x50020054 **CTRL_OP** ^

Flash Control Operation Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F1		F0

#	Field Name	Field Description	Width	Access	Reset
F1	SIZE	SIZE of the write operation. Refer to data sheet for more information of the use of this field.	2	rw	0x0
F0	CHIP	CHIP bit. This bit is only used during the Erase operation. It allows the system to erase more than one sector. 0: The Erase operation will only erase the sector selected by the FLASH_ADDR register value. 1: The Erase operation will erase the full main array of the flash.	1	rw	0x0

8.2.18.11 TRIM

0x50020058 **TRIM** ^

Flash Trim Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	F17	F16	F0															

#	Field Name	Field Description	Width	Access	Reset
F17	SLEEPDEEP_CFG	Deep Sleep VDD_IO configuration. This register will be automatically populated with the value stored in the NVR sector 1 (@0001_0000). When set, the system will NOT be reset if VDD_IO is going away during Deep Sleep mode. Otherwise (0), the system is reset if VDD_IO is removed.	1	rw	0x0
F16	SDIO_TIMING_CFG	SDIO interface timing configuration. This register will be automatically populated with the value stored in the NVR sector 1 (@0001_0000). When set, the SDIO/INT signals are captured on the rising edge of CLK. When cleared, these data are captured on the falling edge of CLK	1	rw	0x1
F0	OSC_TRIM	Oscillator Trim Value. This register will be automatically populated with the value stored in the NVR sector 1 (@0001_0000).	16	rw	0x86

9 DEVICE FUNCTIONAL DESCRIPTION

9.1 MCU FEATURES

9.1.1 Power on sequence

Figure 7 shows the power on sequence , VDD3V3/ VDD1V5 connect to the external 4.7uF capacitor.

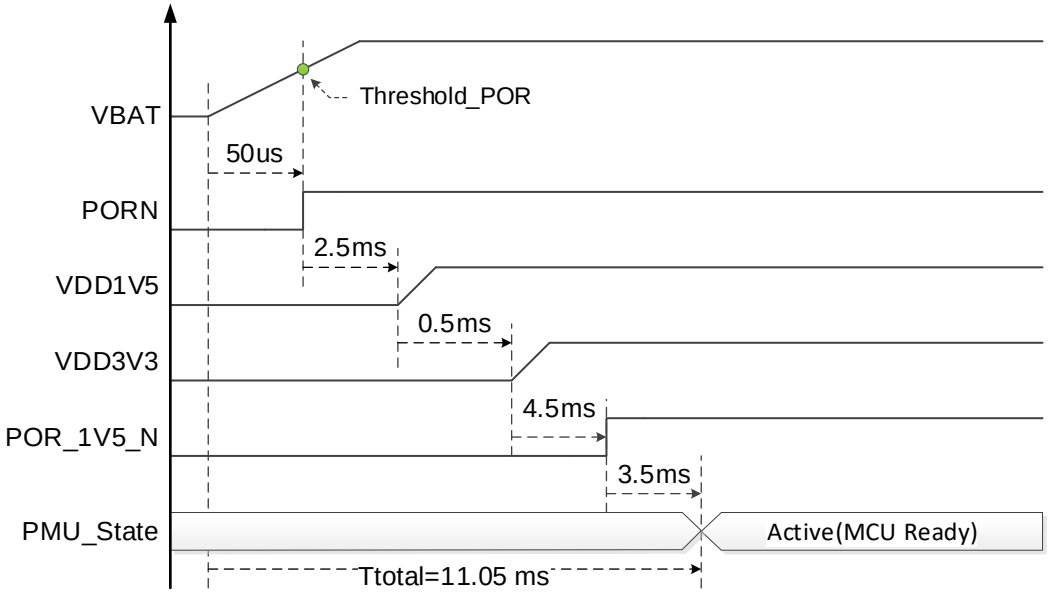

Figure 9 power on sequence

ASIC has an On-chip Brown-out Detection (BOD) circuit for monitoring the VCC level during operation by comparing it to a fixed trigger level. The trigger level for the BOD can be selected by the BOR3V3THRESH / BOR1V5THRESH. The trigger level has a hysteresis to ensure spike free Brown-out Detection.

When the BOR ACTION is configured as hard reset, and VDD_3V3/ VDD_1V5 decreases to a value below the trigger level (Threshold_BOR_3V3/Threshold_BOR_1V5 - in Figure 8), the Brown-out Reset(BORN) is activated. When VCC increases above the trigger level, the BORN is released.

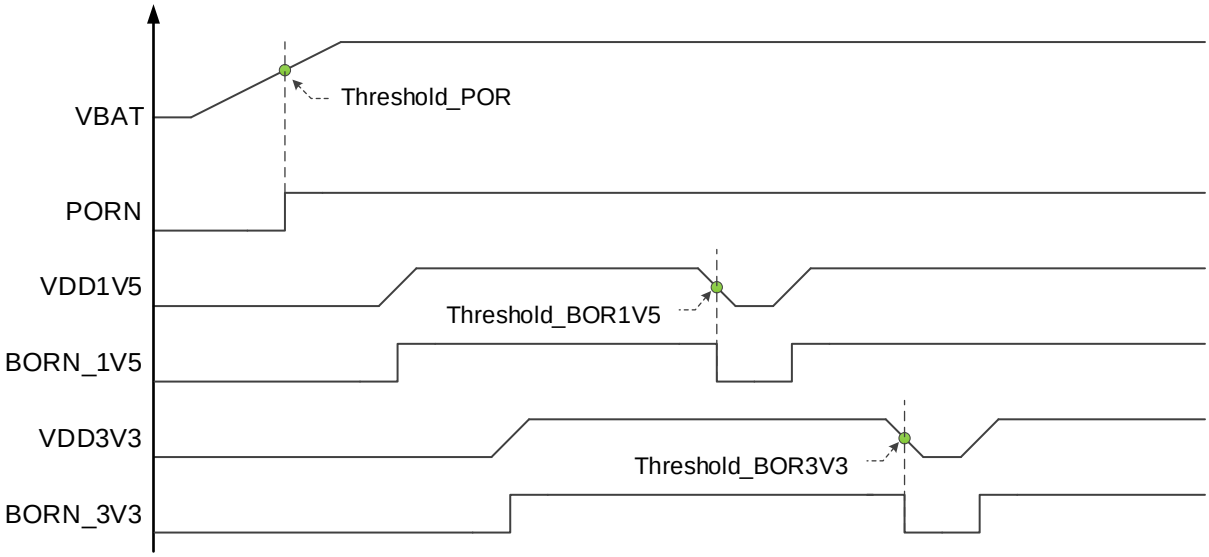

Figure 10 BORN Generation

9.1.2 MCU Core

The chip implements one ARM Cortex M0 core.

Additional documentation on ARM Cortex-M0 32 bits microcontroller can be found at

http://www.arm.com/products/processors/cortex-m/cortex-m0.php

9.1.3 System Memory (SRAM)

MCU core implements 16kbytes of SRAM. MCU can execute codes from the SRAM memories.

9.1.4 Flash Non Volatile Memory

MCU implements a Programmable Flash Memory with x32 configuration, sector and chip erase and byte program capability. It integrates five 512bytes nonvolatile registers (NVR) sectors.

In normal operation the ARM core fetches instructions (or data permanently stored) from the Flash memory but it is also possible for a program to alter the content of the flash memory. The following operations can be performed in the Flash Memory:

- Byte Write
- Sector Erase

- Block Erase
- Code Protect

For a description of the flash memory registers, please refer to the product register map. Here is a simple description of the basic features supported:

- Registers support to write/erase data to a byte, sector address
- Support programmable read wait states*
- Support system clock divider for write/erase functions
- Protection mechanism to unlock flash memory write and start flash memory byte-write
- Protection mechanism to unlock flash memory sector erase

* The design is implemented such that the timings associated with the flash macro meet the maximum speed of the system clock requirements.

9.1.5 Interrupt vectors

The first 148 bytes of Flash Memory are organized following the standard created by ARM. In this standard the Address 0x00000 contains the top-of-stack address (four bytes). The following addresses contain interrupt vectors used by the microcontroller:

Table 10 Interrupt Vector

Vector Name	Address	Comments
STACK_VALUE	0x00000	Typically set to 0x20000FFFF (Top of SRAM)
Reset_Handler	0x00004	Reset routine entry
Reserved	0x00008	Reserved. No NMI implemented.
HardFault Handler	0x0000C	
Reserved	0x00010 to 0x00028	
SVC_Handler	0x0002C	

Reserved	0x00030-0x00034	
PendSV_Handler	0x00038	
SysTick_Handler	0x0003C	
WULIN_Handler,	0x00040	Wake Up LIN Slave
IOCTRLA_Handler,	0x00044	LINS TxD Dominant Timeout
WUTIMER_Handler,	0x00048	Wake Up Timer
BOR_Handler,	0x0004C	Brown out event
WatchdogA_Handler,	0x00050	ASIC watchdog timeout
UV_Handler,	0x00054	Under voltage event
OV_Handler,	0x00058	Over voltage event
LINS_Handler,	0x0005C	LIN Slave bus event
ADC_Handler,	0x00060	ADC data ready
PWM_Handler,	0x00064	PWM event
GPIO_Handler,	0x0006C	GPIO Interrupts
OVTEMP_Handler,	0x00074	Over Temperature event
Reserved	0x00078	Reserved
Lullaby_Handler,	0x0007C	Software Interrupt
Timer0_Handler	0x00080	
Timer1_Handler	0x00084	
Timer2_Handler	0x00088	
Watchdog_Handler	0x0008C	
BTE_Handler	0x00090	Block Transfer – Contact indie to get more information.

Reserved	0x00094	

All other addresses in the flash memory can be used for the user's program.

The meanings of the standard interrupt vectors (Provided with the ARM Cortex M0 core) are defined in ARM's documentation. One of the sources of information is:

http://infocenter.arm.com/help/topic/com.arm.doc.dui0497a/DUI0497A_cortex_m0_r0p0_generic_ug.pdf

9.1.6 Interrupt Enabling/Disabling Process

Cortex-M0 implements a NVIC (**N**ested **V**ector **I**nterrupt **C**ontroller) peripheral capable of handling up to 16 peripheral's interrupts. Upon reset the microcontroller can answer only to Reset, NMI (Non-Maskable Interrupt) and Hard-Fault interrupts/exceptions. All other interrupts must be enabled. To enable and disable the interrupts the user must use access the ISER (Interrupt Set Enable Register) and ICER (Interrupt Clear Enable Interrupt) registers associated with the desired interrupt.

NOTE: Both inline functions and all parameters are defined in the product_file.h file, which must be included in the source files. Besides that the product_file.h file contains a list of available interrupts. The format of this list is as follows:

```
typedef enum IRQn
{
 //******  Cortex-M0 Processor Exceptions Numbers ***************************
 NonMaskableInt_IRQn       = -14,    // Non Maskable Interrupt
 HardFault_IRQn            = -13,    // Hard Fault Interrupt
 SVCall_IRQn               = -5,     // SV Call Interrupt
 PendSV_IRQn               = -2,     // Pend SV Interrupt
 SysTick_IRQn              = -1,     // System Tick Interrupt

 //*****  CM0IKMCU Cortex-M0 specific Interrupt Numbers **********************
 IRQ04_IRQn                = 0,      // Product specific
```

```
  IRQ04_IRQn          = 1,    // Product specific
  IRQ04_IRQn          = 2,    // Product specific
  IRQ04_IRQn          = 3,    // Product specific
  IRQ04_IRQn          = 4,    // Product specific
  IRQ05_IRQn          = 5,    // Product Specific
  IRQ06_IRQn          = 6,    // Product Specific
  IRQ07_IRQn          = 7,    // Product Specific
  IRQ08_IRQn          = 8,    // Product Specific
  IRQ09_IRQn          = 9,    // Product Specific
  IRQ10_IRQn          = 10,   // Product Specific
  IRQ11_IRQn          = 11,   // Product Specific
  IRQ12_IRQn          = 12,   // Product Specific
  IRQ13_IRQn          = 13,   // Product Specific
  IRQ14_IRQn          = 14,   // Product Specific
  IRQ15_IRQn          = 15,   // Product Specific
  TIMER0_IRQn          = 16,   // Timer 0
  TIMER1_IRQn          = 17,   // Timer 1
  TIMER2_IRQn          = 18,   // Timer 2
  WATCHDOG_IRQn          = 19    // Watchdog timer
} IRQn_Type;
```

9.1.7 Flash Code protection

The controlled access to the flash content is based on disabling all communications with the debug interface, therefore preventing any external attack. Hence, the application code is still able to modify the Flash content.

Upon Power-On Reset or Normal Reset, MCU core disables the communication with the debug interface for a small time interval (8192 system clock cycles). If the application needs to be protected it is mandatory to set the protection register with the appropriate code in the beginning of the initialization process and before the internal hardware enable the debug communication. In other

words, if during this time interval the protection register is loaded with a specific pattern, then the communication remains disabled after the end of this interval and stays disabled until this register is loaded with a different pattern. To allow for debug communication the application has only to write a different value in the lock register.

If a part is protected, the emulator can still erase and program the part, but first it will be required to erase the Flash content, therefore protecting it.

9.1.8 Systick Timer

This timer is an optional peripheral created by ARM and implemented in the Cortex M0 160/8. It is fully described in the Cortex-M0 Devices Generic User Guide (Chapter 4.4 Optional System Timer, Systick) found at:

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0497a/Babieigh.html

9.1.9 Timers (0, 1 and 2)

The MCU implements three identical timers: Timer0, Timer1 and Timer2. All three timers operate using the system clock as clock source. They increment at the system clock rate starting from the loaded value in the counter until they roll over from 0xFFFFFFFF to 0x00000000. At this point an interrupt is generated if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.

9.1.10 Watch Dog Timer

The MCU implements a WDT (**W**atch **D**og **T**imer) that can operate in one of two ways:

- Interrupt Mode: In the event of a WDT rollover an interrupt will be generated.
- Reset Mode: In the event of a WDT rollover the microcontroller will reset.

The WDT supports Reset, Enable, status/flag and clear functions. It integrates a pre-scaler that can divide the system clock by 2^{13}, 2^{19}, 2^{22} or 2^{32}. It means that the WDT internal counter will count from 0 to the pre-scaler value at the system clock speed and trigger if not cleared.

For instance, a system running from a 16MHz system clock and 2^{22} pre-scaler value will trigger the WDT after approximately 0.26 seconds if not cleared properly and in time by the application.

9.1.11 MCU Core to ASIC interface

The ASIC die communicates with the indie Cortex M0 MCU through a proprietary interface. The interface enables any swap between ASIC die and MCU die and is transparent to software.

9.2 ASIC FEATURES

9.2.1 Clock Generation

Two clock sources are integrated in the device. The system clock is based on a RC network and will be trimmed to meet the accuracy requirements specified in the EC Table. Additionally, an auxiliary clock will be used during Hibernate/Deepsleep.

9.2.2 Reset

Both ASIC and MCU integrates Power on Reset (POR) circuitry: MCU POR monitors its input supply and generate a reset every time the MCU supply is recycled. ASIC POR monitors the main 1V5 LDO supply and generate a reset every time the LDO supply is recycled. Both POR maintain their output reset active as long as the monitored supply voltage is not above the minimum supply level to ensure safe logic operation of the Power Management Unit including the necessary analog features such as clock generator, bandgap, etc…This level is hardcoded and process technology dependent.

Additionally, the ASIC integrates Brown Out (BOR) circuit detectors that are configurable by SW (enable/disable as well as threshold programmable for the main ASIC core supply) and are actively monitored by the ASIC power management unit (PMU). In case any BOR is triggered, the PMU can be configured to either do the following (per BOR blocks).

- trigger a system reset
- generate an interrupt to the MCU for further actions.
- do nothing

Finally, the MCU watchdog timer (if configured to do so) or a reset instruction can reset the MCU logic while on the ASIC side the watchdog timer (if configured to do so) or a reset register write can reset the ASIC system.

9.2.3 PMU and Load Dump Protect circuits

ASIC integrates battery monitoring functionality that will detect load dump events occurring at the battery supply pin. An analog comparator will detect over voltage transients after going through a load dump limitation circuit. The protection circuit can handle DC voltage up to 45V and will limit these to maximum of *Over Voltage Threshold* nominal, therefore the comparator will detect any over voltage transients at the battery pin beyond that threshold. The circuit will generate a digital output signal to be filtered and sent to the interrupt controller. The circuit will be active during normal operation mode – not during Hibernate condition.

The voltage regulators themselves are supplied by VBAT directly and sustain DC level of load dump voltages.

Meanwhile, the PMU integrated internal reference voltage and power supply, which include analog modules power supply, GPIO power supply 3.3V LDO and digital core power supply 1.5V LDO. And internal powerup state-machine guarantee PMU module to work stably.

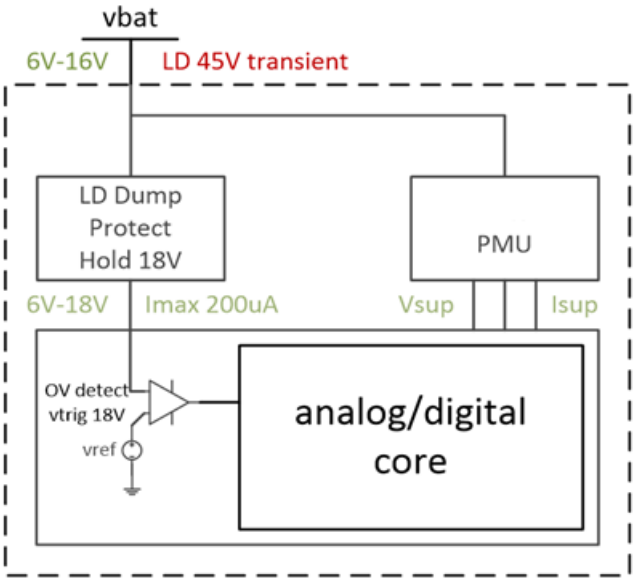

Figure 11 Load Dump Protect

9.2.4 LIN Interface

9.2.4.1 LIN Transceiver

Supports LIN Protocol Controller according to LIN 2.x and SAE J2602 (rev J2602-1_201211). The IC contains an integrated PHYs for low-speed vehicle serial data network communication using the LIN protocol.

9.2.4.1.1 LIN RxD Debounce

For preventing RxD spikes in case of RF interferences and automotive pulses, two digital glitch filters are integrated in the data pathes of LIN RxD.

Debounce thresholds for low to high and high to low can be programmable independently (See Register Description).

$$T_{thres} = \left(T_{hfosc}\right) \times LINDBNCTHRESx$$

For instance, the default DBNCTHRES value is 0x30 and HFOSC freq is 16MHz.Thus the default debounce threshold is 62.5ns * 48 = 3 us.

9.2.4.1.2 LIN TxD Timeout Monitor

TxD Timout monitor is integrated to prevent dominant bus due to internal malfunction. LIN TX is controlled by TxD signal from LIN controller or GPA (Selected by bit LINS_HWMODE in Register Description). If TxD is stuck at low over a specified TxD timeout time due to a crash of MCU/GPA/LIN Controller, the integrated TxD monitor will switch off the LIN TX output automatically until a low to high transition of TxD.

9.2.4.1.3 Short LIN Bus to Ground

If the bus idle timeout monitor detects the bus is shorted to ground (See bit BUS_IDLE_TIMEOUT_DOMINANT in Register Description), LIN Slave's 30K pullup will be automatically switched off to prevent a fast discharge of the car battery.

If enabled, the feature is always on even the chip is in hibernate mode.

9.2.4.1.4 External LIN Transceiver Mode

In this mode, the internal LIN transceiver is bypassed and LIN Slave controller's RxD/TxD can be connected with an external transceiver through GPIO1/2(See HWMODE bits from Register Description).

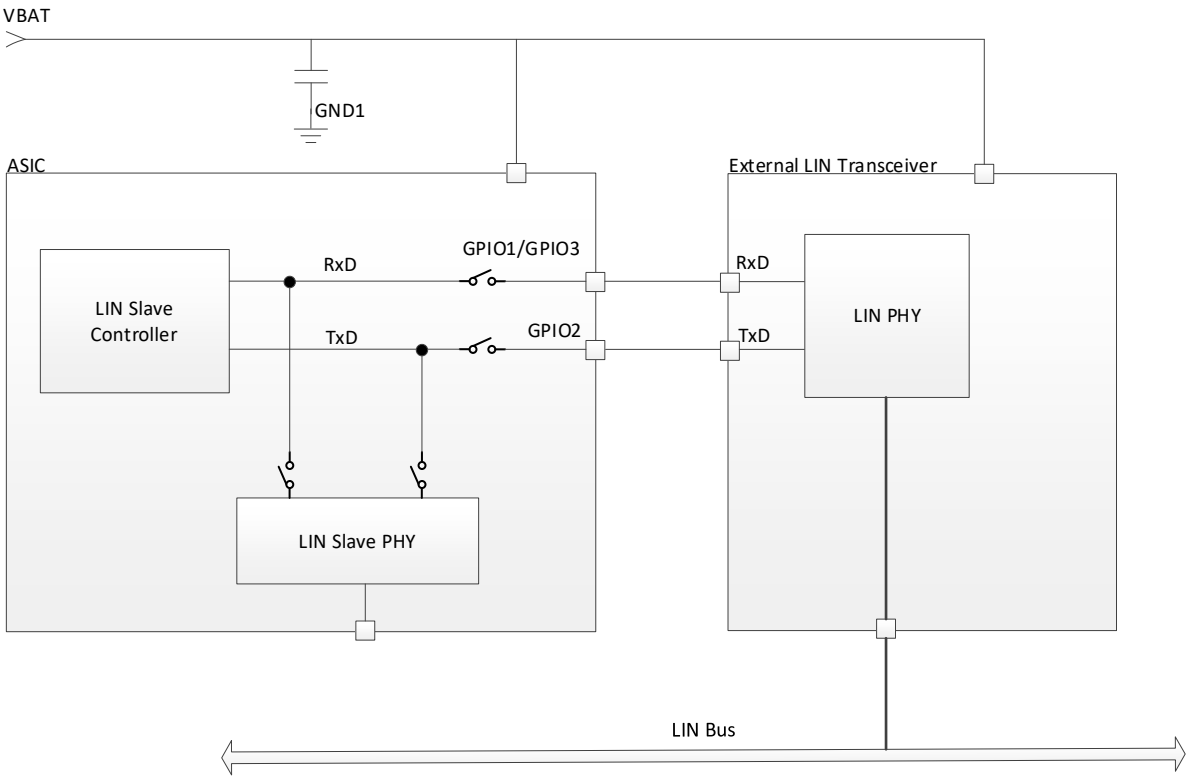

Figure 12 External LIN Transceiver Connection

9.2.4.2 LIN controller

The IC contains a LIN Slave core. The LIN core is a communication controller that performs serial communication. It implements the datalink layer of the LIN Protocol Specification. LIN uses a single master / multiple slave concept for the message transfer between nodes of the LIN network. The LIN controller core comprises an interface to connect a micro controller that accesses the LIN core registers to control the transmission and reception of message frames.

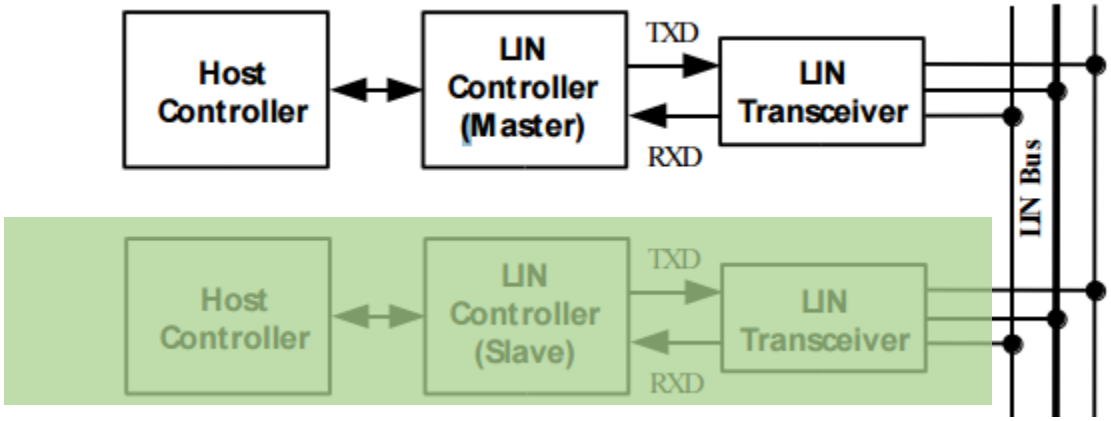

Figure 13 Lin System

Features

- One LIN Slave Controller
  - Support of LIN specification 2.2A/SAE J2602
  - Backward compatibility to LIN 1.3
- Automatic bit rate detection
- 8-byte data buffer
- 8-bit host controller interface
- Fully synchronous design, available in VHDL or Verilog, completely synthesizable

9.2.4.2.1 Data Length Register and Enhanced Checksum

The host controller has to define the length of the data field of the current LIN frame by adjusting the DATA LENGTH register. If the data length bits[3:0] are loaded with the value “1111b” the length of the data field is decoded from Bit 5 and 4 of the identifier register (ID) according to table below (e.g. compatibility to LIN specification 1.1). Otherwise the amount of data bytes can be written directly to the DATA LENGTH register (supported values are 0...8).

Table 11 ID bits and number of bits

ID (Bit 5)	ID (Bit 4)	Number of Bytes in the data field
0	0	2
0	1	2
1	0	4
1	1	8

The LIN core supports classic checksum (Spec 1.3, inverted eight bit sum with carry over all data bytes) and enhanced checksum (Spec. 2.0, inverted eight bit sum with carry over all data bytes and protected identifier). The host controller has to set the checksum type used in the current frame by adjusting Bit ENHCHK in the data length register (‘1’ for enhanced checksum, ‘0’ for classic checksum).

9.2.4.2.2 Wake-up Repeat Time and Bus Inactivity Time

The time for repeating of wake up because of no reaction on the bus and for go to sleep because of inactivity on the bus can be optionally written by the host controller to registers WUPREPEAT and BUSINACTIVE (address 0x0F).

BUSINACTIVE [1:0]	LIN Inactivity Time (sec.)
00	4*
01	6
10	8
11	10

Table 12 LIN Inactivity Time

WUPREPEAT [1:0]	LIN Wake-Up Repeat Time (msec.)
00	180*
01	200
10	220
11	240

Table 13 LIN Wake-Up Repeat Time

9.2.4.2.3 Bit Time Settings

The Bit rate of the LIN system has to be defined in the bit timing registers.

Name	Description	Width(bits)
BTDIV	Bit time divider integer value	9
PRESCL	Clock Prescaler	2

Table 14 Bit Timing Related Registers

The LIN bit rate f_{bit} can be calculated from system clock f_{clk} and bit timing registers according to the following general equation:

$$f_{bit} = \frac{f_{clock}}{2^{prescl} * bt\_div * (bt\_mul + 1)}$$

Note that the procedure of adjusting the bit timing registers is different between master and slave. For the slave controller, the Bit timing register adjustment of slave is the following:

The steps for adjusting the bit timing registers of the LIN slave are explained below. The LIN core slave synchronizes to any bit rate between 1 kbit/s and 20 kbit/s. Nevertheless, the bit timing registers have to be adjusted to adapt the LIN core to the used system clock frequency.

- Setting up the pre-scaler register depending on system clock according to the following equation; the value has to be rounded down to the next integer value:

$$prescl = \ln\left(\frac{f_{clock}}{20kHz * 200}\right) * \frac{1}{\ln 2}$$

- Adjusting the bit time divider depending on system clock and pre-scaler according to the following equation; the value has to be rounded down to the next integer value:

$$bt\_div = \frac{f_{clock}}{2^{prescl} * 20kHz}$$

System Clock	PRESCL	BTDIV
8MHz	1	200
12MHz	1	300
16MHz	2	200

Table 15 Sample value for setting up bit timing registers

9.2.4.2.4 Controlling the LIN core (slave) by a host controller

The first step before transmitting messages with the LIN core is setting up the bit rate of the LIN system. For that, the host controller has to load the bit time registers. After that, the message transfer can be started. The LIN core slave detects the header of the message frame sent by the LIN master and synchronizes its internal bit time to the master bit time. An interrupt to the host controller is requested after the reception of the IDENTIFIER FIELD, after the reception of a wakeup signal (if the slave is in sleep mode), when an error is detected or when the message transfer is completed.

The following steps have to be done by the host controller when an interrupt is requested.

1) Check bit DATAREQ in the status register (it is 1 when the IDENTIFIER FIELD has been received). Proceed with the following if DATAREQ is set else proceed with step 2.

    a. Load the identifier from the ID register and process it.
    b. Adjust the bit TRANSMIT in the control register (“1” - if the current frame is a transmit operation for the slave, “0” – if the current frame is a receive operation for the slave).
    c. Load the data length in the data LENGTH register (number of data bytes or value “1111b” if the data length should be decoded from the identifier) and set the checksum type (enhanced checksum (Bit ENHCHK = ‘1’) or classic checksum (Bit ENHCHK = ’0’)).
    d. Load the data to transmit into the data buffer (for transmit operation only).
    e. Set the bit DATAACK in the control register.

Note 1: Steps a..e have to be done during the IN-FRAME RESPONSE SPACE, if the current frame is a transmit operation for the slave; otherwise a timeout will be detected by the master. If the current frame is a receive operation for the slave, steps a..e have to be finished until the reception of the first byte after the IDENTIFIER FIELD. Otherwise, the internal receive buffer of the slave core will be overwritten and a timeout error will be detected in the slave core.

Note 2: If the host controller of the slave detects an unknown identifier (e.g. extended identifier) it has to write a ‘1’ to bit “stop” in control register instead of setting bit DATAACK (steps b .. e can be skipped). In that case the LIN core slave stops the processing of the LIN communication until the next SYNC BREAK is received.

2) Check bit ERROR in the status register. Perform error handling and proceed with step 6 if bit ERROR is set else proceed with step 3.

Note 3: Bit TIMEOUT in the error register and bit WAKEUP in the status register are set if the slave has sent a wakeup signal but the master did not respond within 150ms.

3) Check bit BUSIDLETIMEOUT in the status register and activate the sleep mode by setting bit SLEEP in the control register if BUSIDLETIMEOUT is set.
4) Check bit WAKEUP in the status register (it is set if the slave has received a wakeup signal). If WAKEUP is set proceed with step 6 else proceed with step 5.

Note 4: Bit COMPLETE in the status register is not changed when a wakeup signal is transmitted or received. Therefore, bit WAKEUP has to be checked before bit COMPLETE

5) Check bit COMPLETE in the status register (it is set if the transmission was successful). If COMPLETE is set and the current frame was a receive operation for the slave, load the received data bytes from the data buffer.
6) Set the bits RSTINT (reset interrupt) and RSTERR (reset error) in the control register to reset the interrupt request and the error flags.

9.2.4.2.5 Sleep Mode and Wakeup

To reduce the systems power consumption the LIN Protocol Specification defines a Sleep Mode. The message used to broadcast a Sleep Mode request has to be started by the host controller of the LIN core master in the same way as a normal transmit message. The host controller of the LIN core slave has to decode the Sleep Mode Frame from Identifier and data bytes. After that, it has to put the LIN slave node into the Sleep Mode by setting bit SLEEP in the control register. If bit SLEEP in the control register of the LIN core slave is not set and there is no bus activity for 4 s to 10 s (specified bus idle timeout), bit SLEEP & BUSIDLETIMOUT are set and an interrupt request is generated. After that application has to understand that the LIN bus is in Sleep Mode. The bus inactivity time which should be defined as bus idle timeout for the slave can optionally set to values 4s, 6s, 8s or 10s as possible accordingly with specification 2.2A.

After receiving a Wakeup signal from the master or any slave node a wakeup request is generated, the host controller terminates the Sleep Mode of the LIN bus by clearing bit SLEEP in the control register.

Notice that don’t enter hibernate mode when bit SLEEP = 0, because in this state dominant signal will not be taken as a wakeup request.

To send a Wakeup signal, the host controller of the LIN core has to set the bit WAKEUPREQ in the control register. After successful transmission of the wakeup signal with the LIN core master the WAKEUP bit in the status register of the sending LIN core master is set and an interrupt request is generated. The LIN core slave does not generate an interrupt request after successful transmission of the Wakeup signal but it generates an interrupt request if the master does not respond to the Wakeup signal within 150ms to 250ms. This value can be set optionally to 180ms, 200ms, 220ms or 240ms as

it is possible accordingly with specification 2.2A. In that case, bit ERROR and bit TIMOUT are set**.** The host controller has to decide whether to transmit another Wakeup signal or not.

9.2.4.2.6 Error Detection and Handling

The LIN core generates an interrupt request and stops the processing of the current frame if it detects the following errors：

- BITMON: The bit value monitored on the bus is different from the sent bit value.
- Timeout caused by wakeup repeat timeout.
- BUS IDLE Timeout.

The errors detected in Break/Sync field will be ignored by LIN controller. The other errors happen in ID field/Data field will be recorded. In DataReq interrupt routine, the application has to check the type of error by processing the ERROR register. After that, it has to reset the ERROR register and the ERROR bit in status register by writing a 1 to bit RSTERR in control register. Starting a new message with the LIN core master or sending a Wakeup signal with master or slave is possible only if bit ERROR in status register is 0.

9.2.5 LED Driver Stage

ASIC integrates a high precision open drain LED Driver Stage that allows for LED currents in the range of 120uA to 60mA in 120uA increments. The LED bias circuit uses a precise bandgap referenced current (CurrentV2I) which is multiplied over stages to sink current via the LED which is connected to the HVIO(LED) pin. After factory test, the trim value for CurrentV2I = 30uA will be recorded and boot program is in charge of initializing the V2I trim bits correctly (refer to Register Description). The mirror stages consist of 120uA unit cells which are weighted linear to provide 120uA ~ 60mA current (CurrentLED). The desired current is provided according the formula below:

$$\mathrm{CurrentLED(mA)} = \mathrm{TRIM}[8:0] * CurrentV2I * 4 = TRIM[8:0] * 120uA$$

After delicate calibration by LED trim bits (refer to Register Description), the combination of stages allows for high accurate LED current in 120uA steps that are combined at the HVIO(LED) pad on chip (refer to Figure 14).

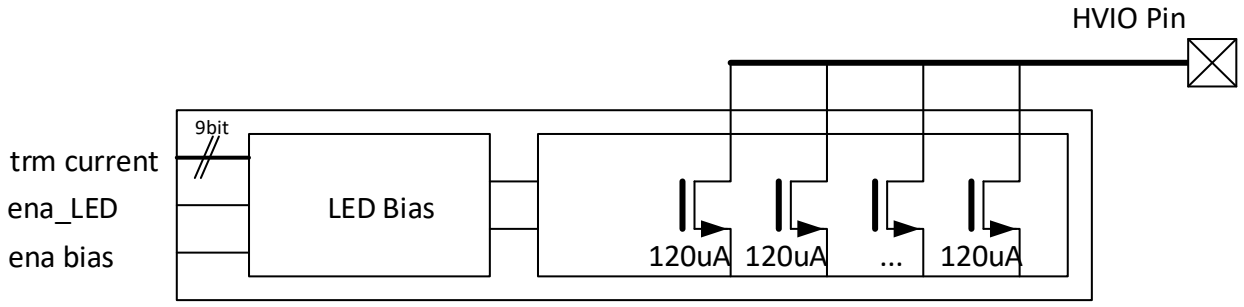

Figure 14 LED Driver Concept

The operation of the LED Driver IP requires two actions. At first the LED bias circuit needs to be enabled (ena_bias) (refer to Register Description), followed by enabling the LED (ena_LED). Latter control signal is driven by the pulse width modulator that will drive the current from the battery via the LED. The PWM signal utilizes an input signal at maximum of 250Hz and modulates its pulse width (refer to section 9.2.6 LED PWM).

9.2.6 LED PWM

LED PWMs are used to control accurately the light intensity.

Features:

- 3x16bit PWM channels with one unified period length, independent pulse rise and pulse fall timestamps.
- Frequency and duty cycle of PWM waveform support up to a maximum Resolution of 16 bits. The 16-bit resolution is only achievable if the pre-scaler from system clock is correctly chosen to have enough clock cycles depth to count up to 2^16.
- Programmable pre-scaler: system clock division (PWM_DIV)
- Programmable PWM Period (PWM_PER)

$$\text{Period} = \frac{(\text{PWM\_PER} \times \text{PWM\_DIV})}{SystemClock}$$

- Programmable duty cycle 0 to 100% (PWM_PW)

$$\text{PulseWidth} = \frac{((\text{PWM}_{\text{PFALL}} - \text{PWM}_{\text{PRISE}}) \times \text{PWM\_DIV}))}{SystemClock}$$

- Pre-scaler, period, pulse rise & pulse fall configurations will be updated at the end of the current output period.
- Support interrupt generation when new programmed PWM control data become active. After new pulse parameters (Period, pulse rise & pulse fall) have been loaded into their respective registers, an UPDATE bit can be set to 1 that will trigger the activation of the new parameters

at the end of the current pulse as not to affect the pulse shape. Basically, the UPDATE bit clear is the interrupt.

- PWM Frequency range 80 - 250 Hz
- Pulse rise -> fall cases, listed in priority:
    - PRISE = 0, PFALL = PERIOD: 100% On
    - PRISE = 0, PFALL = 0: equivalent to PRISE = 0 & PFALL = 1
    - PRISE > PFALL: 100% off
    - PRISE = PFALL: 100% off
    - PRISE < PFALL: Normal case. On at PRISE, Off at PFALL.

9.2.7 Auxiliary PWM

The auxiliary PWM generates PWM waveform to GPIO.

Features:

- 2 shared PWM counter, each channel and counter can be attached freely
- 4x16-bit PWM channels with shared PWM counter, independent pulse rise and independent pulse fall timestamps
- Frequency and duty cycle of PWM waveform support up to a maximum Resolution of 16 bits. The 16-bit resolution is only achievable if the pre-scaler from system clock is correctly chosen to have enough clock cycles depth to count up to 2^16.
- Programmable pre-scaler: system clock division (PWM_DIV)
- Programmable PWM Period (PWM_PER)

$$\text{Period} = \frac{(\text{PWM\_PER} \times \text{PWM\_DIV})}{SystemClock}$$

- Programmable duty cycle 0 to 100% (PWM_PW)

$$\text{PulseWidth} = \frac{((\text{PWM}_{\text{PFALL}} - \text{PWM}_{\text{PRISE}}) \times \text{PWM\_DIV}))}{SystemClock}$$

- Pre-scaler, period, pulse rise & pulse fall configurations will be updated at the end of the current output period.
- Support interrupt generation when new programmed PWM control data become active. After new pulse parameters (Period, pulse rise & pulse fall) have been loaded into their respective registers, an UPDATE bit can be set to 1 that will trigger the activation of the new parameters at the end of the current pulse as not to affect the pulse shape. Basically, the UPDATE bit clear is the interrupt.

- PWM Frequency range 80 - 250 Hz
- Pulse rise -> fall cases, listed in priority:
    - PRISE = 0, PFALL = PERIOD: 100% On
    - PRISE = 0, PFALL = 0: equivalent to PRISE = 0 & PFALL = 1
    - PRISE > PFALL: 100% off
    - PRISE = PFALL: 100% off
    - PRISE < PFALL: Normal case. On at PRISE, Off at PFALL.

9.2.8 House Keeping SAR ADC

- 12-bit resolution
- Differential Input
- Bandgap Voltage reference
- Used for monitoring voltages
    - Bandgap Reference
    - Accurate VBAT Channel (limited to max voltage limited by the load-dump protection circuit)
    - Junction Temperature
    - Analog Input from GPIO x 4
    - Analog Input from LED x 3
    - Forward Voltage of External LED x 3
    - VDD1V5/VDD3V3/VDDPRE5V
- Capable of being configured for converting up to 4 channels successively
- Interrupt on conversion complete regardless of digital comparator configuration

9.2.9 General-purpose I/O

The GPIOs support digital input, digital output, ADC input and can be multiplexed to other peripheral.

Features:

- Up to 4 GPIOs available
- External interrupt for both rising edge and falling edge
- Gated clock to save power

- Read/write multiple GPIOs in a single operation with the **GPADATA** register matrix
- Output drive strength supports 4mA, 8mA, 12mA, 16mA controlled by **PDVR1** and **PDVR0** registers
- Adjustable slew rate controlled by **SL** register (fast/slow)
- Both internal pull-up and pull-down resistor is supported (100kΩ typ.) and controlled by **PUENA** and **PDENA** register
- Standard 3.3V IO, not 5V input tolerant
- One pair of GPIOs support differential ADC input
- All GPIOs support single-ended ADC input
- All GPIOs can be multiplexed as PWM output (up to 4 PWM channels)

There are two GPIO controller units, each unit can manage up to 8 GPIOs. All GPIOs in a unit can be operated in a single operation. The register **GPADATA** is register matrix which both occupy 256 bytes address space (8-bit).

GPIO Controller Address	GPIO Pin Name
GPA[0]	GPIO1
GPA[1]	GPIO2
GPA[2]	LIN_IN
GPA[3]	GPIO3
GPA[4]	GPIO4
GPA[5]	Not used
GPA[6]	Not used
GPA[7]	Not used

In the GPIO register matrix operation, the 8-bit address controls the select signal and the 8-bit value is the level signal. For example, write (1<<0|0<<3) to the **GPADATA** register with byte offset (1<<0|1<<3) will change GPIO1 to low level and change GPIO3 to high level without any influence on other GPIOs. Read/Write the **GPADATA** register with the byte offset 0xFF will read/write all GPIOs at the same time.

There are all available registers about GPIO configuration:

- **GPIO.GPAENA** enables the gated clock of GPIO unit
- **GPIO.GPADIR[n]** (n=0,1,2,3,4) enables the push-pull output
- **IOCTRLA.GPIOx.RDENA** (n=1,2,3,4) enables the input path
- **GPIO.GPADATA<1024>** reads/writes the level of GPIO input/output

- **IOCTRLA.GPIOx.PUENA** and **IOCTRLA.GPIOx.PDENA** (n=1,2,3,4) enables the pull-up and pull-down function
- **GPIO.GPxIE[n]** (n=0,1,2,3,4) enables the edge interrupt
- **GPIO.GPxRE[n]** (n=0,1,2,3,4) enables the rising edge interrupt
- **GPIO.GPxFE[n]** (n=0,1,2,3,4) enables the falling edge interrupt
- **GPIO.GPxACTDET[n]** (n=0,1,2,3,4) indicates the interrupt flag
- **GPIO.GPxACTDETFE[n]** (n=0,1,2,3,4) indicates the rising edge interrupt flag
- **GPIO.GPxACTDETRE[n]** (n=0,1,2,3,4) indicates the falling edge interrupt flag
- **GPIO.GPxCLR[n]** (n=0,1,2,3,4) clears the interrupt flag
- **IOCTRLA.GPIOx.HWMODE** (n=1,2,3,4) controls the digital multiplexing selection
- **SAR_CTRL.CHn_SEL** (n=1,2,3,4) enables the analog path from GPIO to ADC

All GPIO interrupts share a same interrupt number, users must check the **GPIO.GPxACTDET[n]** registers to determine the actual interrupt source.

9.2.10 IO Capture

The ASIC implements 4 individual IO capture channels of 4 GPIOs. Four 16-bit counters are used to measure the period and duty of GPIOs input. The counters are using the system clock as clock source and integrate a pre-scaler that can divide the system clock by 2, 4, 8 or 16.

There are two interrupt sources, one for rising edge signal and one for counter overflow.

9.2.11 Over and Under Voltage detection (VBAT)

The over and under voltage comparators are based on comparing a divided voltage from the Load Dump limiter output feeding an analog comparator with hysteresis (refer to EC Table for electrical parameters and PMU description). The Over and Under voltage events generate Interrupts to the interrupt controller.

9.2.12 Temperature monitor

The MCU is in charge to pull the ADC related data from temperature sensor and in case the measured data is too high, MCU will reduce power profile to reduce heat. Table 16 shows the tempsensor output voltage corresponding to Tj from analog simulation for reference. Calibration is required due to different offset per chip.

Table 16 Tempsensor Output voltage vs Junction Temp

Junction Temp (°C)	Tempsensor Output Voltage(V) @VBAT=13.5V
-40	0.560568295
-30	0.585118532
-20	0.609746794
-10	0.634447014
0	0.659214959
10	0.68404771
20	0.70894409
30	0.733905116
40	0.758934482
50	0.784039045
60	0.809229285
70	0.834519924
80	0.859930773
90	0.885488251
100	0.911227796
110	0.937197714
120	0.963465673
130	0.990130866
140	1.017345206
150	1.045353086

9.2.13 Over Temperature detection

The over temperature comparator monitors the junction temperature with hysteresis. The Over temperature event generates reset or interrupt to the interrupt controller.

9.2.14 ASIC Watchdog Timer

While it exists a watchdog timer in the MCU, the ASIC integrates another watch-dog timer that is intended to be used to recover from a situation where there may have been a software fault or other system failure where the software has ceased to operate correctly. If the timer is not reset by software periodically, it will time out, and this event can be used to reset the system or generate an interrupt (Refer to Register Description).

Features:

- Programmable timeout period (Refer to Register Description) with instantaneous access to the value of watchdog timeout counter
- Status flag, stop and clear/reset control registers
- The Watchdog timer is by default active after power up and set to its maximum duration setting (Refer to Register Description)
- Window mode supported: If enabled, WDTA can only be cleared after the watchdog window opened and before time-out period; Otherwise, WDTA will issue a system reset or an interrupt (Refer to Register Description).

9.2.15 SLEEP (Hibernate/DeepSleep) Modes

IC can enter SLEEP mode through SW request(See 8.2.2.1 PMUA->CTRL.HIBERNATE). The device comes out of SLEEP with either the slow auxiliary or the system clock. It's up to the SW to select which clock shall be used after a wake event is detected. The SW does't have to request to go to SLEEP with the same clock selected for wake up.

There are two major SLEEP modes:

1. Hibernate mode: In this mode, MCU and ASIC's Core(1.5V)/IO(3.3V) power domains are off. In this mode, only lin wakeup is available as the wakeup source. This mode has an extremely low current consumption.
2. Deepsleep mode: If PMUA->CTRL.PD1V5_ENA_HIBERNATE(See 8.2.2.1) is set, ASIC's Core & IO supplies remain active after chip enters low power mode. This mode can keep IO status and supports more wakeup sources in the low power mode.

9.2.15.1 Wake up Sources

Coming out from Hibernate mode can happen through the following events:

- LIN Wakeup : After a low pulse on the LIN pin such that a dominant (low) voltage level is applied for longer than TWAKEUP time. Notice that LIN wakeup interrupts can be generated in either active or Hibernate mode when bit SLEEP = 1. This wakeup source is available in active/hibernate/deepsleep modes.
- GPIOs pin toggling either from high to low or low to high levels (VIL/VIH). This kind of wakeup sources are available in active/deepsleep modes.
- Wake up timer. Programmable range. Wake up timer has the option to be disabled. This wakeup source is available deepsleep mode.

MCU can check which wake up events triggered the system through a status register read. MCU to clear the register after status check.

10 DISCLAIMERS

Indiemicro reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time. Please consult the most recently issued document before initiating or completing a design.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

indie Semiconductor:

IND83212