MR5A16A

32Mb MRAM

2M x 16 MRAM

FEATURES

- +3.3 Volt power supply
- Fast 35ns read/write cycle (45ns for automotive temperature range)
- SRAM compatible timing
- Unlimited read & write endurance
- Data always non-volatile for >20 years at temperature
- RoHS-compliant small footprint 48-pin BGA and TSOP2 package
- All products meet MSL-3 moisture sensitivity level
- Commercial, Industrial and Automotive temperature ranges available

RoHS

BENEFITS

- One memory replaces FLASH, SRAM, EEPROM, NVSRAM and BBSRAM in systems for simpler, more efficient designs
- Improves reliability by replacing battery-backed SRAM

INTRODUCTION

The MR5A16A is a 33,554,432-bit magnetoresistive random access memory (MRAM) device organized as 2,097,152 words of 16 bits. The MR5A16A offers SRAM compatible 35 ns read/write timing (45ns for automotive temperature option) with unlimited endurance. Data is always non-volatile for greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. To simplify fault tolerant design, the MR5A16A includes internal single bit error correction code with 7 ECC parity bits for every 64 data bits. The MR5A16A is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The **MR5A16A** is available in a small footprint 48-pin ball grid array (BGA) package and a 54-pin thin small outline package (TSOP Type 2). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.

The **MR5A16A** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C), industrial temperature (-40 to +85 °C) and automotive temperature (-40 to +125°C) operating temperature options. These products are not AEC Q-100 qualified.

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1. DEVICE PIN ASSIGNMENT

Figure 1.1 Block Diagram

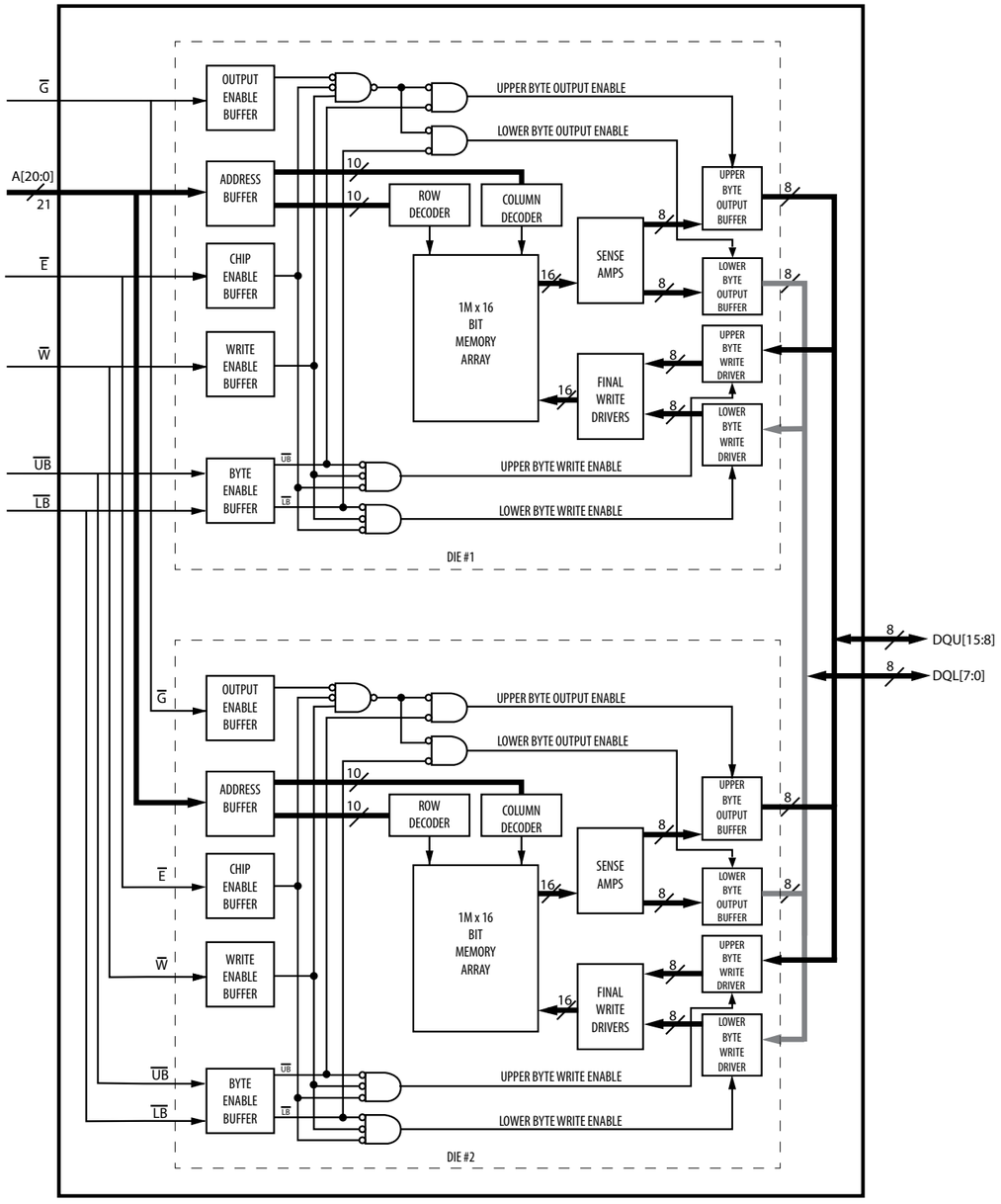
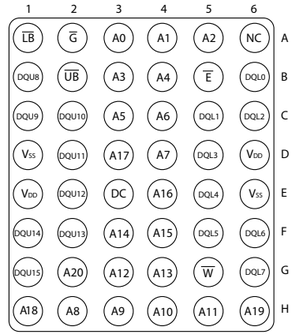


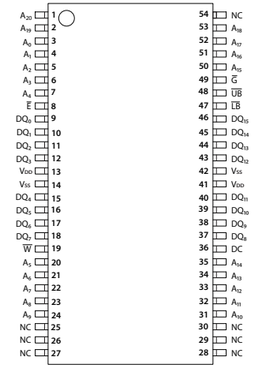
Table 1.1 Pin Functions

Signal Name	Function
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection

Figure 1.1 Package Pin Diagram (Top View)



48-Pin BGA



54-Pin TSOP2

Table 1.2 Operating Modes

$\overline{E}$[1]	$\overline{G}$[1]	$\overline{W}$[1]	$\overline{LB}$[1]	$\overline{UB}$[1]	Mode	V_{DD} Current	DQL[7:0][2]	DQU[15:8][2]
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Lower Byte Read	I_{DDR}	D_{Out}	Hi-Z
L	L	H	H	L	Upper Byte Read	I_{DDR}	Hi-Z	D_{Out}
L	L	H	L	L	Word Read	I_{DDR}	D_{Out}	D_{Out}
L	X	L	L	H	Lower Byte Write	I_{DDW}	D_{in}	Hi-Z
L	X	L	H	L	Upper Byte Write	I_{DDW}	Hi-Z	D_{in}
L	X	L	L	L	Word Write	I_{DDW}	D_{in}	D_{in}

[1] H = high, L = low, X = don't care

[2] Hi-Z = high impedance

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field greater than the maximum field intensity specified in the maximum ratings.

Table 2.1 Absolute Maximum Ratings [1]

Symbol	Parameter	Conditions	Value	Unit
V_{DD}	Supply voltage[2]		-0.5 to 4.0	V
V_{IN}	Voltage on an pin [2]		-0.5 to V_{DD} + 0.5	V
I_{OUT}	Output current per pin		±20	mA
P_D	Package power dissipation [3]		0.600	W
T_{BIAS}	Temperature under bias	Commercial	-10 to 85	°C
		Industrial	-45 to 95	°C
T_{stg}	Storage Temperature		-55 to 150	°C
T_{Lead}	Lead temperature during solder (3 minute max)		260	°C
H_{max_write}	Maximum magnetic field	During Write	8000	A/m
H_{max_read}	Maximum magnetic field	During Read or Standby		

[1] Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

[2] All voltages are referenced to V_{SS}. The DC value of V_{IN} must not exceed actual applied V_{DD} by more than 0.5V. The AC value of V_{IN} must not exceed applied V_{DD} by more than 2V for 10ns with I_{IN} limited to less than 20mA.

[3] Power dissipation capability depends on package characteristics and use environment.

Table 2.2 Operating Conditions

Symbol	Parameter	Temp Range	Min	Typical	Max	Unit
V_{DD}	Power supply voltage		3.0 [1]	3.3	3.6	V
V_{WI}	Write inhibit voltage		2.5	2.7	3.0 [1]	V
V_{IH}	Input high voltage		2.2	-	V_{DD} + 0.3 [2]	V
V_{IL}	Input low voltage		-0.5 [3]	-	0.8	V
T_A	Temperature under bias [4]	Commercial	0	-	70	°C
		Industrial	-40	-	85	°C
		Automotive	-40	-	125	°C

[1] There is a 2 ms startup time once V_{DD} exceeds V_{DD}(min). See **Power Up and Power Down Sequencing** below.

[2] V_{IH}(max) = V_{DD} + 0.3 V_{DC}; V_{IH}(max) = V_{DD} + 2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

[3] V_{IL}(min) = -0.5 V_{DC} ; V_{IL}(min) = -2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

[4] The ambient operature temperature rating assumes a 10% duty cycle (2 years out of 20 years life) for operating temperatures between +85°C and +125°C.

Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The $\overline{E}$ and $\overline{W}$ control signals should track V_{DD} on power up to V_{DD}- 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that a signal remains high if the driving signal is Hi-Z during power up. Any logic that drives $\overline{E}$ and $\overline{W}$ should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

Figure 2.1 Power Up and Power Down Diagram

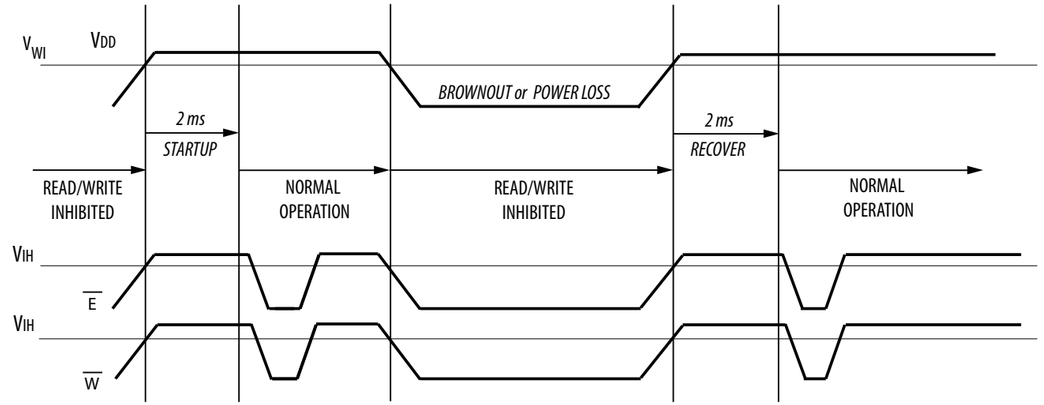


Table 2.3 DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{lkg(I)}$	Input leakage current	All	-	±1	µA
$I_{lkg(O)}$	Output leakage current	All	-	±1	µA
V_{OL}	Output low voltage	I_{OL} = +4 mA	-	0.4	V
		I_{OL} = +100 µA		V_{SS} + 0.2	V
V_{OH}	Output high voltage	I_{OH} = -4 mA	2.4	-	V
		I_{OH} = -100 µA	V_{DD} - 0.2	-	V

Table 2.4 Power Supply Characteristics

Symbol	Parameter	Typical	Max	Unit
I_{DDR}	AC active supply current - read modes[1] (I_{OUT}= 0 mA, V_{DD}= max)	60	75	mA
I_{DDW}	AC active supply current - write modes[1] (V_{DD}= max)	152	180	mA
I_{SB1}	AC standby current (V_{DD}= max, $\overline{E} = V_{IH}$) *no other restrictions on other inputs*	18	28	mA
I_{SB2}	CMOS standby current ($\overline{E} \geq V_{DD}$ - 0.2 V and $V_{In} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} - 0.2 V) (V_{DD} = max, f = 0 MHz)	10	18	mA

[1] All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. TIMING SPECIFICATIONS

Table 3.1 Capacitance [1]

Symbol	Parameter	Typical	Max	Unit
C_{In}	Address input capacitance	-	8	pF
C_{In}	Control input capacitance	-	8	pF
$C_{I/O}$	Input/Output capacitance	-	8	pF

[1] f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

Table 3.2 AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 3.1	
Output load for all other timing parameters	See Figure 3.2	

Figure 3.1 Output Load Test Low and High

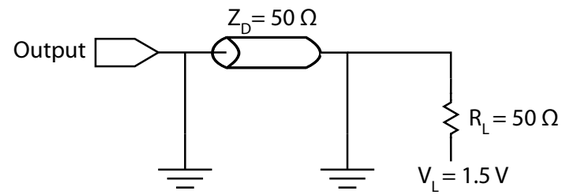
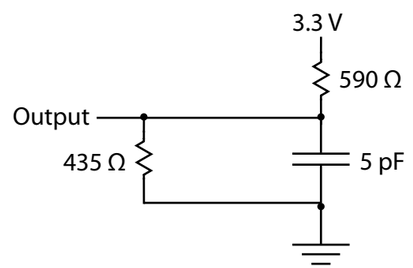


Figure 3.2 Output Load Test All Others



Read Mode

Table 3.3 Read Cycle Timing [1]

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Read cycle time	35 [45] [4]	-	ns
t_{AVQV}	Address access time	-	35 [45] [4]	ns
t_{ELQV}	Enable access time [2]	-	35 [45] [4]	ns
t_{GLQV}	Output enable access time	-	15	ns
t_{BLQV}	Byte enable access time	-	15	ns
t_{AXQX}	Output hold from address change	3	-	ns
t_{ELQX}	Enable low to output active [3]	3	-	ns
t_{GLQX}	Output enable low to output active [3]	0	-	ns
t_{BLQX}	Byte enable low to output active [3]	0	-	ns
t_{EHQZ}	Enable high to output Hi-Z [3]	0	15	ns
t_{GHQZ}	Output enable high to output Hi-Z [3]	0	10	ns
t_{BHQZ}	Byte high to output Hi-Z [3]	0	10	ns

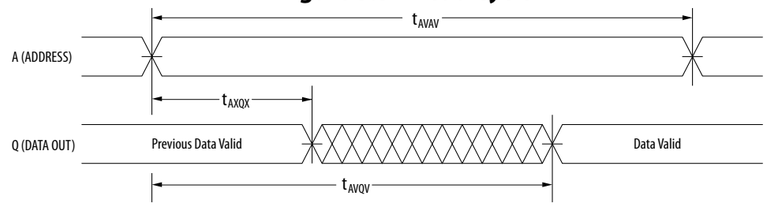
[1] $\overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

[2] Addresses valid before or at the same time $\overline{E}$ goes low.

[3] This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage.

[4] Specification in square brackets [xx] applicable for automotive temperature range option only.

Figure 3.3A Read Cycle 1



Note: Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

Figure 3.3B Read Cycle 2

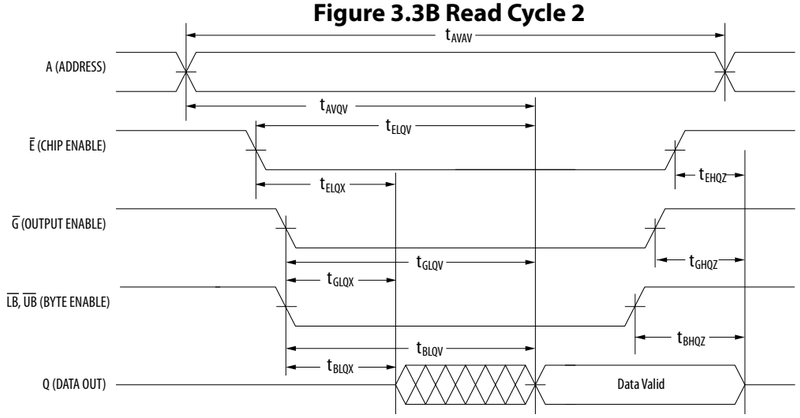


Table 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled) [1]

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Write cycle time [2]	35 [45] [4]	-	ns
t_{AVWL}	Address set-up time	0	-	ns
t_{AVWH}	Address valid to end of write ($\overline{G}$ high)	20 [30] [4]	-	ns
t_{AVWH}	Address valid to end of write ($\overline{G}$ low)	20 [30] [4]	-	ns
t_{WLWH} t_{WLEH}	Write pulse width ($\overline{G}$ high)	15	-	ns
t_{WLWH} t_{WLEH}	Write pulse width ($\overline{G}$ low)	15	-	ns
t_{DVWH}	Data valid to end of write	10	-	ns
t_{WHDX}	Data hold time	0	-	ns
t_{WLQZ}	Write low to data Hi-Z [3]	0	15	ns
t_{WHQX}	Write high to output active [3]	3	-	ns
t_{WHAX}	Write recovery time	12	-	ns

[1] All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If G goes low at the same time or after W goes low, the output will remain in a high impedance state. After W, E or UB/LB has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between E being asserted low in one cycle to E being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

[2] All write cycle timings are referenced from the last valid address to the first transition address.

[3] This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage. At any given voltage or temperate, t_{WLQZ}(max) < t_{WHQX}(min).

[4] Specification in square brackets [xx] applicable for automotive temperature range option only.

Figure 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled)

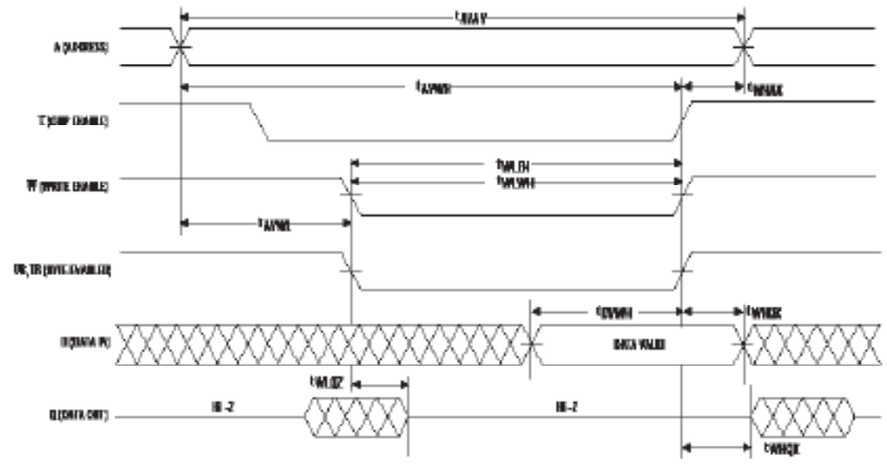


Table 3.5 Write Cycle Timing 2 ($\overline{E}$ Controlled) [1]

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Write cycle time [2]	35 [45] [4]	-	ns
t_{AVEL}	Address set-up time	0	-	ns
t_{AVEH}	Address valid to end of write ($\overline{G}$ high)	20 [30] [4]	-	ns
t_{AVEH}	Address valid to end of write ($\overline{G}$ low)	20 [30] [4]	-	ns
t_{ELEH} t_{ELWH}	Enable to end of write ($\overline{G}$ high)	15	-	ns
t_{ELEH} t_{ELWH}	Enable to end of write ($\overline{G}$ low) [3]	15	-	ns
t_{DVEH}	Data valid to end of write	10	-	ns
t_{EHDX}	Data hold time	0	-	ns
t_{EHAX}	Write recovery time	12	-	ns

[1] All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If G goes low at the same time or after W goes low, the output will remain in a high impedance state. After W, E or UB/ LB has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between E being asserted low in one cycle to E being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

[2] All write cycle timings are referenced from the last valid address to the first transition address.

[3] If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

[4] Specification in square brackets [xx] applicable for automotive temperature range option only.

Figure 3.5 Write Cycle Timing 2 ($\overline{E}$ Controlled)

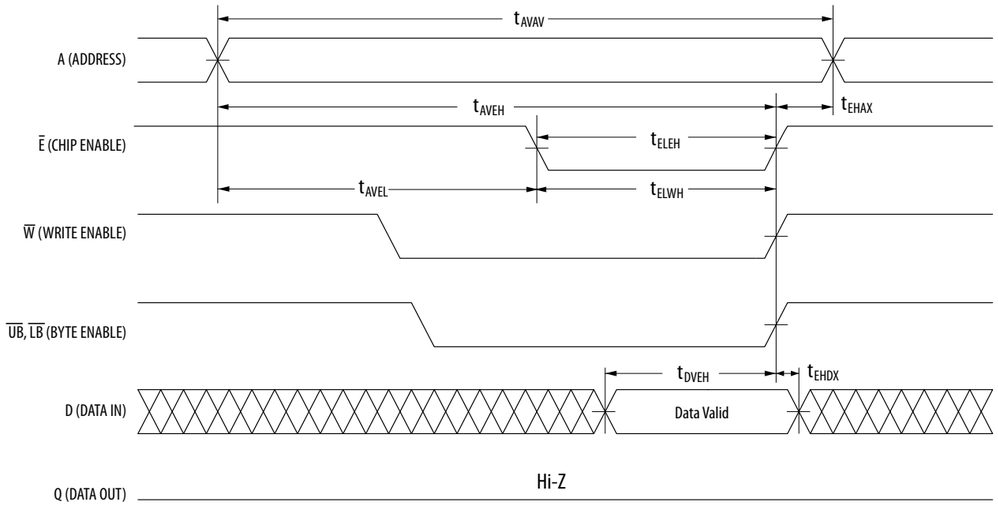


Table 3.6 Write Cycle Timing 3 ($\overline{LB}$/$\overline{UB}$ Controlled) [1]

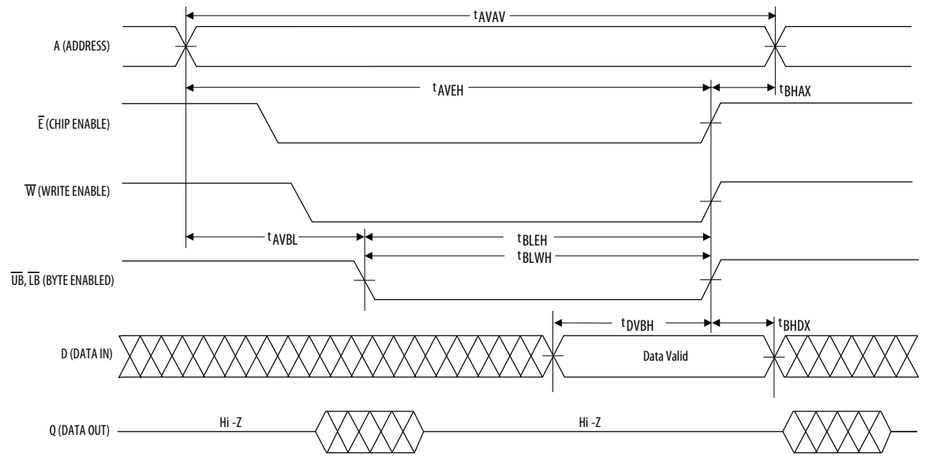
Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Write cycle time [2]	35 [45] [3]	-	ns
t_{AVBL}	Address set-up time	0	-	ns
t_{AVBH}	Address valid to end of write ($\overline{G}$ high)	20 [30] [3]	-	ns
t_{AVBH}	Address valid to end of write ($\overline{G}$ low)	20 [30] [3]	-	ns
t_{BLEH} t_{BLWH}	Write pulse width ($\overline{G}$ high)	15	-	ns
t_{BLEH} t_{BLWH}	Write pulse width ($\overline{G}$ low)	15	-	ns
t_{DVBH}	Data valid to end of write	10	-	ns
t_{BHDX}	Data hold time	0	-	ns
t_{BHAX}	Write recovery time	12	-	ns

[1] All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If G goes low at the same time or after W goes low, the output will remain in a high impedance state. After W, E or UB/LB has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between E being asserted low in one cycle to E being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

[2] All write cycle timings are referenced from the last valid address to the first transition address.

[3] Specification in square brackets [xx] applicable for automotive temperature range option only.

Figure 3.6 Write Cycle Timing 3 ($\overline{LB}$/$\overline{UB}$ Controlled)



4. ORDERING INFORMATION

Figure 4.1 Part Numbering System

MR	5	A	16	A	C	MA	35	R		
									Carrier	Blank = Tray, R = Tape & Reel
									Speed	35ns, 45ns
									Package	MA = FBGA, YS = TSOP
									Temperature Range	Blank= Commercial (0 to +70 °C), C= Industrial (-40 to +85°C) U= Automotive (-40 to +125°C)
									Revision	
									Data Width	16 = 16-bit
									Type	A = Asynchronous
									Density	5 =32Mb
									Magnetoresistive RAM	

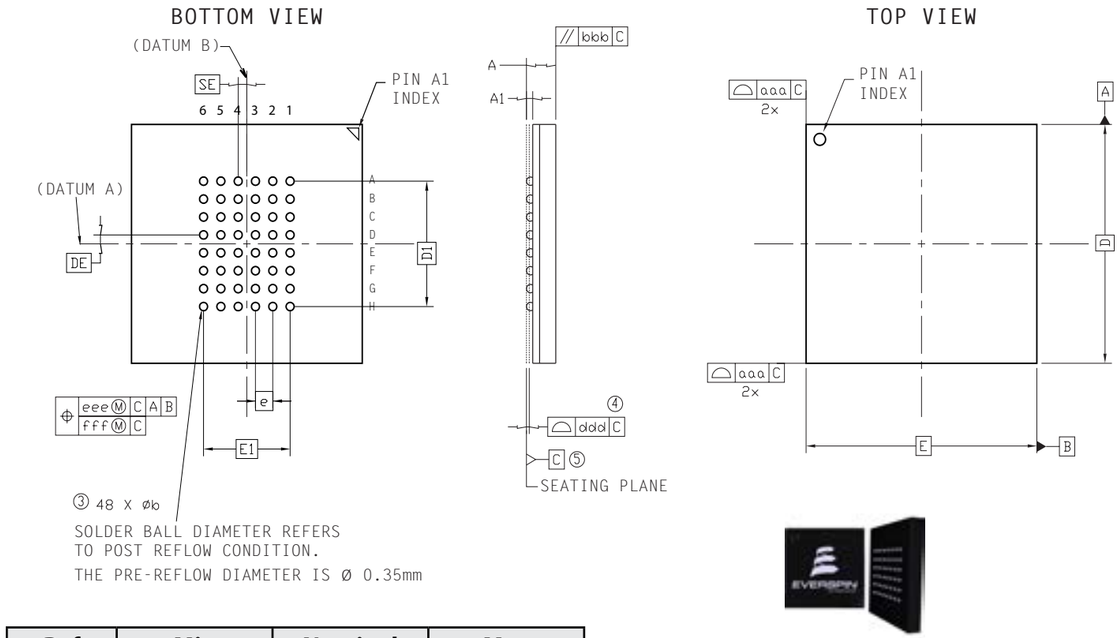
Table 4.1 Available Parts

Grade	Temp Range	Package	Shipping Container	Order Part Number
Commercial	0 to +70 °C	48-BGA	Trays	MR5A16AMA35
			Tape & Reel	MR5A16AMA35R
		54-TSOP2	Trays	MR5A16AYS35
			Tape & Reel	MR5A16AYS35R
Industrial	-40 to +85°C	48-BGA	Tray	MR5A16ACMA35
			Tape & Reel	MR5A16ACMA35R
		54-TSOP2	Tray	MR5A16ACYS35
			Tape & Reel	MR5A16ACYS35R
Automotive[1]	-40 to +125°C	48-BGA	Tray	MR5A16AUMA45
			Tape & Reel	MR5A16AUMA45R
		54-TSOP2	Tray	MR5A16AUYS45
			Tape & Reel	MR5A16AUYS45R

1. Not AEC Q-100 Qualified.

5. MECHANICAL DRAWING

Figure 5.1 48-FBGA



Ref	Min	Nominal	Max
A	1.19	1.27	1.35
A1	0.22	0.27	0.32
b	0.31	0.36	0.41
D		10.00 BSC	
E		10.00 BSC	
D1		5.25 BSC	
E1		3.75 BSC	
DE		0.375 BSC	
SE		0.375 BSC	
e		0.75 BSC	

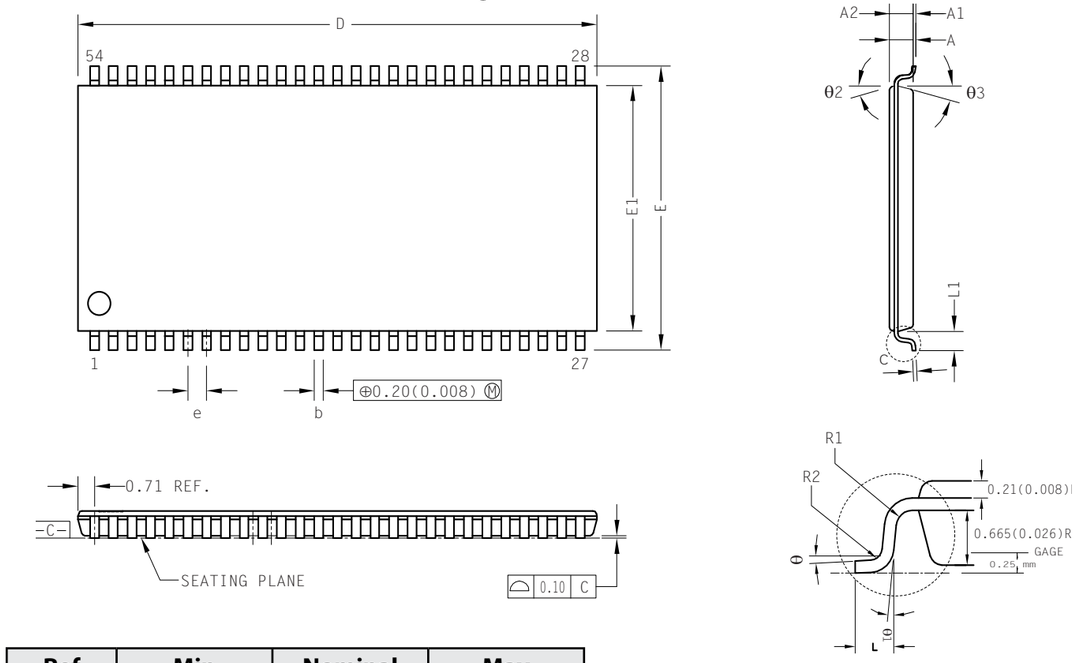
Ref	Tolerance of, from and position
aaa	0.10
bbb	0.10
ddd	0.10
eee	0.15
fff	0.08

Print Version Not To Scale

1. Dimensions in Millimeters.
2. The 'e' represents the basic solder ball grid pitch.
3. 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
4. Dimension 'ddd' is measured parallel to primary datum C.
5. Primary datum C (seating plane) is defined by the crowns of the solder balls.
6. Package dimensions refer to JEDEC MO-205 Rev. G.

5. MECHANICAL DRAWING

Figure 5.2 54-TSOP2



Ref	Min	Nominal	Max
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.45
c	0.12		0.21
D	22.10	22.22	22.35
E	11.56	11.76	11.95
E1	10.03	10.16	10.29
e	0.80 BSC		
L	0.40	0.50	0.60
L1	0.80 REF		
R1	0.12	-	-
R2	0.12	-	0.25
θ	0°	-	8°
θ1	0.40	-	-
θ2	15° REF		
θ3	15° REF		

Print Version Not To Scale

1. Dimensions in Millimeters.
2. Package dimensions refer to JEDEC MS-024

6. REVISION HISTORY

Rev	Date	Description of Change
1.0	Nov 20, 2019	Released first version of the datasheet
1.1	Jan 10, 2023	Removed errata and restored MSL-3

7. HOW TO CONTACT US

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