AsahiKASEI MICRODEVICES

AK7017

HiFi 4 DSP and SRCs

1. General Description

The AK7017 is a highly integrated digital signal processor, including 8 stereo and 4 monaural sampling rate converters supporting sampling frequency up to 192kHz, a DIR, a DIT and DSP for Audio and Voice processing. The DSP1 supports 491.52MHz operation clock and are optimized for C-language support. The AK7017 is a RAM based DSP1 it can be freely programmed for user requirements, such as acoustic effects.

2. Features

- DSP1 (HiFi 4-a):
  - Word Length: 64-bit
  - Operation Clock: 491.52MHz
  - MAC: 32 x 32-bit (Quad) or 16 x 16-bit (Octal)
  - ALU: 4 x 64-bits
  - IRAM0: 64kB
  - IRAM1: 384kB
  - DRAM1: 1024kB
  - Audio I/O Buffer: 4 x I/O x Double Buffer x 4kB
  - SPI Slave I/O Buffer: 2 x 4kB

- SRC
  - 2ch x 8 (Stereo 32bit)
  - 1ch x 4 (Monaural 24bit) or 2ch x 2 (Stereo 24bit)
  - FSI = 8kHz - 192kHz, FSO= 8kHz - 192kHz (FSO/FSI= 0.167 - 6.0)

- DIT
  - S/PDIF, IEC60958, AES/EBU, EIAJ CP1201 Compatible
  - 24-bit x 1
  -

- DIR
  - S/PDIF, IEC60958, AES/EBU, EIAJ CP1201 Compatible
  - Built-in Amplifier x 1
  - De-emphasis Filter (support 32, 44.1, 48 and 96kHz, On/OFF function)
  - Non-PCM Data Stream Detection
  - DTS-CD Data Stream Detection
  - Sampling Frequency Detection (8, 16, 24, 32, 44.1, 48, 88.2, 96, 192kHz)
  - Guaranteed range of jitter tolerance (32, 44.1, 48, 88.2, 96, 192kHz)
  - Unlock & Parity Error Detection
  - Validity Detection Register Read-back Function
  - Buffer for First 42 bits of Channel Status Word
  - Buffer for CD Qsubcode

- Digital Interfaces
  - Digital Input 11 Ports (Max. 152ch, 32ch x 1 + 16ch x 5 + 8ch x 5 when TDM Mode)
  - Digital Output 11 Ports (Max. 152ch, 32ch x 1 + 16ch x 5 + 8ch x 5 when TDM Mode)
  - Independent LRCK/BICK Input/Output Ports x 8
  - Data format: MSB justified 32, 24-bit/ LSB justified 4, 20, 16-bit / I^2S
  - Short/ Long Frame
  - TDM Input/Output Mode
  - Digital Microphone Input Port (2ch x 2)

- SPI Slave Interface (Quad, Dual Support) x 2
- SPI Master Interface (Quad, Dual Support) x 2
- I^2C Interface x 2
- GPIO: 16 Ports (for Both DSP1 and 2)
- JTAG for On-chip debugging
- UART 1 port:
- I^2C Master

- Digital Mixer x 2

- PLL Circuit

- MCU Interface 1/2: SPI (49.152MHz Max.) x 2 / I^2C (400kHz Fast Mode) x 2

- Power Supply:

Digital:	VDDC:	0.85V - 0.95V (Typ. 0.9V)
I/F:	TVDD1:	1.7V - 3.47V (Typ. 3.3V)
	TVDD2:	1.7V - 3.47V (Typ. 3.3V)
	TVDD3:	1.7V - 3.47V (Typ. 3.3V)
	AVDD:	3.13V - 3.47V (Typ. 3.3V)

- Operating Temperature Range: Ta= -40 - 105ºC

- Package: 100-pin HLQFP 14.0mm x 14.0mm / 0.5mm pitch

3. Table of Contents

4. Block Diagram and Functions

4.1. Overall Block Diagram

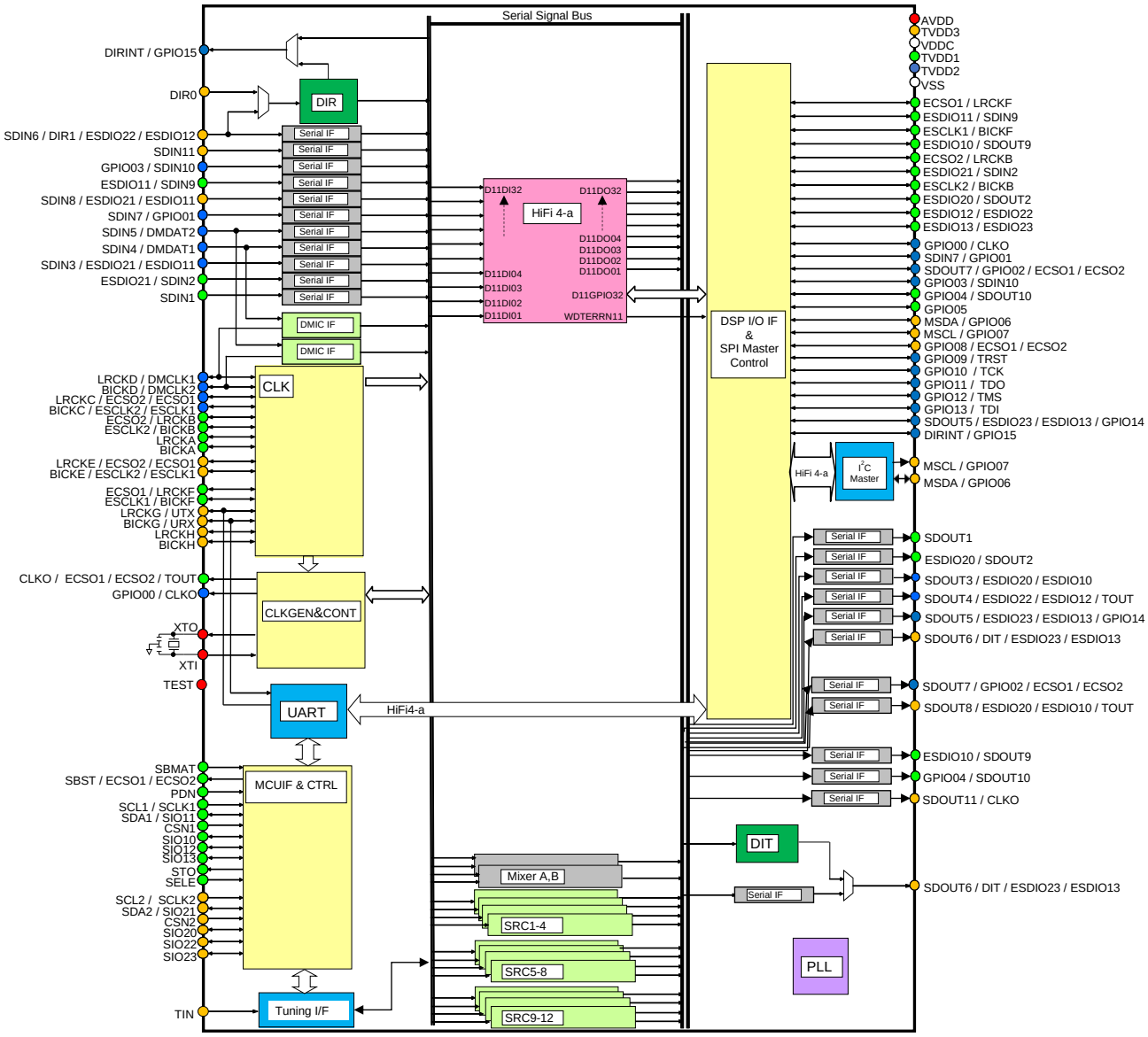


Figure 1. Overall Block Diagram

4.2. DSP1(HiFi 4-a) Block Diagram

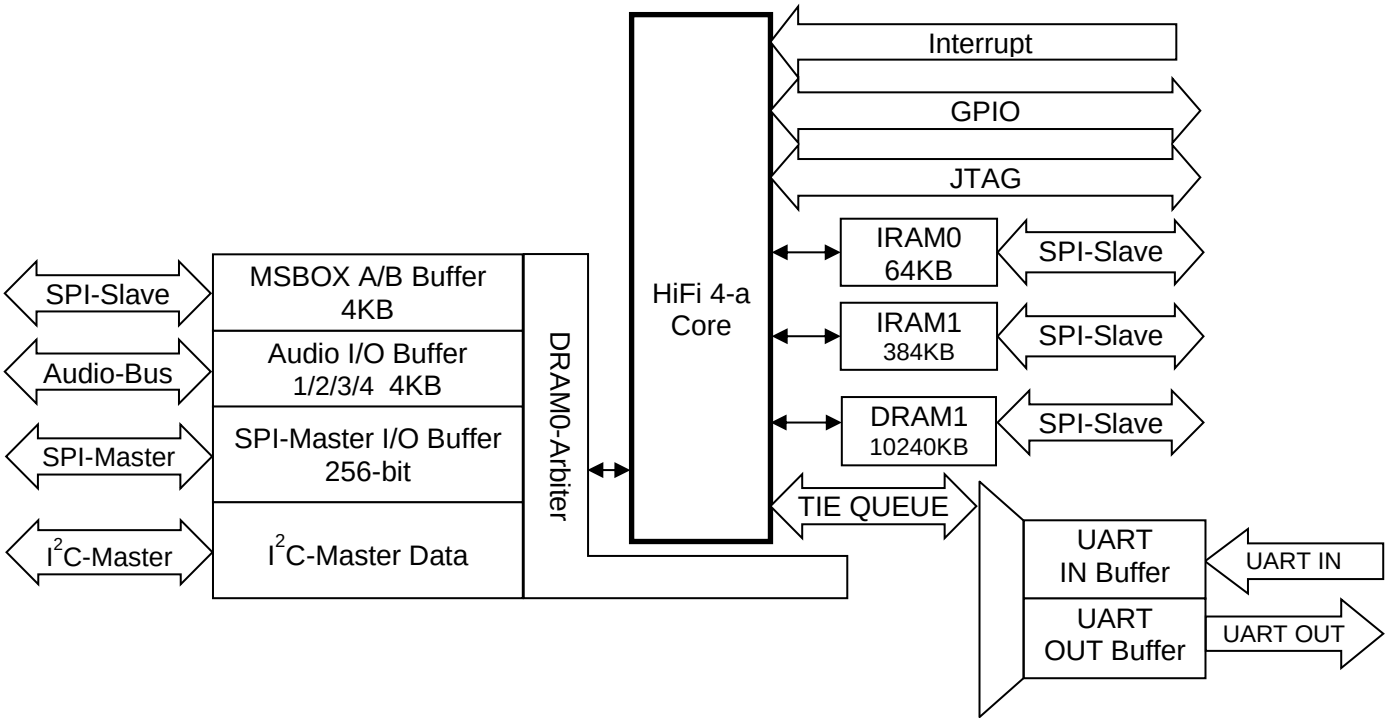


Figure 2. DSP1(HiFi 4-a) Block Diagram

5. Pin Configurations and Functions

5.1. Pin Configurations

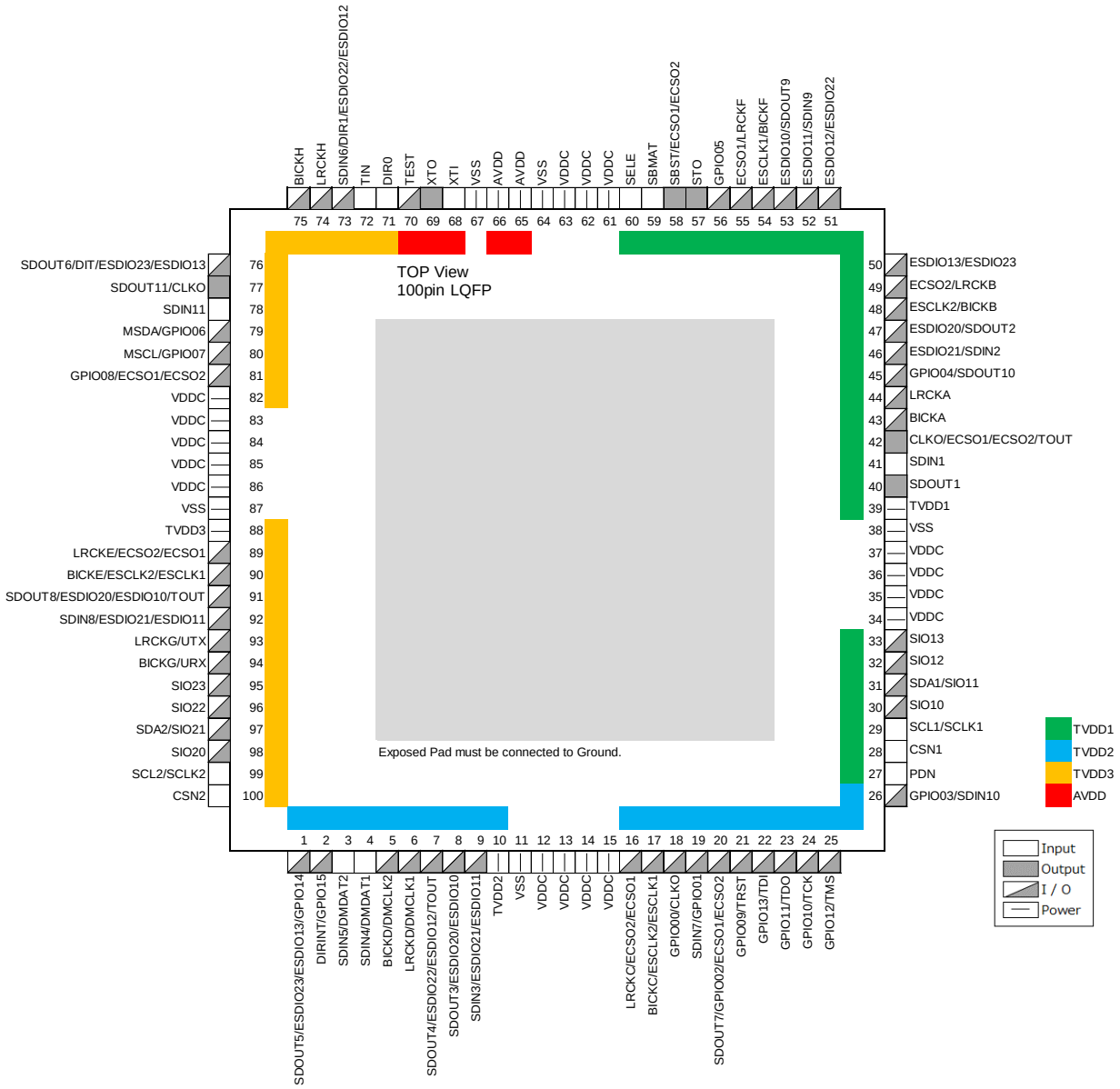


Figure 3. Pin Configurations

5.2. Pin Functions

No.	Pin Name	I/O	Function	Power
1	SDOUT5	O	Serial Digital Data Output 5	TVDD2
	ESDIO23	I/O	SPI Master Interface 2 In/Output 3 (Input Pulled-down)	
	ESDIO13	I/O	SPI Master Interface 1 In/Output 3 (Input Pulled-down)	
	GPIO14	I/O	DSP1 GPIO14 (Input Pulled-down) Controlled by DSP1 program.	
2	DIRINT	O	DIR Interrupt Output Alert	TVDD2
	GPIO15	I/O	DSP1 GPIO15 (Input Pulled-down) Controlled by DSP1 program.	
3	SDIN5	I	Serial Digital Data Input (Input Pulled-down)	TVDD2
	DMDAT2	I	DATA 2 Input for Digital Microphone (Input Pulled-down)	
4	SDIN4	I	Serial Digital Data Input (Input Pulled-down)	TVDD2
	DMDAT1	I	DATA 1 Input for Digital Microphone (Input Pulled-down)	
5	BICKD	I/O	Serial Bit Clock D (Input Pulled-down)	TVDD2
	DMCLK2	O	Clock Output 2 for Digital Microphone	
6	LRCKD	I/O	Frame Sync / Left-Right Clock D (Input Pulled-down)	TVDD2
	DMCLK1	O	Clock Output 1 for Digital Microphone	
7	SDOUT4	O	Serial Digital Data Output 4	TVDD2
	ESDIO22	I/O	SPI Master Interface 2 In/Output 2 (Input Pulled-down)	
	ESDIO12	I/O	SPI Master Interface 1 In/Output 2 (Input Pulled-down)	
	TOUT	O	TEST Output	
8	SDOUT3	O	Serial Digital Data Output 3	TVDD2
	ESDIO20	I/O	SPI Master Interface2 In/Output pin0 (Input Pulled-down)	
	ESDIO10	I/O	SPI Master Interface1 In/Output pin0 (Input Pulled-down)	
9	SDIN3	I	Serial Digital Data Input 3 (Input Pulled-down)	TVDD2
	ESDIO21	I/O	SPI Master Interface 2 In/Output (Input Pulled-down)	
	ESDIO11	I/O	SPI Master Interface 1 In/Output (Input Pulled-down)	
10	TVDD2	-	Digital Interface Power Supply 2 Typ. 3.3V (1.7V - 3.47V)	-
11	VSS	-	Ground 0V	-
12	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
13	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
14	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
15	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
16	LRCKC	I/O	Frame Sync / Left-Right Clock C (Input Pulled-down)	TVDD2
	ECSO2	O	SPI Master Interface 2 Output for External Devices (Connect to the CS pin of External Device 2)	
	ECSO1	O	SPI Master Interface 1 Output for External Devices (Connect to the CS pin of External Device 1)	
17	BICKC	I/O	Serial Bit Clock C (Input Pulled-down)	TVDD2
	ESCLK2	O	SPI Master Interface 2 Clock Output for External Devices (Connect to the SCLK pin of External Device 2)	
	ESCLK1	O	SPI Master Interface 1 Clock Output for External Devices (Connect to the SCLK pin of External Device 1)	
18	GPIO00	I/O	DSP1 GPIO00 (Input Pulled-down) Controlled by DSP1 program.	TVDD2
	CLKO	O	Master Clock Output	

No.	Pin Name	I/O	Function	Power
19	SDIN7	I	Serial Digital Data Input 7 (Input Pulled-down)	TVDD2
	GPIO01	I/O	DSP1 GPIO 01 (Input Pulled-down) Controlled by DSP1 program.	
20	SDOUT7	O	Serial Digital Data Output 7	TVDD2
	GPIO02	I/O	DSP1 GPIO 02 (Input Pulled-down) Controlled by DSP1 program.	
	ECSO1	O	SPI Master Interface 1 Output for External Devices (Connect to the CS pin of External Device 1)	
	ECSO2	O	SPI Master Interface 2 Output for External Devices (Connect to the CS pin of External Device 2)	
21	GPIO09	I/O	DSP1 GPIO 09 (Input Pulled-down) Controlled by DSP1 program.	TVDD2
	TRST	I	JTAG Input (Input Pulled-down)	
22	GPIO13	I/O	DSP1 GPIO 13 (Input Pulled-down) Controlled by DSP1 program.	TVDD2
	TDI	I	JTAG Input (Input Pulled-down)	
23	GPIO11	I/O	DSP1 GPIO 11 (Input Pulled-down) Controlled by DSP1 program.	TVDD2
	TDO	O	JTAG Output	
24	GPIO10	I/O	DSP1 GPIO 10 (Input Pulled-down) Controlled by DSP1 program.	TVDD2
	TCK	I	JTAG Input (Input Pulled-down)	
25	GPIO12	I/O	DSP1 GPIO 12 (Input Pulled-down) Controlled by DSP1 program.	TVDD2
	TMS	I	JTAG Input (Input Pulled-down)	
26	GPIO03	I/O	DSP1 GPIO 03 (Input Pulled-down) Controlled by DSP1 program.	TVDD2
	SDIN10	I	Serial Digital Data Input 10(Input Pulled-down)	
27	PDN	I	Power-down Pin The AK7017 can be powered down by the PDN pin. Set this pin to “L” upon power-up the AK7017.	TVDD1
28	CSN1	I	I^2C Mode: Bus Address for I^2C Interface 1 This pin must be pulled up or pulled down.	TVDD1
			SPI Mode: Chip Select for SPI Interface 1 Set this pin to “H” in power-down state or when not interfacing to MCU.	
29	SCL1	I	Serial Data Clock Input for I^2C Interface 1	TVDD1
	SCLK1	I	Serial Data Clock Input for SPI interface 1	

No.	Pin Name	I/O	Function	Power
30	SIO10	I/O	SPI Slave Interface 1 Data In/Output 0 (Input Pulled-down) Connect a Pull-Down resistor (22kΩ recommended).	TVDD1
31	SDA1	I/O	SDA Pin for I^2C Interface 1 Connect a Pull-Down resistor (2.2kΩ recommended).	TVDD1
	SIO11	I/O	SPI Slave Interface 1 Data In/Output 1 (Input Pulled-down) Connect a Pull-Down resistor (22kΩ recommended).	
32	SIO12	I/O	SPI Slave Interface 1 Data In/Output 2 (Input Pulled-down) Connect a Pull-Down resistor (22kΩ recommended).	TVDD1
33	SIO13	I/O	SPI Slave Interface 1 Data In/Output 3 (Input Pulled-down) Connect a Pull-Down resistor (22kΩ recommended).	TVDD1
34	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
35	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
36	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
37	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
38	VSS	-	Ground 0V	-
39	TVDD1	-	Digital Interface Power Supply 1 Typ. 3.3V (1.7V - 3.47V)	-
40	SDOUT1	O	Serial Digital Data Output 1	TVDD1
41	SDIN1	I	Serial Digital Data Input 1 (Input Pulled-down)	TVDD1
42	CLKO	O	Master Clock Output	TVDD1
	ECSO1	O	SPI Master Interface 1 Data Output for External Device (Connected device side is CS)	
	ECSO2	O	SPI Master Interface 2 Data Output for External Device (Connected device side is CS)	
	TOUT	O	TEST Output	
43	BICKA	I/O	Serial Bit Clock A (Input Pulled-down)	TVDD1
44	LRCKA	I/O	Frame Sync / Left-Right Clock A (Input Pulled-down)	TVDD1
45	GPIO04	I/O	DSP1 GPIO04 (Input Pulled-down) Controlled by DSP1 program.	TVDD1
	SDOUT10	O	Serial Digital Data Output 10	
46	ESDIO21	I/O	SPI Master Interface 2 Data 1 In/Output (Input Pulled-down) (Connected device side is DIO)	TVDD1
	SDIN2	I	Serial Digital Data Input 2 (Input Pulled-down)	
47	ESDIO20	I/O	SPI Master Interface 2 Data 0 In/Output (Input Pulled-down) (Connected device side is DIO)	TVDD1
	SDOUT2	O	Serial Digital Data Output 2	
48	ESCLK2	O	SPI Master Interface 2 Clock Output for External Devices (Connect to the SCLK pin of External Device)	TVDD1
	BICKB	I/O	Serial Bit Clock B (Input Pulled-down)	
49	ECSO2	O	SPI Master Interface 2 Data Output for External Device (Connected device side is CS)	TVDD1
	LRCKB	I/O	Frame Sync / Left-Right Clock B (Input Pulled-down)	

No.	Pin Name	I/O	Function	Power
50	ESDIO13	I/O	SPI Master Interface 1 Data 3 In/Output (Input Pulled-down) (Connected device side is DIO)	TVDD1
	ESDIO23	I/O	SPI Master Interface 2 Data 3 In/Output (Input Pulled-down) (Connected device side is DIO)	
51	ESDIO12	I/O	SPI Master Interface 1 Data 2 In/Output (Input Pulled-down) (Connected device side is DIO)	TVDD1
	ESDIO22	I/O	SPI Master Interface 2 Data 2 In/Output (Input Pulled-down) (Connected device side is DIO)	
52	ESDIO11	I/O	SPI Master Interface 1 Data 1 In/Output (Input Pulled-down) (Connected device side is DIO)	TVDD1
	SDIN9	I	Serial Digital Data Input 9 (Input Pulled-down)	
53	ESDIO10	I/O	SPI Master Interface 1 Data 0 In/Output (Input Pulled-down) (Connected device side is DIO)	TVDD1
	SDOUT9	O	Serial Digital Data Output 9	
54	ESCLK1	O	SPI Master Interface 1 Clock Output for External Devices (Connect to the SCLK pin of External Device)	TVDD1
	BICKF	I/O	Serial Bit Clock F (Input Pulled-down)	
55	ECSO1	O	SPI Master Interface Data Output for External Device 1 (Connected device side is CS)	TVDD1
	LRCKF	I/O	Frame Sync / Left-Right Clock F (Input Pulled-down)	
56	GPIO05	I/O	DSP1 GPIO05 (Input Pulled-down) Controlled by DSP1 program.	TVDD1
57	STO	O	Status Output	TVDD1
58	SBST	O	Self-boot Status Output	TVDD1
	ECSO1	O	SPI Master Interface 1 Data Output for External Device (Connected device side is CS)	
	ECSO2	O	SPI Master Interface 2 Data Output for External Device (Connected device side is CS)	
59	SBMAT	I	Self-boot Program Selection (Input Pulled-down)	TVDD1
60	SELE	I	Self-boot Enable (Input Pulled-down)	TVDD1
61	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
62	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
63	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
64	VSS	-	Ground 0V	-
65	AVDD	-	Analog Power Supply Typ. 3.3V (3.13V - 3.47V)	-
66	AVDD	-	Analog Power Supply Typ. 3.3V (3.13V - 3.47V)	-
67	VSS	-	Ground 0V	-
68	XTI	I	Oscillation Circuit Input Connect a crystal oscillator between the XTI pin and the XTO pin. When not using a crystal oscillator, connect an external clock to this pin.	AVDD
69	XTO	O	Oscillation Circuit Output Connect a crystal oscillator between the XTI pin and the XTO pin. When not using crystal oscillator, this pin should be open.	AVDD
70	TEST	I/O	TEST In/Output (This pin should be left unconnected)	AVDD
71	DIR0	I	DIR Data Input 0	TVDD3
72	TIN	I	Tuning Interface Input pin (Input Pulled-down) This pin should be connected to VSS if not in use.	TVDD3

No.	Pin Name	I/O	Function	Power
73	SDIN6	I	Serial Digital Data Input 6(Input Pulled-down)	TVDD3
	DIR1	I	DIR Data Input 1 (Input Pulled-down)	
	ESDIO22	I/O	SPI Master Interface 2 Data 2 In/Output (Input Pulled-down) (Connected device side is DIO)	
	ESDIO12	I/O	SPI Master Interface 1 Data 2 In/Output (Input Pulled-down) (Connected device side is DIO)	
74	LRCKH	I/O	Frame Sync / Left-Right Clock H (Input Pulled-down)	TVDD3
75	BICKH	I/O	Serial Bit Clock H (Input Pulled-down)	TVDD3
76	SDOUT6	O	Serial Digital Data Output 6	TVDD3
	DIT	O	DIT Data Output	
	ESDIO23	I/O	SPI Master Interface 2 Data 3 In/Output (Input Pulled-down) (Connected device side is DIO)	
	ESDIO13	I/O	SPI Master Interface 1 Data 3 In/Output (Input Pulled-down) (Connected device side is DIO)	
77	SDOUT11	O	Serial Digital Data Output 11	TVDD3
	CLKO	O	Master Clock Output	
78	SDIN11	I	Serial Digital Data Input 11 (Input Pulled-down)	TVDD3
79	MSDA	I/O	I^2C Master Interface SDA Connect a Pull-Down resistor (2.2kΩ recommended).	TVDD3
	GPIO06	I/O	DSP1 GPIO06 (Input Pulled-down) Controlled by DSP1 program.	
80	MSCL	I/O	I^2C Master Interface SCL Connect a Pull-Down resistor (2.2kΩ recommended).	TVDD3
	GPIO07	I/O	DSP1 GPIO07 (Input Pulled-down) Controlled by DSP1 program.	
81	GPIO08	I/O	DSP1 GPIO08 (Input Pulled-down) Controlled by DSP1 program.	TVDD3
	ECSO1	O	SPI Master Interface 1 Data Output for External Device (Connected device side is CS)	
	ECSO2	O	SPI Master Interface 2 Data Output for External Device (Connected device side is CS)	
82	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
83	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
84	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
85	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
86	VDDC	-	Digital Core Power Supply Typ. 0.9V (0.85 - 0.95V)	-
87	VSS	-	Ground 0V	-
88	TVDD3	-	Digital Interface Power Supply 3 Typ. 3.3V (1.7V - 3.47V)	-
89	LRCKE	I/O	Frame Sync / Left-Right Clock E (Input Pulled-down)	TVDD3
	ECSO2	O	SPI Master Interface 2 Data Output for External Device (Connected device side is CS)	
	ECSO1	O	SPI Master Interface 1 Data Output for External Device (Connected device side is CS)	
90	BICKE	I/O	Serial Bit Clock E (Input Pulled-down)	TVDD3
	ESCLK2	O	SPI Master Interface 2 Clock Output for External Devices (Connect to the SCLK pin of External Device)	
	ESCLK1	O	SPI Master Interface 1 Clock Output for External Devices (Connect to the SCLK pin of External Device)	

No.	Pin Name	I/O	Function	Power
91	SDOUT8	O	Serial Digital Data Output 8	TVDD3
	ESDIO20	I/O	SPI Master Interface 2 Data 0 In/Output (Input Pulled-down) (Connected device side is DIO)	
	ESDIO10	I/O	SPI Master Interface 1 Data 0 In/Output (Input Pulled-down) (Connected device side is DIO)	
	TOUT	O	Tuning Interface Output	
92	SDIN8	I	Serial Digital Data Input 10 (Input Pulled-down)	TVDD3
	ESDIO21	I/O	SPI Master Interface 2 Data 1 In/Output (Input Pulled-down) (Connected device side is DIO)	
	ESDIO11	I/O	SPI Master Interface 1 Data 1 In/Output (Input Pulled-down) (Connected device side is DIO)	
93	LRCKG	I/O	Frame Sync / Left-Right Clock G (Input Pulled-down)	TVDD3
	UTX	O	UART Output	
94	BICKG	I/O	Serial Bit Clock G (Input Pulled-down)	TVDD3
	URX	I	UART Input (Input Pulled-down)	
95	SIO23	I/O	SPI Slave Interface 2 Data In/Output 3 (Input Pulled-down) Connect a Pull-Down resistor (22kΩ recommended).	TVDD3
96	SIO22	I/O	SPI Slave Interface 2 Data In/Output 2 (Input Pulled-down) Connect a Pull-Down resistor (22kΩ recommended).	TVDD3
97	SDA2	I/O	SDA Pin for I^2C Interface 2 Connect a Pull-Down resistor (2.2kΩ recommended).	TVDD3
	SIO21	I/O	SPI Slave Interface 2 Data In/Output 1 (Input Pulled-down) Connect a Pull-Down resistor (22kΩ recommended).	
98	SIO20	I/O	SPI Slave Interface 2 Data In/Output 0 (Input Pulled-down) Connect a Pull-Down resistor (22kΩ recommended).	TVDD3
99	SCL2	I	Serial Data Clock Input for I^2C Interface 2	TVDD3
	SCLK2	I	Serial Data Clock Input for SPI interface 2	
100	CSN2	I	I^2C Mode: Bus Address for I^2C Interface 2 This pin must be pulled up or pulled down.	TVDD3
		I	SPI Mode: Chip Select for SPI Interface 2 Set this pin to “H” in power-down state or when not interfacing to MCU.	
-	Exposed Pad	-	The exposed pad on the bottom surface of the package must be connected to the ground.	-

Notes:
*1. The exposed pad on the bottom surface of the package must be connected to the ground.
*2. All digital input pins must not be allowed to float. If analog inputs are not used, leave them open.
*3. The description of “Internal Pull-down” above indicates the pin status just after power-down is released. (PDN pin = “H”)

5.3. Handling of Unused Pins

Unused I/O pins must be connected appropriately.

Table 1. Handling of Unused Pin

Classification	Pin Name	Setting
Analog	XTO, TEST	Open
Digital	SDOUT5/ESDIO23/ESDIO13/GPIO14, DIRINT/GPIO15, SDOUT4/ESDIO22/ESDIO12/TOUT, SDOUT3/ESDIO20/ESDIO10, SDOUT7/GPIO02/ECSO1/ECSO2, SDOUT1, CLKO/ECSO1/ECSO2/TOUT, ESCLK2/BICKB, ECSO2/LRCKB, ESCLK1/BICKF, ECSO1/LRCKF, STO, SBST/ECSO1/ECSO2, SDOUT6/DIT/ESDIO23/ESDIO13, SDOUT11/CLKO, SDOUT8/ESDIO20/ESDIO10/TOUT	Open
	SDIN5/DMDAT2, SDIN4/DMDAT1, BICKD/DMCLK2, LRCKD/DMCLK1, SDIN3/ESDIO21/ESDIO11, LRCKC/ECSO2/ECSO1, BICKC/ESCLK2/ESCLK1, GPIO00/CLKO, SDIN7/GPIO01, GPIO09/TRST, GPIO13/TDI, GPIO11/TDO, GPIO10/TCK, GPIO12//TMS, GPIO03/SDIN10, SDIN1, BICKA, LRCKA, GPIO04/SDOUT10, ESDIO21/SDIN2, ESDIO20/SDOUT2, ESDIO13/ESDIO23, ESDIO12/ESDIO22, ESDIO11/SDIN9, ESDIO10/SDOUT9, GPIO05, SBMAT, SELE, SDIN6/DIR1/ESDIO22/ESDIO12, LRCKH, BICKH, SDIN11, GPIO08/ECSO1/ECSO2, LRCKE/ECSO2/ECSO1, BICKE/ESCLK2/ESCLK1, SDIN8/ESDIO21/ESDIO11, LRCKG/UTX, BICKG/URX	Connect to VSS or Open
	CSN1, SCL1/SCLK1, SIO10, SDA1/SIO11, SIO12, SIO13, MSDA/GPIO06, MSCL/GPIO07, SIO23, SIO22, SDA2/SIO21, SIO20, SCL2/SCLK2, CSN2, DIR0, TIN	Connect to VSS

5.4. Relationship of Input/Output Pins and Digital Power Supplies

Table 2. Relationship between Input / Output Pins and Digital Power Supplies

Power Supply	Input / Output Pin
TVDD1 (1.7-3.3V)	PDN, CSN1, SCL1/SCLK1, SIO10, SDA1/SIO11, SIO12, SIO13, SDOUT1, SDIN1, CLKO/ECSO1/ECSO2/TOUT, BICKA, LRCKA, GPIO04/SDOUT10, ESDIO21/SDIN2, ESDIO20/SDOUT2, ESCLK2/BICKB, ECSO2/LRCKB, ESDIO13/ESDIO23, ESDIO12/ESDIO22, ESDIO11/SDIN9, ESDIO10/SDOUT9, ESCLK1/BICKF, ECSO1/LRCKF, GPIO05, STO, SBST/ECSO1/ECSO2, SBMAT, SELE
TVDD2 (1.7-3.3V)	SDOUT5/ESDIO23/ESDIO13/GPIO14, DIRINT/GPIO15, SDIN5/DMDAT2, SDIN4/DMDAT1, BICKD/DMCLK2, LRCKD/DMCLK1, SDOUT4/ESDIO22/ESDIO12/TOUT, SDOUT3/ESDIO20/ESDIO10, SDIN3/ESDIO21/ESDIO11, LRCKC/ECSO2/ECSO1, BICKC/ESCLK2/ESCLK1, GPIO00/CLKO, SDIN7/GPIO01, SDOUT7/GPIO02/ECSO1/ECSO2, GPIO09/TRST, GPIO13/TDI, GPIO11/TDO, GPIO10/TCK, GPIO12/TMS, GPIO03/SDIN10
TVDD3 (1.7-3.3V)	SDIN6/DIR1/ESDIO22/ESDIO12, LRCKH, BICKH, SDOUT6/DIT/ESDIO23/ESDIO13, SDOUT11/CLKO, SDIN11, MSDA/GPIO06, MSCL/GPIO07, GPIO08/ECSO1/ECSO2, LRCKE/ECSO2/ECSO1, BICKE/ESCLK2/ESCLK1, SDOUT8/ESDIO20/ESDIO10/TOUT, SDIN8/ESDIO21/ESDIO11, LRCKG/UTX, BICKG/URX, SIO23, SIO22, SDA2/SIO21, SIO20, SCL2/SCLK2, CSN2, TIN
TVDD3 (3.3V)	DIR0
AVDD (3.3V)	XTO, XTI, TEST

5.5. Power-down and Power-down Release Status of Output Pins

Table 3. Power-down Pin Status (just after Power-up)

No.	Pin Name	I/O	Power-down Status (PDN pin = "L")	Power Down Release (PDN pin = "H") I/O pin: Input or Pull Down	Power Down Release (PDN pin = "H") I/O pin: Output
1	SDOUT5	O	Pull Down: Typ.77kΩ	-	Output
	ESDIO23	I/O		Input (Pull Down: Typ.77kΩ)	
	ESDIO13	I/O			
	GPIO14	I/O			
2	DIRINT	O	Pull Down: Typ.77kΩ	-	Output
	GPIO15	I/O		Input (Pull Down: Typ.77kΩ)	
3	SDIN5	I	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	-
	DMDAT2	I			
4	SDIN4	I	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	-
	DMDAT1	I			
5	BICKD	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	DMCLK2	O		-	
6	LRCKD	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	DMCLK1	O		-	
7	SDOUT4	O	Pull Down: Typ.77kΩ	-	Output
	ESDIO22	I/O		Input (Pull Down: Typ.77kΩ)	
	ESDIO12	I/O			
	TOUT	O		-	
8	SDOUT3	O	Pull Down: Typ.77kΩ	-	Output
	ESDIO20	I/O		Input (Pull Down: Typ.77kΩ)	
	ESDIO10	I/O			
9	SDIN3	I	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	-
	ESDIO21	I/O			Output
	ESDIO11	I/O			
16	LRCKC	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	ECSO2	O		-	
	ECSO1	O		-	
17	BICKC	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	ESCLK2	O		-	
	ESCLK1	O		-	
18	GPIO00	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	CLKO	O		-	
19	SDIN7	I	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	-
	GPIO01	I/O			Output
20	SDOUT7	O	Pull Down: Typ.77kΩ	-	Output
	GPIO02	I/O		Input (Pull Down: Typ.77kΩ)	
	ECSO1	O		-	
	ECSO2	O		-	
21	GPIO09	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	TRST	I			-

No.	Pin Name	I/O	Power-down Status (PDN pin = “L”)	Power Down Release (PDN pin = “H”) I/O pin: Input or Pull Down	Power Down Release (PDN pin = “H”) I/O pin: Output
22	GPIO13	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	TDI	I			-
23	GPIO11	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	TDO	O		-	
24	GPIO10	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	TCK	I			-
25	GPIO12	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	TMS	I			-
26	GPIO03	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	SDIN10	I			-
27	PDN	I	Input (“L”)	Input (“H”)	-
28	CSN1	I	Input (“Hi-Z”)	Input (“Hi-Z”)	-
29	SCL1	I	Input (“Hi-Z”)	Input (“Hi-Z”)	-
	SCLK1	I			
30	SIO10	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
31	SDA1	I/O	Input (“Hi-Z”)	Input (“Hi-Z”)	Output
	SIO11	I/O		Input (Pull Down: Typ.77kΩ)	
32	SIO12	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
33	SIO13	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
40	SDOUT1	O	“L”	Pull Down: Typ.77kΩ (DOSEL1 bit = “1”)	Output (DOSEL1 bit = “0”)
41	SDIN1	I	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	-
42	CLKO	O	“L”	-	Output
	ECSO1	O			
	ECSO2	O			
	TOUT	O			
43	BICKA	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
44	LRCKA	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
45	GPIO04	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	SDOUT10	O		-	
46	ESDIO21	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	SDIN2	I			-
47	ESDIO20	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	SDOUT2	O		Pull Down: Typ.77kΩ (MSTN2SO bit = “1” and DOSEL2 bit = “0”)	Output (MSTN2SO bit = “1” and DOSEL2 bit = “1”)
48	ESCLK2	O	“L”	-	Output
	BICKB	I/O		Input (Pull Down: Typ.77kΩ)	
49	ECSO2	O	“H”	-	Output
	LRCKB	I/O		Input (Pull Down: Typ.77kΩ)	
50	ESDIO13	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	ESDIO23	I/O			
51	ESDIO12	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	ESDIO22	I/O			
52	ESDIO11	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	SDIN9	I			-
53	ESDIO10	I/O	Input (Pull Down: Typ.77kΩ)	Input (Pull Down: Typ.77kΩ)	Output
	SDOUT9	O		-	
54	ESCLK	O	“L”	-	Output
	BICKF	I/O		Input (Pull Down: Typ.77kΩ)	

No.	Pin Name	I/O	Power-down Status (PDN pin = “L”)	Power Down Release (PDN pin = “H”) I/O pin: Input or Pull Down	Power Down Release (PDN pin = “H”) I/O pin: Output
55	ECSO1	O	“H”	-	Output
	LRCKF	I/O		Input (Pull Down : Typ.77kΩ)	
56	GPIO05	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
57	STO	O	“H”	-	Output
58	SBST	O	“L”	-	Output
	ECSO1	O			
	ECSO2	O			
59	SBMAT	I	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	-
60	SELE	I	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	-
68	XTI	I	Input (“Hi-Z”)	Input (“Hi-Z”)	-
69	XTO	O	SELE= “L”: “H” Output SELE= “H”: Inverted Output of XTI	-	Inverted Output of XTI
70	TEST	I/O	“Hi-Z”	“Hi-Z”	“Hi-Z”
71	DIR0	I	Input (“Hi-Z”)	Input (“Hi-Z”)	-
72	TIN	I	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	-
73	SDIN6	I	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	-
	DIR1	I			
	ESDIO22	I/O			Output
	ESDIO12	I/O			
74	LRCKH	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
75	BICKH	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
76	SDOUT6	O	Pull Down : Typ.77kΩ	-	Output
	DIT	O			
	ESDIO23	I/O		Input (Pull Down : Typ.77kΩ)	
	ESDIO13	I/O			
77	SDOUT11	O	“L”	-	Output
	CLKO	O			
78	SDIN11	I	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	-
79	MSDA	I/O	Input (“Hi-Z”)	Input (“Hi-Z”)	Output
	GPIO06	I/O		Input (Pull Down : Typ.77kΩ)	
80	MSCL	I/O	Input (“Hi-Z”)	Input (“Hi-Z”)	Output
	GPIO07	I/O		Input (Pull Down : Typ.77kΩ)	
81	GPIO08	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
	ECSO1	O		-	
	ECSO2	O		-	
89	LRCKE	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
	ECSO2	O		-	
	ECSO1	O		-	
90	BICKE	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
	ESCLK2	O		-	
	ESCLK1	O		-	
91	SDOUT8	O	Input (Pull Down : Typ.77kΩ)	-	Output
	ESDIO20	I/O		Input (Pull Down : Typ.77kΩ)	
	ESDIO10	I/O			
	TOUT	O			
92	SDIN8	I	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	-
	ESDIO21	I/O			Output
	ESDIO11	I/O			
93	LRCKG	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
	UTX	O		-	
94	BICKG	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
	URX	I			-
95	SIO23	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output

No.	Pin Name	I/O	Power-down Status (PDN pin = “L”)	Power Down Release (PDN pin = “H”) I/O pin: Input or Pull Down	Power Down Release (PDN pin = “H”) I/O pin: Output
96	SIO22	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
97	SDA2	I/O	Input (“Hi-Z”)	Input (“Hi-Z”)	Output
	SIO21	I/O		Input (Pull Down : Typ.77kΩ)	
98	SIO20	I/O	Input (Pull Down : Typ.77kΩ)	Input (Pull Down : Typ.77kΩ)	Output
99	SCL2	I	Input (“Hi-Z”)	Input (“Hi-Z”)	-
	SCLK2	I			
100	CSN2	I	Input (“Hi-Z”)	Input (“Hi-Z”)	-

Definition of terms in the tables

Pull-down typ.77KΩ:	PAD is in pull-down state. Input not allowed
Input (pull-down typ. 77KΩ):	PAD is pulled down. Input possible
Input (Hi-Z):	PAD is in Hi-Z status. Input possible
Output:	PAD is in output status ("L"/"H" output is possible)
"L":	PAD is "L" output state
"H":	PAD is "H" output state
“Hi-Z”:	PAD is in Hi-Z status.

6. Absolute Maximum Ratings

(VSS=0V:*4)

Parameter	Symbol	Min.	Max.	Unit
Power Supply				
Analog	AVDD	-0.3	3.9	V
Digital1(Core:LVDD)	VDDC	-0.3	1.1	V
Digital2(I/F:TVDD1)	TVDD1	-0.3	3.9	V
Digital3(I/F:TVDD2)	TVDD2	-0.3	3.9	V
Digital4(I/F:TVDD3)	TVDD3	-0.3	3.9	V
Difference (VSS) (*4)	ΔGND	-0.3	0.3	V
Input Current (Expect: Power Supply Pins)	IIN	-	±10	mA
Analog Input Voltage (*5)	VINA	-0.3	(AVDD+0.3) or 3.9	V
Digital Input Voltage1 (*6)	VIND1	-0.3	3.9	V
Digital Input Voltage2 (*7)	VIND2	-0.3	3.9	V
Digital Input Voltage3 (*8)	VIND3	-0.3	3.9	V
Operation Temperature	Ta	-40	105	°C
Storage Temperature	Tstg	-65	150	°C

Notes:
*4. All voltages are with respect to ground. VSS must be connected to the same ground.
*5. The maximum analog input voltage is smaller value between (AVDD+0.3) V and 3.9V.
*6. Digital Input Voltage1 is for pins of TVDD1 power supply domain.
*7. Digital Input Voltage2 is for pins of TVDD2 power supply domain.
*8. Digital Input Voltage3 is for pins of TVDD3 power supply domain.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS=0V:*4, PDN pin = “H”)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply					
Analog	AVDD	3.13	3.3	3.47	V
Digital(Core)	VDDC	0.85	0.9	0.95	V
Digital(I/F)	TVDD1	1.7	3.3	3.47	V
Digital(I/F)	TVDD2	1.7	3.3	3.47	V
Digital(I/F)	TVDD3	1.7	3.3	3.47	V

Notes:
*9. VDDC must be powered up after or at the same time as other power supplies. VDDC must be powered down before or at the same time as AVDD, TVDD1, TVDD2, TVDD3.
*10. All power supplies must be turned on.
*11. PDN pin should be held “L” when power is supplied. PDN pin is allowed to be “H” after all power supplies are applied and settled.
*12. The power-up sequence must be re-executed from the beginning when changing the voltage supply level of TVDD1, TVDD2 and TVDD3 (e.g., 1.8 V → 3.3 V). TVDD3 must be 3.3 V when using the DIR.
*13. When using the I^2C interface, the power of this product can be turned off while peripheral devices are powered on.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

8.1. SRC1/2/3/4/5/6/7/8

(Ta= 25°C; VDDC=0.9V, AVDD= TVDD1= TVDD2=TVDD3= 3.3V; VSS= 0V; Signal Frequency= 1kHz; 32-bit Data; Measurement Frequency = 20Hz - FSO/2)

	Parameter		Symbol	Min.	Typ.	Max.	Unit
SRC	Resolution					32	bit
	Input Sample Rate		FSI	8		192	kHz
	Output Sample Rate		FSO	8		192	kHz
	THD+N (Input=1kHz, 0dBFS)						
	Audio Mode (SRCFAUDx bit = "1", SRCFECx bit = "0")	FSO/FSI=192kHz/48kHz		-	-132	-	dB
		FSO/FSI=44.1kHz/48kHz		-	-131	-	dB
		FSO/FSI=48kHz/88.2kHz		-	-131	-	dB
		FSO/FSI=48kHz/96kHz		-	-185	-	dB
		FSO/FSI=44.1kHz/96kHz		-	-123	-	dB
		FSO/FSI=48kHz/192kHz		-	-185	-	dB
		FSO/FSI=8kHz/48kHz		-	-185	-	dB
	Voice Mode (SRCFAUDx bit = "0", SRCFECx bit = "0")	FSO/FSI=24kHz/32kHz		-	-97	-	dB
		FSO/FSI=16kHz/24kHz		-	-100	-	dB
		FSO/FSI=24kHz/44.1kHz			-80		dB
		FSO/FSI=16kHz/44.1kHz			-71		dB
		FSO/FSI=8kHz/32kHz		-	-177	-	dB
	Dynamic Range (Input=1kHz, -60dBFS)						
	Audio Mode (SRCFAUDx bit = "1", SRCFECx bit = "0")	FSO/FSI=192kHz/48kHz		-	180	-	dB
		FSO/FSI=44.1kHz/48kHz		-	184	-	dB
		FSO/FSI=48kHz/88.2kHz		-	183	-	dB
		FSO/FSI=48kHz/96kHz		-	185	-	dB
		FSO/FSI=44.1kHz/96kHz		-	182	-	dB
		FSO/FSI=48kHz/192kHz		-	185	-	dB
		FSO/FSI=8kHz/48kHz		-	185	-	dB
	Voice Mode (SRCFAUDx bit = "0", SRCFECx bit = "0")	FSO/FSI=24kHz/32kHz		-	157	-	dB
		FSO/FSI=16kHz/24kHz		-	160	-	dB
		FSO/FSI=24kHz/44.1kHz			140		dB
		FSO/FSI=16kHz/44.1kHz			131		dB
		FSO/FSI=8kHz/32kHz		-	179	-	dB
	Dynamic Range (Input=1kHz, -60dBFS,A-weighted)						
	FSO/FSI=44.1kHz/48kHz			-	186	-	dB
	Ratio between Input and Output Sample Rate		FSO/FSI	0.167		6	-

8.2. SRC9/10/11/12

(Ta= 25°C; VDDC=0.9V, AVDD= TVDD1= TVDD2=TVDD3= 3.3V; VSS= 0V; Signal Frequency = 1kHz; 24-bit Data; Measurement Frequency =20Hz - FSO/2)

	Parameter		Symbol	Min.	Typ.	Max.	Unit
SRC	Resolution					24	bit
	Input Sample Rate		FSI	8		192	kHz
	Output Sample Rate		FSO	8		192	kHz
	THD+N (Input=1kHz, 0dBFS)						
	Voice Mode (SRCFAUDx bit = "0", SRCFECx bit = "0")	FSO/FSI = 16kHz / 8kHz		-	-125	-	dB
		FSO/FSI = 44.1kHz / 48kHz		-	-125	-	dB
		FSO/FSI = 24kHz / 32kHz		-	-95	-	dB
		FSO/FSI = 16kHz / 24kHz		-	-98	-	dB
		FSO/FSI = 24kHz / 44.1kHz		-	-78	-	dB
		FSO/FSI = 16kHz / 44.1kHz		-	-69	-	dB
		FSO/FSI = 8kHz / 32kHz		-	-130	-	dB
		FSO/FSI = 8kHz / 48kHz		-	-130	-	dB
	Audio Mode (SRCFAUDx bit = "1", SRCFECx bit = "0")	FSO/FSI = 24kHz / 44.1kHz		-	-120	-	dB
		FSO/FSI = 24kHz / 48kHz		-	-133	-	dB
		FSO/FSI = 16kHz / 44.1kHz		-	-98	-	dB
	Dynamic Range (Input=1kHz, -60dBFS)						
	Voice Mode (SRCFAUDx bit = "0", SRCFECx bit = "0")	FSO/FSI = 16kHz / 8kHz		-	135	-	dB
		FSO/FSI = 44.1kHz / 48kHz		-	136	-	dB
		FSO/FSI = 24kHz / 32kHz		-	134	-	dB
		FSO/FSI = 16kHz / 24kHz		-	117	-	dB
		FSO/FSI = 24kHz / 44.1kHz		-	132	-	dB
		FSO/FSI = 16kHz/44.1kHz		-	128	-	dB
		FSO/FSI = 8kHz /32kHz		-	130	-	dB
		FSO/FSI = 8kHz /48kHz		-	130	-	dB
	Audio Mode (SRCFAUDx bit = "1", SRCFECx bit = "0")	FSO/FSI = 24kHz / 44.1kHz		-	136	-	dB
		FSO/FSI = 24kHz / 48kHz		-	135	-	dB
		FSO/FSI = 16kHz / 44.1kHz		-	135	-	dB
	Dynamic Range (Input=1kHz, -60dBFS,A-weighted)						
	FSO/FSI=44.1kHz/48kHz			-	137	-	dB
	Ratio between Input and Output Sample Rate		FSO/FSI	0.167		6	-

8.3. SPDIF Characteristics

(Ta= -40 - 105ºC, TVDD3= 3.13 - 3.47V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DIR0 input voltage level	VIH	100			mV
(Internally biased at TVDD3 /2)	VIL			-100	mV
Input Hysteresis	VTY		50		mV
Input Reference Voltage	INVREF		TVDD3 /2		V
Input resistance	Zin		10		kΩ
Input Sampling Frequency	fs	32		192	kHz

8.4. PLL

(Ta=25°C; VDDC=0.9V, AVDD=TVDD1=TVDD2=TVDD3= 3.3V; VSS=0V)

Parameter		Min.	Typ.	Max.	Unit
Reference Clock Input Frequency	(48kHz)	1.536		3.072	MHz
	(44.1kHz)	1.411		2.822	MHz
VCOCLK Frequency	(48kHz)		491.52		MHz
	(44.1kHz)		451.584		MHz

8.5. Power Consumption

(Ta= 25ºC; AVDD=3.13 - 3.47V (Typ.=3.3V, Max.=3.47V);
VDDC=0.85 - 0.95V(Typ.=0.9V, Max.=0.95V); TVDD1=1.7 - 3.47V(Typ.=3.3V, Max.=3.47V);
TVDD2=1.7 - 3.47V(Typ.=3.3V, Max.=3.47V); TVDD3=1.7 - 3.47V(Typ.=3.3V, Max.=3.47V); VSS= 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-up (*14)	AVDD		15	27	mA
	VDDC		180	590	mA
	TVDD1		8	14	mA
	TVDD2		8	14	mA
	TVDD3		8	14	mA
Power-down (PDN pin = “L”)	AVDD		0.01		mA
	VDDC		6	450	mA
	TVDD1		0.01		mA
	TVDD2		0.01		mA
	TVDD3		0.01		mA

Note:
*14. The current changes depending on the system frequency and contents of DSP program.
Max value condition is AVDD=TVDD1=TVDD2=TVDD3=3.47V, VDDC=0.95V, CL=6pF.

9. Digital Filter Characteristics

9.1. DMIC

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V; AVDD=3.13 - 3.47V; TVDD1/2/3=1.7 - 3.47V; VSS= 0V) (*15)

1.1. VOICE Filter (SDAD[1:0] bits = “00”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Voice Filter						
Passband	-0.5dB - 0.5dB	PB	0	―	6.3	kHz
	-3.0dB	PB	―	6.9	―	kHz
Stopband (*16)		SB	8	―	―	kHz
Passband Ripple (*17)		PR	-0.47	―	0	dB
Stopband Attenuation (*16)		SA	59.5		―	dB
Group Delay Distortion: 0Hz - 8kHz		ΔGD	―	0	―	1/fs
Group Delay		GD	―	14.1	―	1/fs

Notes:
*15. The passband and stopband frequencies scale with “fs” (system sampling rate).
*16. The passband is from DC to 6.3 kHz when fs = 16 kHz.
*17. The stopband is from 8 kHz to 1.016 MHz when fs = 16 kHz.

1.2. SHARP ROLL OFF Filter (SDAD[1:0] bits = “01”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Sharp Roll Off Filter						
Passband	+0.14dB/-0.12dB	PB	0	―	20.7	kHz
	-0.87dB	PB	―	21.6	―	kHz
	-3.0dB	PB	―	22.8	―	kHz
	-6.0dB	PB	―	23.8	―	kHz
	-7.0dB	PB	―	24	―	kHz
Stopband (*19)		SB	28.4	―	―	kHz
Passband Ripple (*18)		PR	―	―	±0.14	dB
Stopband Attenuation (*19)		SA	65	―	-	dB
Group Delay Distortion: 0Hz - 20kHz		ΔGD	―	0	―	μs
Group Delay		GD	―	12.5	―	1/fs

Notes:
*18. The passband is from DC to 20.7 kHz when fs = 48 kHz.
*19. The stopband is from 28.4 kHz to 3.0436 MHz when fs = 48 kHz.

9.2. SRC1/2/3/4/5/6/7/8

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V; AVDD=3.13 - 3.47V; TVDD1/2/3=1.7 - 3.47V; VSS= 0V)

2.1. Audio Mode (SRCFAUDx bit = “1”, SRCFECx bit = “0” (x = 1-8))

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980≦FSO/FSI≦6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900≦FSO/FSI＜0.990	PB	0		0.4167FSI	kHz
	-0.01dB	0.533≦FSO/FSI＜0.909	PB	0		0.2182FSI	kHz
	-0.01dB	0.490≦FSO/FSI＜0.539	PB	0		0.2177FSI	kHz
	-0.01dB	0.450≦FSO/FSI＜0.495	PB	0		0.1948FSI	kHz
	-0.01dB	0.225≦FSO/FSI＜0.455	PB	0		0.1312FSI	kHz
	-0.50dB	0.167≦FSO/FSI＜0.227	PB	0		0.0658FSI	kHz
Stopband		0.980≦FSO/FSI≦6.000	SB	0.5417FSI			kHz
		0.900≦FSO/FSI＜0.990	SB	0.5021FSI			kHz
		0.533≦FSO/FSI＜0.909	SB	0.2974FSI			kHz
		0.490≦FSO/FSI＜0.539	SB	0.2812FSI			kHz
		0.450≦FSO/FSI＜0.495	SB	0.2604FSI			kHz
		0.225≦FSO/FSI＜0.455	SB	0.1802FSI			kHz
		0.167≦FSO/FSI＜0.227	SB	0.0970FSI			kHz
Passband Ripple		0.225≦FSO/FSI≦6.000	PR			±0.01	dB
		0.167≦FSO/FSI＜0.227	PR			±0.50	dB
Stopband Attenuation		0.225≦FSO/FSI≦6.000	SA	95.2			dB
		0.167≦FSO/FSI＜0.227	SA	85.0			dB
Group Delay (Ts=1/fs) (*20)			GD		67 (55/FSI+12/FSO)		Ts

Note:

*20. This parameter is measured only for the SRC block. This time is measured from a rising edge of LRCK after a signal input to the SRC until a rising edge of LRCK before data output when there is no phase difference between input and output.

2.2. Voice Mode (SRCFAUDx bit = “0”, SRCFECx bit = “0 (x = 1-8))

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980≦FSO/FSI≦6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900≦FSO/FSI＜0.990	PB	0		0.4167FSI	kHz
	-0.50dB	0.711≦FSO/FSI＜0.910	PB	0		0.3420FSI	kHz
	-0.50dB	0.653≦FSO/FSI＜0.718	PB	0		0.3007FSI	kHz
	-0.50dB	0.450≦FSO/FSI＜0.660	PB	0		0.2230FSI	kHz
	-0.50dB	0.327≦FSO/FSI＜0.455	PB	0		0.1417FSI	kHz
	-0.50dB	0.225≦FSO/FSI＜0.330	PB	0		0.1018FSI	kHz
	-0.50dB	0.167≦FSO/FSI＜0.227	PB	0		0.0658FSI	kHz
Stopband		0.980≦FSO/FSI≦6.000	SB	0.5417FSI			kHz
		0.900≦FSO/FSI＜0.990	SB	0.5021FSI			kHz
		0.711≦FSO/FSI＜0.910	SB	0.3735FSI			kHz
		0.653≦FSO/FSI＜0.718	SB	0.3320FSI			kHz
		0.450≦FSO/FSI＜0.660	SB	0.2490FSI			kHz
		0.327≦FSO/FSI＜0.422	SB	0.1660FSI			kHz
		0.225≦FSO/FSI＜0.330	SB	0.1248FSI			kHz
		0.167≦FSO/FSI＜0.227	SB	0.0970FSI			kHz
Passband Ripple		0.900≦FSO/FSI≦6.000	PR			±0.01	dB
		0.167≦FSO/FSI＜0.909	PR			±0.50	dB
Stopband Attenuation		0.900≦FSO/FSI≦6.000	SA	95.2			dB
		0.653≦FSO/FSI＜0.909	SA	90.0			dB
		0.450≦FSO/FSI≦0.660	SA	70.0			dB
		0.167≦FSO/FSI＜0.455	SA	60.0			dB
Group Delay (Ts=1/fs) (*20)			GD		67 (55/FSI+12/FSO)		Ts

2.3. Echo Canceller Mode (SRCFECx bit = “1” (x = 1-8))

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.167≦FSO/FSI≦6.000	PB	0		0.4583FSI	kHz
Stopband		0.167≦FSO/FSI≦6.000	SB	0.5417FSI			kHz
Passband		0.167≦FSO/FSI≦6.000	PR			±0.01	dB
Stopband Attenuation		0.167≦FSO/FSI≦6.000	SA	95.2			dB
Group Delay (Ts=1/fs) (*20)			GD		67 (55/FSI+12/FSO)		Ts

9.3. SRC9/10/11/12

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V; AVDD=3.13 - 3.47V; TVDD1/2/3=1.7 - 3.47V; VSS= 0V)

3.1. Audio Mode (SRCFAUDx bit = “1”, SRCFECx bit = “0” (x = 9-12))

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980≦FSO/FSI≦6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900≦FSO/FSI＜0.990	PB	0		0.4167FSI	kHz
	-0.01dB	0.533≦FSO/FSI＜0.909	PB	0		0.2182FSI	kHz
	-0.01dB	0.490≦FSO/FSI＜0.539	PB	0		0.2177FSI	kHz
	-0.01dB	0.450≦FSO/FSI＜0.495	PB	0		0.1948FSI	kHz
	-0.01dB	0.225≦FSO/FSI＜0.455	PB	0		0.1312FSI	kHz
	-0.50dB	0.167≦FSO/FSI＜0.227	PB	0		0.0658FSI	kHz
Stopband		0.980≦FSO/FSI≦6.000	SB	0.5417FSI			kHz
		0.900≦FSO/FSI＜0.990	SB	0.5021FSI			kHz
		0.533≦FSO/FSI＜0.909	SB	0.2974FSI			kHz
		0.490≦FSO/FSI＜0.539	SB	0.2812FSI			kHz
		0.450≦FSO/FSI＜0.495	SB	0.2604FSI			kHz
		0.225≦FSO/FSI＜0.455	SB	0.1802FSI			kHz
		0.167≦FSO/FSI＜0.227	SB	0.0970FSI			kHz
Passband Ripple		0.225≦FSO/FSI≦6.000	PR			±0.01	dB
		0.167≦FSO/FSI＜0.227	PR			±0.50	dB
Stopband Attenuation		0.225≦FSO/FSI≦6.000	SA	95.2			dB
		0.167≦FSO/FSI＜0.227	SA	85.0			dB
Group Delay (Ts=1/fs) (*20)			GD		67 (55/FSI+12/FSO)		Ts

3.2. Voice Mode (SRCFAUDx bit = “0”, SRCFECx bit = “0 (x = 9-12))

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980≦FSO/FSI≦6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900≦FSO/FSI＜0.990	PB	0		0.4167FSI	kHz
	-0.50dB	0.711≦FSO/FSI＜0.910	PB	0		0.3420FSI	kHz
	-0.50dB	0.653≦FSO/FSI＜0.718	PB	0		0.3007FSI	kHz
	-0.50dB	0.450≦FSO/FSI＜0.660	PB	0		0.2230FSI	kHz
	-0.50dB	0.327≦FSO/FSI＜0.455	PB	0		0.1417FSI	kHz
	-0.50dB	0.225≦FSO/FSI＜0.330	PB	0		0.1018FSI	kHz
	-0.50dB	0.167≦FSO/FSI＜0.227	PB	0		0.0658FSI	kHz
Stopband		0.980≦FSO/FSI≦6.000	SB	0.5417FSI			kHz
		0.900≦FSO/FSI＜0.990	SB	0.5021FSI			kHz
		0.711≦FSO/FSI＜0.910	SB	0.3735FSI			kHz
		0.653≦FSO/FSI＜0.718	SB	0.3320FSI			kHz
		0.450≦FSO/FSI＜0.660	SB	0.2490FSI			kHz
		0.327≦FSO/FSI＜0.422	SB	0.1660FSI			kHz
		0.225≦FSO/FSI＜0.330	SB	0.1248FSI			kHz
		0.167≦FSO/FSI＜0.227	SB	0.0970FSI			kHz
Passband Ripple		0.900≦FSO/FSI≦6.000	PR			±0.01	dB
		0.167≦FSO/FSI＜0.909	PR			±0.50	dB
Stopband Attenuation		0.900≦FSO/FSI≦6.000	SA	95.2			dB
		0.653≦FSO/FSI＜0.909	SA	90.0			dB
		0.450≦FSO/FSI≦0.660	SA	70.0			dB
		0.167≦FSO/FSI＜0.455	SA	60.0			dB
Group Delay (Ts=1/fs) (*20)			GD		67 (55/FSI+12/FSO)		Ts

3.3. Echo Canceller Mode (SRCFECx bit = “1” (x = 9-12))

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.167≦FSO/FSI≦6.000	PB	0		0.4583FSI	kHz
Stopband		0.167≦FSO/FSI≦6.000	SB	0.5417FSI			kHz
Passband Ripple		0.167≦FSO/FSI≦6.000	PR			±0.01	dB
Stopband Attenuation		0.167≦FSO/FSI≦6.000	SA	95.2			dB
Group Delay (Ts=1/fs) (*20)			GD		67 (55/FSI+12/FSO)		Ts

10. DC Characteristics

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V; AVDD=3.13 - 3.47V; TVDD1/2/3=1.7 - 3.47V; VSS= 0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage 1 (*21)		VIH1	75%TVDD1			V
Low-Level Input Voltage 1 (*21)		VIL1			25%TVDD1	V
High-Level Input Voltage 2 (*22)		VIH2	75%TVDD2			V
Low-Level Input Voltage 2 (*22)		VIL2			25%TVDD2	V
High-Level Input Voltage 3 (*23)		VIH3	75%TVDD3			V
Low-Level Input Voltage 3 (*23)		VIL3			25%TVDD3	V
High-Level Input Voltage A (*24)		VIHA	75%AVDD			V
Low-Level Input Voltage A (*24)		VILA			25%AVDD	V
SCL1, SDA1 High-Level Input Voltage		VIH4	70%TVDD1			V
SCL1, SDA1 Low-Level Input Voltage		VIL4			30%TVDD1	V
SCL2, SDA2, MSCL High-Level Input Voltage		VIH5	70%TVDD3			V
SCL2, SDA2, MSDA Low-Level Input Voltage		VIL5			30%TVDD3	V
DMDAT1/2 High-Level Input Voltage (*25)		VIH2DM	65%TVDD2			V
DMDAT1/2 Low-Level Input Voltage (*25)		VIL2DM			35%TVDD2	V
High-Level Output Voltage 1 Iout= -100μA (*26)		VOH1	TVDD1-0.3			V
Low-Level Output Voltage 1 Iout=100μA (*26)		VOL1			0.3	V
High-Level Output Voltage 2 Iout= -100μA (*27)		VOH2	TVDD2-0.3			V
Low-Level Output Voltage 2 Iout=100μA (*27)		VOL2			0.3	V
High-Level Output Voltage 3 Iout= -100μA (*28)		VOH3	TVDD3-0.3			V
Low-Level Output Voltage 3 Iout=100μA (*28)		VOL3			0.3	V
SDA1 Low-Level Output Voltage	Fast Mode					
	TVDD1≧2.0V (Iout= 3mA)	VOL4			0.4	V
	TVDD1＜2.0V (Iout= 3mA)	VOL4			20%TVDD1	V
SDA2, MSCL, MSDA Low-Level Output Voltage	Fast Mode					
	TVDD3≧2.0V (Iout= 3mA)	VOL5			0.4	V
	TVDD3＜2.0V (Iout= 3mA)	VOL5			20%TVDD3	V
Input Leak Current (*29)		Iin			±10	μA
Input Leak Current, Pulled down pin (*30)		Iid		45		μA
				77		kΩ
Input Leak Current, XTI pin		Iix			±10	μA

Notes:
*21. Input pins of TVDD1 power supply domain. However, SCL1, SDA1 pins are excluded.
*22. Input pins of TVDD2 power supply domain.
*23. Input pins of TVDD3 power supply domain. However, DIR0, SCL2, SDA2, MSDA, MSCL pins are excluded.
*24. XTI pin
*25. When Digital MIC Setting.
*26. Output pins of TVDD1 power supply domain. However, SDA1 pin is excluded.
*27. Output pins of TVDD2 power supply domain.
*28. Output pins of TVDD3 power supply domain. However, SDA2,MSDA,MSCL pins are excluded.
*29. XTI pin when inputting externally.
*30. pins with a pull-down resistor (Typ. 77 kΩ @3.3V), refer to Power-down and Power-down Release Status of Output Pins.

11. Switching Characterstics

11.1. System Clock

1.1. TVDD1/2/3 =3.13 - 3.47V
(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V; AVDD=3.13 - 3.47V; TVDD1/2/3 =3.13 - 3.47V; VSS= 0V; CL= 6pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XTI Input Timing					
a) X'tal Oscillator(*31)					
Input Frequency	fXTI		12.288 24.576		MHz
b) XTI Clock Input					
Duty Cycle		45	50	55	%
Input Frequency	fXTI	11.2896		49.152	MHz
CLKO Output Timing					
Output Frequency	fCLKO	2.048		49.152	MHz
Duty Cycle	dCLKO		50		%
LRCK/BICK Input Timing (Slave Mode)					
LRCK Input Timing					
Frequency	fs	8		768	kHz
BICK Input Timing					
Frequency (*32)	fBCLK	0.256		49.152	MHz
Duty Cycle	dBCLK	45	50	55	%
LRCK/BICK Output Timing (PLL Master Mode)					
LRCK Output Timing					
Frequency	fs	8		768	kHz
Pulse Width High					
PCM Mode	tLRCKH		1/fBCLK		s
Except PCM Mode	tLRCKH		50		%
BICK Output Timing					
Frequency (*32)	fBCLK	0.256		49.152	MHz
Duty Cycle	dBCLK		50		%

Notes:
*31. Crystal Oscillator must have Typ. ±100ppm frequency accuracy.
*32. Required to meet the following expression: BCLK ≥ 2 x fs x (In/Output Data Length)

1.2. TVDD1/2/3 =1.7 - 3.47V

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V; AVDD=3.13 - 3.47V; TVDD1/2/3 =1.7 - 3.47V; VSS= 0V; CL= 6pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XTI Input Timing					
a) X'tal Oscillator(*31)					
Input Frequency	fXTI		12.288 24.576		MHz
b) XTI Clock Input					
Duty Cycle		45	50	55	%
Input Frequency	fXTI	11.2896		24.576	MHz
CLKO Output Timing					
Output Frequency	fCLKO	2.048		24.576	MHz
Duty Cycle	dCLKO		50		%
LRCK/BICK Input Timing (Slave Mode)					
LRCK Input Timing					
Frequency	fs	8		384	kHz
BICK Input Timing					
Frequency (*32)	fBCLK	0.256		24.576	MHz
Duty Cycle	dBCLK	45	50	55	%
LRCK/BICK Output Timing (PLL Master Mode)					
LRCK Output Timing					
Frequency	fs	8		384	kHz
Pulse Width High					
PCM Mode	tLRCKH		1/fBCLK		s
Except PCM Mode	tLRCKH		50		%
BICK Output Timing					
Frequency (*32)	fBCLK	0.256		24.576	MHz
Duty Cycle	dBCLK		50		%

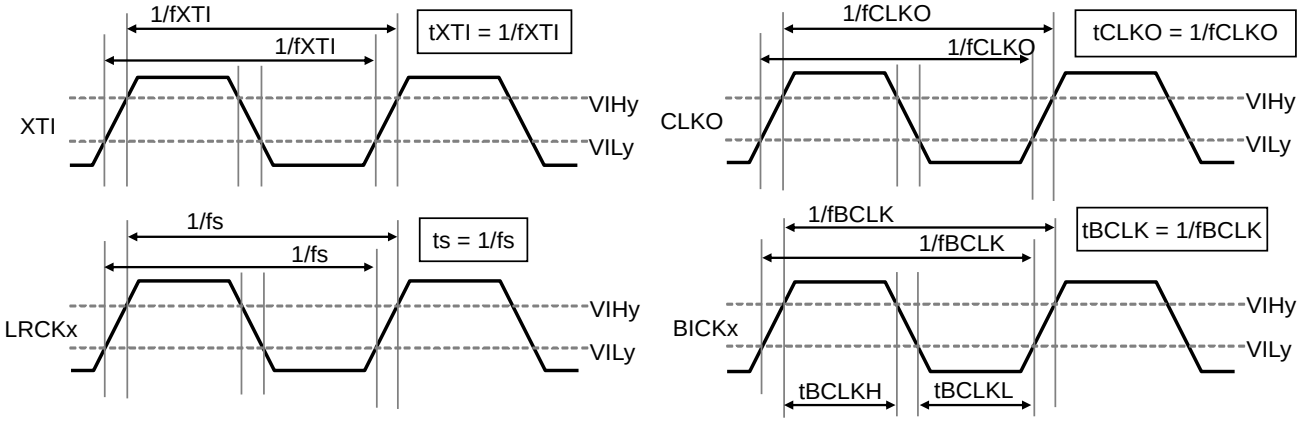


Figure 4. System Clock Timing

11.2. Power-down

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V;AVDD=3.13 - 3.47V; TVDD1/2/3 =1.7 - 3.47V; VSS= 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width (*33)	tRST	600			ns

Note:
*33. The PDN pin must be “L” when power up the AK7017.

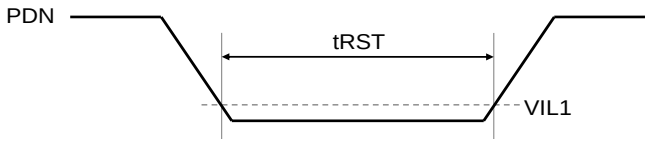


Figure 5. Reset Timing

11.3. Serial Data Interface (SDIN1-11, SDOUT1-11)

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V;AVDD=3.13 - 3.47V; TVDD1/2/3 =1.7 - 3.47V; VSS= 0V; CL= 6pF)

3.1. BICK Frequency=Max.24.576MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK	tBLRD	3.0			ns
Delay Time from LRCK to BICK "↑"	tLRBD	3.0			ns
Serial data input Latch Setup Time for BICK "↑"	tBSIDS	1.0			ns
Serial data input Latch Hold Time for BICK "↑"	tBSIDH	4.0			ns
Delay Time from BICK “↓” to Serial Data Output	tBSOD1			16.0	ns
Delay Time from BICK "↑" to Serial Data Output	tBSOD2	3.0		16.0	ns
Master Mode					
BICK Frequency	fBCLK		32,48,64,128, 256,512,1024		fs
BICK Duty Cycle			50		%
Delay Time from BICK “↓” to LRCKx	tMBL	-3.0		7.0	ns
Serial data input Latch Setup Time for BICK "↑"	tBSIDS	0.5			ns
Serial data input Latch Hold Time for BICK "↑"	tBSIDH	4.0			
Delay Time from BICK “↓” to Serial Data Output	tBSOD1			5.0	ns

3.2. BICK Frequency=Max.49.152MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK	tBLRD	3.0			ns
Delay Time from LRCK to BICK "↑"	tLRBD	3.0			ns
Serial data input Latch Setup Time for BICK "↑"	tBSIDS	1.0			ns
Serial data input Latch Hold Time for BICK "↑"	tBSIDH	3.0			ns
Delay Time from BICK "↓" to Serial Data Output	tBSOD1			12.0	ns
Delay Time from BICK "↑" to Serial Data Output	tBSOD2	3.0		12.0	ns
Master Mode					
BICK Frequency	fBCLK		32,48,64,128, 256,512,1024		fs
BICK Duty Cycle			50		%
Delay Time from BICK "↓" to LRCKx	tMBL	-5.0		7.0	ns
Serial data input Latch Setup Time for BICK "↑"	tBSIDS	1.0			ns
Serial data input Latch Hold Time for BICK "↑"	tBSIDH	3.0			ns
Delay Time from BICK "↓" to Serial Data Output	tBSOD1			5.0	ns

3.3. Slave Mode

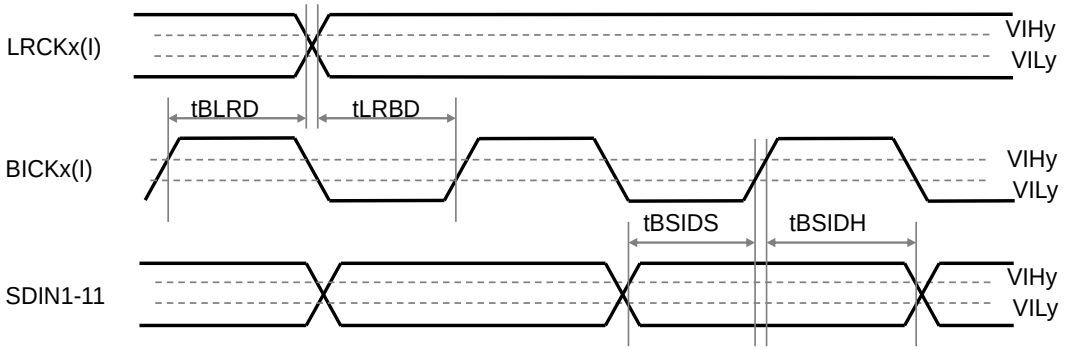


Figure 6. Serial Interface Input Timing in Slave Mode

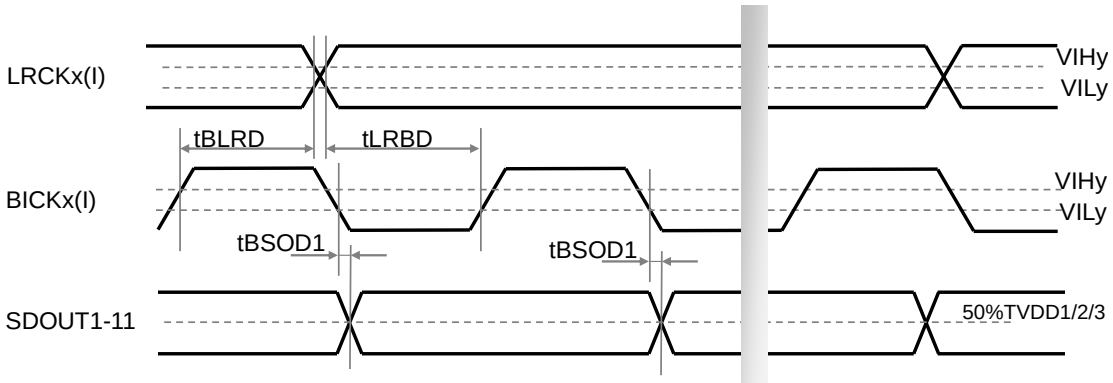


Figure 7. Serial Interface Output Timing in Slave Mode (SDOPHx bit = "0")

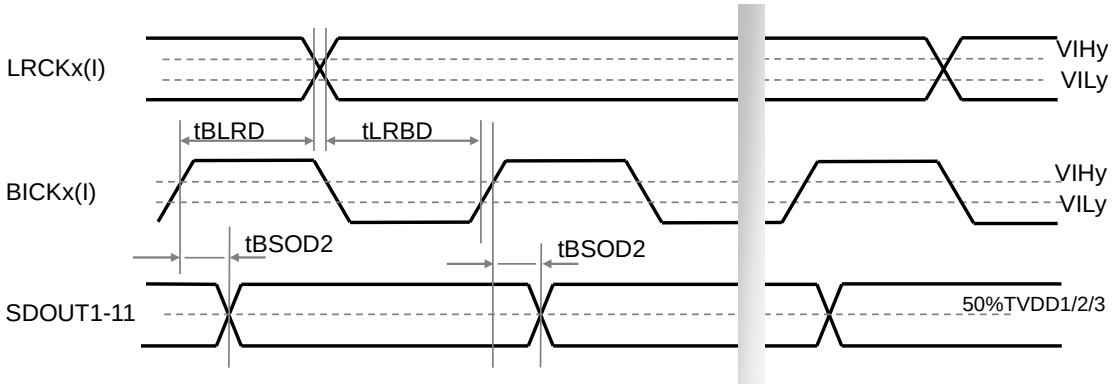


Figure 8. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “1”)

3.4. Master Mode

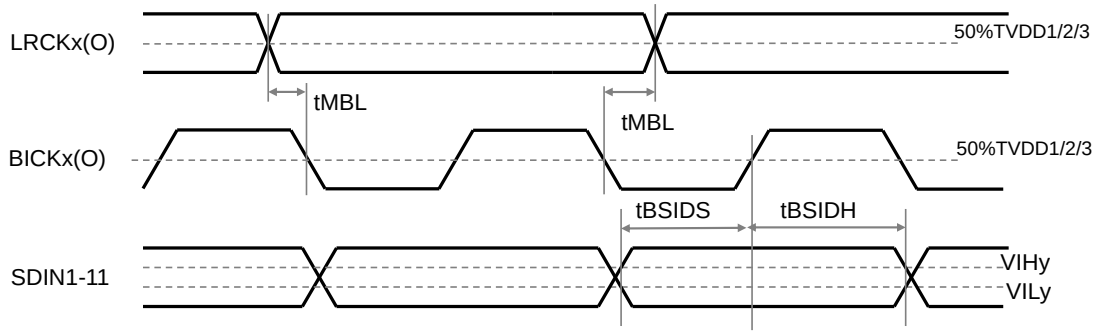


Figure 9. Serial Interface Input Timing in Master Mode

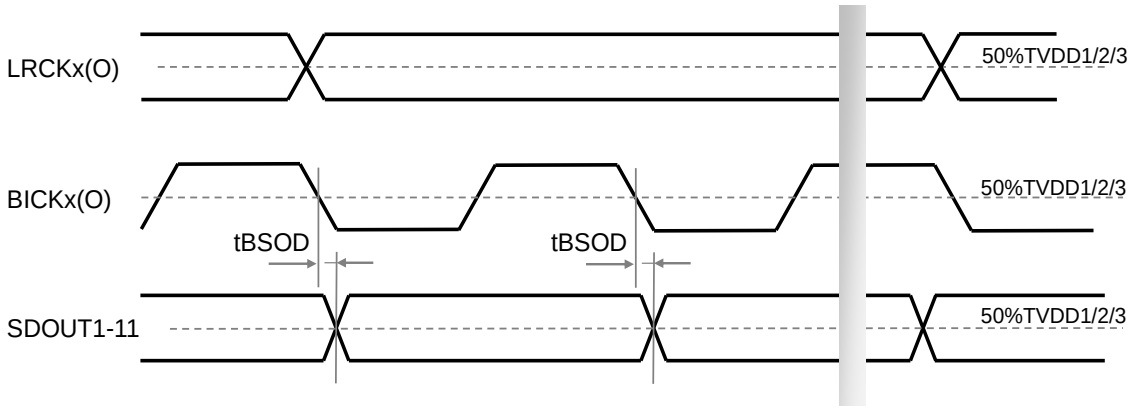


Figure 10. Serial Interface Output Timing in Master Mode

11.4. SPI Interface

4.1. SCLK1/SCLK2 Frequency = Max.13MHz

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V;AVDD=3.13 - 3.47V; TVDD1/2/3 =1.7 - 3.47V; VSS= 0V; CL= 6pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCU IF Interface Signal					
SCLK1/SCLK2 Frequency (*34)	fSCLK			13	MHz
SCLK1/SCLK2 Low-level Width	tSCLKL	35			ns
SCLK1/SCLK2 High-level Width	tSCLKH	35			ns
MCU → this Product					
CSN1/CSN2 High-level Width	tWRQH	250			ns
From CSN1 "↑" to PDN "↑" From CSN2 "↑" to PDN "↑"	tRST	180			ns
From PDN "↑" to CSN1 "↓" From PDN "↑" to CSN2 "↓"	tIRRQ	1			ms
From CSN1 "↓" to SCLK1 "↓" From CSN2 "↓" to SCLK2 "↓"	tWSC	35			ns
From SCLK1 "↑" to CSN1 "↑" From SCLK2 "↑" to CSN2 "↑"	tSCW	35			ns
SIO10-SIO13, SIO20-SIO23 Latch Setup Time	tSIS	3			ns
SIO10-SIO13, SIO20-SIO23 Latch Hold Time	tSIH	3			ns
this Product → MCU					
Delay Time from SCLK1 "↓" to SIO10-SIO13 Output Delay Time from SCLK2 "↓" to SIO20-SIO23 Output	tSOS1			20	ns
SIO10-SIO13 Output Hold Time from SCLK1 "↑" SIO20-SIO23 Output Hold Time from SCLK2 "↑"	tSOH1	20			ns

4.2. SCLK1/SCLK2 Frequency = Max.50MHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
MCU IF Interface Signal						
SCLK1/SCLK2 Frequency (*35)	48kHz base	fSCLK			50	MHz
	44.1kHz base	fSCLK			46	MHz
SCLK1/SCLK2 Low-level Width		tSCLKL	8			ns
SCLK1/SCLK2 High-level Width		tSCLKH	8			ns
MCU → this Product						
CSN1/CSN2 High-level Width		tWRQH	250			ns
From CSN1 "↑" to PDN "↑" From CSN2 "↑" to PDN "↑"		tRST	180			ns
From PDN "↑" to CSN1 "↓" From PDN "↑" to CSN2 "↓"		tIRRQ	1			ms
From CSN1 "↓" to SCLK1 "↓" From CSN2 "↓" to SCLK2 "↓"		tWSC	15			ns
From SCLK1 "↑" to CSN1 "↑" From SCLK2 "↑" to CSN2 "↑"		tSCW	15			ns
SIO10-SIO13, SIO20-SIO23 Latch Setup Time		tSIS	3			ns
SIO10-SIO13, SIO20-SIO23 Latch Hold Time		tSIH	3			ns
this Product → MCU (*38)						
Delay Time from SCLK1 "↓" to SIO10-SIO13 Output Delay Time from SCLK2 "↓" to SIO20-SIO23 Output		tSOS2	3		12	ns
SIO10-SIO13 Output Hold Time from SCLK1 "↑" SIO20-SIO23 Output Hold Time from SCLK2 "↑"		tSOH2	3			ns

Notes:
*34. Do not set the frequency higher than 13MHz when throughing to the SPI master port.
*35. When the PLL frequency is 491.52MHz (reference clock is 48kHz base), the maximum SCLK frequency is 50MHz.
When the PLL frequency is 451.584MHz (reference clock is 44.1kHz base), the maximum SCLK frequency is 46MHz.
*36. Observe the following restrictions when using an SCLK frequency higher than 13MHz.
1) When SPIFAST Mode= “0”: Access to control register, SPI control, and device status register read is enabled except access to DSP1.
2) When SPIFAST Mode= “1”: All accesses of this product are enabled.
*37. After setting CKRESETN bit = “0” → “1”, it takes up to 10ms for PLL to lock. After the PLL locks, shift to SPIFAST Mode. Refer to the user's guide for how to switch to SPIFAST Mode.
*38. When SCLK is faster than 25MHz, set SOPHx Mode="1" (x=1,2) and output data based on SCLK “↑”.

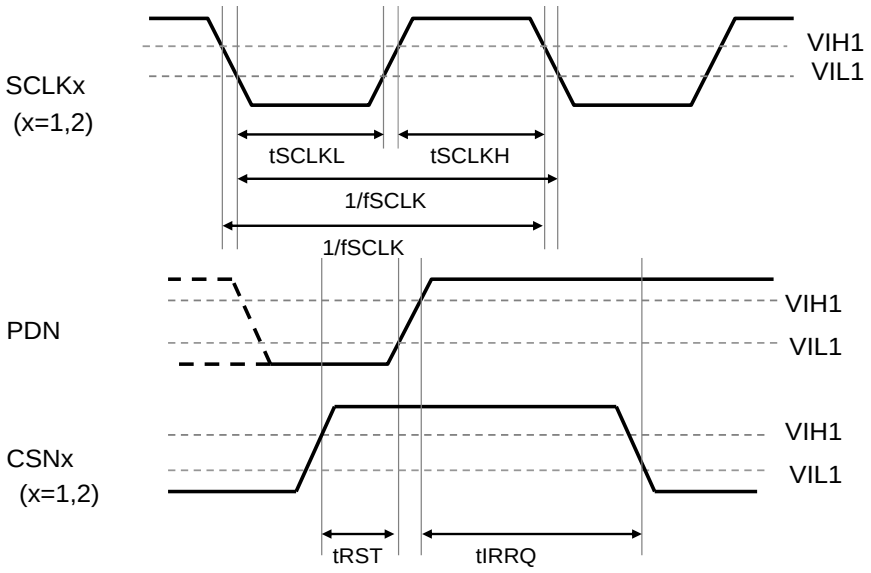


Figure 11. SPI Interface Timing 1

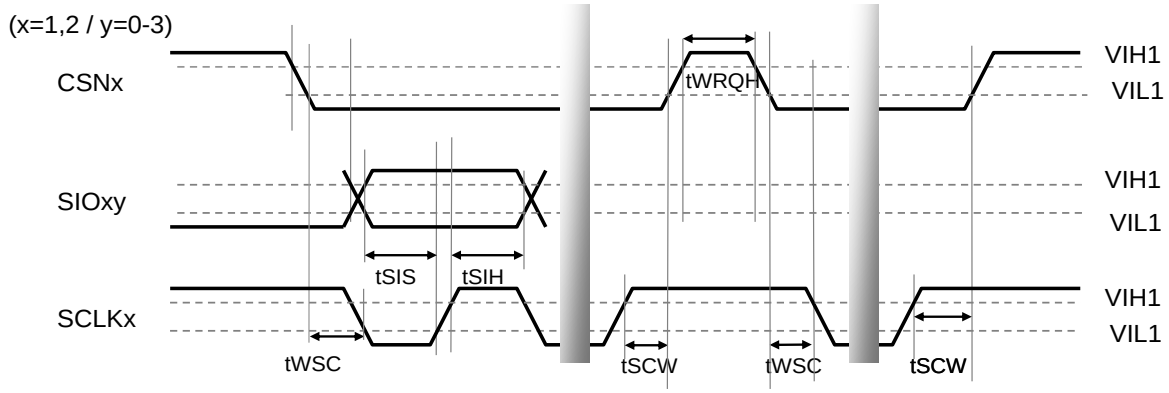


Figure 12. SPI Interface timing 2(MCU → this Product)

(x=1,2 / y=0-3)

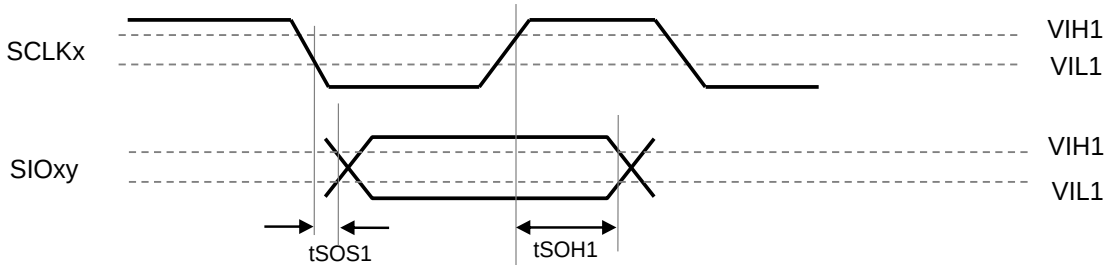


Figure 13. SPI Interface timing 3 (this Product → MCU) SOPHx Mode= “0”

(x=1,2 / y=0-3)

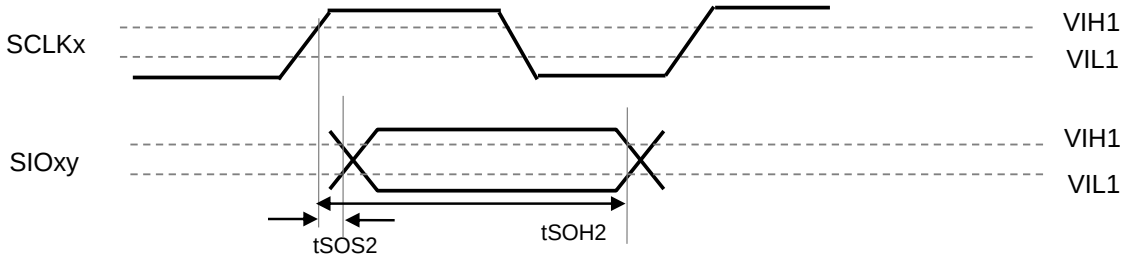


Figure 14. SPI Interface timing 4（this Product → MCU）SOPHx Mode= “1”

11.5. I²CBUS Interface

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V;AVDD=3.13 - 3.47V; TVDD1/2/3 =1.7 - 3.47V; VSS= 0V)
<I²C: Fast Mode>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL1/SCL2/MSCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA1 Hold Time from SCL1 Falling SDA2 Hold Time from SCL2 Falling MSDA Hold Time from MSCL Falling	tHD:DAT	0	-	-	µs
SDA1 Setup Time from SCL1 Rising SDA2 Setup Time from SCL2 Rising MSDA Setup Time from MSCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA1 and SCL1 Lines Rise Time of Both SDA2 and SCL2 Lines Rise Time of Both MSDA and MSCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA1 and SCL1 Lines Fall Time of Both SDA2 and SCL2 Lines Fall Time of Both MSDA and MSCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF

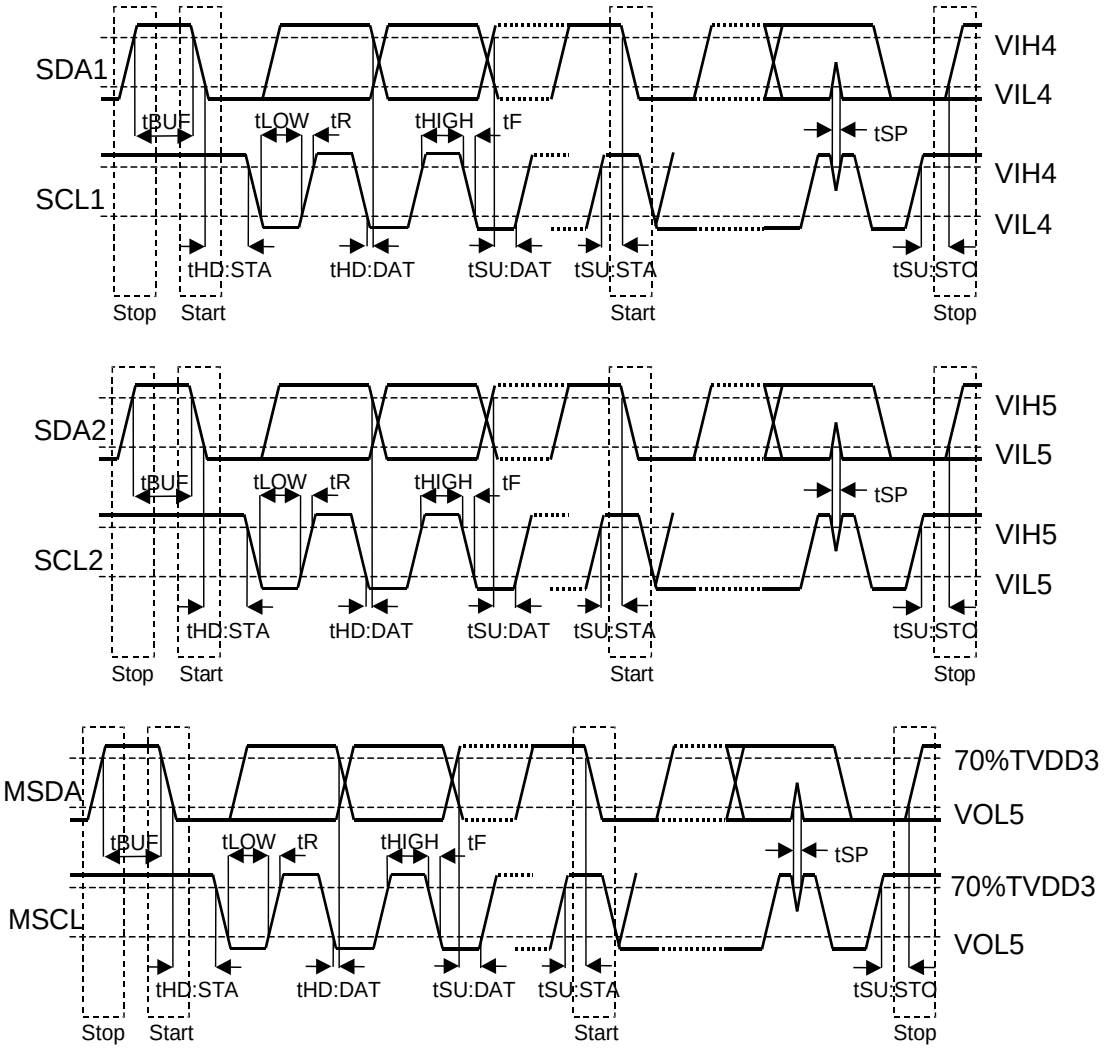


Figure 15. I²C BUS Interface Timing

11.6. SPI Master Interface

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V;AVDD=3.13 - 3.47V; TVDD1/2/3 =1.7 - 3.47V; VSS= 0V; CL= 6pF)

6.1. SPI Master Port: ESCLK Max. Frequency=24.576MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Mode					
ESCLK1 / ESCLK2 Frequency	-			24.576	MHz
ESCLK1 / ESCLK2 Duty Cycle (*39)	-		50		%
From ECSO1 "↓" to ESCLK1"↑" (*40) From ECSO2 "↓" to ESCLK2"↑" (*40)	-	50			ns
Delay Time from ESCLK1"↓" to ESDIO10-13 Delay Time from ESCLK2"↓" to ESDIO20-23	-	-5		5	ns
ESDIO10-13 Hold Time from ESCLK1 "↑" ESDIO20-23 Hold Time from ESCLK2 "↑"	-	3			ns
ESDIO10-13 Setup Time from ESCLK1 "↑" ESDIO20-23 Setup Time from ESCLK2 "↑"	-	3			ns

Notes:

*39. With an even dividing number.

*40. The pins for outputting ECSO1 can be switched by setting ECSOSEL1[2:0] bits.
The pins for outputting ECSO2 can be switched by setting ECSOSEL2[2:0] bits.

6.2. SPI Master Port: ESCLK Max. Frequency=49.152MHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master Mode						
ESCLK1 / ESCLK2 Frequency	48kHz base	-			49.152	MHz
	44.1kHz base				45.1584	MHz
ESCLK1 / ESCLK2 Duty Cycle(*39)		-		50		%
From ECSO1 "↓" to ESCLK1"↑" (*40) From ECSO2 "↓" to ESCLK2"↑" (*40)		-	25			ns
Delay Time from ESCLK1"↓" to ESDIO10-13 Delay Time from ESCLK2"↓" to ESDIO20-23		-	-5		5	ns
ESDIO10-13 Hold Time from ESCLK1 "↑" ESDIO20-23 Hold Time from ESCLK2 "↑"		-	3			ns
ESDIO10-13 Setup Time from ESCLK1 "↑" ESDIO20-23 Setup Time from ESCLK2 "↑"		-	3			ns

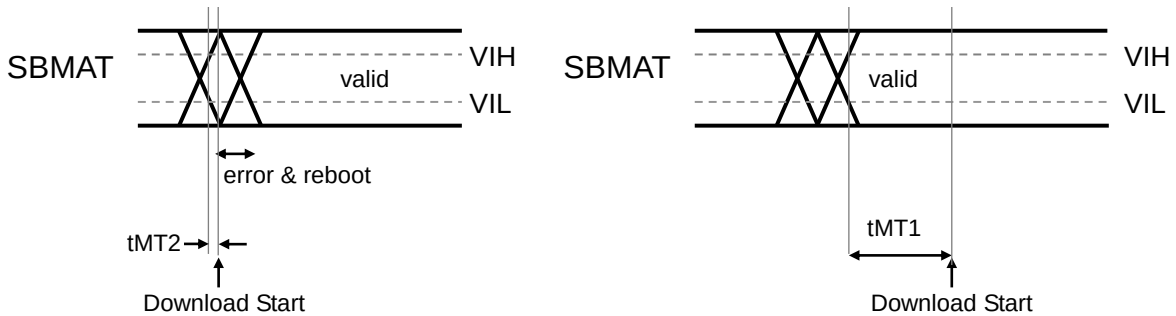
6.3. SPI Through Mode

Through Mode		Symbol	Min.	Typ.	Max.	Unit
Slave Port → Master Port						
ECSO1 Output Delay Time from CSN1 (*40) ECSO1 Output Delay Time from CSN2 (*40) ECSO2 Output Delay Time from CSN1 (*40) ECSO2 Output Delay Time from CSN2 (*40)		-	0		15	ns
ESCLK1 Output Delay Time from SCLK1 ESCLK1 Output Delay Time from SCLK2 ESCLK2 Output Delay Time from SCLK1 ESCLK2 Output Delay Time from SCLK2		-	0		15	ns
ESDIO10 Output Delay Time from SIO10 ESDIO10 Output Delay Time from SIO20 ESDIO20 Output Delay Time from SIO10 ESDIO20 Output Delay Time from SIO20		-	0		15	ns
Master Port → Slave Port						
SIO11 Output Delay Time from ESDIO11 SIO11 Output Delay Time from ESDIO21 SIO21 Output Delay Time from ESDIO11 SIO21 Output Delay Time from ESDIO21		-	0		15	ns
SELE pin L Pulse Width (*41)	MATNFN bit = “0”	-	16000/ fXTI			us
	MATNFN bit = “1”	-	700			ns
SBMAT selected Download Start pulse width (*42)	MATNFN bit = “0”	tMT1	16000/ fXTI			us
	MATNFN bit = “1”	tMT2	700			ns

Notes:

*41. It is necessary to keep SELE pin “L” for this amount of time when re-loading (SELE pin “H” to “L” to ”H”) after self-bootup.

*42. Further bootloads may be performed by keeping PDN pin =“H” and SELE pin =“H” while toggling the SBMAT pin.



a. MATNFN bit = “1” b. MATNFN bit = “0”

Figure 16. SBMAT download starting timing

When MATNFN bit = “1” (no noise filter setting), download starts after tMT2 after SBMAT pin state is changed. If the SBMAT pin is changed after the download starts, an error will occur, and the self-boot will be re-executed up to 3 times. In the case of MATNFN bit = “0” (with noise filter setting), download starts when the state is held for tMT1 or more after the SBMAT pin is changed.

11.7. JTAG Interface

(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V; AVDD=3.13 - 3.47V; TVDD1/2/3=1.7 - 3.47V; VSS= 0V; CL= 20pF)

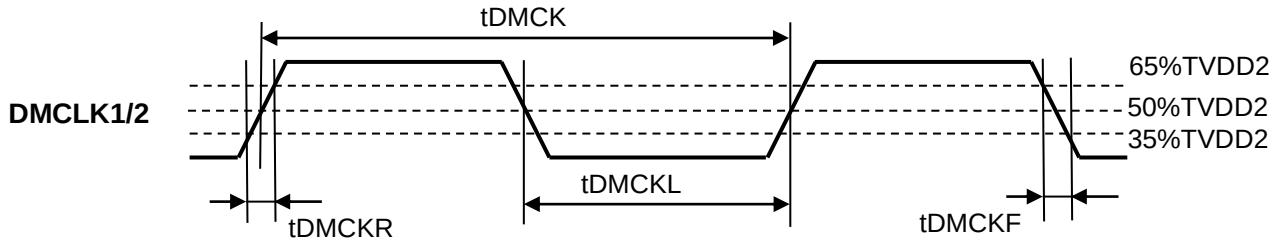
Parameter	Symbol	Min.	Typ.	Max.	Unit
TCK frequency				10	MHz
TCK Pulse width Low		40			ns
TCK Pulse width High		40			ns
TMS Setup Time from TCK rising		40			ns
TMS Hold Time from TCK rising		40			ns
TDI Setup Time from TCK rising		40			ns
TDI Hold Time from TCK rising		40			ns
TRST Setup Time from TCK rising		120			ns
From TRST “↑” to TCK “↑”		120			ns
Delay Time from TCK falling to TDO				40	ns

11.8. Digital Microphone Interface

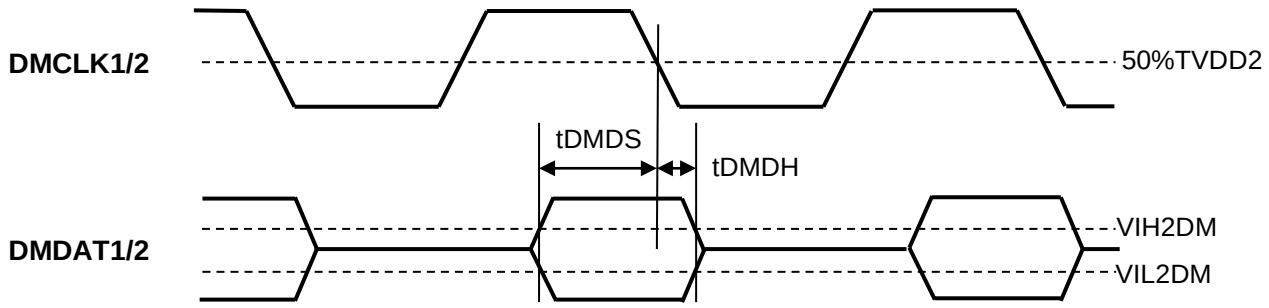
(Ta= -40 - 105ºC; VDDC=0.85 - 0.95V; AVDD=3.13 - 3.47V; TVDD1/2/3=1.7 - 3.47V; VSS= 0V; CL= 100pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DMDAT1/2					
Serial Data Input Latch Setup Time	tDMDS	50			ns
Serial Data Input Latch Hold Time	tDMDH	0			ns
DMCLK1/2					
Clock Frequency (*43)	fDMCK	0.5	64fs	6.2	MHz
Duty Cycle	dDMCK	40	50	60	%
Rise time	tDMCKR			10	ns
Fall time	tDMCKF			10	ns

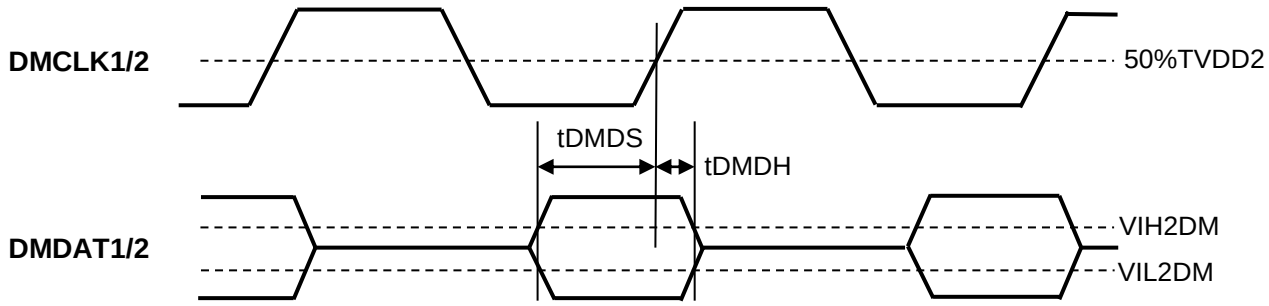
Note:
*43. The clock frequency depends on the sampling rate (fs) set by SDDMIC1[2:0], SDDMIC2[2:0] bits.



fDMCK = 1 / tDMCK
dDMCK = 100 x tDMKL / tDMCK



DMCLKP1/2 bit = “1”



DMCLKP1/2 bit = “0”

Figure 17. Digital Microphone Interface Timing Diagram

12. Recommended External Circuits

12.1. Connection Diagram

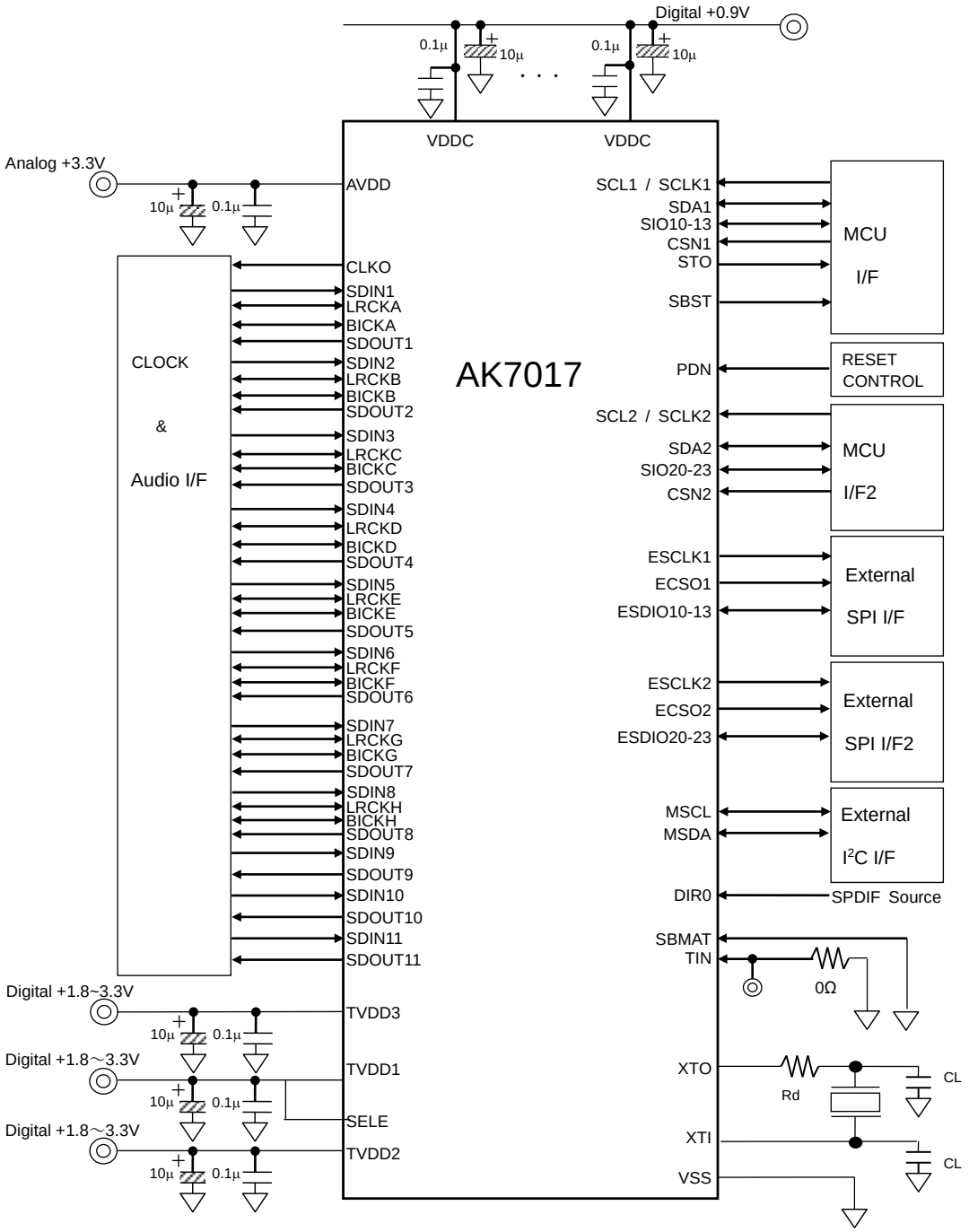


Figure 18. Connection Example

12.2. Peripheral Circuit

2.1. Ground

All VSS should be connected to the same ground. Decoupling capacitors, particularly ceramic capacitors of small capacity, should be placed at positions as closed as possible to this device. Connect at least one set of 0.1μF and 10μF decoupling capacitors for the VDDC power supply to the VDDC pins on the four sides of the chip.

2.2. Connection to Digital Circuit

To minimize the noise from digital circuits, the digital output of this device must be connected to CMOS or low voltage logic ICs.

2.3. Digital Input/Output Pin

48, 49, 54, 55pin outputs “L” or “H” when powering down, so please insert a damping resistor when using these pins as input pins.

2.4. Crystal Oscillator

From the viewpoint of the oscillation margin, it is recommended that the Crystal Oscillator connected to XTI pin and XTO pin of this product satisfy the following equivalent circuit parameters, and that the capacitance connected to XTI and XTO pins be used with the following values.

Table 4. Recommended Resistance and Capacitance with Crystal Oscillator

XTAL Oscillation Frequency	R1 (Max.)	C0 (Max.)	XTI/XTO pin Connection Capacity (CL)
12.288MHz	75Ω	1.5pF	8pF
24.576MHz	50Ω	1.5pF	8pF

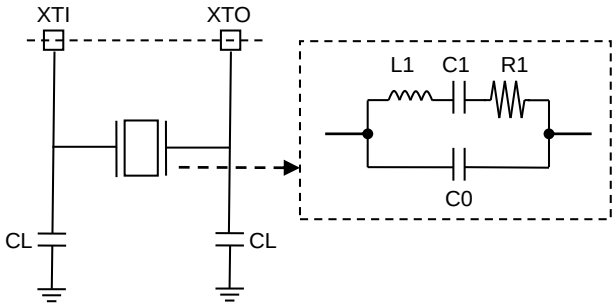
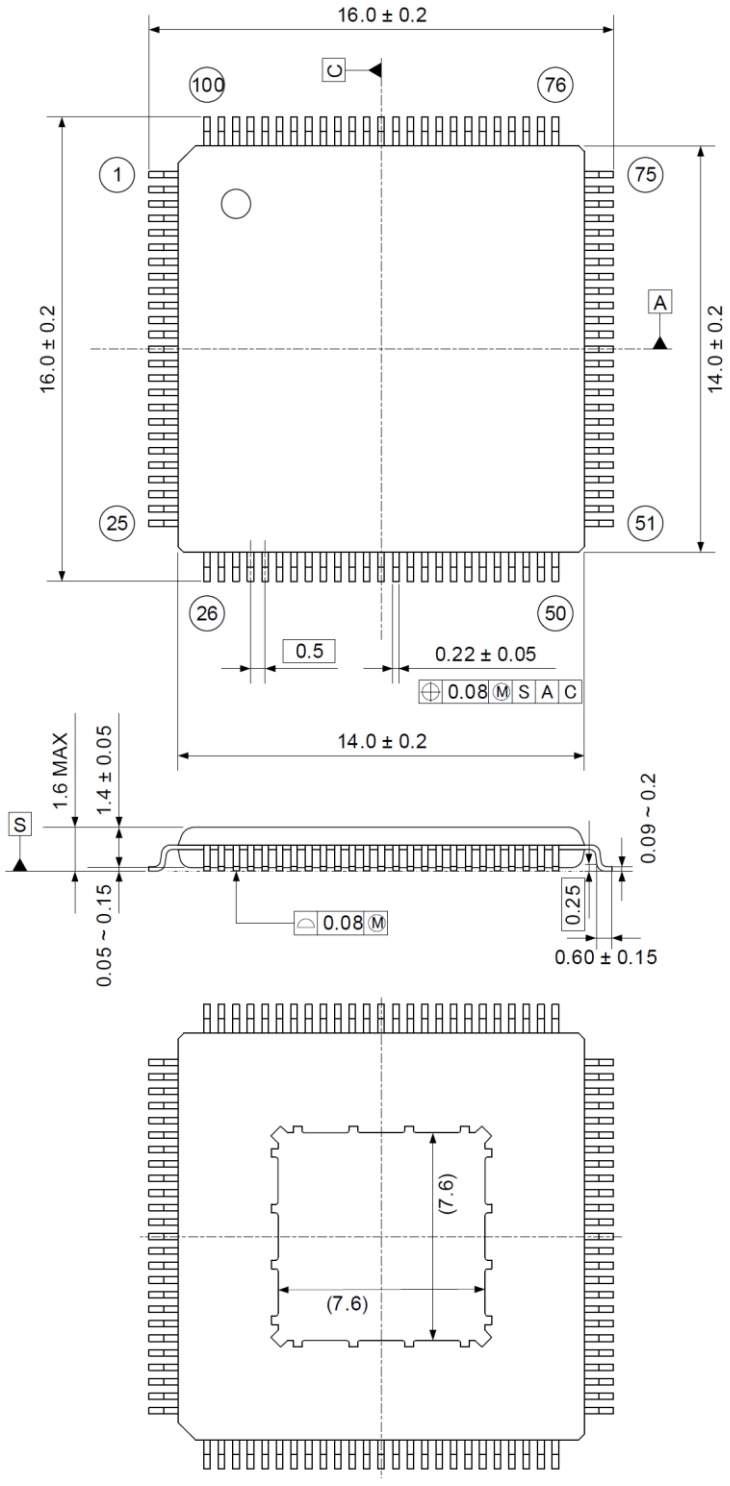


Figure 19. Electric Equivalent Circuit of Crystal Oscillator

13. Package

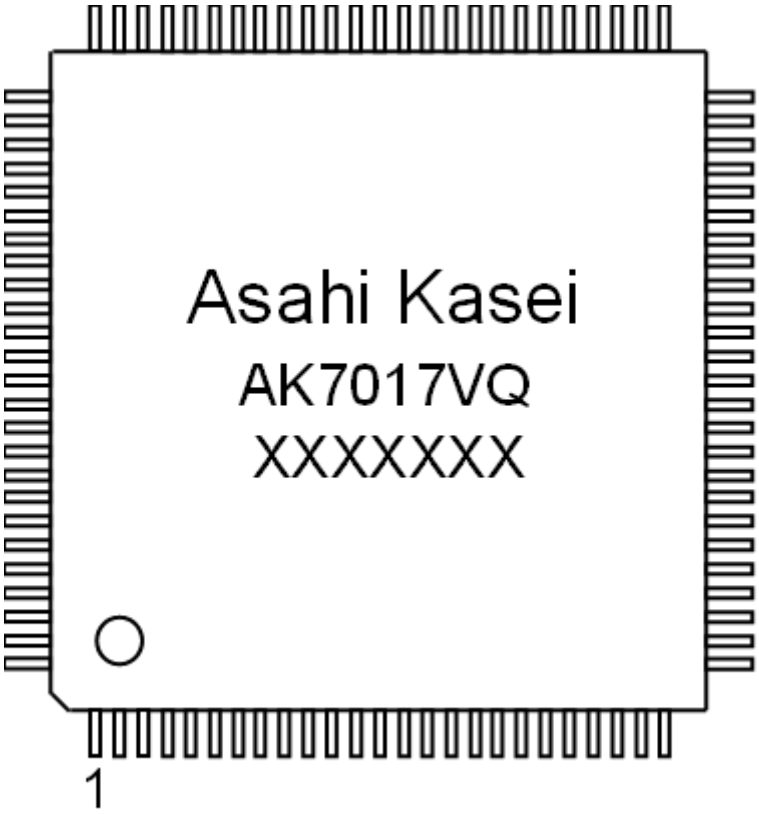
13.1. Outline Dimensions



13.2. Material and Finish

Package:	Epoxy
Lead Frame:	Cu
Lead Finishing:	Sn (Pb free)

13.3. Marking



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK7017VQ
4) Asahi Kasei Logo

14. Ordering Guide

AK7017VQ	-40 - +105ºC	100-pin HLQFP (0.5mm pitch)
AKD7017	AK7017 Evaluation Board	

15. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
2023/12/14	00	First edition		

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