AK4377

High Sound Quality Advanced DAC with HP

1. General Description

The AK4377 is stereo advanced 32-bit high sound quality audio DAC with a built-in ground-referenced headphone amplifier that adopted VELVET SOUND™ technology. The AK4377 has four types of 32-bit digital filters for better sound quality, achieving low distortion characteristics and wide dynamic range. AK4377 accepts up to 768 kHz PCM data and DSD256 input. The AK4377 is available in a 36-pin CSP package, utilizing less board space than competitive offerings.

2. Features

1. **Stereo High Sound Quality Advanced 32-bit DAC**
   - **4-types of Digital Filter for Sound Color Selection**
   - **2-types of Operation Mode (High Performance Mode / Low Power Mode)**
2. **Ground-referenced Class-G Stereo Headphone Amplifier**
   - **Output Power: 60 mW @ 16Ω**
   - **THD+N: –109 dB @ Po = 10 mW, R_L = 32Ω**
     –106 dB @ Po = 25 mW, R_L = 32Ω
   - **S/N: 128 dB**
   - **Output Noise Level: –129 dBV**
   - **Analog Volume: +4 to –20 dB & Mute**
   - **Ground Loop Noise Cancellation**
3. **Headphone Amplifier Output Pins Comply with IEC61000-4-2 Level4 ESD Protection**
4. **Digital Audio Interface**
   - **Master/Slave Mode**
   - **Sampling Frequency:**
     Slave Mode: 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 128 k, 176.4 k, 192 k, 256 k, 352.8 k, 384 k, 512 k, 705.6 k, 768 kHz
     Master Mode: 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 128 k, 176.4 k, 192 k, 256 k, 352.8 k, 384 kHz
   - **Interface Format: 32/24/16-bit I^2S/MSB justified**
   - **DSD Support by DoP: DSD64, DSD128, DSD256**
5. **Power Management**
6. **PLL**
7. **X'tal Oscillator**
8. **µP Interface: I^2C-bus (400 kHz)**
9. **Operation Temperature Range: Ta = –40 to 85°C**
10. **Power Supply:**
    - **AVDD (DAC, PLL): 1.7 to 1.9 V**
    - **CVDD (Headphone Amplifiers, Charge Pump): 1.7 to 1.9 V**
    - **LVDD (LDO2 for Digital Core): 1.7 to 1.9 V (built-in LDO)**
    - **TVDD (Digital Interface): 1.65 to 3.6 V**
11. **Package: 36-pin CSP (2.893 x 3.082 mm, 0.4 mm pitch)**

3. Table of Contents

4. Block Diagram and Functions

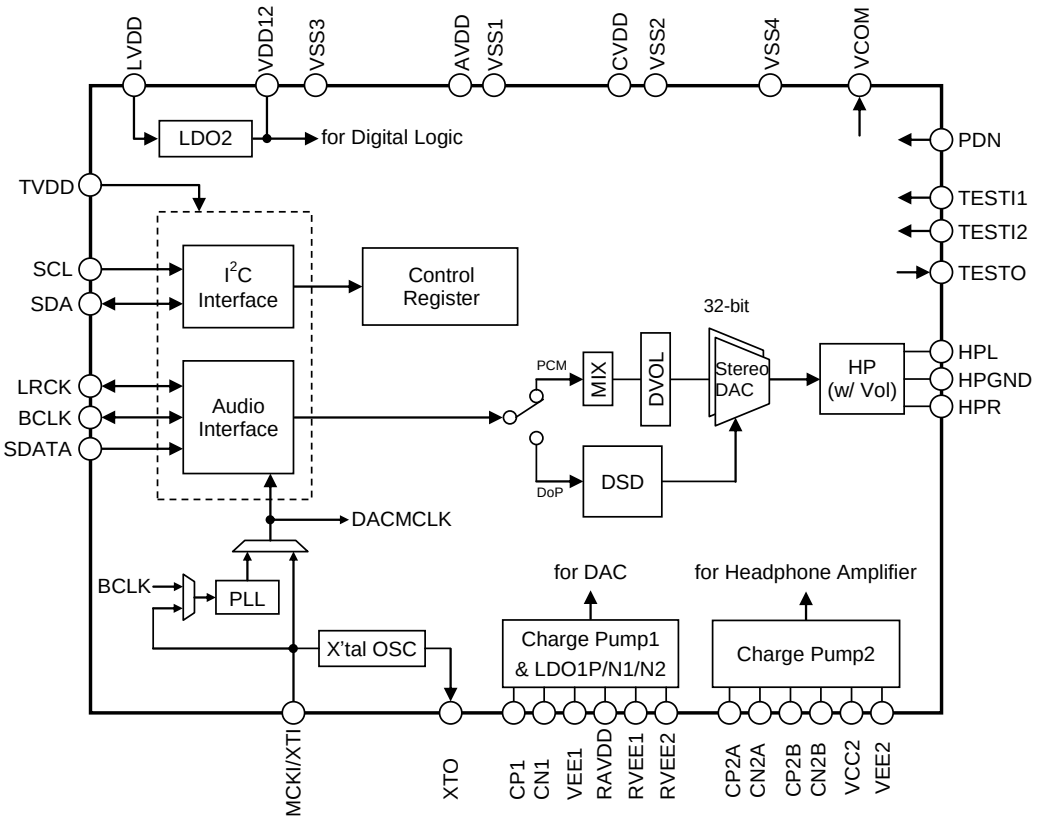
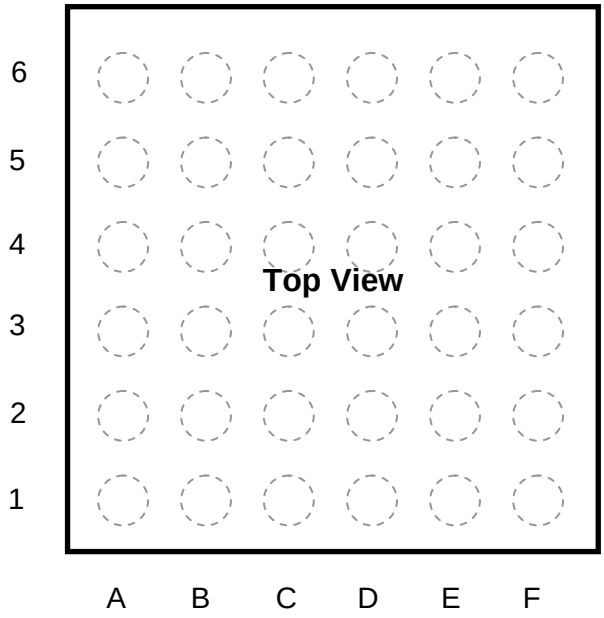


Figure 1. AK4377 Block Diagram

5. Pin Configurations and Functions

5-1 Pin Configurations

36-pin CSP (2.893 x 3.082 mm, 0.4 mm pitch)



6	VDD12	SDATA	LVDD	VEE1	CN1	CVDD
5	VSS3	LRCK	PDN	CP1	CP2B	CN2B
4	BCLK	TVDD	TESTI1	VSS2	CP2A	CN2A
3	MCKI /XTI	SDA	TESTI2	TESTO	VCC2	VEE2
2	XTO	SCL	VSS4	VSS1	HPGND	HPR
1	RVEE2	RAVDD	RVEE1	AVDD	VCOM	HPL
	A	**B**	**C**	**D**	**E**	**F**

Top View

5-2 Pin Function Difference with AK4376A

Pin No.	AK4376A		AK4377	
	Pin Name	Function	Pin Name	Function
A1	XTI	X'tal Oscillator Input Pin Left floating when not in use.	RVEE2	LDO1N (−1.5 V) Output 2 Pin Connect capacitor from this pin to VSS1 pin.
A3	MCKI	External Master Clock Input Pin Connect to VSS3 when not in use.	MCKI/XTI	External Master Clock Input / X'tal Oscillator Input Pin Connect to VSS3 and set PMOSC bit to "0" when not in use.
C1	RVEE	LDO1N (−1.5 V) Output Pin Connect capacitor from this pin to VSS1 pin.	RVEE1	LDO1N (−1.5 V) Output 1 Pin Connect capacitor from this pin to VSS1 pin.

5-3 Pin Functions

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Power Supply					
D1	AVDD	-	Analog Power Supply Pin	-	AVDD
D2	VSS1	-	Analog Ground Pin	-	-
F6	CVDD	-	Headphone Amplifier / Charge Pump Power Supply Pin	-	CVDD
D4	VSS2	-	Headphone Amplifier / Charge Pump Ground Pin	-	-
C6	LVDD	-	Digital Core & LDO2 Power Supply Pin	-	LVDD
A5	VSS3	-	Digital Ground Pin	-	-
C2	VSS4	-	Substrate Pin	-	-
B4	TVDD	-	Digital Interface Power Supply Pin	-	TVDD
E1	VCOM	O	Common Voltage Output Pin Connect a 2.2 µF ±50% capacitor from this pin to VSS1 pin. (Note 2)	AVDD / VSS1	-
A6	VDD12	-	LDO2 (1.2 V) Output Power Supply Pin (Note 1) Connect capacitor from this pin to VSS3 pin. (Note 2)	LVDD / VSS3	LVDD

Note 1. Capacitor value should be selected from 2.2 µF ±50% to 4.7 µF ±50% to VDD12 pin.
Note 2. Do not connect a load to VCOM pin and VDD12 pin.

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Charge Pump & LDO					
D5	CP1	O	Positive Charge Pump Capacitor Terminal 1 Pin Connect a 2.2 µF ±50% capacitor from this pin to CN1 pin.	CVDD / VSS2	CVDD
E6	CN1	I	Negative Charge Pump Capacitor Terminal 1 Pin Connect a 2.2 µF ±50% capacitor from this pin to CP1 pin.	CVDD	CVDD
D6	VEE1	O	Charge Pump Circuit Negative Voltage (–CVDD) Output 1 Pin Connect a 2.2 µF ±50% capacitor from this pin to VSS2 pin. (Note 5)	CVDD / VSS2	-
B1	RAVDD	O	LDO1P (1.5 V) Output Pin (Note 3) Connect capacitor from this pin to VSS1 pin. (Note 5)	AVDD / VSS1	-
C1	RVEE1	O	LDO1N (–1.5 V) Output 1 Pin (Note 3) Connect capacitor from this pin to VSS1 pin. (Note 5)	AVDD / VSS1	-
A1	RVEE2	O	LDO1N (–1.5 V) Output 2 Pin (Note 4) Connect capacitor from this pin to VSS1 pin. (Note 5)	AVDD / VSS1	-
E3	VCC2	O	Charge Pump Circuit Positive Voltage (CVDD or 1/2*CVDD) Output Pin Connect a 2.2 µF ±50% capacitor from this pin to VSS2 pin. (Note 5)	CVDD / VSS2	CVDD
E4	CP2A	O	Positive Charge Pump Capacitor Terminal 2A Pin Connect a 2.2 µF ±50% capacitor from this pin to CN2A pin.	CVDD / VSS2	CVDD
F4	CN2A	I	Negative Charge Pump Capacitor Terminal 2A Pin Connect a 2.2 µF ±50% capacitor from this pin to CP2A pin.	CVDD	CVDD
E5	CP2B	O	Positive Charge Pump Capacitor Terminal 2B Pin Connect a 2.2 µF ±50% capacitor from this pin to CN2B pin.	CVDD / VSS2	CVDD
F5	CN2B	I	Negative Charge Pump Capacitor Terminal 2B Pin Connect a 2.2 µF ±50% capacitor from this pin to CP2B pin.	CVDD	CVDD
F3	VEE2	O	Charge Pump Circuit Negative Voltage (–CVDD or –1/2*CVDD) Output 2 Pin Connect a 2.2 µF ±50% capacitor from this pin to VSS2 pin. (Note 5)	CVDD / VSS2	-

Note 3. Capacitor value should be selected from 2.2 µF ±50% to 4.7 µF ±50% to RAVDD pin and RVEE1 pin.

Note 4. Capacitor value should be selected from 1.0 µF ±50% to 4.7 µF ±50% to RVEE2 pin.

Note 5. Do not connect a load to VEE1 pin, VCC2 pin, VEE2 pin, RAVDD pin, RVEE1 pin and RVEE2 pin.

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Control Interface					
B2	SCL	I	I^2C Serial Data Clock Pin	TVDD / VSS3	TVDD
B3	SDA	I/O	I^2C Serial Data Input/Output Pin	TVDD / VSS3	TVDD
Audio Interface					
A3	MCKI	I	External Master Clock Input Pin (PMOSC bit = “0”)	TVDD / VSS3	TVDD
	XTI	I	X’tal Oscillator Input Pin (PMOSC bit = “1”)		
A2	XTO	O	X’tal Oscillator Output Pin	TVDD / VSS3	TVDD
A4	BCLK	I/O	Audio Serial Data Clock Pin	TVDD / VSS3	TVDD
B5	LRCK	I/O	Frame Sync Clock Pin	TVDD / VSS3	TVDD
B6	SDATA	I	Audio Serial Data Input Pin	TVDD / VSS3	TVDD
Analog Output					
F1	HPL	O	Lch Headphone Amplifier Output Pin	CVDD / VEE2	CVDD / VEE2
F2	HPR	O	Rch Headphone Amplifier Output Pin	CVDD / VEE2	CVDD / VEE2
E2	HPGND	I	Headphone Amplifier Ground Loop Noise Cancellation Pin	-	-
Others					
C5	PDN	I	Power down Pin “L”: Power-Down, “H”: Power-Up	TVDD / VSS3	TVDD
C4	TESTI1	I	Test Input Pin It must be tied “L”.	TVDD / VSS3	TVDD
C3	TESTI2	I	Test Input Pin It must be tied “L”.	TVDD / VSS3	TVDD
D3	TESTO	O	Test Output Pin	AVDD / VSS1	AVDD

Note 6. The SCL pin, SDA pin, MCKI/XTI pin, BCLK pin, LRCK pin, SDATA pin, HPGND pin, PDN pin, TESTI1 pin and theTESTI2 pin must not be allowed to float.

5-4 Handing of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	HPL, HPR	Open
Digital	XTO, TESTO	Open
	MCKI/XTI	Connect to VSS3 (PMOSC bit is fixed to “0”)
	TESTI1, TESTI2	Connect to VSS3

6. Absolute Maximum Ratings

(VSS1 = VSS2 = VSS3 = VSS4 = 0 V; Note 7, Note 8)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies: (Note 9)	Analog	AVDD	–0.3	4.3	V
	Headphone Amplifier / Charge Pump	CVDD	–0.3	4.3	V
	LDO2 for Digital Core	LVDD	–0.3	4.3	V
	Digital Interface	TVDD	–0.3	4.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 10)		VIND	–0.3	TVDD+0.3 or 4.3	V
Ambient Temperature (Powered Applied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 7. All voltages with respect to ground.

Note 8. VSS1, VSS2, VSS3, VSS4 must be connected to the same analog ground plane.

Note 9. Charge pump 1 & 2 are not in operation. In the case that charge pump 1 & 2 are in operation, the maximum values of AVDD and CVDD become 2.15 V.

Note 10. MCKI/XTI, BCLK, LRCK, SDATA, SCL, SDA, PDN, TESTI1, TESTI2 pins
The maximum value of input voltage is lower value between (TVDD+0.3) V and 4.3 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 = VSS2 = VSS3 = VSS4 = 0 V; Note 11)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 12)	Analog	AVDD	1.7	1.8	1.9	V
	Headphone Amplifier / Charge Pump	CVDD	1.7	1.8	1.9	V
	LDO2 for Digital Core	LVDD	1.7	1.8	1.9	V
	Digital Interface	TVDD	1.65	1.8	3.6	V

Note 11. All voltages with respect to ground.

Note 12. Each power-up/down sequence is shown below.

<Power-Up>

1. PDN pin = “L”
2. TVDD, AVDD, LVDD, CVDD
   (AVDD must be powered up before or at the same time of CVDD. The power-up sequence of TVDD and LVDD is not critical.)
3. The PDN pin is allowed to be “H” after all power supplies are applied and settled.

<Power-Down>

1. PDN pin = “L”
2. TVDD, AVDD, LVDD, CVDD
   (CVDD must be powered down before or at the same time of AVDD. The power-down sequence of TVDD and LVDD is not critical.)

8. Electrical Characteristics

8-1 Analog Characteristics

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; Signal Frequency = 1 kHz; 24-bit Data; fs = 44.1 kHz, BCLK = 64fs; Measurement Bandwidth = 20 Hz to 20 kHz; unless otherwise specified)

< High Performance Mode >

Parameter		Min.	Typ.	Max.	Unit
Stereo DAC Characteristics:					
Resolution		-	-	32	Bits
Headphone Amplifier Characteristics: DAC (Stereo) → HPL/HPR pins, OVL/R = 0 dB, HPG = 0 dB, R_L = 32Ω					
Output Power					
0 dBFS, R_L = 32Ω, HPG = 0 dB		-	25	-	mW
0 dBFS, R_L = 32Ω, HPG = –4 dB		-	10	-	mW
R_L = 16Ω, HPG = 0 dB, THD+N < –60 dB		-	45	-	mW
R_L = 16Ω, HPG = +2 dB, THD+N < –20 dB		-	60	-	mW
Output Level (0 dBFS, R_L = 32Ω, HPG = –4 dB) (Note 13)		0.52	0.57	0.61	Vrms
THD+N					
0 dBFS, R_L = 32Ω, HPG = –4 dB (Po = 10 mW)	fs = 44.1 kHz BW = 20 kHz	-	–109	-	dB
	fs = 96 kHz BW = 40 kHz	-	–106	-	dB
	fs = 192 kHz BW = 40 kHz	-	–106	-	dB
	fin = 10 kHz fs = 44.1 kHz BW = 20 kHz	-	–106	-	dB
0 dBFS, R_L = 32Ω, HPG = 0 dB (Po = 25 mW)	fs = 44.1 kHz BW = 20 kHz	-	–106	-	dB
0 dBFS, R_L = 32Ω, OVL/R = –10 dB, HPG = 0 dB (Po = 2.5 mW)	fs = 44.1 kHz BW = 20 kHz	-	–102	–92	dB
0 dBFS, R_L = 16Ω, HPG = –4 dB (Po = 20 mW)	fs = 44.1 kHz BW = 20 kHz	-	–107	-	dB
0 dBFS, R_L = 600Ω, HPG = +2 dB (Po = 2.0 mW @ 1.1 Vrms)	fs = 44.1 kHz BW = 20 kHz	-	–104	-	dB

Parameter		Min.	Typ.	Max.	Unit
Dynamic Range –60 dBFS, A-weighted, HPG = 0 dB		110	118	-	dB
S/N (A-weighted, Noise Gate Enable) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / "0" Data)		-	128	-	dB
S/N (A-weighted, Noise Gate Disable) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / "0" Data)		110	118	-	dB
Output Noise Level (Noise Gate Enable, A-weighted)		-	–129	-	dBV
Output Noise Level (Noise Gate Disable, A-weighted, HPG ≤ –14 dB)		-	–127	-	dBV
Interchannel Isolation 0 dBFS, HPG = –4 dB (Po = 10 mW) External Impedance = 0.01Ω (Note 14) External Impedance = 0.1Ω (Note 14)		 74 -	 94 74	 - -	 dB dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance		7.2	32	-	Ω
Load Capacitance		-	-	1000	pF
Load Inductance		-	-	0.375	μH
PSRR (HPG = –4 dB) (Note 15) 217 Hz 1 kHz		 - -	 85 85	 - -	 dB dB
DC-offset (Note 16) HPG = 0 dB HPG = All Gain		 –0.15 –0.2	 0 0	 +0.15 +0.2	 mV mV
Headphone Output Volume Characteristics:					
Gain Setting		–20	-	+4	dB
Step Width (Note 17)	HPG[3:0] bits: between DH and EH HPG[3:0] bits: between BH and DH HPG[3:0] bits: between 1H and BH	1.5 0.5 1	2 1 2	2.5 1.5 3	dB dB dB

Note 13. Output level is proportional to AVDD. Typ. 0.57 Vrms x AVDD / 1.8 V @headphone amplifier gain = –4 dB.
Note 14. Impedance between the HPGND pin and the system ground.
Note 15. PSRR is referred to all power supply voltages with 100 mVpp sine wave.
Note 16. When there is no gain change nor a temperature drift after headphone amplifier is power-up.
Note 17. Output level variation of headphone amplifier that is adjusted by HPG[3:0] bits (1 step)

Parameter	Value	Unit
ESD Immunity IEC61000-4-2 Level4, Contact (Note 18)	±8	kV

Note 18. It is measured at the HPL and HPR pins using an evaluation board (AKD4377-SA Rev.1).

< Low Power Mode >

Parameter		Min.	Typ.	Max.	Unit
Headphone Amplifier Characteristics: DAC (Stereo) → HPL/HPR pins, OVL/R = 0 dB, HPG = 0 dB, R_L = 32Ω					
Output Power					
0 dBFS, R_L = 32Ω, HPG = 0 dB		-	25	-	mW
0 dBFS, R_L = 32Ω, HPG = –4 dB		-	10	-	mW
R_L = 16Ω, HPG = 0 dB, THD+N < –60 dB		-	45	-	mW
R_L = 16Ω, HPG = +2 dB, THD+N < –20 dB		-	60	-	mW
Output Level (0 dBFS, R_L = 32Ω, HPG = –4 dB) (Note 13)		0.52	0.57	0.61	Vrms
THD+N					
0 dBFS, R_L = 32Ω, HPG = –4 dB (Po = 10 mW)	fs = 44.1 kHz BW = 20 kHz	-	–100	-	dB
0 dBFS, R_L = 32Ω, HPG = 0 dB (Po = 25 mW)	fs = 44.1 kHz BW = 20 kHz	-	–100	-	dB
0 dBFS, R_L = 16Ω, HPG = –4 dB (Po = 20 mW)	fs = 44.1 kHz BW = 20 kHz	-	–98	-	dB
0 dBFS, R_L = 600Ω, HPG = +2 dB (Po = 2.0 mW @ 1.1 Vrms)	fs = 44.1 kHz BW = 20 kHz	-	–98	-	dB
Dynamic Range –60 dBFS, A-weighted, HPG = 0 dB		-	115	-	dB
S/N (A-weighted) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / "0" Data)		-	115	-	dB
Interchannel Isolation 0 dBFS, HPG = –4 dB (Po = 10 mW)					
External Impedance = 0.01Ω (Note 14)		74	94	-	dB
External Impedance = 0.1Ω (Note 14)		-	74	-	dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance		7.2	32	-	Ω
Load Capacitance		-	-	1000	pF
Load Inductance		-	-	0.375	μH
PSRR (HPG = –4 dB) (Note 15)					
217 Hz		-	85	-	dB
1 kHz		-	85	-	dB
DC-offset (Note 16)					
HPG = 0 dB		–0.3	0	+0.3	mV
HPG = All Gain		–0.4	0	+0.4	mV
Headphone Output Volume Characteristics:					
Gain Setting		–20	-	+4	dB
Step Width (Note 17)	HPG[3:0] bits: between DH and EH	1.5	2	2.5	dB
	HPG[3:0] bits: between BH and DH	0.5	1	1.5	dB
	HPG[3:0] bits: between 1H and BH	1	2	3	dB

Note 13. Output level is proportional to AVDD. Typ. 0.57 Vrms x AVDD / 1.8 V @headphone amplifier gain = –4 dB.
Note 14. Impedance between the HPGND pin and the system ground.
Note 15. PSRR is referred to all power supply voltages with 100 mVpp sine wave.
Note 16. When there is no gain change nor a temperature drift after headphone amplifier is power-up.
Note 17. Output level variation of headphone amplifier that is adjusted by HPG[3:0] bits (1 step)

Parameter	Value	Unit
ESD Immunity IEC61000-4-2 Level4, Contact (Note 18)	±8	kV

Note 18. It is measured at the HPL and HPR pins using an evaluation board (AKD4377-SA Rev.1).

8-2 PLL Characteristics

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit
PLL Characteristics				
Reference Clock (Figure 11)	0.256	-	3.072	MHz
PLLCLK Frequency (Figure 11)				
44.1 kHz * 256fs * 9	-	101.6064	-	MHz
48.0 kHz * 256fs * 9	-	110.592	-	MHz
44.1 kHz * 256fs * 10	-	112.896	-	MHz
48.0 kHz * 256fs * 10	-	122.880	-	MHz
Lock Time	-	-	2	msec

8-3 Charge Pump & LDO Circuit Power-Up Time

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; unless otherwise specified)

Parameter	Capacitor	Min.	Typ.	Max.	Unit
Block Power-Up Time					
CP1 (Note 19)	2.2 µF @VEE1	-	-	6.5	msec
CP2 (Class-G) (Note 19, Note 20)	2.2 µF @VEE2	-	-	4.5	msec
LDO1P (Note 21)	2.2 µF @RAVDD	-	-	1	msec
LDO1N1 (Note 21)	2.2 µF @RVEE1	-	-	1	msec
LDO1N2 (Note 21)	1.0 µF @RVEE2	-	-	1	msec
LDO2 (Note 19)	2.2 µF @VDD12	-	-	1	msec

Note 19. Power-up time is a fixed value that is not affected by a capacitor.

Note 20. Power-up time is a value to –1/2 CVDD, since CP2 starts with 1/2 VDD Mode as part of Class-G operation.

Note 21. Power-up time is proportional to a capacitor value. For instance, if a 4.7 µF is connected to RVEE1 pin, LDO1N1 power-up time is 2.1 msec (Max.). If 2.2 µF is connected to RVEE2 pin, LDO1N2 power-up time is 2.2 msec (Max.).

8-4 Power Supply Current

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; BCLK = 64fs; Slave Mode, No Data Input, R_L = 32Ω; unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit
Power Supply Current:				
Power-Up (PDN pin = “H”, All Circuits Power-Up) (Note 22)				
AVDD + CVDD + LVDD + TVDD	-	35	-	mA
Power-Up (PDN pin = “H”, DAC + Headphone Amplifier Power-Up, PLL & X’tal OSC Power-Down)				
AVDD + CVDD + LVDD + TVDD	-	33	50	mA
Power-Down (PDN pin = “L”) (Note 23)				
AVDD + CVDD + LVDD + TVDD	-	0	10	µA

Note 22. DAC, Headphone Amplifier, PLL and X’tal OSC are all powered up.

Note 23. All digital input pins are fixed to TVDD or VSS3.

8-5 Power Consumption for Each Operation Mode

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = VSS4 = 0 V; MCKI = 256fs, BCLK = 64fs; Slave Mode, No Data Input, R_L = 32Ω, PLL Circuits Power-Down, X'tal OSC Power-Down)

< High Performance Mode >

Mode	Typical Current [mA]				Total Power [mW]
	AVDD	CVDD	LVDD	TVDD	
DAC → Headphone (fs = 44.1 kHz)	14.52	17.53	1.10	0.02	59.71
DAC → Headphone (fs = 96 kHz)	14.52	17.53	1.80	0.02	60.97
DAC → Headphone (fs = 192 kHz)	14.52	17.53	3.10	0.02	63.31

< Low Power Mode >

Mode	Typical Current [mA]				Total Power [mW]
	AVDD	CVDD	LVDD	TVDD	
DAC → Headphone (fs = 44.1 kHz)	4.89	5.68	0.90	0.02	20.68

8-6 Sharp Roll-Off Filter (fs = 44.1 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 44.1 kHz; DASD bit = "0", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 24)	–0.006 to +0.124 dB	PB	0	-	20.42	kHz
	–6.0 dB		-	22.05	-	kHz
Stopband (Note 24)		SB	24.1	-	-	kHz
Passband Ripple		PR	–0.006	-	+0.124	dB
Stopband Attenuation (Note 25)		SA	69.9	-	-	dB
Group Delay (Note 26)		GD	-	26	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 20.0 kHz		FR	–0.12	-	+0.03	dB
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ Low power mode:						
Frequency Response: 0 to 20.0 kHz		FR	–0.68	-	+0.03	dB

Note 24. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4630 × fs (@–0.006/+0.124 dB), SB = 0.547 × fs. Each frequency response refers to that of 1 kHz.

Note 25. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 26. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-7 Sharp Roll-Off Filter (fs = 96 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 96 kHz; DASD bit = "0", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 27)	–0.003 to +0.127 dB	PB	0	-	44.4	kHz
	–6.0 dB		-	48.01	-	kHz
Stopband (Note 27)		SB	52.5	-	-	kHz
Passband Ripple		PR	–0.003	-	+0.127	dB
Stopband Attenuation (Note 25)		SA	69.9	-	-	dB
Group Delay (Note 26)		GD	-	26	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 40.0 kHz		FR	–0.72	-	+0.11	dB
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ Low power mode:						
Frequency Response: 0 to 40.0 kHz		FR	–2.18	-	+0.10	dB

Note 27. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4625 × fs (@–0.003/+0.127 dB), SB = 0.547 × fs. Each frequency response refers to that of 1 kHz.

8-8 Sharp Roll-Off Filter (fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 192 kHz; DASD bit = "0", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 28)	−0.002 to +0.13 dB	PB	0	-	88.94	kHz
	−6.0 dB		-	96.01	-	kHz
Stopband (Note 28)		SB	105	-	-	kHz
Passband Ripple		PR	−0.002	-	+0.13	dB
Stopband Attenuation (Note 25)		SA	69.9	-	-	dB
Group Delay (Note 26)		GD	-	26	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 80.0 kHz		FR	−2.90	-	+0.35	dB

Note 25. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 26. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

Note 28. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4538 × fs (@−0.002/+0.13 dB), SB = 0.547 × fs. Each frequency response refers to that of 1 kHz.

8-9 Slow Roll-Off Filter (fs = 44.1 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 44.1 kHz; DASD bit = "0", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 29)	–0.07 to +0.006 dB	PB	0	-	7.7	kHz
	–3.0 dB		-	18.34	-	kHz
Stopband (Note 29)		SB	39.1	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.006	dB
Stopband Attenuation (Note 30)		SA	72.8	-	-	dB
Group Delay (Note 31)		GD	-	26	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 20.0 kHz		FR	–4.44	-	+0.03	dB
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ Low power mode:						
Frequency Response: 0 to 20.0 kHz		FR	–5.00	-	+0.03	dB

Note 29. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1746 × fs (@–0.07/+0.006 dB), SB = 0.887 × fs. Each frequency response refers to that of 1 kHz.

Note 30. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 31. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-10 Slow Roll-Off Filter (fs = 96 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 96 kHz; DASD bit = "0", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 32)	–0.07 to +0.007 dB	PB	0	-	16.76	kHz
	–3.0 dB		-	39.9	-	kHz
Stopband (Note 32)		SB	85.2	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.007	dB
Stopband Attenuation (Note 30)		SA	72.8	-	-	dB
Group Delay (Note 31)		GD	-	26	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 40.0 kHz		FR	–4.00	-	+0.10	dB
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ Low power mode:						
Frequency Response: 0 to 40.0 kHz		FR	–5.46	-	+0.10	dB

Note 32. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1746 × fs (@–0.07/+0.007 dB), SB = 0.888 × fs. Each frequency response refers to that of 1 kHz.

8-11 Slow Roll-Off Filter (fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 192 kHz; DASD bit = "0", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 33)	−0.07 to +0.007 dB	PB	0	-	33.56	kHz
	−3.0 dB		-	79.9	-	kHz
Stopband (Note 33)		SB	170.3	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.007	dB
Stopband Attenuation (Note 30)		SA	72.8	-	-	dB
Group Delay (Note 31)		GD	-	26	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 80.0 kHz		FR	−6.00	-	+0.35	dB

Note 30. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 31. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

Note 33. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1748 × fs (@−0.07/+0.007 dB), SB = 0.887 × fs. Each frequency response refers to that of 1 kHz.

8-12 Short Delay Sharp Roll-Off Filter (fs = 44.1 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 44.1 kHz; DASD bit = "1", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 34)	–0.008 to +0.126 dB	PB	0	-	20.4	kHz
	–6.0 dB		-	22.18	-	kHz
Stopband (Note 34)		SB	24.1	-	-	kHz
Passband Ripple		PR	–0.008	-	+0.126	dB
Stopband Attenuation (Note 35)		SA	56.4	-	-	dB
Group Delay (Note 36)		GD	-	5.5	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 20.0 kHz		FR	–0.12	-	+0.03	dB
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ Low power mode:						
Frequency Response: 0 to 20.0 kHz		FR	–0.68	-	+0.03	dB

Note 34. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4626 × fs (@–0.008/+0.126 dB), SB = 0.547 × fs. Each frequency response refers to that of 1 kHz.

Note 35. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 36. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-13 Short Delay Sharp Roll-Off Filter (fs = 96 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 96 kHz; DASD bit = "1", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 37)	–0.003 to +0.132 dB	PB	0	-	44.4	kHz
	–6.0 dB		-	48.28	-	kHz
Stopband (Note 37)		SB	52.5	-	-	kHz
Passband Ripple		PR	–0.003	-	+0.132	dB
Stopband Attenuation (Note 35)		SA	56.4	-	-	dB
Group Delay (Note 36)		GD	-	5.5	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 40.0 kHz		FR	–0.90	-	+0.11	dB
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ Low power mode:						
Frequency Response: 0 to 40.0 kHz		FR	–2.36	-	+0.10	dB

Note 37. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4625 × fs (@–0.003/+0.132 dB), SB = 0.547 × fs. Each frequency response refers to that of 1 kHz.

8-14 Short Delay Sharp Roll-Off Filter (fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 192 kHz; DASD bit = "1", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 38)	−0.001 to +0.135 dB	PB	0	-	88.8	kHz
	−6.0 dB		-	96.57	-	kHz
Stopband (Note 38)		SB	105	-	-	kHz
Passband Ripple		PR	−0.001	-	+0.135	dB
Stopband Attenuation (Note 35)		SA	56.4	-	-	dB
Group Delay (Note 36)		GD	-	5.5	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 80.0 kHz		FR	−3.00	-	+0.36	dB

Note 35. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 36. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

Note 38. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4625 × fs (@−0.001/+0.135 dB), SB = 0.547 × fs. Each frequency response refers to that of 1 kHz.

8-15 Short Delay Slow Roll-Off Filter (fs = 44.1 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 44.1 kHz; DASD bit = "1", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 39)	–0.07 to +0.025 dB	PB	0	-	8.83	kHz
	–3.0 dB		-	18.72	-	kHz
Stopband (Note 39)		SB	39.5	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.025	dB
Stopband Attenuation (Note 40)		SA	75.1	-	-	dB
Group Delay (Note 41)		GD	-	4.7	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 20.0 kHz		FR	–4.16	-	+0.05	dB
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ Low power mode:						
Frequency Response: 0 to 20.0 kHz		FR	–4.66	-	+0.03	dB

Note 39. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2002 × fs (@–0.07/+0.025 dB), SB = 0.896 × fs. Each frequency response refers to that of 1 kHz.

Note 40. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 41. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-16 Short Delay Slow Roll-Off Filter (fs = 96 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 96 kHz; DASD bit = "1", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 42)	–0.07 to +0.027 dB	PB	0	-	19.29	kHz
	–3.0 dB		-	40.78	-	kHz
Stopband (Note 42)		SB	86.0	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.027	dB
Stopband Attenuation (Note 40)		SA	75.1	-	-	dB
Group Delay (Note 41)		GD	-	4.7	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 40.0 kHz		FR	–3.80	-	+0.10	dB
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ Low power mode:						
Frequency Response: 0 to 40.0 kHz		FR	–5.26	-	+0.10	dB

Note 42. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2009 × fs (@–0.07/+0.027 dB), SB = 0.896 × fs. Each frequency response refers to that of 1 kHz.

8-17 Short Delay Slow Roll-Off Filter (fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; fs = 192 kHz; DASD bit = "1", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (LPF):						
Passband (Note 43)	−0.07 to +0.027 dB	PB	0	-	38.63	kHz
	−3.0 dB		-	81.57	-	kHz
Stopband (Note 43)		SB	172	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.027	dB
Stopband Attenuation (Note 40)		SA	75.1	-	-	dB
Group Delay (Note 41)		GD	-	4.7	-	1/fs
Digital Filter (LPF) + DACANA (Headphone Amplifier) @ High performance mode:						
Frequency Response: 0 to 80.0 kHz		FR	−5.90	-	+0.35	dB

Note 40. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 41. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

Note 43. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2012 × fs (@−0.07/+0.027 dB), SB = 0.896 × fs. Each frequency response refers to that of 1 kHz.

8-18 DSD Filter Characteristics

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V, VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; FS[4:0] bits = “01001”, DOP bit = “1”, DSDFS[1:0] bits = “00”)

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 45, Note 46)					
DSDF bit = “0” DSDD bit = “0”	20 kHz	-	−0.81	-	dB
	50 kHz	-	−6.01	-	dB
	100 kHz	-	−21.60	-	dB
DSDF bit = “1” DSDD bit = “0” or “1”	20 kHz	-	−0.25	-	dB
	100 kHz	-	−7.97	-	dB
	150 kHz	-	−20.31	-	dB

Note 44. The peak level of DSD signal should be in the range of 25% to 75% duty.

Note 45. The output level is assumed as 0 dB when applying a 1 kHz sine wave in 25 to 75% duty. Click noise may occur if the input signal exceeds 0 dB.

Note 46. The frequency (20 k, 50 k, 100 k and 150 kHz) will be doubled in case of DSDFS[1:0] bits = “01” and it will be quadrupled in case of DSDFS[1:0] bits = “10”.

8-19 DC Characteristics

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
I/O Pins (Note 47)					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage (Iout = −200 µA)	VOH	TVDD − 0.2	-	-	V
Low-Level Output Voltage					
LRCK pin, BCLK pin (Iout = 200 µA)	VOL	-	-	0.2	V
SDA pin					
2 V < TVDD ≤ 3.6 V (Iout = 3 mA)	VOL	-	-	0.4	V
1.65 V ≤ TVDD ≤ 2 V (Iout = 2 mA)	VOL	-	-	20%TVDD	V
Input Leakage Current	Iin	−5	-	+5	µA

Note 47. MCKI/XTI, BCLK, LRCK, SDATA, SCL, SDA, PDN, TESTI1, TESTI2 pins

8-20 Switching Characteristics

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; C_L = 80 pF; unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCKI					
Input Frequency	fMCK	0.256	-	49.152	MHz
Pulse Width Low	tMCKL	0.4 / fMCK	-	-	nsec
Pulse Width High	tMCKH	0.4 / fMCK	-	-	nsec
X'tal Oscillator (XTI pin)					
Input Frequency	fMCK	11.2896	-	24.576	MHz
Audio Interface Timing					
Master Mode					
LRCK Output Timing					
Frequency	fs	8	-	384	kHz
Duty	LRDuty	-	50	-	%
BCLK Output Timing					
Period (BCKO bit = "0")	tBCK	-	1/(64fs)	-	nsec
Period (BCKO bit = "1")	tBCK	-	1/(32fs)	-	nsec
Duty	BCKDuty	-	50	-	%
BCLK "↓" to LRCK Edge	tBLR	−10	-	10	nsec
SDATA Setup Time	tBDS	5	-	-	nsec
SDATA Hold Time	tBDH	5	-	-	nsec
Slave Mode					
LRCK Input Timing					
Frequency	fs	8	-	768	kHz
Duty	LRDuty	45	50	55	%
BCLK Input Timing					
Frequency (Note 48)	fBCK	0.256	-	49.152 or 512fs	MHz
Pulse Width Low	tBCKL	0.4 / fBCK	-	-	nsec
Pulse Width High	tBCKH	0.4 / fBCK	-	-	nsec
BCLK "↑" to LRCK Edge	tBLR	8	-	-	nsec
LRCK Edge to BCLK "↑"	tLRB	8	-	-	nsec
SDATA Setup Time	tBDS	5	-	-	nsec
SDATA Hold Time	tBDH	5	-	-	nsec

Note 48. The maximum value is lower frequency between "49.152 MHz" and "512fs".

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C-bus mode): (Note 49)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μsec
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μsec
Clock Low Time	tLOW	1.3	-	-	μsec
Clock High Time	tHIGH	0.6	-	-	μsec
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μsec
SDA Hold Time from SCL Falling (Note 50)	tHD:DAT	0	-	-	μsec
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μsec
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μsec
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μsec
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μsec
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	nsec
Power-Down & Reset Timing					
PDN Accept Pulse Width (Note 51)	tPDN	1	-	-	msec
PDN Reject Pulse Width (Note 51)	tRPD	-	-	50	nsec

Note 49. I^2C-bus is a registered trademark of NXP B.V.

Note 50. Data must be held long enough to bridge the 300 nsec-transition time of SCL.

Note 51. The AK4377 will be reset by bringing the PDN pin = “L”. The PDN pin must held “L” for longer period than or equal to tPDN period. The AK4377 will not be reset by the “L” pulse shorter than or equal to 50 nsec.

8-21 Timing Diagram (System Clock)

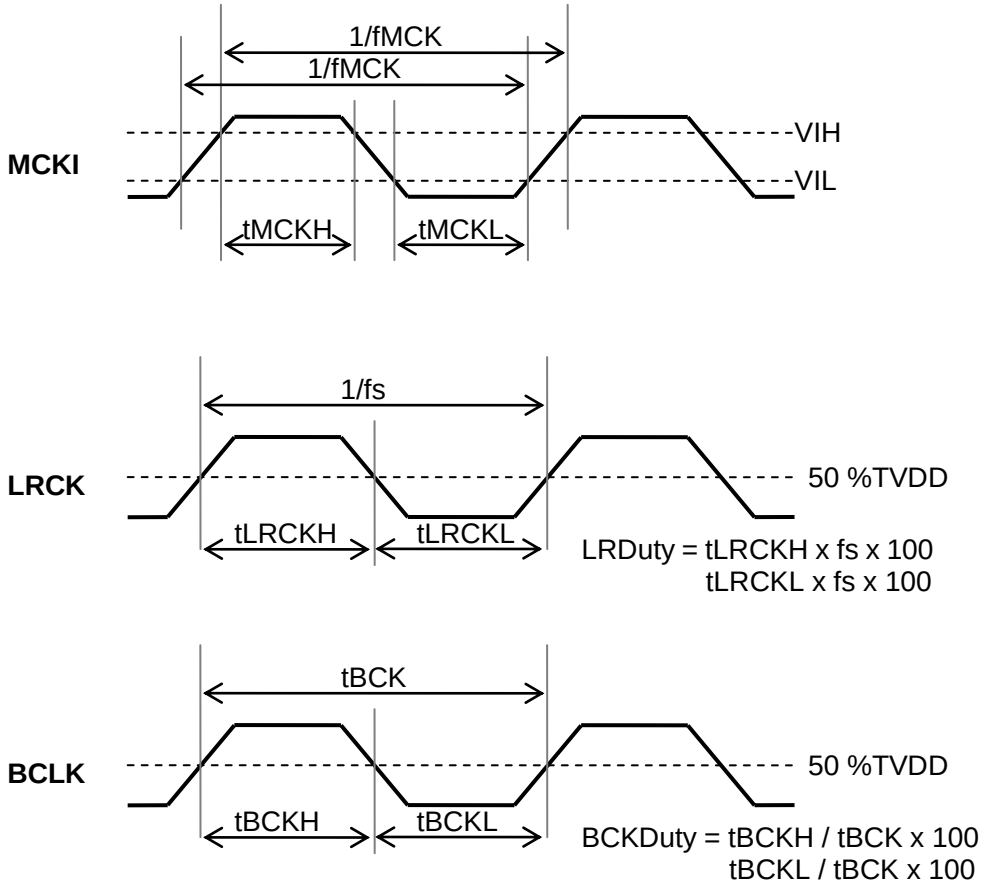


Figure 2. System Clock (Master Mode)

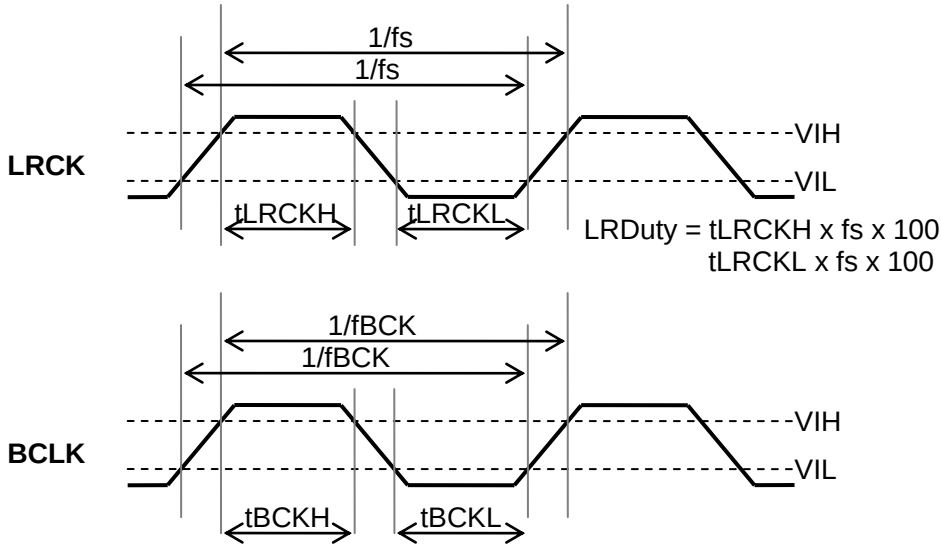


Figure 3. System Clock (Slave Mode)

8-22 Timing Diagram (Serial Audio Interface)

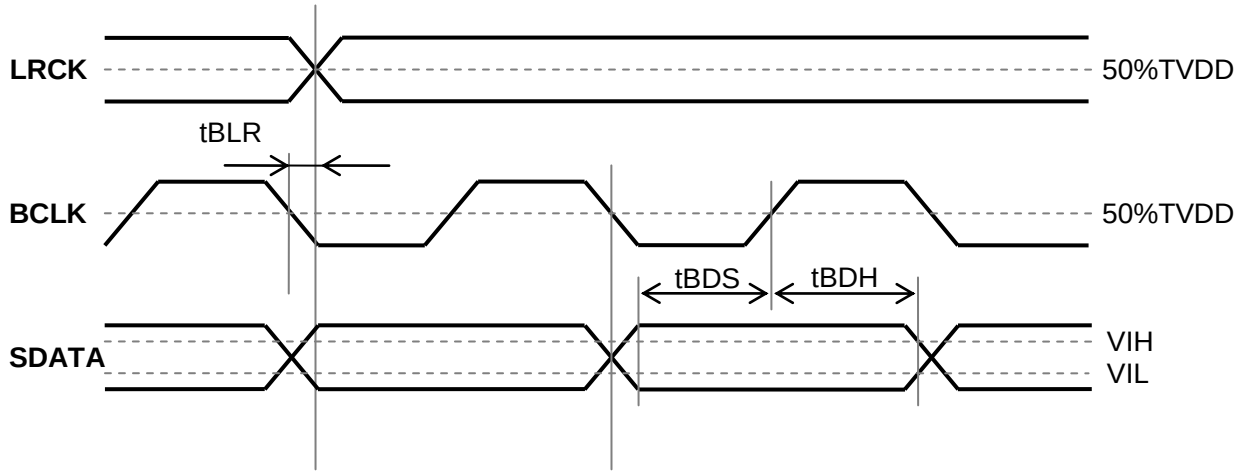


Figure 4. Serial Audio Interface (Master Mode)

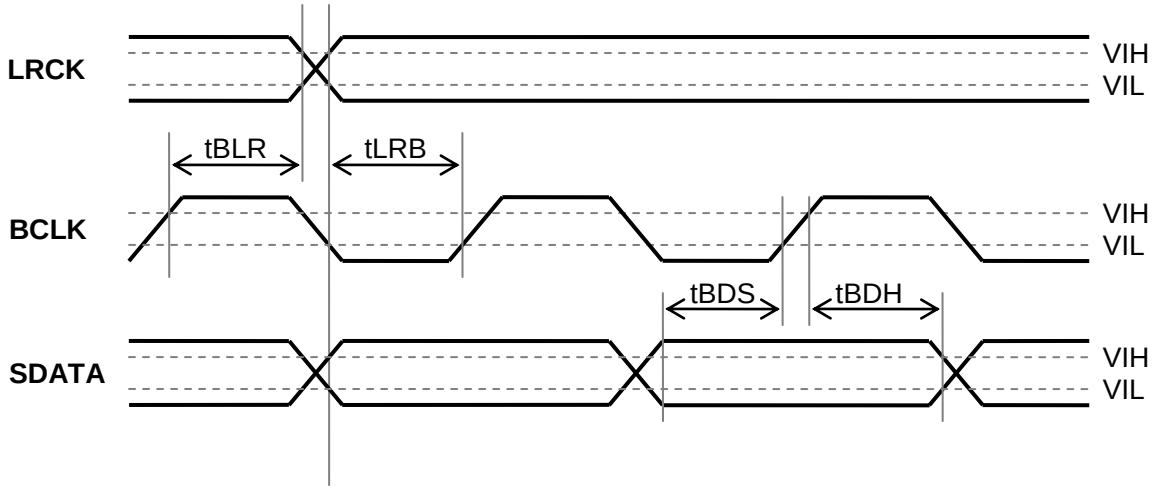


Figure 5. Serial Audio Interface (Slave Mode)

8-23 Timing Diagram (I^2C-bus Interface)

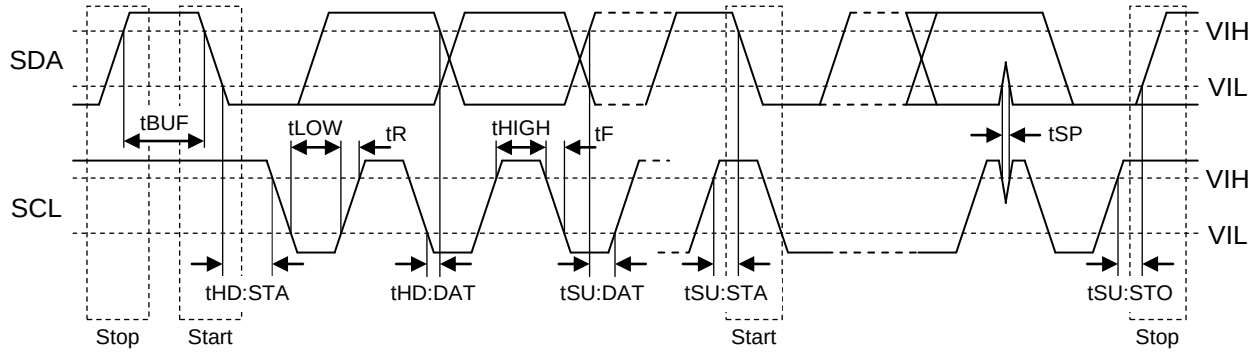


Figure 6. I^2C-bus Mode Timing

8-24 Timing Diagram (Reset)

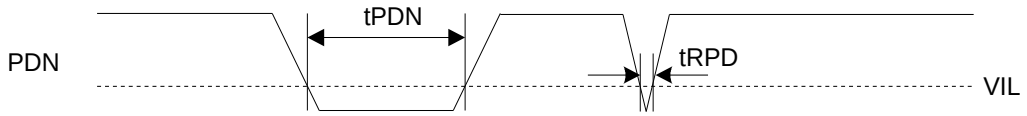


Figure 7. Power Down and Standby

9. Functional Descriptions

9-1 System Clock

The AK4377 is operated by a clock generated by PLL or an externally input clock or X'tal oscillator (MCKI/XTI pin). DACCKS bit select the clock source of the DAC (Table 1). PLL clock source is selected from external MCKI, the clock by X'tal oscillator or BCLK (Table 7). Master clock frequency and sampling frequency are set by CM[1:0] bits and FS[4:0] bits, respectively. PMDA, PMHPL and PMHPR bits must be set to "0" when changing these frequencies.

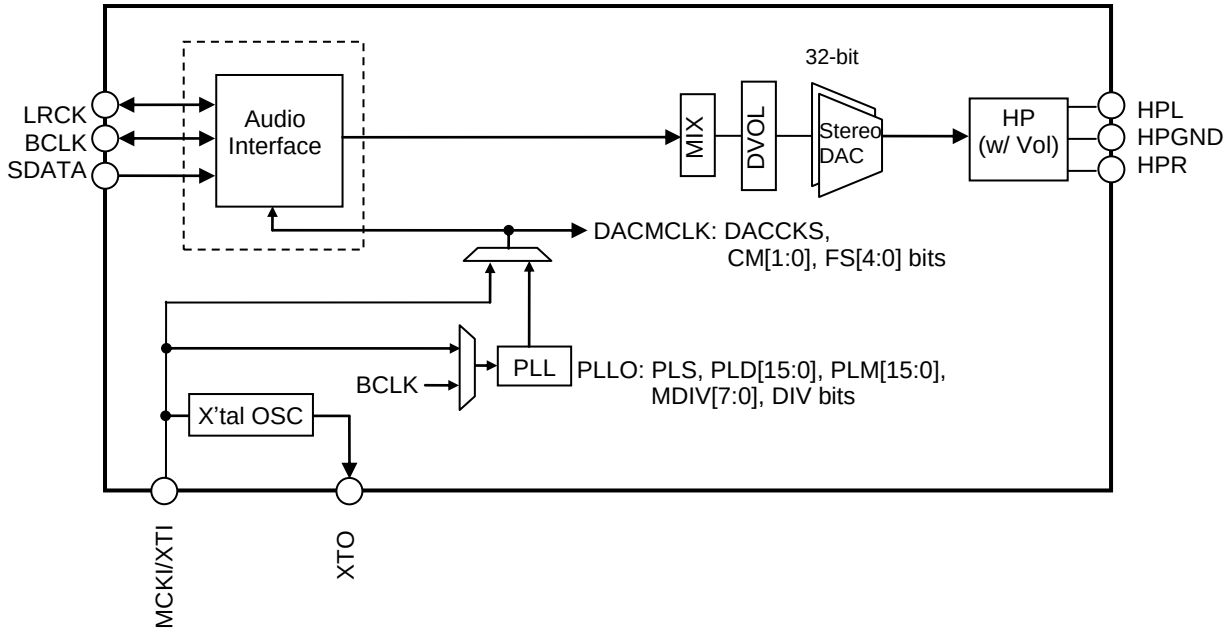


Figure 8. Clock & Data Flow

Table 1. DAC Master Clock Source Select

DACCKS bit	DAC Master Clock	
0	MCKI/XTI pin	(default)
1	PLLO	

The AK4377 can be operated in both Master and Slave modes. Clock mode of LRCK pin and BCLK pin can be selected by MS bit. When using Master mode, the LRCK pin and the BCLK pin should be pulled down or pulled up with an external resistor (about 100 kΩ) because both pins are floating state until MS bit becomes “1”.

Table 2. Master/Slave Mode Select

MS bit	LRCK pin, BCLK pin	
0	Slave Mode	(default)
1	Master Mode	

Master/Slave mode switching is not allowed while the AK4377 is in normal operation. The DAC and the headphone amplifier must be powered down before Master/Slave mode is switched. Furthermore PLL and the charge pump must also be powered down in case that sampling frequency is changed or PLLCLK is stopped.

<MS bit Setting Sequence Example>

1. DAC, Headphone Amplifier (PLL, Charge Pump) Power-down
2. Clock Mode of ACPU Setting (In case clock mode of ACPU is Master, switch to Slave.)
3. MS bit Selection
4. Clock Mode of ACPU Setting (In case clock mode of ACPU is Slave, switch to Master.)
5. DAC, Headphone Amplifier (PLL, Charge Pump) Power-up

Figure 9 shows clock & data flow in Slave mode. Figure 10 shows clock & data flow in Master mode.

< Salve Mode >
MS bit = “0”, PMPLL bit = “0”, DACCKS bit = “0”

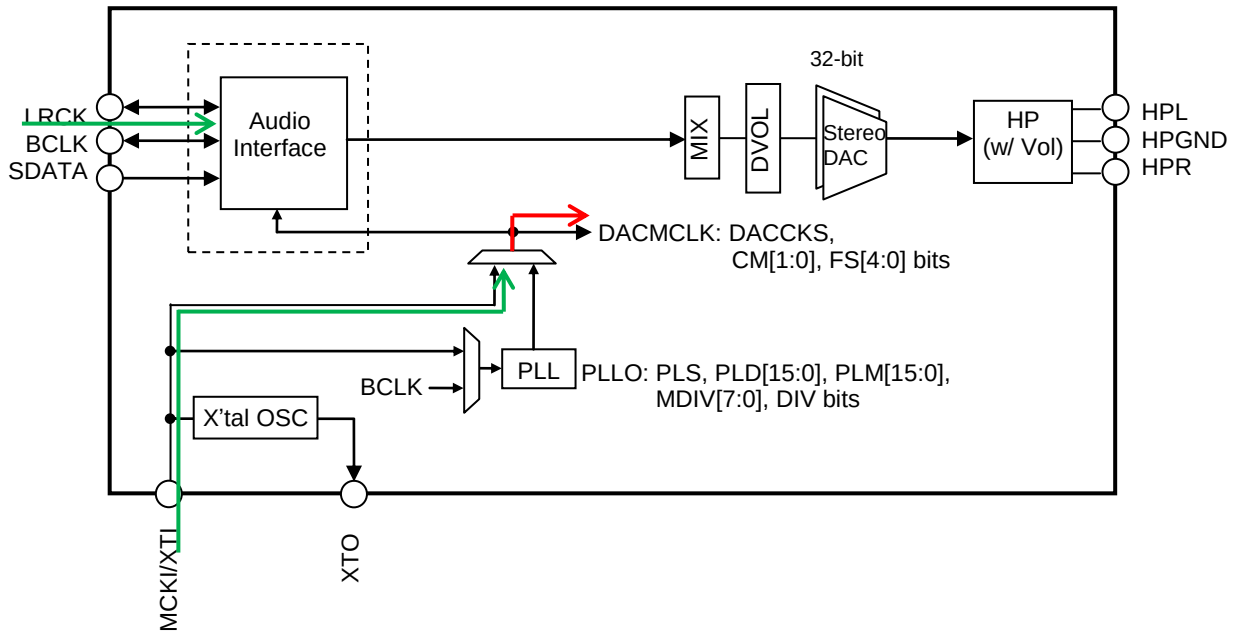


Figure 9. Example of Clock and Data Flow (Slave Mode, Not using PLL)

< Master Mode >
MS bit = “1”, PMPLL bit = “1”, PLS bit = “0”, DACCKS bit = “1”

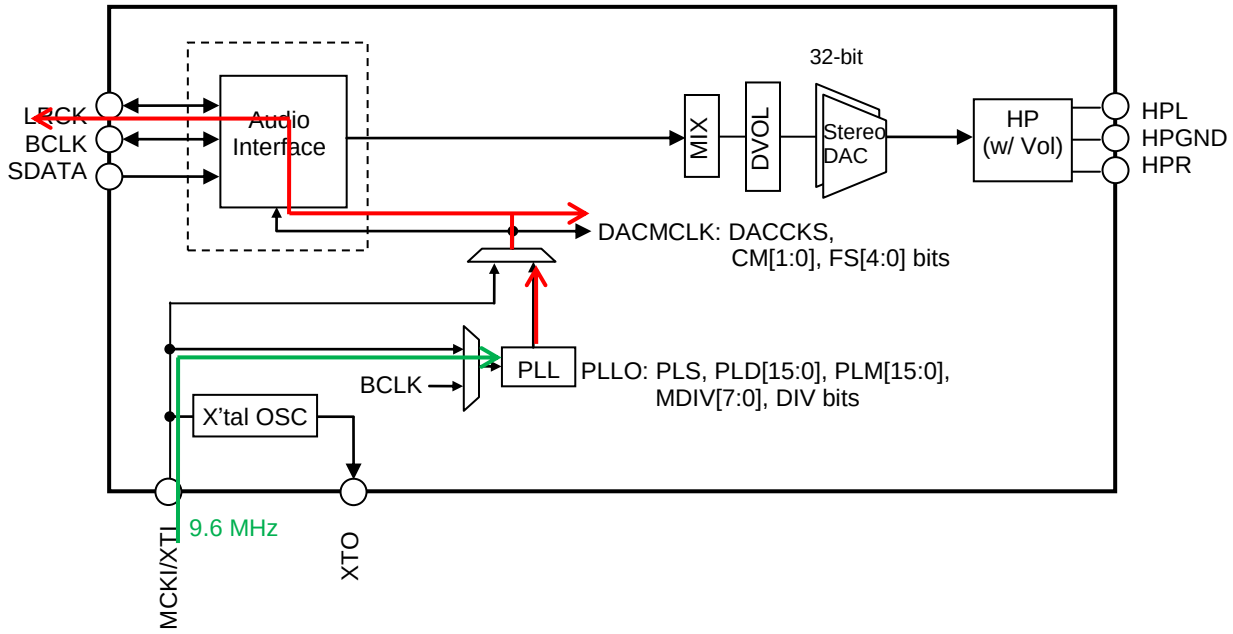


Figure 10. Example of Clock and Data Flow (Master Mode, Using PLL)

<High Performance Mode: LPMODE bit = "0">

Table 3. Setting of Master Clock Frequency (High Performance Mode) (x: Do not Care)

DSMLP bit	CM1 bit	CM0 bit	Master Clock Frequency	Sampling Frequency Range	
1	0	0	256fs	8 to 12 kHz	
0	0	0	256fs	16 to 192 kHz	
			32fs	256 to 768 kHz (Note 52)(Note 53)	(default)
0	0	1	512fs	8 to 96 kHz	
			64fs	256 to 768 kHz (Note 52)	
0	1	x	1024fs	8 to 48 kHz	

Note 52. Hex Speed Mode (fs = 512 to 768 kHz) is only supported in Slave Mode.

Note 53. The AK4377 operates correctly in master mode only if BCKO bit = "0" (BCLK Frequency = 32fs) and DL[1:0] bits = "01" (Data Length = 16-bit Linear).

<Low Power Mode: LPMODE bit = "1">

Table 4. Setting of Master Clock Frequency (Low Power Mode) (x: Do not Care)

DSMLP bit	CM1 bit	CM0 bit	Master Clock Frequency	Sampling Frequency Range	
1	0	0	256fs	8 to 96 kHz	(default)
1	0	1	512fs	8 to 96 kHz	
1	1	x	1024fs	8 to 48 kHz	

Note 54. Quad / Oct / Hex Speed Mode (fs = 128 to 768 kHz) is not supported in Low Power Mode.

Table 5. Setting of Sampling Frequency (N/A: Not available)

FS4 bit	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8 kHz	(default)
0	0	0	0	1	11.025 kHz	
0	0	0	1	0	12 kHz	
0	0	1	0	0	16 kHz	
0	0	1	0	1	22.05 kHz	
0	0	1	1	0	24 kHz	
0	1	0	0	0	32 kHz	
0	1	0	0	1	44.1 kHz	
0	1	0	1	0	48 kHz	
0	1	1	0	0	64 kHz	
0	1	1	0	1	88.2 kHz	
0	1	1	1	0	96 kHz	
1	0	0	0	0	128 kHz	
1	0	0	0	1	176.4 kHz	
1	0	0	1	0	192 kHz	
1	0	1	0	0	256 kHz	
1	0	1	0	1	352.8 kHz	
1	0	1	1	0	384 kHz	
1	1	0	0	0	512 kHz	
1	1	0	0	1	705.6 kHz	
1	1	0	1	0	768 kHz	
Others					N/A	

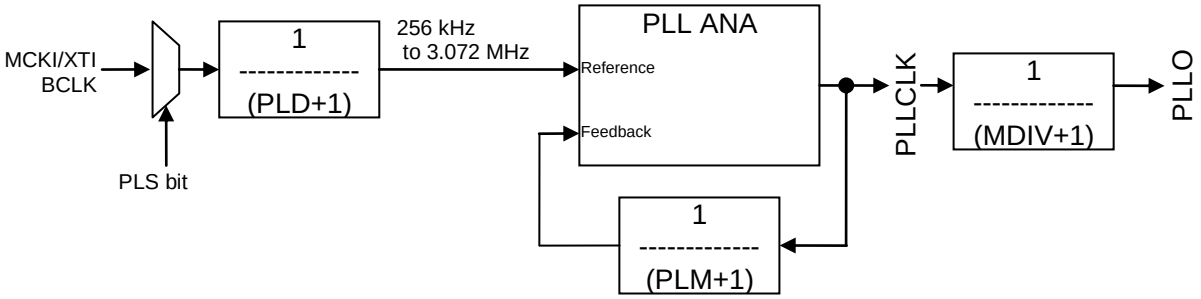
* Depending on the PLL divider setting, the sampling frequency may differ. Please set PLD[15:0] and PLM[15:0] bits precisely.

9-2 PLL

The PLL generates a PLLO which is used as the DAC operation clock DACMCLK. The oscillation frequency PLLCLK should be set in the range from 101.6064 to 122.88 MHz (Table 6 shows setting example of 48 kHz and 44.1 kHz base rates). Refer to Table 11 and Table 12 for PLL setting examples. Reference clock of PLL should be set in the range from 256 kHz to 3.072 MHz.

Table 6. PLLCLK Setting Example

	48 kHz base rate	44.1 kHz base rate
2560fs	122.88 MHz	112.896 MHz
2304fs	110.592 MHz	101.6064 MHz



Reference clock = PLL Source / (PLD + 1)
PLLCLK = Reference clock x (PLM + 1)
PLLO = PLLCLK / (MDIV + 1)

Figure 11. PLL Block Diagram

9-2-1 Input Clock Select Function

The PLL has a function that selects the input clock. The clock source pin is selected by PLS bit.

Table 7. PLL Clock Source Select

PLS bit	Clock Source	
0	MCKI/XTI pin	(default)
1	BCLK pin	

9-2-2 PLL Reference Clock Divider

The PLL can set the dividing number of the reference clock in 16-bit. The input clock is used as PLL reference clock by dividing by (PLD + 1).

Table 8. PLL Reference Clock Divider

PLD[15:0] bits	Dividing Number	
0000H	1	(default)
0001H to FFFFH	1 / (PLD + 1)	

Note 55. The reference clock divided by PLD should be set in the range from 256 kHz to 3.072 MHz.

9-2-3 PLL Feedback Clock Divider

The dividing number of feedback clock can be set freely in 16-bit. PLLCLK is divided by (PLM + 1) and used as PLL feedback clock. The feedback clock is fixed to “L” without dividing when PLM[15:0] bits = 0000H.

Table 9. PLL Feedback Clock Divider

PLM[15:0] bits	Dividing Number	
0000H	Clock Stop	(default)
0001H to FFFFH	1 / (PLM + 1)	

9-2-4 Power Management (PMPLL)

PLL can be powered down by a control register setting.

Table 10. PLL Power Control

PMPLL bit	PLL Status	
0	Power-Down	(default)
1	Power-Up	

< PLL Power-Up Sequence Example >
1. PLL Clock Source, Reference Clock Divider, Feedback Clock Divider and DACMCLK Generating Divider Settings
2. PLL Power-Up (PMPLL bit: “0” → “1”)
3. Wait 2 msec
4. PLLO Frequency is Stable

9-2-5 PLL Setting Examples

Table 11. PLL Setting Example (PLL reference source: MCKI)

CLKIN		PLL condition			PLLCLK		
Source	Frequency [Hz]	D+1	REFCLK [Hz]	M+1	Base Rate [Hz]	[fs]	[Hz]
MCKI	9,600,000	5	1,920,000	64	48,000	2,560	122,880,000
	19,200,000	10	1,920,000	64		2,560	122,880,000
	12,288,000	4	3,072,000	40		2,560	122,880,000
	24,576,000	8	3,072,000	40		2,560	122,880,000
	12,000,000	25	480,000	256		2,560	122,880,000
	24,000,000	25	960,000	128		2,560	122,880,000
	9,600,000	25	384,000	294	44,100	2,560	112,896,000
	19,200,000	25	768,000	147		2,560	112,896,000
	11,289,600	4	2,822,400	40		2,560	112,896,000
	22,579,200	8	2,822,400	40		2,560	112,896,000

Table 12. PLL Setting Example (PLL reference source: BCLK)

CLKIN			PLL condition			PLLCLK		
Source	Sampling Frequency[Hz]	Frequency [Hz]	D+1	REFCLK [Hz]	M+1	Base Rate [Hz]	[fs]	[Hz]
BCLK (32fs)	8,000	256,000	1	256,000	480	48,000	2,560	122,880,000
	11,025	352,800	1	352,800	320	44,100	2,560	112,896,000
	16,000	512,000	1	512,000	240	48,000	2,560	122,880,000
	22,050	705,600	1	705,600	160	44,100	2,560	112,896,000
	24,000	768,000	1	768,000	160	48,000	2,560	122,880,000
	32,000	1,024,000	1	1,024,000	120	48,000	2,560	122,880,000
	44,100	1,411,200	1	1,411,200	80	44,100	2,560	112,896,000
	48,000	1,536,000	1	1,536,000	80	48,000	2,560	122,880,000
BCLK (48fs)	8,000	384,000	1	384,000	320	48,000	2,560	122,880,000
	11,025	529,200	1	529,200	192	44,100	2,304	101,606,400
	16,000	768,000	1	768,000	160	48,000	2,560	122,880,000
	22,050	1,058,400	3	352,800	320	44,100	2,560	112,896,000
	24,000	1,152,000	3	384,000	320	48,000	2,560	122,880,000
	32,000	1,536,000	1	1,536,000	80	48,000	2,560	122,880,000
	44,100	2,116,800	3	705,600	160	44,100	2,560	112,896,000
	48,000	2,304,000	3	768,000	160	48,000	2,560	122,880,000
BCLK (64fs)	8,000	512,000	1	512,000	240	48,000	2,560	122,880,000
	11,025	705,600	1	705,600	160	44,100	2,560	112,896,000
	16,000	1,024,000	1	1,024,000	120	48,000	2,560	122,880,000
	22,050	1,411,200	1	1,411,200	80	44,100	2,560	112,896,000
	24,000	1,536,000	1	1,536,000	80	48,000	2,560	122,880,000
	32,000	2,048,000	1	2,048,000	60	48,000	2,560	122,880,000
	44,100	2,822,400	1	2,822,400	40	44,100	2,560	112,896,000
	48,000	3,072,000	1	3,072,000	40	48,000	2,560	122,880,000

9-2-6 DACMCLK Generating Divider Setting

MDIV[7:0] bits control DACMCLK divider.
Set MDIV[7:0] bits = 4H (dividing by 5) and DIV bit = “1” when supplying a 45.1584 MHz or 49.152 MHz clock to DACMCLK.

Table 13. DACMCLK Divider Setting

DIV bit	MDIV[7:0] bits	Dividing Number	
0	00H	1	(default)
0	01H to FFH	1 / (MDIV + 1)	
1	04H	1 / 2.5	

9-3 Crystal Oscillator

The clock for the MCKI/XTI pin can be generated by two methods. PMOSC bit must be set to “1” when using a crystal oscillator.

1) X’tal Mode (PMOSC bit = “1”)

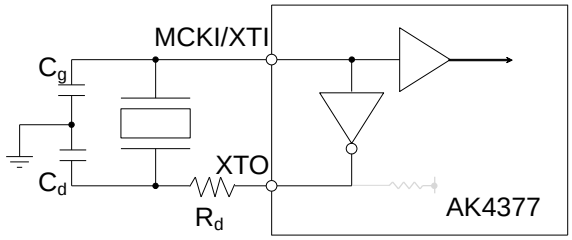


Figure 12. X’tal Mode

Note 56. The capacitor value is dependent on the crystal resonator.
$C_d = C_g$ = 20.0 pF (Max.), Rl (Equivalent Series Resistance) = 80Ω (Max.) @ 24.576 MHz
$C_d = C_g$ = 21.5 pF (Max.), Rl (Equivalent Series Resistance) = 60Ω (Max.) @ 19.2 MHz
$C_d = C_g$ = 30.6 pF (Max.), Rl (Equivalent Series Resistance) = 200Ω (Max.) @ 11.2896 MHz

Note 57. Damping resistor “R_d” is necessary when TVDD is 2.0 V or more.
R_d = 1.5 kΩ @ 24.576 MHz, RI = 80Ω (Max.)
R_d = 1.8 kΩ @ 19.2 MHz, RI = 60Ω (Max.)
R_d = 1.8 kΩ @ 11.2896 MHz, RI = 200Ω (Max.)

2) External Clock Mode (PMOSC bit = “0”)

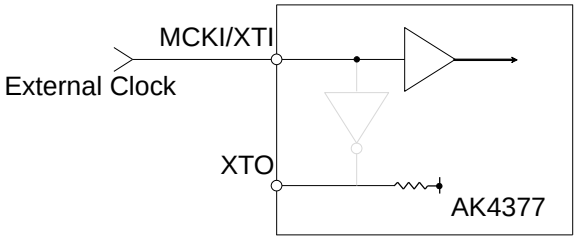


Figure 13. External Clock Mode

Note 58. Do not input a clock more than TVDD.

3) OFF Mode (Not Using MCKI/XTI pin and XTO pin (PMOSC bit = “0”))

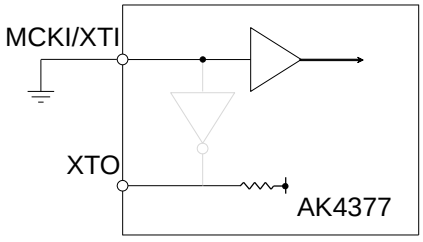


Figure 14. OFF Mode

9-4 DAC Digital Filter

The AK4377 has four types of digital filter. The filter mode of DAC can be selected by DASD and DASL bits. The default setting is DASL bit = DASD bit = "0" (Sharp Roll-Off Filter).

Table 14. DAC Digital Filter Setting

DASD bit	DASL bit	DAC Filter Mode Setting	
0	0	Sharp Roll-Off Filter	(default)
0	1	Slow Roll-Off Filter	
1	0	Short Delay Sharp Roll-Off Filter	
1	1	Short Delay Slow Roll-Off Filter	

9-5 Digital Mixing

The AK4377 has digital mixing circuits for each L channel and R channel. They can mix the data digitally and convert the polarity. The inverted data by this polarity conversion is calculated in 2's complement format.

Table 15. DAC L/R Channel Input Signal Select

MDACL bit MDACR bit	RDACL bit RDACR bit	LDACL bit LDACR bit	DAC Lch Input Data DAC Rch Input Data	
0	0	0	MUTE	(default)
0	0	1	Lch	
0	1	0	Rch	
0	1	1	Lch + Rch	
1	0	0	MUTE	
1	0	1	Lch / 2	
1	1	0	Rch / 2	
1	1	1	(Lch + Rch) / 2	

Table 16. DAC L/R Channel Input Signal Polarity Select

INVL bit INVR bit	Output Data	
0	Normal	(default)
1	Inverting	

9-6 Digital Volume

The AK4377 has a 64-level digital volume in front of DAC for each L and R channel. The volume is changed from +3 dB to −28 dB in 0.5 dB step including Mute. The volume change is executed immediately by setting registers. A pop noise may occur if changing the volume when PMDA bit = “1”.

When OVOLCN bit is “1”, the OVL[5:0] bits control L channel level and OVR[5:0] bits control R channel level. When OVOLCN bit = “0”, the OVL[5:0] bits control both L channel and R channel volume levels. In this case, the setting of OVR[5:0] bits is ignored.

Digital volume function is not available in Oct and Hex Speed Mode (fs = 256 to 768 kHz).

Table 17. Digital Volume Setting (default = 39H, 0 dB)

OVL[5:0] bits OVR[5:0] bits	Volume (dB)	OVL[5:0] bits OVR[5:0] bits	Volume (dB)
3FH	+3	1FH	−13
3EH	+2.5	1EH	−13.5
3DH	+2	1DH	−14
3CH	+1.5	1CH	−14.5
3BH	+1	1BH	−15
3AH	+0.5	1AH	−15.5
39H (default)	0	19H	−16
38H	−0.5	18H	−16.5
37H	−1	17H	−17
36H	−1.5	16H	−17.5
35H	−2	15H	−18
34H	−2.5	14H	−18.5
33H	−3	13H	−19
32H	−3.5	12H	−19.5
31H	−4	11H	−20
30H	−4.5	10H	−20.5
2FH	−5	0FH	−21
2EH	−5.5	0EH	−21.5
2DH	−6	0DH	−22
2CH	−6.5	0CH	−22.5
2BH	−7	0BH	−23
2AH	−7.5	0AH	−23.5
29H	−8	09H	−24
28H	−8.5	08H	−24.5
27H	−9	07H	−25
26H	−9.5	06H	−25.5
25H	−10	05H	−26
24H	−10.5	04H	−26.5
23H	−11	03H	−27
22H	−11.5	02H	−27.5
21H	−12	01H	−28
20H	−12.5	00H	MUTE

9-7 Headphone Amplifier Output (HPL/HPR pins)

Headphone amplifiers are operated by positive and negative power that is supplied from internal charge pump circuit. The VEE2 pin outputs the negative voltage generated by the internal charge pump circuit from CVDD. This charge pump circuit is switched between VDD mode and 1/2VDD mode by the output level of the headphone amplifiers. The headphone amplifier output is single-ended and centered on HPGND (0 V). Therefore, a capacitor for AC-coupling is not necessary. The minimum load resistance is 7.2Ω. The output power is 10 mW (@ 0 dBFS, R_L = 32Ω, AVDD = CVDD = 1.8 V and HPG = –4 dB) and 25 mW (@ 0 dBFS, R_L = 32Ω, AVDD = CVDD = 1.8 V and HPG = 0 dB). Ground loop noise cancelling function for headphone amplifier is available by connecting the HPGND pin to the ground of the jack.

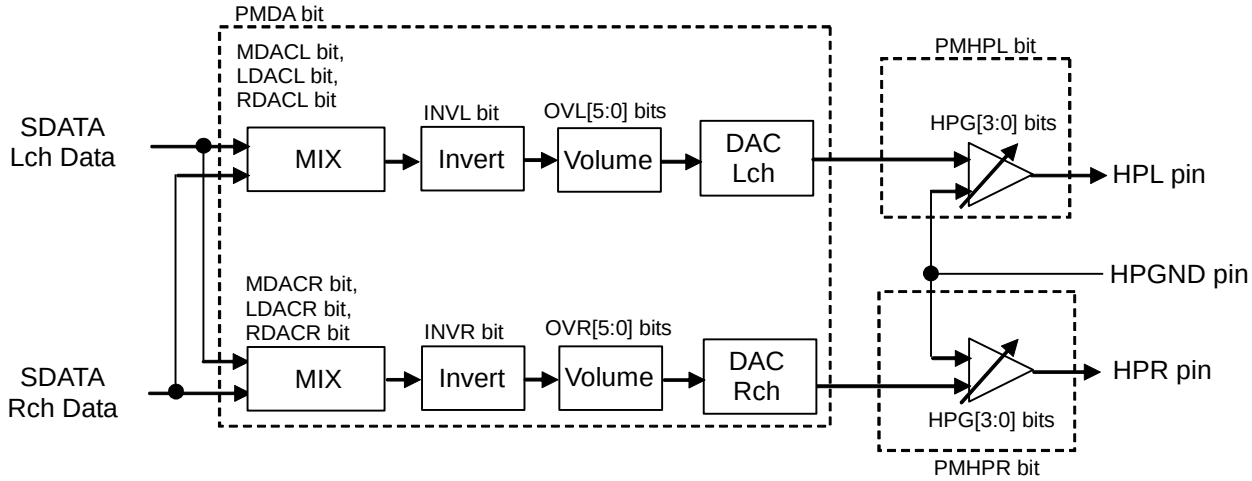


Figure 15. DAC & Headphone Amplifier Block Diagram

Table 18. Charge Pump Mode Setting (N/A: Not available)

CPMODE1 bit	CPMODE0 bit	Mode	Operation Voltage	
0	0	Class-G Operation Mode	Automatic Switching	(default)
0	1	±VDD Operation Mode	±VDD	
1	0	±1/2VDD Operation Mode	±1/2VDD	
1	1	N/A	N/A	

The charge pump mode is fixed to VDD mode regardless of CPMODE[1:0] bits setting in DSD mode (DOP bit = “1”).

< Class-G Mode Switching Level >

A switching threshold level of VDD and 1/2VDD modes can be set by LVDSEL bit. LVDSEL bit should be set before PMHPL bit or PMHPR bit is set to "1".

LVDSEL bit = "0" (default: Assuming connecting a 32Ω headphone or more**)**
VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V, R_L = 32Ω)
1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V, R_L = 32Ω)

LVDSEL bit = "1" (Assuming connecting a 16Ω headphone or when the impedance cannot be detected**)**
VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V, R_L = 16Ω)
1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V, R_L = 16Ω)

Do not use 1/2VDD mode when using a headphone under 16Ω. In this case, CPMODE[1:0] bits should be set to "01".

When the charge pump operation mode is changed to VDD mode from 1/2VDD mode, an internal counter for holding VDD mode starts (Table 19). The charge pump changes to 1/2VDD mode if the output signal level is lower than the switching level and 1/2VDD mode detection time that is set by LVDTM[2:0] bits is passed after VDD mode hold time is finished.

Table 19. VDD Mode Holding Period Setting (x: Do not Care)

VDDTM[3:0] bits		VDD Mode Holding Period				
		8 kHz	44.1 kHz	96 kHz	192 kHz	
0000	1024/fs	128 msec	23.2 msec	10.7 msec	5.3 msec	(default)
0001	2048/fs	256 msec	46.4 msec	21.3 msec	10.7 msec	
0010	4096/fs	512 msec	92.9 msec	42.7 msec	21.3 msec	
0011	8192/fs	1024 msec	186 msec	85.3 msec	42.7 msec	
0100	16384/fs	2048 msec	372 msec	170.7 msec	85.3 msec	
0101	32768/fs	4096 msec	743 msec	341.3 msec	170.7 msec	
0110	65536/fs	8192 msec	1486 msec	682.7 msec	341.3 msec	
0111	131072/fs	16384 msec	2972 msec	1365.3 msec	682.7 msec	
1xxx	262144/fs	32768 msec	5944 msec	2730.7 msec	1365.3 msec	

Note 59. Oct Speed Mode (fs = 256 k / 352.8 k / 384 kHz) has the same cycle as fs = 32 k / 44.1 k / 48 kHz.
Hex Speed Mode (fs = 512 k / 705.6 k / 768 kHz) has the same cycle as fs = 64 k / 88.2 k / 96 kHz.

When the output voltage becomes less than class-G mode switching level, the internal detection counter for 1/2VDD mode which is set by LVDTM[2:0] bits starts. This counter is reset when the output voltage exceeds class-G mode switching level. The charge pump operation mode is changed to VDD from 1/2VDD if the detection counter of 1/2VDD mode is finished and also the VDD mode hold period is passed.

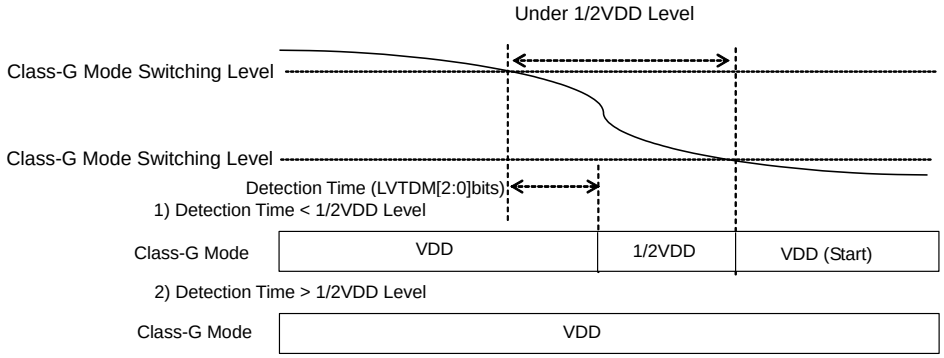


Figure 16. Transition to 1/2VDD Mode from VDD Mode

Table 20. 1/2VDD Detection Period (Minimum frequency that is not detected)

LVDTM[2:0] bits		1/2VDD Mode Detection Time/ Minimum Frequency that is Not Detected				
		8 kHz	44.1 kHz	96 kHz	192 kHz	
000	64/fs	8 msec	1.5 msec	0.67 msec	0.33 msec	(default)
		62.5 Hz	344.5 Hz	750 Hz	1500 Hz	
001	128/fs	16 msec	2.9 msec	1.3 msec	0.67 msec	
		31.3 Hz	172.3 Hz	375 Hz	750 Hz	
010	256/fs	32 msec	5.8 msec	2.7 msec	1.3 msec	
		15.6 Hz	86.1 Hz	187.5 Hz	375 Hz	
011	512/fs	64 msec	11.6 msec	5.3 msec	2.7 msec	
		7.8 Hz	43.1 Hz	93.8 Hz	187.5 Hz	
100	1024/fs	128 msec	23.2 msec	10.7 msec	5.3 msec	
		3.9 Hz	21.5 Hz	46.9 Hz	93.8 Hz	
101	2048/fs	256 msec	46.4 msec	21.3 msec	10.7 msec	
		2.0 Hz	10.8 Hz	23.4 Hz	46.9 Hz	
110	4096/fs	512 msec	92.9 msec	42.7 msec	21.3 msec	
		1.0 Hz	5.4 Hz	11.7 Hz	23.4 Hz	
111	8192/fs	1024 msec	185.8 msec	92.9 msec	42.7 msec	
		0.5 Hz	2.7 Hz	5.9 Hz	11.7 Hz	

Note 60. Oct Speed Mode (fs = 256 k / 352.8 k / 384 kHz) has the same cycle as fs = 32 k / 44.1 k / 48 kHz.
Hex Speed Mode (fs = 512 k / 705.6 k / 768 kHz) has the same cycle as fs = 64 k / 88.2 k / 96 kHz.

< Headphone Amplifier Volume Circuit >

The output level of headphone amplifier can be controlled by HPG[3:0] bits. The volume setting is common for both L and R channels and ranges from +4 dB to −20 dB (Table 21). When the volume is changed, zero cross detection is executed independently on L and R channels. Zero crossing timeout period is set by HPTM[2:0] bits (Table 23).
Zero cross detection will not be executed when ZCDIS bit = "1".
The headphone amplifier volume should be changed with an interval of zero cross timeout period after setting HPG[3:0] bits once. If the volume is changed continuously without the interval, the gain setting at the next zero crossing point will be applied.

Zero cross detection is not available in DSD mode (DOP bit = "1"). ZCDIS bit must be set to "1".

Table 21. Headphone Amplifier Volume Setting (N/A: Not available)

HPG[3:0] bits	Volume (dB)	
FH	N/A	
EH	+4	
DH	+2	
CH	+1	
BH	0	(default)
AH	−2	
9H	−4	
8H	−6	
7H	−8	
6H	−10	
5H	−12	
4H	−14	
3H	−16	
2H	−18	
1H	−20	
0H	MUTE	

Table 22. Zero Cross Detection Setting

ZCDIS bit	Zero Cross Detection Setting	
0	Enable	(default)
1	Disable	

Table 23. Headphone Amplifier Zero Crossing Timeout Period Setting

HPTM[2:0] bits		Zero Crossing Timeout Period				
		8 kHz	44.1 kHz	96 kHz	192 kHz	
000	128/fs	16 msec	2.9 msec	1.3 msec	0.67 msec	
001	256/fs	32 msec	5.8 msec	2.7 msec	1.3 msec	
010	512/fs	64 msec	11.6 msec	5.3 msec	2.7 msec	
011	1024/fs	128 msec	23.2 msec	10.7 msec	5.3 msec	(default)
100	2048/fs	256 msec	46.4 msec	21.3 msec	10.7 msec	
101	4096/fs	512 msec	92.9 msec	42.7 msec	21.3 msec	
110	8192/fs	1024 msec	185.8 msec	85.3 msec	42.7 msec	
111	16384/fs	2048 msec	371.5 msec	170.7 msec	85.3 msec	

Note 61. Oct Speed Mode (fs = 256 k / 352.8 k / 384 kHz) has the same cycle as fs = 32 k / 44.1 k / 48 kHz.
Hex Speed Mode (fs = 512 k / 705.6 k / 768 kHz) has the same cycle as fs = 64 k / 88.2 k / 96 kHz.

< Headphone Amplifier External Circuit >

It is necessary to put an oscillation prevention circuit (0.1 μF ±20% capacitor and 10Ω ±20% resistor) because there is a possibility that the headphone amplifier oscillates.

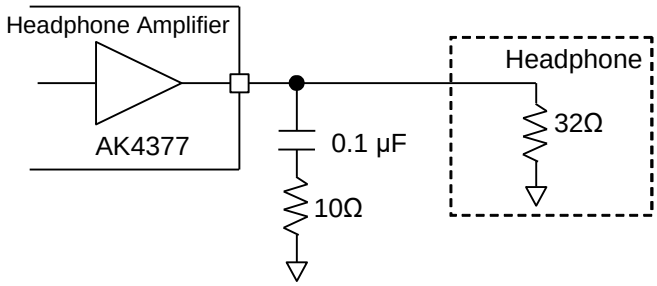


Figure 17. Example of Headphone Amplifier Oscillation Prevention Circuit

< Power-Up/Down Sequence of Headphone Amplifier >

After releasing DAC power-down state by PMDA bit, the headphone amplifier should be powered up by PMHPL/R bits. A wait time from DAC power-up to headphone power-up is not necessary.
PMDA bit releases a power-down of the digital block of the DAC, PMHPL bit or PMHPR bit powers up the analog block of the DAC and the headphone amplifier. Then, initialization cycle of the headphone amplifier is executed. The gain setting (HPG[3:0] bits) should be made before PMHPL bit or PMHPR bit is set to "1". Do not change the gain setting (HPG[3:0] bits) during the headphone initialization cycle. The gain setting can be changed after the headphone initialization cycle is finished. A wait time from the gain setting to PMHPL bit or PMHPR bit = "1" is not necessary.

When the AK4377 is powered down, the headphone amplifier should be powered down first. The DAC should be powered down next. A wait time from a headphone power-down to the DAC power-down is not necessary.
When the headphone amplifier is powered down, the HPL pin and HPR pin are pulled down to HPGND via the internal pull-down register. The pull-down resistor is 9Ω (Typ.) @HPLHZ bit = HPRHZ bit = "0". The HPL pin and HPR pin are also pulled down to HPGND via 117 kΩ (Typ.) if HPLHZ bit and HPRHZ bit are set to "1" while CP1, CP2, LDO1P, LDO1N1N and LDO1N2 are powered up. These bits must be set to "0" before power-up the headphone amplifier.

Table 24. Headphone L Channel Output Status (N/A: Not available)

PMHPL bit	HPLHZ bit	Headphone Amplifier Status
0	0	Pull-Down by 9Ω (Typ.)
0	1	Pull-Down by 117 kΩ (Typ.)
1	0	Normal Operation
1	1	N/A

Table 25. Headphone R Channel Output Status (N/A: Not available)

PMHPR bit	HPRHZ bit	Headphone Amplifier Status
0	0	Pull-Down by 9Ω (Typ.)
0	1	Pull-Down by 117 kΩ (Typ.)
1	0	Normal Operation
1	1	N/A

When the HPL pin and the HPR pin are connected to analog signal pins of an external device by Wire-OR, CP1, CP2, LDO1P, LDO1N1 and LDO1N2 should be powered up. Do not input a negative voltage to the HPL pin and HPR pin when the headphone amplifier is powered down by 117 kΩ (Typ.) pull-down and CP1, CP2, LDO1P, LDO1N1 and LDO1N2 are also powered down.

If the pop noise at power-down exceeds an acceptable range, headphone amplifier should be powered down after attenuating the headphone volume gradually until mute.

The power-up time of headphone amplifier is shown in Table 26. The HPL pin and the HPR pin output 0 V (HPGND) when the headphone amplifier is powered up. The power-down is executed immediately.

Table 26. Headphone Power-Up Time

Sampling Frequency [kHz]	Power-Up Time (Max.)
8/12/16/24/32/48/64/96/128/192/256/384/512/768	23.9 msec
11.025/22.05/44.1/88.2/176.4/352.8/705.6	25.9 msec

< Low Power Mode >

The DAC and the headphone amplifier will be in low power mode by setting LPMODE bit and DSMLP bit to “1”. PMHPL bit and PMHPR bit must be set to “0” when changing operation mode of the DAC and the headphone amplifier between high performance mode and low power mode. The AK4377 does not support Quad, Oct and Hex speed mode (fs = 128 to 768 kHz) in low power mode.

Table 27. DAC and Headphone Amplifier Mode Setting (N/A: Not available)

LPMODE bit	DSMLP bit	Mode	
0	0	High Performance Mode	(default)
0	1	High Performance Mode (@CM[1:0] bits = “00”, fs = 8 to 12 kHz)	
1	0	N/A	
1	1	Low Power Mode	

< Noise Gate >

When NGDIS bit = “0”, a noise gate is enabled and noise level will be improved if both L and R channels input data of the DAC is continuously “0” for the period set by NGT and FS[4:0] bits. The noise gate will be disabled if one of these L channel and R channel input data of the DAC is not “0” even once and the AK4377 returns to normal operation. The noise gate is always disable when NGDIS bit = “1”, or when LPMODE bit = “1” (in low power mode) or when DOP bit = “1” (in DSD Mode). PMDA bit, PMHPL bit and PMHPR bit must be set to “0” when changing NGT bit.

Table 28. Noise Gate Setting

NGDIS bit	Noise Gate Status	
0	Enable	(default)
1	Disable	

Table 29. Noise Gate Zero Detection Period 1 (NGT bit = “0”) (N/A: Not available)

NGT bit	FS4 bit	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (fs)	Zero Detection Time	
0	0	0	0	0	0	8 kHz	128.0 msec	1024/fs
	0	0	0	0	1	11.025 kHz	92.9 msec	1024/fs
	0	0	0	1	0	12 kHz	85.3 msec	1024/fs
	0	0	1	0	0	16 kHz	128.0 msec	2048/fs
	0	0	1	0	1	22.05 kHz	92.9 msec	2048/fs
	0	0	1	1	0	24 kHz	85.3 msec	2048/fs
	0	1	0	0	0	32 kHz	128.0 msec	4096/fs
	0	1	0	0	1	44.1 kHz	92.9 msec	4096/fs
	0	1	0	1	0	48 kHz	85.3 msec	4096/fs
	0	1	1	0	0	64 kHz	128.0 msec	8192/fs
	0	1	1	0	1	88.2 kHz	92.9 msec	8192/fs
	0	1	1	1	0	96 kHz	85.3 msec	8192/fs
	1	0	0	0	0	128 kHz	128.0 msec	16384/fs
	1	0	0	0	1	176.4 kHz	92.9 msec	16384/fs
	1	0	0	1	0	192 kHz	85.3 msec	16384/fs
	1	0	1	0	0	256 kHz	128.0 msec	32768/fs
	1	0	1	0	1	352.8 kHz	92.9 msec	32768/fs
	1	0	1	1	0	384 kHz	85.3 msec	32768/fs
	1	1	0	0	0	512 kHz	128.0 msec	65536/fs
	1	1	0	0	1	705.6 kHz	92.9 msec	65536/fs
	1	1	0	1	0	768 kHz	85.3 msec	65536/fs
	Others					N/A	-	N/A

Table 30. Noise Gate Zero Detection Period 2 (NGT bit = “1”) (N/A: Not available)

NGT bit	FS4 bit	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (fs)	Zero Detection Time	
1	0	0	0	0	0	8 kHz	256.0 msec	2048/fs
	0	0	0	0	1	11.025 kHz	185.8 msec	2048/fs
	0	0	0	1	0	12 kHz	170.7 msec	2048/fs
	0	0	1	0	0	16 kHz	256.0 msec	4096/fs
	0	0	1	0	1	22.05 kHz	185.8 msec	4096/fs
	0	0	1	1	0	24 kHz	170.7 msec	4096/fs
	0	1	0	0	0	32 kHz	256.0 msec	8192/fs
	0	1	0	0	1	44.1 kHz	185.8 msec	8192/fs
	0	1	0	1	0	48 kHz	170.7 msec	8192/fs
	0	1	1	0	0	64 kHz	256.0 msec	16384/fs
	0	1	1	0	1	88.2 kHz	185.8 msec	16384/fs
	0	1	1	1	0	96 kHz	170.7 msec	16384/fs
	1	0	0	0	0	128 kHz	256.0 msec	32768/fs
	1	0	0	0	1	176.4 kHz	185.8 msec	32768/fs
	1	0	0	1	0	192 kHz	170.7 msec	32768/fs
	1	0	1	0	0	256 kHz	256.0 msec	65536/fs
	1	0	1	0	1	352.8 kHz	185.8 msec	65536/fs
	1	0	1	1	0	384 kHz	170.7 msec	65536/fs
	1	1	0	0	0	512 kHz	256.0 msec	131072/fs
	1	1	0	0	1	705.6 kHz	185.8 msec	131072/fs
	1	1	0	1	0	768 kHz	170.7 msec	131072/fs
	Others					N/A	-	N/A

< Overcurrent Protection Circuit >

If the headphone amplifier is in an overcurrent state, such as when output pins are shorted, the headphone amplifier limits the operation current. The headphone amplifier returns to a normal operation state if all causes are cleared.

9-8 Charge Pump & LDO Circuits

The charge pump circuits are operated by CVDD power supply voltage. CVDD is used to generate negative voltage. The power-up/down sequence of charge pump and LDO circuits are as follows. CP1 should be powered up before LDO1P/N1/N2 are powered up. CP2 should be powered up after LDO1P/N1/N2 are powered up. LDO1P, LDO1N1 and LDO1N2 blocks must be powered up or down at the same time.

Power-Up Sequence: CP1 → LDO1P, LDO1N1, LDO1N2 → CP2
Power-Down Sequence: CP2 → LDO1P, LDO1N1, LDO1N2 → CP1

LDO1P, LDO1N1 and LDO1N2 have an overcurrent protection circuit. When overcurrent flows in a normal operation, the LDO1P, LDO1N1 and LDO1N2 circuits limit the operation current. If the overcurrent state is cleared, the overcurrent protection will be off and the LDO1P, LDO1N1 and LDO1N2 circuits will return to normal operation.

LDO2 has an overvoltage protection circuit. This overvoltage protection circuit powers the LDO2 down when the power supply becomes unstable by an instantaneous power failure, etc. during operation. The LDO2 circuit will not return to a normal operation until being reset by the PDN pin ("L" → "H") after removing the problems.

The charge pump and the LDO circuits can be powered up again while they are in power-down state.

Table 31. Input/Output Voltage and Operation Block of the Charge Pump

Charge Pump	Power Management bit	Input Voltage	Output Voltage (Typ.)	Operation Block
CP1	PMCP1	CVDD	−1.8 V	LDO1N1, LDO1N2, DAC
CP2 (Class-G)	PMCP2	CVDD	±1.8 V / ±0.9 V	Headphone

Table 32. Input/Output Voltage and Operation Block of the LDO

LDO	Power Management bit	Power Supply	Output Voltage (Typ.)	Operation Block
LDO1P	PMLDO1P	AVDD / VSS1	+1.5 V	VREF+ for DAC, Headphone
LDO1N1	PMLDO1N1	VSS1 / CP1 Output	−1.5 V	VREF− for DAC, Headphone
LDO1N2	PMLDO1N2	VSS1 / CP1 Output	−1.5 V	DAC
LDO2	-	LVDD / VSS3	+1.2 V	Digital Core

9-9 Serial Audio Interface

9-9-1 PCM Mode

The serial audio interface format is set by DIF bit and its data length is controlled by DL[1:0] bits. In case that the input data length is less than the value which set by DL[1:0] bits, unused lower bits are filled with "0". When using master mode, DL[1:0] bits is set in accordance with the setting of BCKO bit.

Table 33. Digital Audio Interface Format Setting

DIF bit	Digital Interface Format	
0	I^2S Compatible	(default)
1	MSB justified	

Table 34. Data Length Setting (x: Do not Care)

DL1 bit	DL0 bit	Data Length	BCLK Frequency		
			Slave Mode	Master Mode	
0	0	24-bit linear	≥ 48fs	64fs (BCKO bit = "0")	(default)
0	1	16-bit linear	≥ 32fs	32fs (BCKO bit = "1")	
1	x	32-bit linear	≥ 64fs	64fs (BCKO bit = "0")	

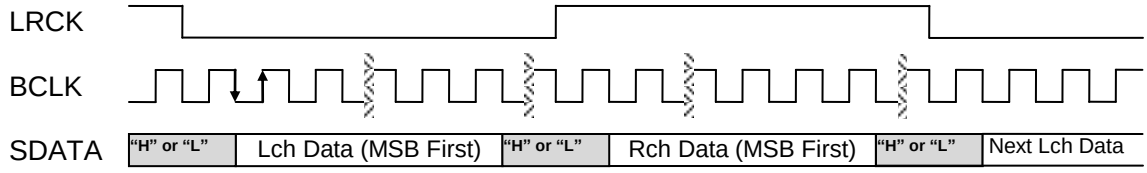


Figure 18. I^2S Compatible Format (DIF bit = "0")

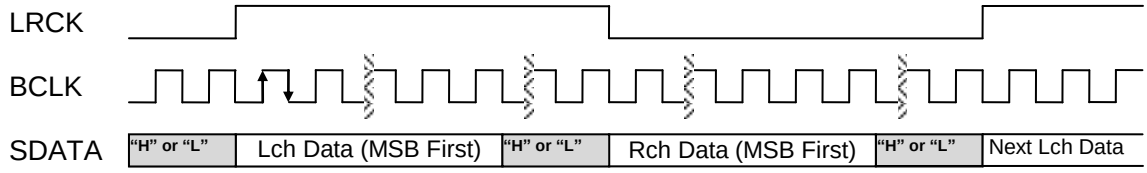


Figure 19. MSB Justified format (DIF bit = "1")

9-9-2 DSD Mode

The AK4377 is in DSD mode by setting DOP bit = “1”. Register setting must be changed while PMDA bit = PMHPL bit = PMHPR bit = “0”.
Set DSD data stream frequency by DSDFS[1:0] bits in DSD mode. FS[4:0] bits must be set to “01001” (44.1 kHz) or “01010” (48 kHz).

Select DoP (DSD Audio over PCM Frames) Marker code by DMMI[1:0] bits.
The output will be muted if data other than DoP Marker code is input continuously for LRCK times set by DETD2P bit to the SDATA pin when DOP bit = “1”. The mute state is released if DoP Marker code is input for LRCK times set by DETP2D bit. Pop noise may occur when transferring or releasing the mute state.

BCLK can be selected from 48 clock / LRCK (Slave mode only) and 64 clock / LRCK. Lower 8 bits should be set to 00H when BCLK is 64 clock / LRCK. Set DL[1:0] bits to “00” when BCLK is 48 clock / LRCK (Slave mode only). DL[1:0] bits must be set to “00” or “1x” when BCLK is 64 clock / LRCK.
Audio interface format can be selected by DIF bit.

Level detection of Class-G, Mixing, Zero Cross Detection and Noise Gate functions are not available in DSD mode.

When DSMLP bit = “1”, only the setting DSDFS[1:0] bits = “00” is available.

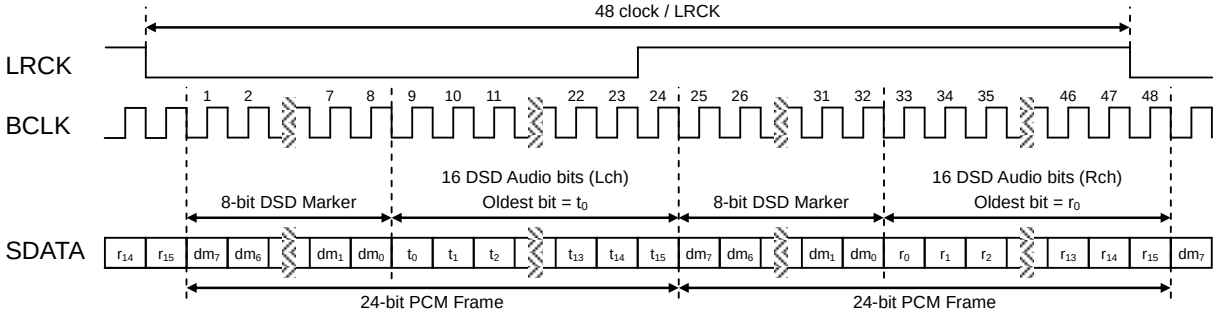


Figure 20. DoP Format (I^2S Compatible, DIF bit = “0”, 48 clock / LRCK, DL[1:0] bits = “00”)

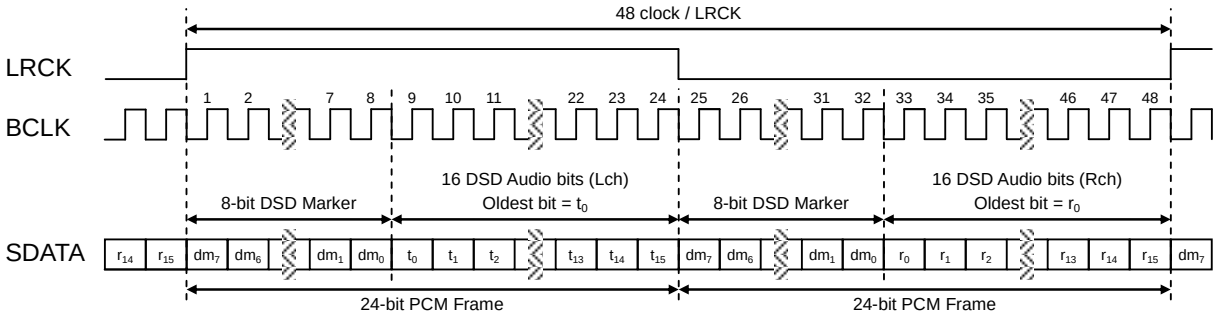


Figure 21. DoP Format (MSB Justified, DIF bit = “1”, 48 clock / LRCK, DL[1:0] bits = “00”)

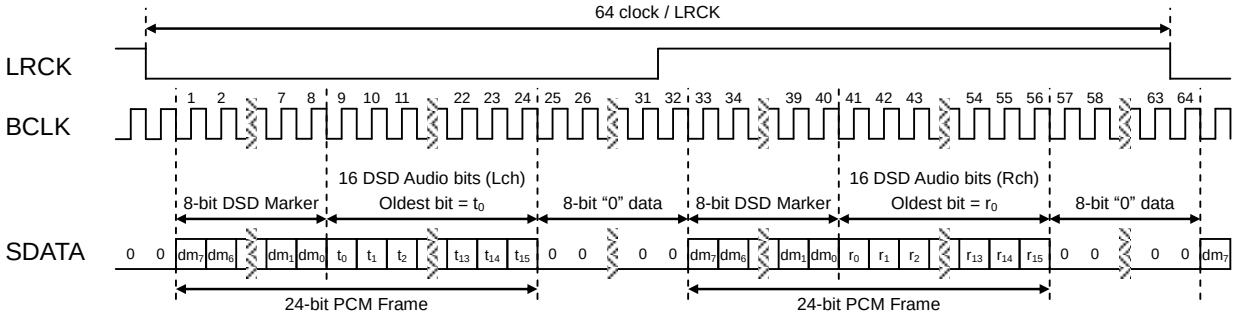


Figure 22. DoP Format (I^2S Compatible, DIF bit = "0", 64 clock / LRCK, DL[1:0] bits = "00" or "1x")

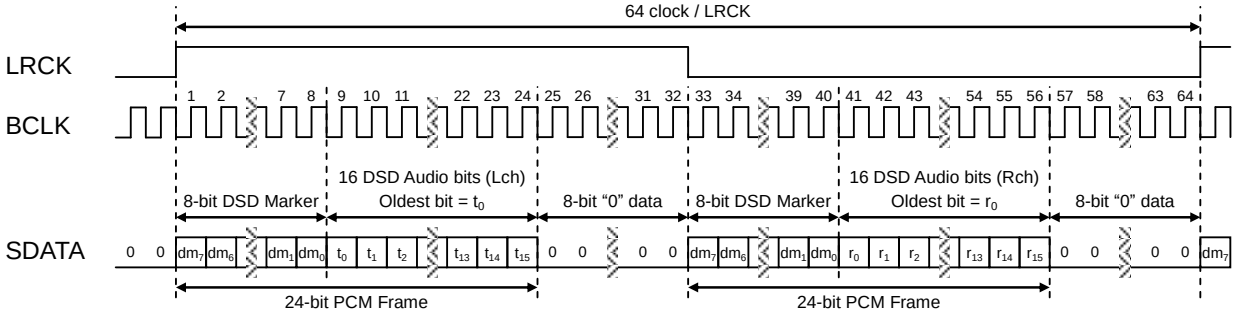


Figure 23. DoP Format (MSB Justified, DIF bit = "1", 64 clock / LRCK, DL[1:0] bits = "00" or "1x")

Table 35. DSD Sampling Speed Setting: Slave Mode (MS bit = "0")

(x: Do not Care, N/A: Not available)

Mode	DSDFS [1:0] bits	FS[4:0] bits	DSD Data Stream (MHz)	LRCK Input Frequency (kHz)	BCLK Input Frequency (MHz)	Master Clock Frequency (MHz) (Note 62)		
						CM[1:0] bits = "00"	CM[1:0] bits = "01"	CM[1:0] bits = "1x"
DSD64	00	01001	2.8224	176.4	8.4672 or 11.2896	11.2896	22.5792	45.1584
		01010	3.072	192	9.216 or 12.288	12.288	24.576	49.152
DSD128	01 (default)	01001	5.6448	352.8	16.9344 or 22.5792	11.2896	22.5792	45.1584
		01010	6.144	384	18.432 or 24.576	12.288	24.576	49.152
DSD256	10	01001	11.2896	705.6	33.8688 or 45.1584	N/A	22.5792	45.1584
		01010	12.288	768	36.864 or 49.152	N/A	24.576	49.152
-	11	xxxxx	N/A					

Note 62. Set a clock that has half frequency of BCLK or higher as the master clock.

Table 36. DSD Sampling Speed Setting: Master Mode (MS bit = “1”)
(x: Do not Care, N/A: Not available)

Mode	DSDFS [1:0] bits	FS[4:0] bits	DSD Data Stream (MHz)	LRCK Output Frequency (kHz)	BCLK Output Frequency (MHz) (Note 63)	Master Clock Frequency (MHz) (Note 63)		
						CM[1:0] bits = “00”	CM[1:0] bits = “01”	CM[1:0] bits = “1x”
DSD64	00	01001	2.8224	176.4	11.2896	11.2896	22.5792	45.1584
		01010	3.072	192	12.288	12.288	24.576	49.152
DSD128	01 (default)	01001	5.6448	352.8	22.5792	N/A	22.5792	45.1584
		01010	6.144	384	24.576	N/A	24.576	49.152
-	10	xxxxx	N/A					
-	11	xxxxx	N/A					

Note 63. Set BCKO bit = “0”. Set a clock that has the same frequency of BCLK or higher as the master clock.

A bypass setting for internal volume circuit and delta-sigma modulator is selectable in DSD mode (Table 37). When setting DSDD bit = “1”, Mixing, Digital volume, Level detection of Class-G, Zero Cross Detection and Noise Gate functions are not available since the volume circuit is bypassed.

DSDFS[1:0] bits must be set to “0x” when setting DSDD bit = “1”.

Table 37. DSD Path Select

DSDD bit	Mode	
0	DSD Normal	(default)
1	DSD Direct	

< DSD Signal Full Scale (FS) Detection >

DSD signal full scale detection function is available for L and R channels independently on DSD mode. If the DSD data is “0” (–FS) or “1” (+FS) for 128 LRCK times continuously, DSD full scale is detected and a corresponding channel bit (FSDETL and FSDETR bits) becomes “1” independently. FSDETL bit and FSDETR bit can be read out at the register address 17H.
When the AK4377 detects full scale signal while DSDMUTEEN bit = “0”, the analog output is muted. (Pop noise may occur on a switching timing to the mute state.)
When setting DSDMUTEEN bit = “1”, full scale detection function is available but the analog output will not be muted.

9-10 Power-Up & Operation Mode

9-10-1 Power-Down State (PDN pin = "L")

When the PDN pin is "L", the AK4377 is in a power-down state. Power supplies must be applied when the PDN pin = "L". Set the PDN pin to "H" to release the Power-Down state after all the power supplies are on. More than one tPDN cycle of "L" period is needed before releasing the Power-Down state. The state of the AK4377 transitions to LDO2 Ctrl state by bringing the PDN pin to "H".

9-10-2 LDO2 Ctrl State

This is a state to control the LDO2.
LDO2 is powered up and the internal DRSTN signal is changed from "L" to "H" after Max. 1 msec, and the AK4377 enters a Standby state.

9-10-3 Standby State

I^2C interface is powered up and register accesses are enabled.

*2 msec (Min.) wait time for power-up of analog circuit blocks (CP1, CP2, LDO1P, LDO1N1, LDO1N2, DAC, Headphone Amplifier and PLL) is needed after setting the PDN pin to "H" to release the Power-Down state.

< State Transition Diagram >

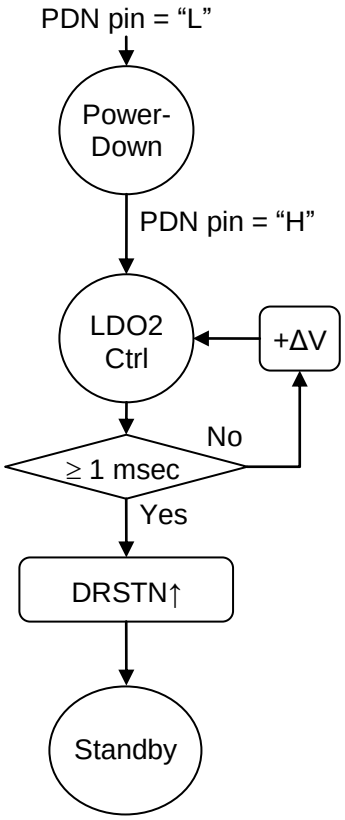


Figure 24. Device State Diagram

1. PDN pin = "L" to "H"
2. Wait 1 msec until LDO2 1.2V output is stable.
3. Internal DRSTN Signal = "L" to "H"
4. Register Access Ready

9-11 Serial Control Interface (I^2C-bus)

The AK4377 supports the fast-mode I^2C-bus (Max. 400 kHz). Pull-up resistors at the SDA and SCL pins must be connected to (TVDD + 0.3) V or less voltage.

9-11-1 WRITE Operation

Figure 25 shows the data transfer sequence for the I^2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 31). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as “0010000”. If the slave address matches that of the AK4377, the AK4377 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 32). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4377. The format is MSB first 8 bits (Figure 27). The data after the second byte contains control data. The format is MSB first, 8 bits (Figure 28). The AK4377 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 31).

The AK4377 can perform more than one byte write operation per sequence at address from 00H to 1AH. After receipt of the third byte the AK4377 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 1AH prior to generating a stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 33) except for the START and STOP conditions.

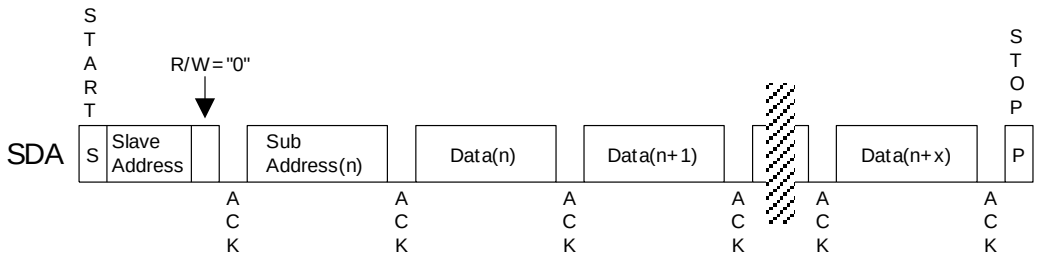


Figure 25. Data Transfer Sequence in I^2C Bus Mode

0	0	1	0	0	0	0	R/W

Figure 26. The First Byte

A7	A6	A5	A4	A3	A2	A1	A0

Figure 27. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 28. The Third Byte

9-11-2 READ Operation

Set the R/W bit = “1” for the READ operation of the AK4377. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 1AH prior to generating stop condition, the address counter will “roll over” to 00H and the data of 00H will be read out.

The AK4377 supports two basic read operations: Current Address READ and Random Address READ.

9-11-2-1 Current Address READ

The AK4377 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next Current READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4377 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4377 ceases the transmission.

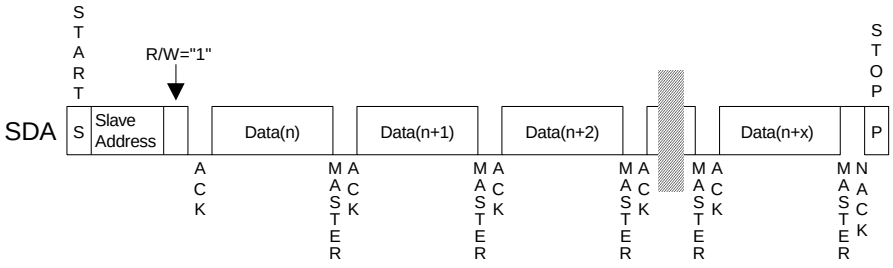


Figure 29. Current Address READ

9-11-2-2 Random Address READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4377 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4377 ceases the transmission.

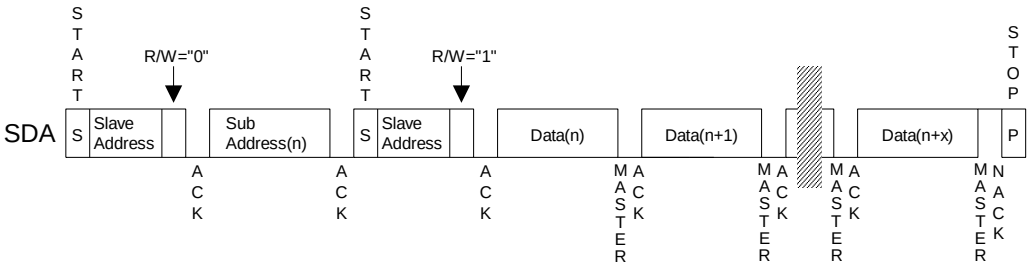


Figure 30. Random Address READ

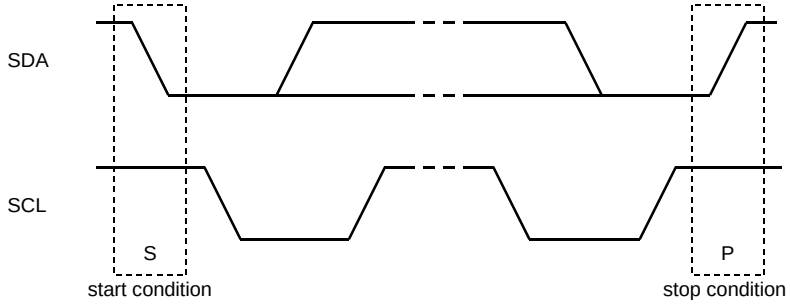


Figure 31. Start Condition and Stop Condition

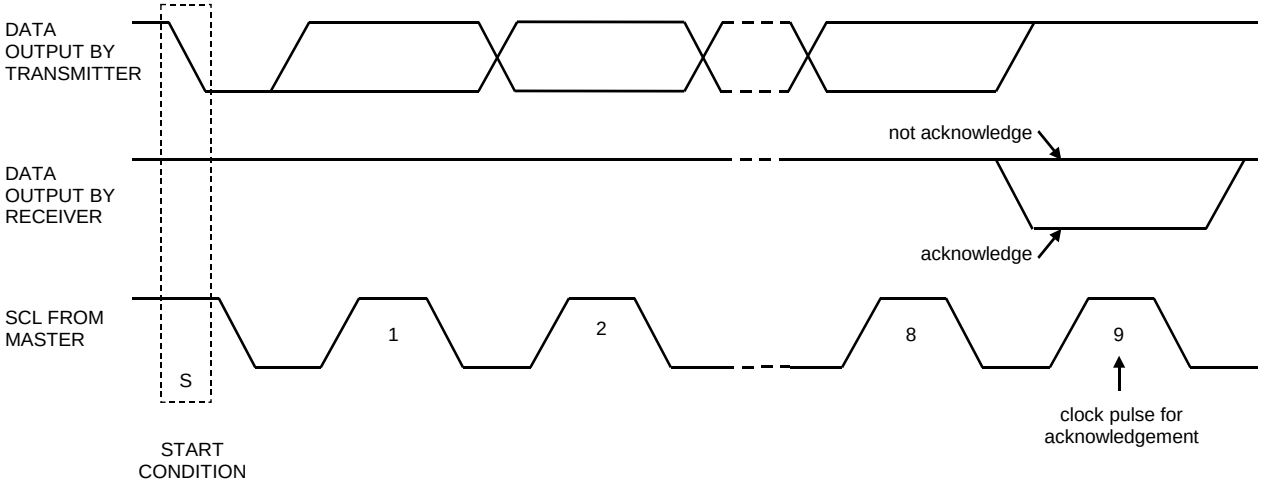


Figure 32. Acknowledge (I^2C Bus)

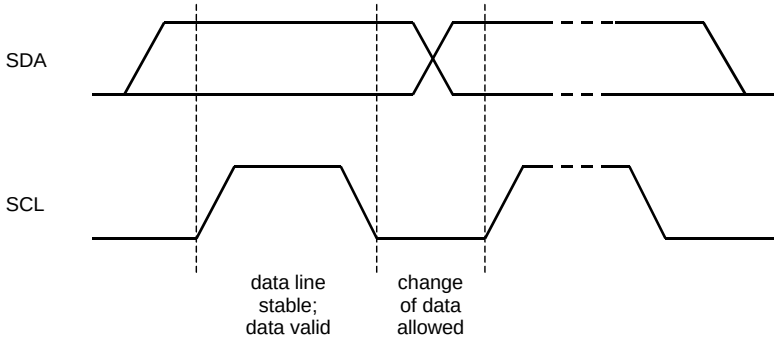


Figure 33. Bit Transfer (I^2C Bus)

9-12 Control Sequence

Figure 34 shows power-up sequence of DAC and headphone amplifier.

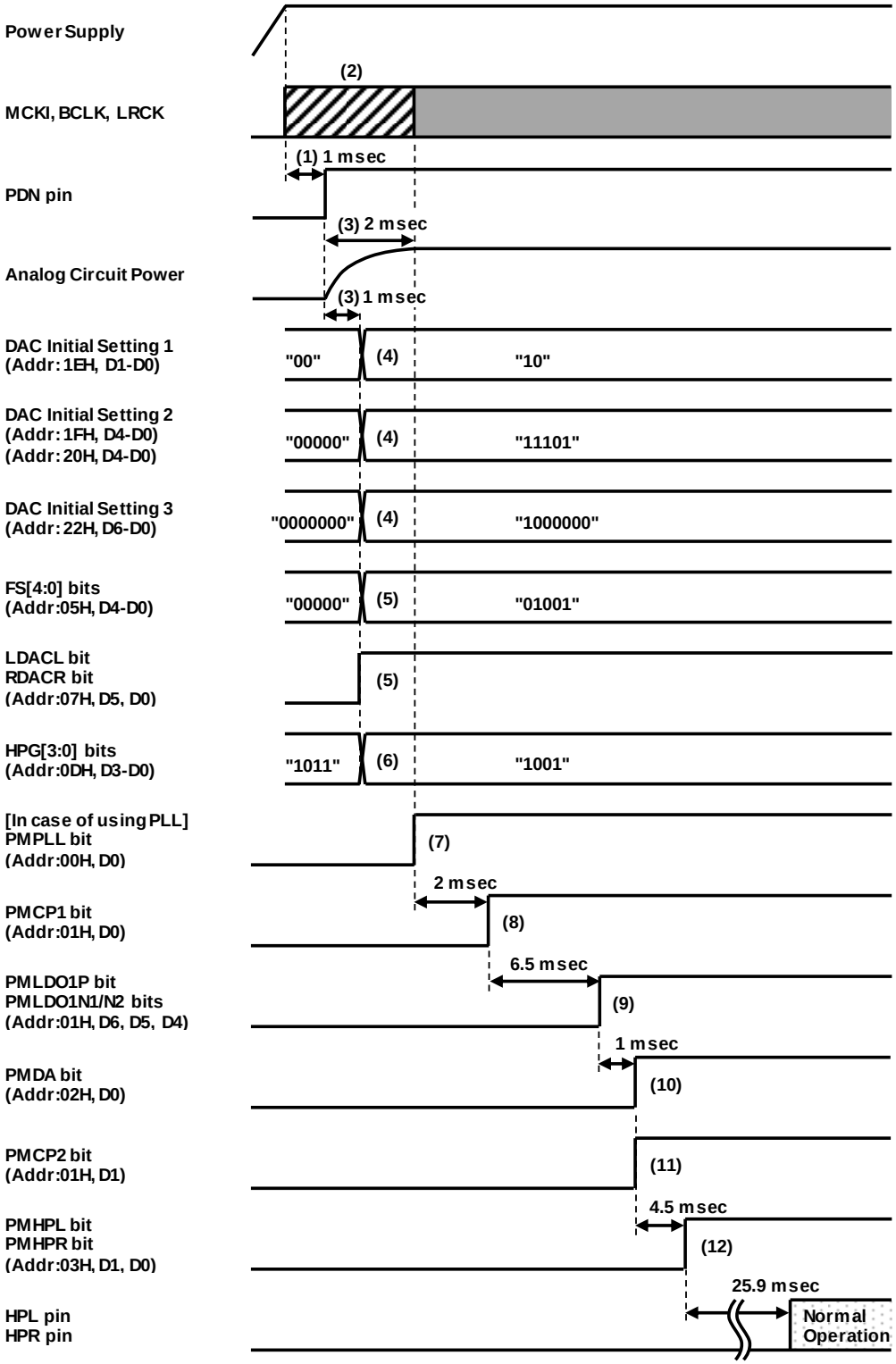


Figure 34. Power-Up Sequence Example of DAC and Headphone Amplifier

< Power-Up Sequence Example >

(1) Set the PDN pin from “L” to “H” after turning on all power supplies. In this case, 1 msec or more “L” time is needed for a certain reset.
(2) After all power supplies are ON, MCKI, BCLK and LRCK should be input before powering up PLL or CP1.
(3) Set the PDN pin = “H” to release the power-down. Register access will be valid after Max. 1 msec. However, a wait time of 2 msec is needed to access power management bits of the analog circuit (PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N1 bit, PMLDO1N2 bit, PMDA bit, PMHPL bit, PMHPR bit and PMPLL bit) until the analog circuit is powered up.
(4) Set DAC initial settings.
(Write “10” data into DACADJ1[1:0] bits (Address 1EH), write “11101” data into both DACADJ2[4:0] bits and DACADJ3[4:0] bits (Address 1FH/20H) and write “1000000” data into DACADJ4[6:0] bits (Address 22H))
(5) Set sampling frequency (FS[4:0] bits) and the input signal path of the DAC
(LDACL bit = RDACR bit = “0” → “1”).
(6) Set headphone amplifier volume by HPG[3:0] bits.
(7) In case of using PLL, power-up PLL (PMPLL bit = “0” → “1”) and wait 2 msec for PLL output stabilization.
(8) Power-up CP1 (PMCP1 bit = “0” → “1”) and wait 6.5 msec (Note 64) for CP1 output voltage stabilization.
(9) Power-up LDO1P, LDO1N1 and LDO1N2 (PMLDO1P bit = PMLDO1N1 bit = PMLDO1N2 bit = “0” → “1”) and wait 1 msec (Note 64) for each LDO output voltage stabilization.
(10) Power-up DAC (PMDA bit = “0” → “1”).
(11) Power-up CP2 (PMCP2 bit = “0” → “1”) and wait 4.5 msec (Note 64) for CP2 output voltage stabilization.
(12) Power-up headphone amplifier (PMHPL bit = PMHPR bit = “0” → “1”). The power-up time of headphone amplifier is 25.9 msec (@ fs = 44.1 kHz). The HPL pin and the HPR pin output 0 V until the headphone amplifier is powered up.

Note 64. Refer to “8-3 Charge Pump & LDO Circuit Power-Up Time”

Figure 35 shows power-down sequence of headphone amplifier and DAC.

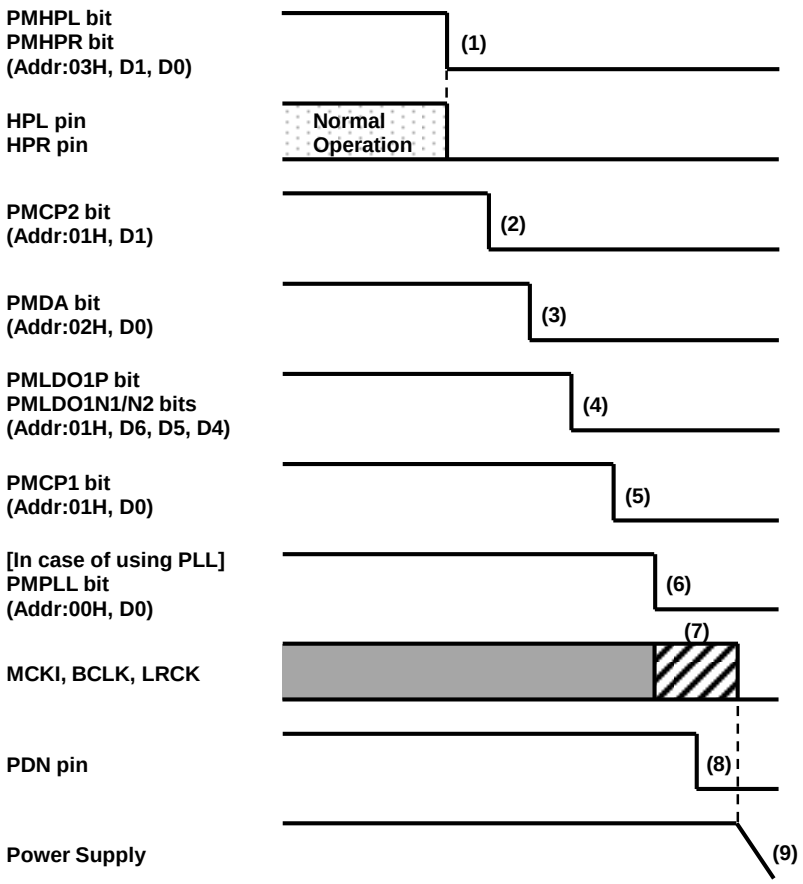


Figure 35. Power-Down Sequence Example of Headphone Amplifier and DAC

< Power-Down Sequence Example >

(1) Power-down headphone amplifier (PMHPL bit = PMHPR bit = “1” → “0”).
When the headphone amplifier is powered down, the HPL pin and HPR pin are pulled down to HPGND via the internal pull-down register.
(2) Power-down CP2 (PMCP2 bit = “1” → “0”).
(3) Power-down DAC (PMDA bit = “1” → “0”).
(4) Power-down LDO1P, LDO1N1 and LDO1N2 (PMLDO1P bit = PMLDO1N1 bit = PMLDO1N2 bit = “1” → “0”).
(5) Power-down CP1 (PMCP1 bit = “1” → “0”).
(6) In case of using PLL, power-down PLL (PMPLL bit = “1” → “0”).
(7) Stop MCKI, BCLK and LRCK supply before turning off each of power supplies.
(8) Set the PDN pin from “H” to “L”.
(9) Turn off each of power supplies.

9-13 Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	0	0	PMOSC	0	0	0	PMPLL
01H	Power Management 2	0	PMLDO1N2	PMLDO1N1	PMLDO1P	0	0	PMCP2	PMCP1
02H	Power Management 3	0	0	0	LPMODE	0	0	0	PMDA
03H	Power Management 4	LVDSEL	LVDTM[2:0]			CPMODE[1:0]		PMHPR	PMHPL
04H	Output Mode Setting	0	0	VDDTM[3:0]				HPRHZ	HPLHZ
05H	Clock Mode Select	0	CM[1:0]		FS[4:0]				
06H	Digital Filter Select	DASD	DASL	T2	0	T1	0	NGT	NGDIS
07H	DAC Mono Mixing	INVR	MDACR	RDACR	LDACR	INVL	MDACL	RDACL	LDACL
08H	Reserved	0	0	0	0	0	0	0	0
09H	Reserved	0	0	0	0	0	0	0	0
0AH	Reserved	0	0	0	0	0	0	0	0
0BH	Lch Output Volume	OVOLCN	0	OVL[5:0]					
0CH	Rch Output Volume	0	0	OVR[5:0]					
0DH	HP Volume Control	HPTM[2:0]			ZCDIS	HPG[3:0]			
0EH	PLL CLK Source Select	0	T4	T3	0	0	0	0	PLS
0FH	PLL Ref CLK Divider 1	PLD[15:8]							
10H	PLL Ref CLK Divider 2	PLD[7:0]							
11H	PLL FB CLK Divider 1	PLM[15:8]							
12H	PLL FB CLK Divider 2	PLM[7:0]							
13H	DAC CLK Source	0	0	0	DIV	T6	T5	0	DACCKS
14H	DAC CLK Divider	MDIV[7:0]							
15H	Audio Interface Format	DEVICEID[2:0]			MS	BCKO	DIF	DL[1:0]	
16H	DSDCTRL	0	0	0	0	0	DOP	DSDFS[1:0]	
17H	DSDERR	0	0	FSDETR	FSDETL	0	0	0	0
18H	DSDICTRL	0	DSDMUTEEN	DETP2D	DETD2P	DMMI[1:0]		DSDD	DSDF
19H	DSDMARKERE	DMIE[7:0]							
1AH	DSDMARKERO	DMIO[7:0]							
1EH	DAC Adjustment 1	0	0	0	0	0	0	DACADJ1[1:0]	
1FH	DAC Adjustment 2	0	0	0	DACADJ2[4:0]				
20H	DAC Adjustment 3	0	0	0	DACADJ3[4:0]				
22H	DAC Adjustment 4	0	DACADJ4[6:0]						
24H	Mode Control	0	DSMLP	0	T7	0	0	0	0

Note 65. PDN pin = “L” resets the registers to their default value.
Note 66. The bits defined as “0” must contain a “0” value.
Note 67. Writing access from 1BH to 1DH, 21H, 23H, 25H to FFH is prohibited.

9-14 Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	0	0	PMOSC	0	0	0	PMPLL
R/W		R	R	R	R/W	R	R	R	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: Power-Down (default)
1: Power-Up

PMOSC: Crystal Oscillator Power Management
0: Power-Down (default)
1: Power-Up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	PMLDO1N2	PMLDO1N1	PMLDO1P	0	0	PMCP2	PMCP1
R/W		R	R/W	R/W	R/W	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMCP1: Charge Pump 1 Power Management
0: Power-Down (default)
1: Power-Up

PMCP2: Charge Pump 2 Power Management
0: Power-Down (default)
1: Power-Up

PMLDO1P: LDO1P Power Management
0: Power-Down (default)
1: Power-Up

PMLDO1N1: LDO1N1 Power Management
0: Power-Down (default)
1: Power-Up

PMLDO1N2: LDO1N2 Power Management
0: Power-Down (default)
1: Power-Up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Management 3	0	0	0	LPMODE	0	0	0	PMDA
R/W		R	R	R	R/W	R	R	R	R/W
Default		0	0	0	0	0	0	0	0

PMDA: DACDIG Power Management
0: Power-Down (default)
1: Power-Up

LPMODE: DAC & Headphone Amplifier Low Power Mode Setting
0: High Performance Mode (default)
1: Low Power Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Power Management 4	LVDSEL	LVDTM[2:0]			CPMODE[1:0]		PMHPR	PMHPL
R/W		R/W	R/W			R/W		R/W	R/W
Default		0	000			00		0	0

PMHPL/R: Headphone Amplifier L/R Channel Power Management
0: Power-Down (default)
1: Power-Up

CPMODE[1:0]: Charge Pump Mode Setting (Table 18)
Default: “00” (Automatic Switching Mode)

LVDTM[2:0]: Class-G 1/2VDD Mode Detection Time Setting (Table 20)
Default: “000” (64/fs)

LVDSEL: Switching Threshold between VDD Mode and 1/2VDD Mode of CP2
0: VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V, R_L = 32Ω)
1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V, R_L = 32Ω)
(Default: Assuming when connecting a Headphone that is 32Ω or more)
1: VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V, R_L = 16Ω)
1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V, R_L = 16Ω)
(Assuming when connecting a 16Ω Headphone or when impedance is not able to be detected)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Output Mode Setting	0	0	VDDTM[3:0]				HPRHZ	HPLHZ
R/W		R	R	R/W				R/W	R/W
Default		0	0	0000				0	0

HPLHZ/HPRHZ: GND Switch Setting for Headphone Amplifier Output
0: Pull-Down by 9Ω (Typ.) (default)
1: Pull-Down by 117 kΩ (Typ.)

VDDTM[3:0]: Class-G VDD Mode Hold Time Setting (Table 19)
Default: “0000” (1024/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Clock Mode Select	0	CM[1:0]		FS[4:0]				
R/W		R	R/W		R/W				
Default		0	00		00000				

FS[4:0]: Sampling Frequency Setting (Table 5)
Default: "00000" (fs = 8 kHz)

CM[1:0]: Master Clock Setting (Table 3, Table 4)
Default: "00" (256fs @Normal/Double/Quad Speed Mode / 32fs @Oct/Hex Speed Mode)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Digital Filter Select	DASD	DASL	T2	0	T1	0	NGT	NGDIS
R/W		R/W	R/W	R/W	R	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

NGDIS: Noise Gate Setting
0: Noise Gate Enable (default)
1: Noise Gate Disable

NGT: Noise Gate Timer Setting (Table 29, Table 30)
Default: "0"

T1, T2: Write "0" into this bit.

DASD, DASL: DAC Digital Filter Mode Setting (Table 14)
Default: "0, 0" (Sharp Roll-Off Filter)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	DAC Mono Mixing	INVR	MDACR	RDACR	LDACR	INVL	MDACL	RDACL	LDACL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MDACL, RDACL, LDACL: DAC L Channel Input Signal Select (Table 15)
Default: "0, 0, 0" (MUTE)

MDACR, RDACR, LDACR: DAC R Channel Input Signal Select (Table 15)
Default: "0, 0, 0" (MUTE)

INVL/R: DAC Input Signal Polarity Select
0: Normal (default)
1: Inverting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H 09H 0AH	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Write "0" to the addresses from 08H to 0AH.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Lch Output Volume	OVOLCN	0	OVL[5:0]					
0CH	Rch Output Volume	0	0	OVR[5:0]					
R/W		0BH: R/W 0CH: R	R	R/W					
Default		0	0	39H					

OVL[5:0]: DAC L Channel Digital Volume Setting; +3 dB to −28 dB & Mute, 0.5 dB step (Table 17)
OVR[5:0]: DAC R Channel Digital Volume Setting; +3 dB to −28 dB & Mute, 0.5 dB step (Table 17)
Default: 39H (0 dB)

OVOLCN: Digital Volume Control
0: Dependent (default)
1: Independent
When OVOLCN bit = “0”, OVL[5:0] bits control both L channel and R channel volume levels while register values of OVL[5:0] bits are not written to OVR[5:0] bits. When OVOLCN bit = “1”, OVL[5:0] bits control L channel level and OVR[5:0] bits control R channel level, respectively.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	HP Volume Control	HPTM[2:0]			ZCDIS	HPG[3:0]			
R/W		R/W			R/W	R/W			
Default		011			0	BH			

HPG[3:0]: Headphone Amplifier Analog Volume Setting; +4 dB to −20 dB (Table 21)
Default: BH (0 dB)

ZCDIS: Zero Cross Detection Setting
0: Zero Cross Detection Enable (default)
1: Zero Cross Detection Disable

HPTM[2:0]: Headphone Amplifier Zero Crossing Timeout Period Setting (Table 23)
Default: “011” (1024/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	PLL CLK Source Select	0	T4	T3	0	0	0	0	PLS
R/W		R	R/W	R/W	R	R	R	R	R/W
Default		0	0	0	0	0	0	0	0

PLS: PLL Clock Source Select (Table 7)
0: MCKI/XTI pin (default)
1: BCLK pin

T3, T4: Write “0” into this bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	PLL Ref CLK Divider 1	PLD[15:8]							
10H	PLL Ref CLK Divider 2	PLD[7:0]							
R/W		R/W							
Default		0000H							

PLD[15:0]: PLL Reference Clock Divider Setting (Table 8)
Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	PLL FB CLK Divider 1	PLM[15:8]							
12H	PLL FB CLK Divider 2	PLM[7:0]							
R/W		R/W							
Default		0000H							

PLM[15:0]: PLL Feedback Clock Divider Setting (Table 9)
Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	DAC CLK Source	0	0	0	DIV	T6	T5	0	DACCKS
R/W		R	R	R	R/W	R/W	R/W	R	R/W
Default		0	0	0	0	0	0	0	0

DACCKS: DAC Master Clock Source Select (Table 1)
0: MCKI/XTI pin (default)
1: PLLO

T5, T6: Write “0” into this bit.

DIV: DACMCLK Divider 2 Setting (Table 13)
Default: “0” (Divided by 1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	DAC CLK Divider	MDIV[7:0]							
R/W		R/W							
Default		00H							

MDIV[7:0]: DACMCLK Divider Setting (Table 13)
Default: 00H (Divided by 1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	Audio Interface Format	DEVICEID[2:0]			MS	BCKO	DIF	DL[1:0]	
R/W		R			R/W	R/W	R/W	R/W	
Default		011			0	0	0	00	

DL[1:0]: Data Length Setting (Table 34)
Default: “00” (24-bit linear)

DIF: Digital Audio Interface Format Setting (Table 33)
0: I^{2}S Compatible (default)
1: MSB justified

BCKO: BCLK Output Frequency
0: 64fs (default)
1: 32fs

MS: Master/Slave Mode Setting (Table 2)
0: Slave Mode (default)
1: Master Mode

DEVICEID[2:0]: Device ID
Default: “011” (AK4375: “000”, AK4375A: “001”, AK4376/AK4376A: “010”, AK4377: “011”)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	DSDCTRL	0	0	0	0	0	DOP	DSDFS[1:0]	
R/W		R	R	R	R	R	R/W	R/W	
Default		0	0	0	0	0	0	01	

DSDFS[1:0]: DSD Sampling Speed Setting (Table 35, Table 36)
Default: “01” (DSD128)

DOP: PCM/DSD Mode Select
0: PCM Mode (default)
1: DSD Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	DSDERR	0	0	FSDETR	FSDETL	0	0	0	0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

FSDETL: L Channel DSD Full Scale Detect
FSDETR: R Channel DSD Full Scale Detect
0: Not Full Scale data (default)
1: Full Scale data

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	DSDICTRL	0	DSDMUTEEN	DETP2D	DETD2P	DMMI[1:0]		DSDD	DSDF
R/W		R	R/W	R/W	R/W	R/W		R/W	R/W
Default		0	0	0	0	0		0	0

DSDF: Cut-Off Frequency of DSD Filter Setting
0: 50 kHz @DSDFS[1:0] bits = “00”, FS[4:0] bits = “01001” (default)
1: 100 kHz @DSDFS[1:0] bits = “00”, FS[4:0] bits = “01001”

DSDD: DSD Path Setting
0: Normal Path (default)
1: Digital Volume and Delta-Sigma Modulator Bypass

DMMI[1:0]: DoP Marker Mode
00: 05H, FAH (default)
01: AAH
10: Register Setting
(Set by DMIE[7:0] bits and DMIO[7:0] bits. The AK4377 detects DoP input when the input DoP marker is Lch: DMIE → Rch: DMIE → Lch: DMIO → Rch: DMIO → …)
11: 05H or FAH or AAH

DETD2P: Number of Detection of Non DoP Data
0: 1 Time (default)
1: 16 Times

DETP2D: Number of Detection of DoP Data
0: 16 Times (default)
1: 32 Times

DSDMUTEEN: DSD Mute Disable
0: Mute DAC Output when DSD Input Data is continuously “0” or “1” for 128 LRCK times. (default)
1: Mute Function is Disabled (FSDETL and FSDETR bits settings are valid)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	DSDMARKERE	DMIE[7:0]							
1AH	DSDMARKERO	DMIO[7:0]							
R/W		R/W							
Default		DMIE[7:0]: 05H, DMIO[7:0]: FAH							

DMIE [7:0]: DoP Marker Setting (EVEN) when DMMI[1:0] bits = “10”
Default: 05H
DMIO [7:0]: DoP Marker Setting (ODD) when DMMI[1:0] bits = “10”
Default: FAH
The AK4377 detects DoP input when the input DoP marker is Lch: DMIE → Rch: DMIE → Lch: DMIO → Rch: DMIO → …

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	DAC Adjustment 1	0	0	0	0	0	0	DACADJ1[1:0]	
R/W		R	R	R	R	R	R	R/W	
Default		0	0	0	0	0	0	00	

DACADJ1[1:0]: DAC Adjustment 1

Default: "00"

"10" data must be written to DACADJ1[1:0] bits before analog blocks (CP1, CP2, LDO1P, LDO1N1, LDO1N2, DAC, Headphone Amplifier, PLL) are powered up.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1FH	DAC Adjustment 2	0	0	0	DACADJ2[4:0]				
20H	DAC Adjustment 3	0	0	0	DACADJ3[4:0]				
R/W		R	R	R	R/W				
Default		0	0	0	00000				

DACADJ2[4:0]: DAC Adjustment 2

DACADJ3[4:0]: DAC Adjustment 3

Default: "00000"

"11101" data must be written to DACADJ2[4:0] bits and DACADJ3[4:0] bits before analog blocks (CP1, CP2, LDO1P, LDO1N1, LDO1N2, DAC, Headphone Amplifier, PLL) are powered up.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22H	DAC Adjustment 4	0	DACADJ4[6:0]						
R/W		R	R/W						
Default		0	00H						

DACADJ4[6:0]: DAC Adjustment 4

Default: 00H

40H data must be written to DACADJ4[6:0] bits before analog blocks (CP1, CP2, LDO1P, LDO1N1, LDO1N2, DAC, Headphone Amplifier, PLL) are powered up.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24H	Mode Control	0	DSMLP	0	T7	0	0	0	0
R/W		R	R/W	R	R/W	R	R	R	R
Default		0	0	0	0	0	0	0	0

T7: Write "0" into this bit.

DSMLP: DAC Operation Mode Setting (Table 3, Table 4, Table 27)

Default: "0"

10. Recommended External Circuits

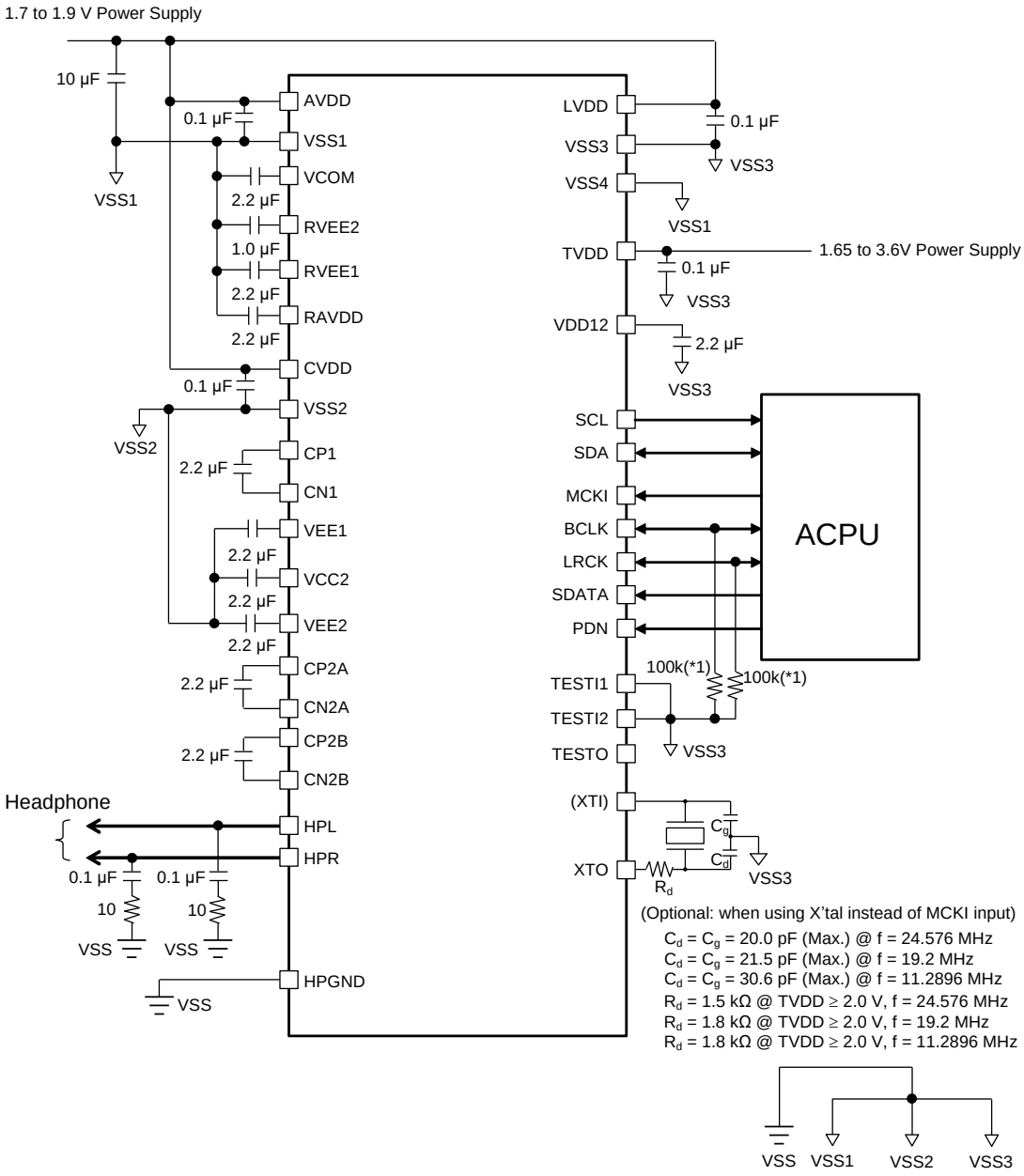


Figure 36. System Connection Diagram

*1: When AK4377 is in master mode, a pull-down resistor (e.g. 100 kΩ) is needed.

10-1 Grounding and Power Supply Decoupling

The AK4377 requires careful attention to power supply and grounding arrangements. The PDN pin should be held “L” when power supplies are tuning on. AVDD should be powered up before or at the same time of CVDD. Power-up sequence of TVDD and LVDD is not critical. The PDN pin is allowed to be “H” after all power supplies are applied and settled. To power down the AK4377, set the PDN pin to “L” and power down CVDD before or at the same time of AVDD. Power-down sequence of LVDD and TVDD is not critical.

To avoid pop noise on analog output when power-up/down, the AK4377 should be operated along the following recommended power-up/down sequence.

1) Power-up
   - The PDN pin should be held “L” when power supplies are turning on. The AK4377 can be reset by keeping the PDN pin “L” for 1 msec or longer after all power supplies are applied and settled. Then release the reset by setting the PDN pin to “H”.

2) Power-down
   - Each of power supplies can be powered OFF after the PDN pin is set to “L”.

VSS1, VSS2, VSS3 and VSS4 of the AK4377 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value ceramic capacitor is to be closest.

10-2 Voltage Reference

VCOM is a common voltage of this chip. A 2.2 µF ceramic capacitor attached between the VCOM pin eliminates the effects of high frequency noise. No load current is allowed to be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4377.

10-3 Charge Pump and LDO Circuits

Capacitors for CP1 block (connected between the CP1 pin and the CN1 pin, between the VEE1 pin and the VSS2 pin) and for CP2 block (connected between the CP2A pin and the CN2A pin, between the CP2B pin and the CN2B pin, between the VCC2 pin and the VSS2 pin, between the VEE2 pin and the VSS2 pin) should be low ESR 2.2 µF ±50%.
Capacitors for LDO1P block (connected between the RAVDD pin and the VSS1 pin) and for LDO1N1 block (connected between the RVEE1 pin and the VSS1 pin) should be low ESR from 2.2 µF ±50% to 4.7 µF ±50%. Capacitors for LDO1N2 block (connected between the RVEE2 pin and the VSS1 pin) should be low ESR from 1.0 µF ±50% to 4.7 µF ±50%.
These capacitors must be connected as close as possible to the pins. No load current may be drawn from the Positive / Negative Power Output pin (VEE1, RAVDD, RVEE1, RVEE2, VCC2 and VEE2 pins).

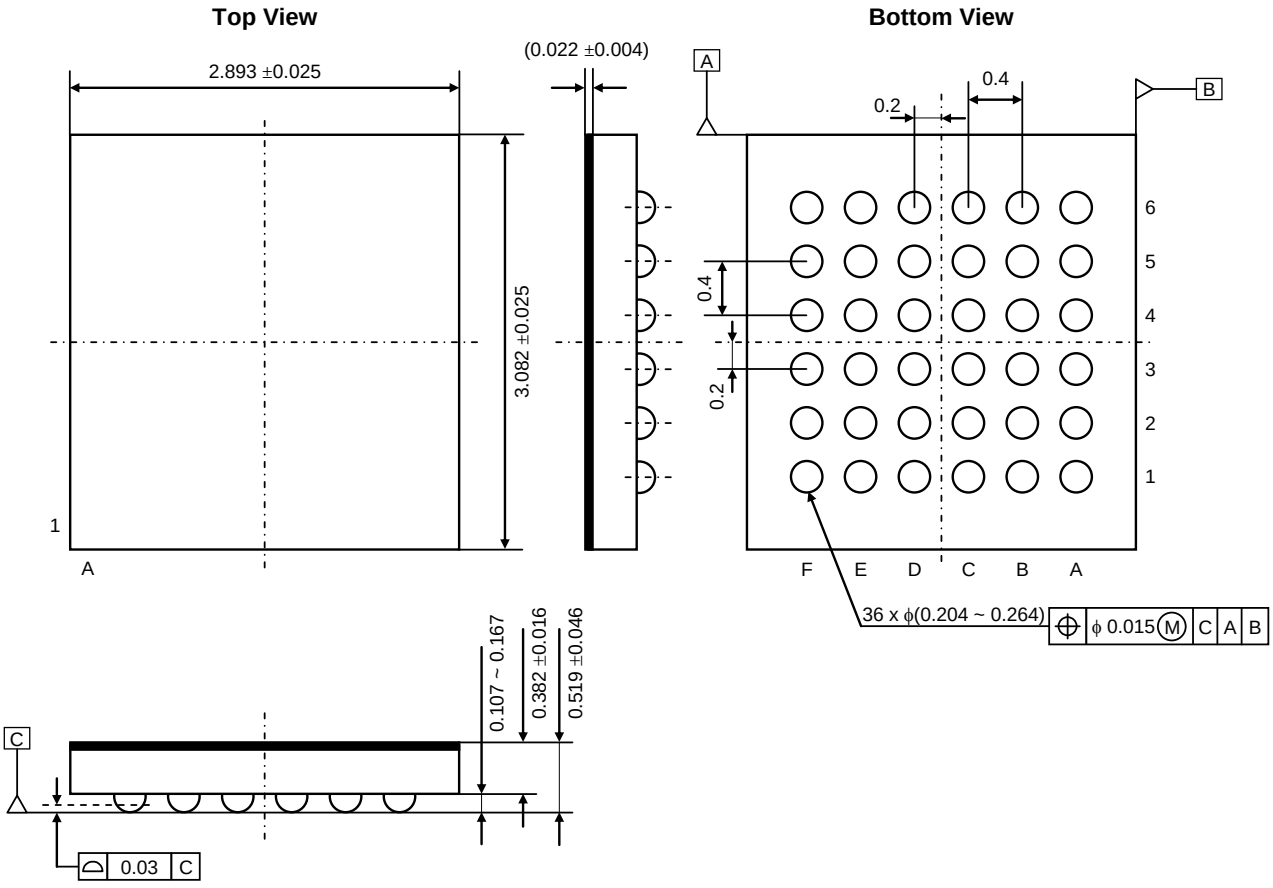
10-4 Analog Outputs

Headphone outputs are single-ended and centered at HPGND (0 V). They should be directly connected to a headphone without AC coupling.

11. Package

11-1 Outline Dimensions

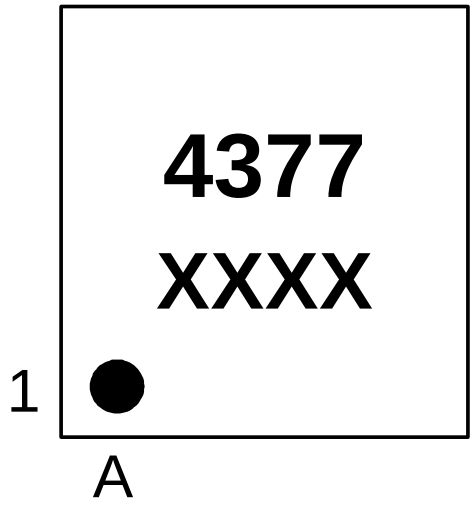
36-pin CSP (Unit: mm)



11-2 Material and Lead Finish

Package molding compound:	Epoxy Resign, Halogen free
Solder ball material:	SnAgCu

11-3 Marking



XXXX: Date code (4 digits)
Pin #A1 indication

12. Ordering Guide

AK4377ECB	−40 to 85 °C	36-pin CSP (0.4 mm pitch)
AKD4377	Evaluation board for AK4377	

13. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
18/02/27	00	First Edition		

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Asahi Kasei Microdevices:

AK4377ECB