Power Line Smart AC Switch Controller

Features

- Low energizing current 60uA (typical)
- Line to Neutral voltage monitoring
- Line to Load voltage monitoring
- User adjustable maximum load voltage
- 'In-cycle' Over-Voltage load isolation
- Suitable for use with IGBT AC switch
- Zero-volt (Line to Load) AC switch connect
- Zero-volt (Line to Load) AC switch disconnect
- Compatible with 50Hz/240V and 60Hz/110V
- Output gate drive voltage of 16V
- Timing pin for programmable recovery delay
- SOIC 8-pin package

Applications

- White Goods, Home Appliances
- Air conditioners
- Motor Control & Protection
- Servers and Data Routers
- Sensitive Electronics

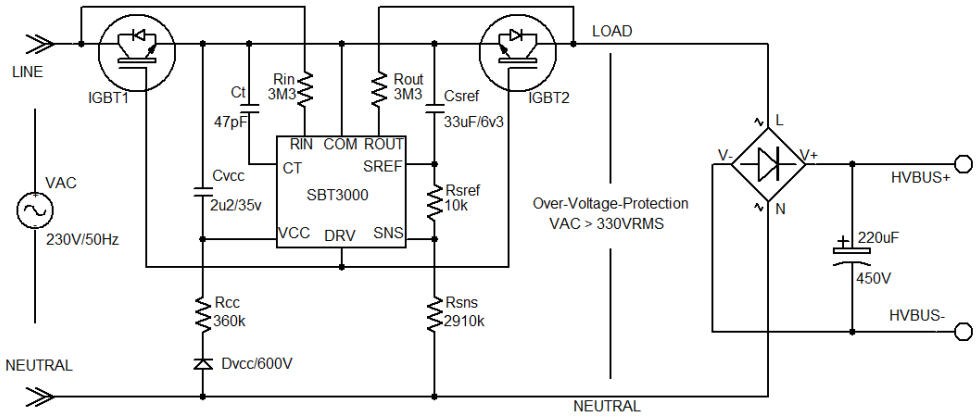
Product Description

The SBT3000 is a patented, high voltage AC switch controller device, which monitors incoming line voltage to ensure that the downstream load only operates within its safe maximum continuous voltage ratings. In the event of an over-voltage line conditions, the SBT3000 will disable the AC switch to protect and isolate the load and minimize the potential of catastrophic failure modes.

Once the line voltage has stabilized back within safe operating range for the duration of the recovery timer interval (user adjustable via external timing capacitor), normal load operation will resume in the following cycle and be synchronized to zero Line to Load voltage condition, thereby resulting in minimal in-rush current stress.

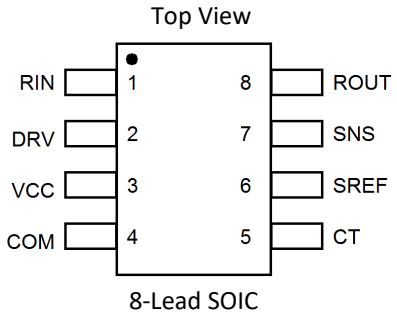
Equipped with an output drive of 16V, the SBT3000 is an ideal solution for controlling any type of cost effective IGBT's. In addition, the device is housed in a convenient small form factor SOIC-8 package to suit a wide variety of applications.

Figure 1: Typical Application Circuit ($230V_{rms}$ systems)



(Input Common Mode Filter, Inrush NTC limiter, and XY caps are not shown for simplicity)

Pin Configuration



Ordering Information

Part Number	Package	Qty/Reel	Marking
SBT3000	SOIC-8	3000	YYWWS
YY: Year WW: Week S: SOIC			

Pin Table

Pin	Name	Description
1	RIN	Positive sense input for Line to Load monitor (external resistor to Line side)
2	DRV	Output to control IGBT gate drive
3	VCC	Supply bias voltage input
4	COM	Ground reference point for all voltages (connect to IGBT common emitter point)
5	CT	Restart timing delay control (external capacitor to COM pin)
6	SREF	Sense reference pin for Line-Neutral monitor (connect with 33uF capacitor to COM pin and 10k resistor to SNS pin)
7	SNS	Sense input voltage for overvoltage monitoring (external resistor to Neutral)
8	ROUT	Negative sense input for Line to Load monitor (external resistor to Load side)

Figure 2: SBT3000 Simplified Block Diagram

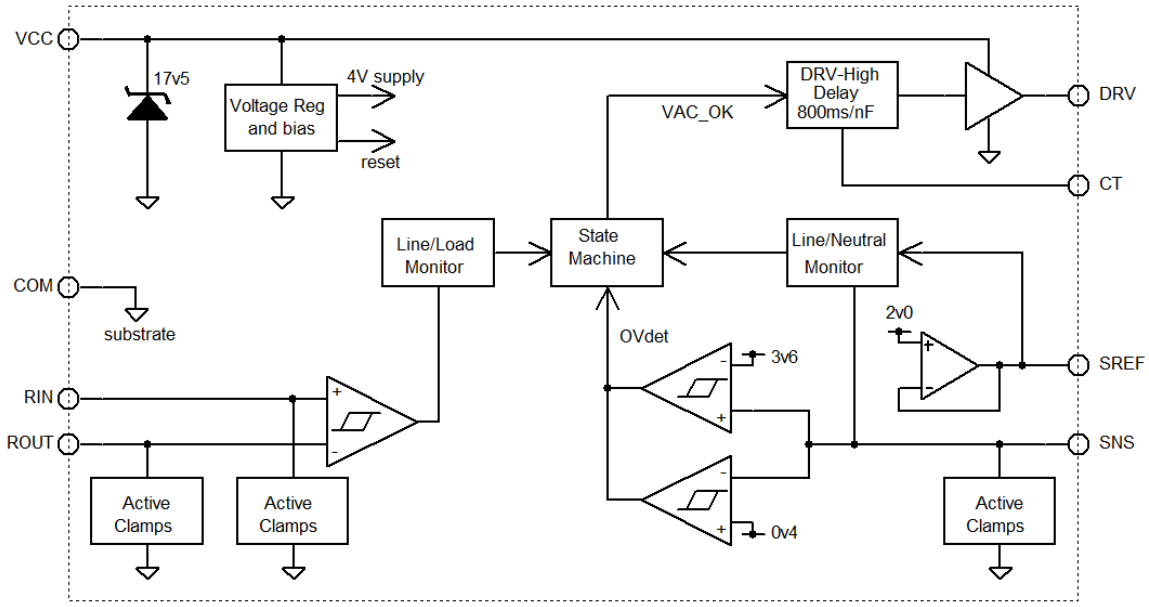


Table 1: Absolute Maximum Ratings

Stress levels that exceed the absolute maximum ratings may cause damage to the device.
Functional operation at conditions other than the recommended operating conditions is not implied.
All electrical parameters are with respect to COM pin.

Parameters	Value	Unit
VCC , DRV	-0.3 to +20	V
RIN, ROUT, CT, SNS, SREF	-0.3 to 5.5	V
Clamping current VCC to COM	0 to +20	mA
Clamping current RIN, ROUT, SNS	-2 to +2	mA
Operating Junction Temperature	-40 to +150	°C
Storage Junction Temperature	-65 to +150	°C
Package Thermal Resistance (Theta-JA, Junction to Ambient)	170	°C/W

Table 2: Compliance Ratings

Parameters	Value	Unit
Human Body Model , ESD immunity , JS-001-2017	±2	kV
Charge Device Model ESD immunity, JS-002-2018	±1	kV
Latch-up Immunity , JESD78E, Class2, +125°C	±100	mA
Moisture Sensitivity Level	MSL1	

Table 3: Recommended Operating Conditions

Refer to Figure 1, Typical Application Circuit, for component designators

Symbol	Parameters	Value	Unit
Icc peak	Peak bias current into Vcc pin (1)	0 to +10	mA
Rcc	VCC bias resistor	100 to 360	kΩ
Cvcc	VCC bypass supply capacitor	2.2 to 3.3	µF
Rsref	SREF resistor	9 to 11	kΩ
Csref	Sense reference filter capacitor	22 to 47	µF
Rin/Rout	Line-load sense resistors	2.2 to 3.3	MΩ
$DRV_{C\text{-}LOAD}$	DRV pin load capacitance	< 30	nF
T_{AMB}	Ambient Operating temperature	-40 to +105	°C

Note 1: Icc peak current applies to worst case maximum continuous VAC peak voltage: (VAC peak voltage-18V)/Rcc

Table 4: Electrical Characteristics

Unless noted otherwise, characteristics apply to Application Circuit component values shown in Figure 1.
Typical values are at an ambient temperature of 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VCC_{UVLO_R}	Under-Voltage-Lockout	Vcc rising.	13.8	14.6	15.4	V
VCC_{UVLO_F}	Under-Voltage-Lockout	Vcc falling		13.3		V
VCC_{UVLO_HYST}	UVLO Hysteresis	VCC_{UVLO_R} - VCC_{UVLO_F}		1.3		V
$VCC_{CLAMP1mA}$	1mA VCC clamp voltage	I_{VCC} = 1mA		17.6		V
$VCC_{CLAMP10mA}$	10mA VCC clamp voltage	I_{VCC} = 10mA		18.2		V
$I_{ENERGIZE}$	Energizing Current (min)	I_{VCC} startup current	40	60	80	µA rms
$T_{ENERGIZE}$	Energizing Start up time	VAC = 230V RMS 50Hz		0.4		sec
V_{SREF}	SREF regulated voltage	In normal operation	-5%	2.0	+5%	V
$V_{STARTMAX}$ (2)	Maximum for load startup	$\lvert V_{SNS} - V_{SREF} \rvert$ absolute	-6%	1.5	+6%	V
OVP_{TRIP} (3)	Over Voltage detect	$\lvert V_{SNS} - V_{SREF} \rvert$ absolute	-5%	1.6	+5%	V
T_{CT}	CT timing delay	1nF from CT to COM		0.8		sec/nF
I_{CT}	CT timing current	Source/Sink current	6	9	12	uA
T_{DRV-HI}	DRV high rise time	10% to 90%		6		us
DRV_{LO}	DRV low sink current	IGBT gate discharge		20		mA
DRV_{ROL}	DRV off state resistance	DRV < 0.6V		10		Ω
RIN_{CL}	RIN clamp voltage	I_{RIN} = ± 1mA	-0.3		4.4	V
$ROUT_{CL}$	ROUT clamp voltage	I_{ROUT} = ± 1mA	-0.3		4.4	V
SNS_{CL}	SNS clamp voltage	I_{SNS} = ± 1mA	-0.3		4.4	V
I_{LEAK_RIN}	RIN leakage current	-40mV < V_{RIN} <+40mV	-0.05	0	0.05	µA
I_{LEAK_ROUT}	ROUT leakage current	-40mV < V_{ROUT} <+40mV	-0.05	0	0.05	µA
I_{LEAK_SNS}	SNS leakage current	+0.2V < V_{SNS} <+3.8V	-0.05	0	0.05	µA
$TSD_{JUNCTION}$	Thermal Shutdown	Drive pin low		150		°C
TSD_{HYST}	Thermal Hysteresis			25		°C

*Note 2: VAC peak input voltage for Figure 1 circuit load startup = $V_{STARTMAX}$ * (Rsns+Rsref)/(Rsref) peak = ~ 438Vpk = ~310V RMS*
*Note 3: VAC peak input voltage for Figure 1 load isolation = OVP_{TRIP} * (Rsns+Rsref)/(Rsref) peak = ~ 467V peak = ~ 330V RMS*

Typical Device Characteristics T_{AMB} = 25°C unless otherwise noted

Figure 3: VCC operating current (uA)

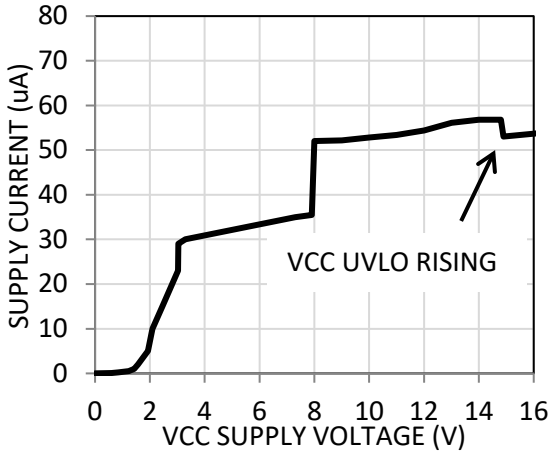


Figure 4: VCC clamping current (mA DC)

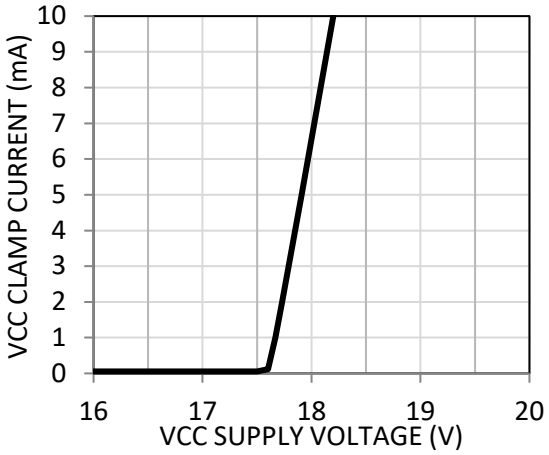


Figure 5: RIN/ROUT/SNS Clamping

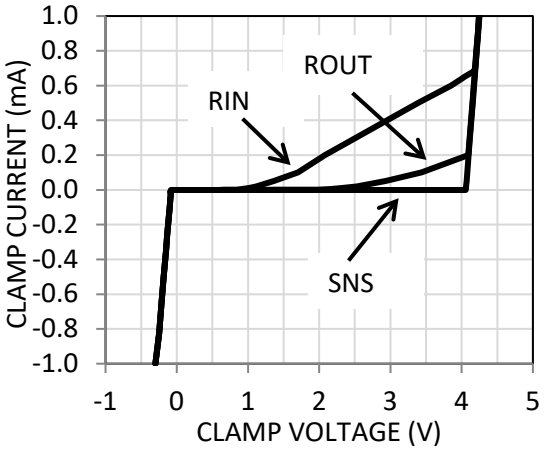


Figure 6: Normalized OVP threshold vs Temperature

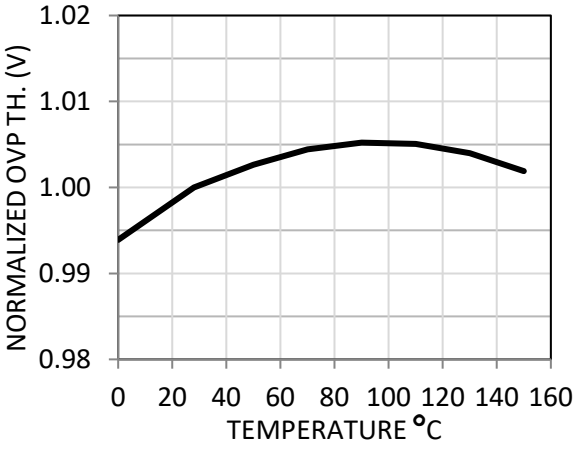


Figure 7: DRV transient turn-on (10nF load)

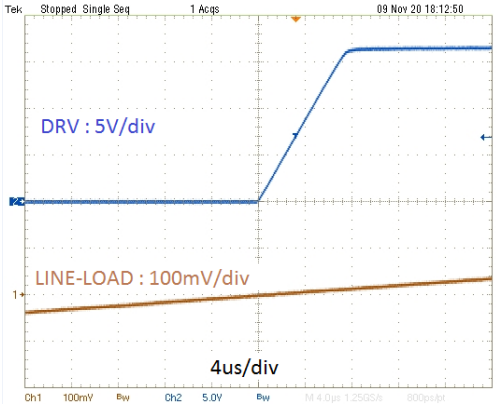


Figure 8: DRV transient turn-off (10nF load)

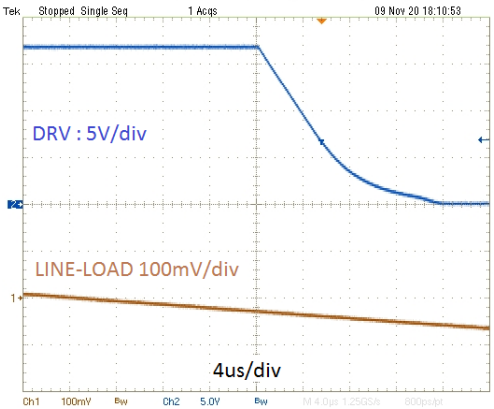
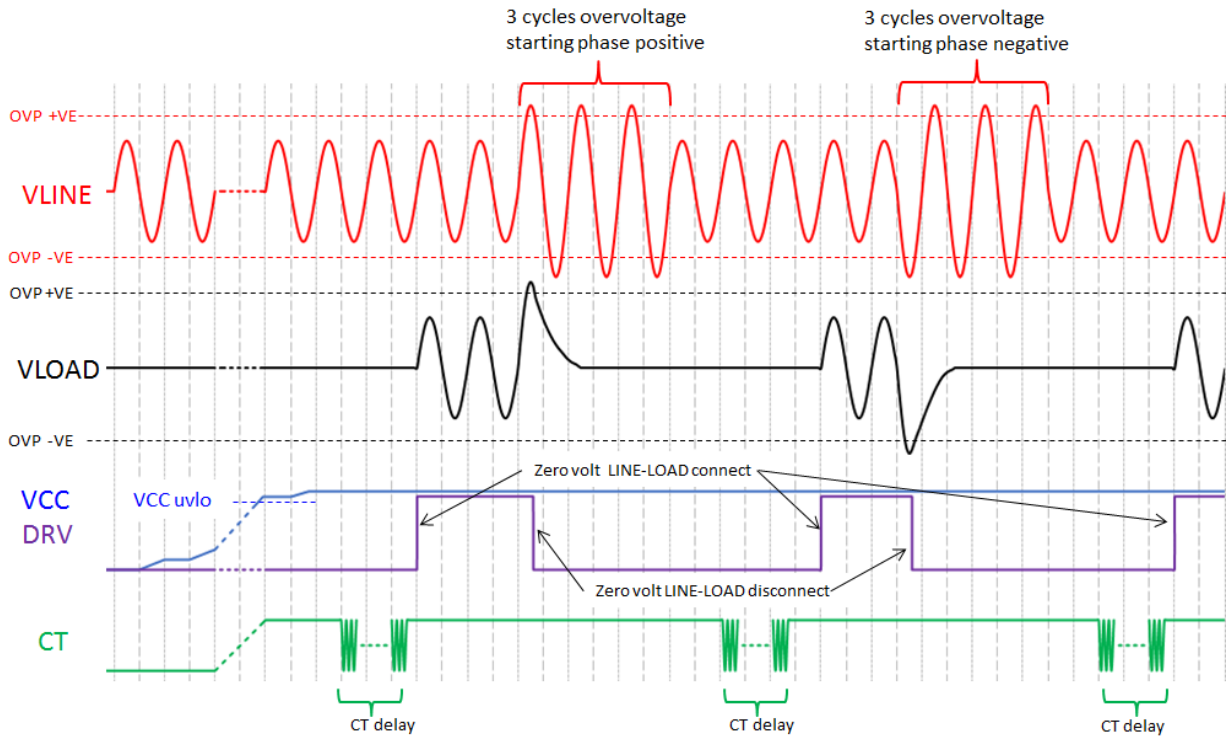


Figure 9: Over-Voltage Protection Timing Diagram Example



DETAILED OPERATING DESCRIPTION

Introduction

The SBT3000 is an AC switch controller, which automatically disconnects the incoming AC power whenever unsafe over-voltages are detected that ultimately prevents the load from sustained operation beyond its maximum ratings. Once the incoming AC power voltage has stabilized back to within safe levels, the load is reconnected and normal operation resumes. To avoid any excessive in-rush currents or inductive "kick-back" spikes, the AC switch 'connect/disconnect' is always synchronized to when voltage across the AC switch is zero (i.e. zero volt Line to Load condition). Both, the over-voltage-protection (OVP) level and stabilization timer interval (CT delay), are user adjustable via external component values, CT and RSNS.

Vcc pin of the SBT3000 is the supply bias voltage and contains UVLO (undervoltage lockout) circuitry to prevent operation until adequate voltage is available to drive the external IGBT's (VCC UVLO is nominally 14.6V rising and 13.3V falling). The typical input supply bias current needed to exceed UVLO is only 60uA rms, at which point the device can begin normal operation. Using the component values as shown in the Figure 1 (Rcc of 360k), the UVLO level can be achieved at around $60V_{rms}$ of VAC input.

Selecting alternative, higher or lower, values for Rcc bias resistor will accordingly adjust the nominal VAC input voltage at which the UVLO level is achieved. Any additional Icc current injected into the Vcc pin will be safely clamped once VCC rises to 17.5V. The peak VCC pin current is recommended to be less than 10mA.

SREF pin contains an internal 2V regulator to provide an accurate AC reference for sensing overvoltage events. The SREF pin requires an external capacitor (22uf ~ 47uF range) to the COM pin along with and external resistor (9KΩ ~ 11KΩ range) to the SNS pin.

The 2V bias reference at the SREF pin, does result in a small offset shift from the nominal OVP target setting. Positive OVP events will typically trigger 2V lower than the design target and negative OVP events will trigger 2V higher. For OVP settings of around 330V RMS (267V peak), this equates to less than 0.5% shift from nominal design target.

RIN/ROUT pins contain the necessary circuitry to detect the zero-voltage condition across the AC switch, which synchronizes the AC switch turn-on/off events. In addition, both RIN/ROUT pins incorporate active current clamp circuitry to ensure their voltage levels are contained within safe operating levels.

The maximum current clamping level, into either pin, is whenever the AC switch is in the off condition and occurs at VAC peak positive phase for RIN pin and at VAC peak negative phase for ROUT pin.

With current clamping levels in excess of 1mA, the external resistors for RIN/ROUT resistor values should be chosen in the range of 2.2MΩ to 3.3MΩ, which allows VAC peak voltages of beyond 2kV to be accommodated. The pin capacitance of RIN and ROUT is around 5pF, which results in a time constant delay of ~ 15us when 3.3MΩ external resistors are used.

SNS pin is the over-voltage-protection sense input voltage and is referenced back to the SREF pin via a 10kΩ nominal resistor. For initial start-up, or for over-voltage recovery, the peak voltage difference between SNS and SREF must be within the ±1.5V range, after which the AC-switch turn-on sequence will commence.

When the device is in normal operation, with AC-switch turned-on, an over-voltage event will be detected if the peak voltage difference between SNS and SREF exceeds the range of ±1.6V (i.e. SNS input voltage exceeds 3.6V or falls below 0.4V), at which point the AC switch is turned-off upon the next zero volt Line to Load event. A phase positive over-voltage event, will turn-off the AC-switch on the falling edge of Line to Load zero voltage and a negative phase over-voltage event will turn-off the AC-switch on a rising edge of Line to Load zero voltage.

Start-up VAC peak < 1.5V x (Rsns + Rsref)/Rsref (V)

OVP trip VAC peak > 1.6V x (Rsns + Rsref)/Rsref (V)

For the component values as shown in Figure 1, this equates to:

Start-up VAC peak < 1.5V x 2920k/10k = 438 (V)
< 315V RMS

OVP trip VAC peak > 1.6V x 2920k/10k = 467 (V)
> 330V RMS

The SNS pin input also contains internal active current clamping circuitry in the event of extreme over-voltage conditions that can safely clamp current level in excess of 1mA.

CT pin allows the user to set a pre-determined timer interval (CT delay) in which the VAC voltage must remain stabilized below the maximum start-up voltage. The timer begins operating after one full cycle of the VAC being within the start-up voltage range. This applies to both initial power up condition and also for OVP recovery. An external capacitor connected from CT pin to COM pin determines the overall duration of the timer.

The CT timing circuitry contains an internal pull-down current of 9uA followed by a pull-up current of 9uA, sequentially ramps the external capacitor between 3.7V and 0.3V and back to 3.7V. This sequence continues for 1024 cycles to produce an overall timer coefficient of 0.8sec/nF. The timer equation is:

Interval (sec) = # cycles x Vramp x 2 x CT (F) / Iramp

= 1024 x 3.4 x 2 x CT (F) / 9u = 0.774 sec/nF

Once the timer interval has completed, the AC-switch will be synchronized to turn-on at the next zero voltage rising edge of Line to Load voltage.

If, at any point during the timer interval, VAC exceeds its allowed start-up voltage the timer interval will be reset and wait for the next full cycle of VAC being back within its start-up voltage, after which the timer will be reactivated again.

DRV pin of the SBT3000 delivers the necessary voltage to adequately drive the external high voltage back-to-back IGBT's which form the AC-switch. The internal circuitry contains an Nfet 'voltage follower', which drives the output to within 0.75V of VCC voltage. Under heavy VCC current clamping conditions, the DRV voltage output will be typically rise 17.5V, and during VCC falling back to UVLO level, the DRV voltage output will be 13V.

Because the AC-switch turn-on/off is always synchronized to its zero-voltage condition, it is not critical to drive the IGBT's extremely fast.

For IGBT turn-on events, the DRV output ramps smoothly over a 6µs time interval, irrespective of the external capacitive load. For IGBT turn-off events, the DRV pin discharges via a 20mA current sink, which safely drives the IGBT's to their 'off' state within 8µs and once the DRV voltage falls below 0.6V, 10Ω internal pull-down is activated.

Internally, the DRV circuitry also contains a power diode which allows reverse current to flow from DRV pin back to VCC pin. This ensures that during initial power-up of the SBT3000, when VCC is still/near zero volts, the DRV voltage output will always remain low enough to prevent IGBT turn-on conditions.

THERMAL DISSIPATION of the SBT3000 is dominated by the VCC clamping current levels involved.

Consider the maximum conditions of Table 3, where the ambient operating temperature is +105°C and the clamping current into VCC is a half-sine wave of 10mA maximum peak. The VCC voltage would typically be 18V and the average clamping current would be 3.75mA (50% x 10mA / √2).
The average power dissipation will be:

Pdiss = 18V x 3.75mA = 68mW

Using the SOIC-8 package junction to ambient thermal resistance (ThetaJA) of 170°C /W, the resulting junction temperature with 68mW dissipation at +105°C ambient would be:

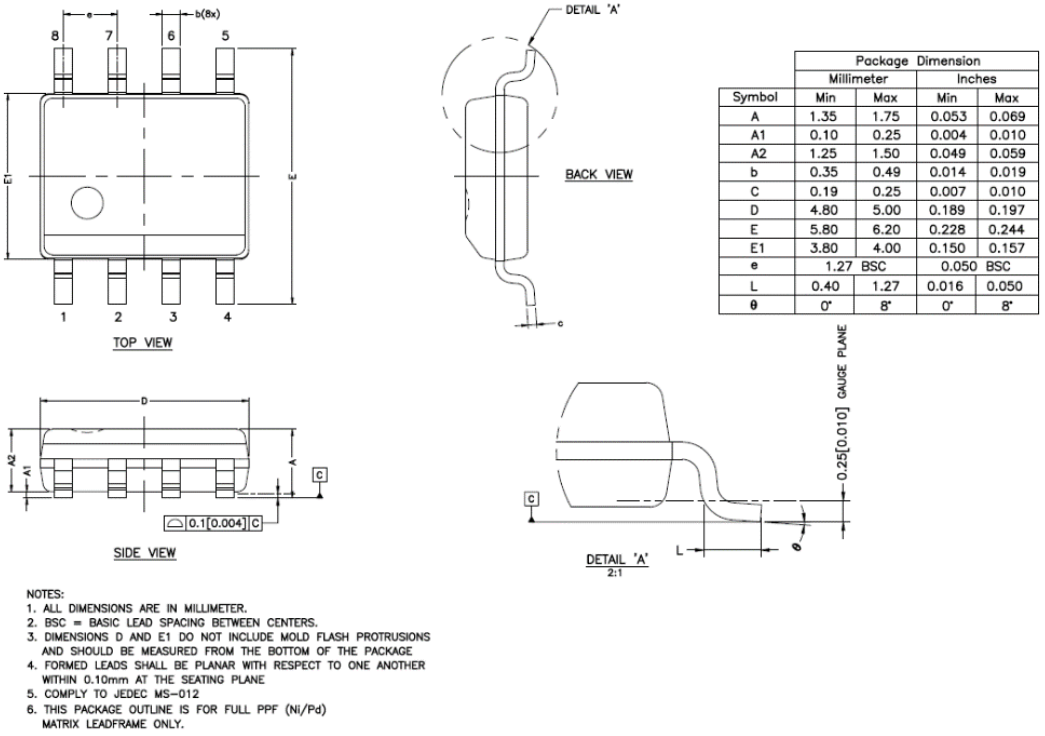
Tjunct = Pdiss x ThetaJA + Tambient

= 68mW x 170 ℃ /W + 105 ℃

= 12 ℃ + 105 ℃ = 117 ℃

In the unusual event of thermal overload, where the junction reaches 150°C, the load will be isolated upon the next falling edge of Line to Load zero voltage event. Once the junction temperature falls back below 125°C, the normal start-up sequence will commence.

SBT3000 SOIC-8 Package Dimensions



Symbol	Package Dimension			
	Millimeter		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.50	0.049	0.059
b	0.35	0.49	0.014	0.019
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. BSC = BASIC LEAD SPACING BETWEEN CENTERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS AND SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.10mm AT THE SEATING PLANE
5. COMPLY TO JEDEC MS-012
6. THIS PACKAGE OUTLINE IS FOR FULL PPF (Ni/Pd) MATRIX LEADFRAME ONLY.

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