

# Approval Sheet

|                       |                           |
|-----------------------|---------------------------|
| Customer              |                           |
| Product Number        | M5U0-AGM2JAVP             |
| Data Rate             | 4800 MT/s                 |
| Pin                   | 288 pin                   |
| CI-tRCD-tRP           | 40-39-39                  |
| Operating temperature | Tc=-40 to 105°C           |
| Date                  | 23 <sup>th</sup> May 2023 |

Rev 1.0

## 1. Features

- JEDEC Standard 288-pin Dual In-Line Memory Module
- VDD=VDDQ= 1.1V (1.067V ~ 1.166V)
- VPP=1.8V (1.746V ~ 1.908V)
- VDDSPD= 1.8V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42
- tREFI 3.9us for  $-40^{\circ}\text{C} \leq T_{\text{case}} < 85^{\circ}\text{C}$ , tREFI 1.95us for  $85^{\circ}\text{C} < T_{\text{case}} \leq 105^{\circ}\text{C}$
- On-Die ECC
- PMIC on DIMM, nominal supply 5V, VIN\_Bulk input supply range: 4.25 V to 5.5 V
- Fly-by topology
- I3C/I2C support
- Terminated control and C/A bus
- SPD EEPROM Hub and Integrated Thermal Sensor
- Halogen-free

### Specification

| Density | Data Rate | IC Configuration | DIMM Organization | Number of IC | Number of rank | Side | ECC |
|---------|-----------|------------------|-------------------|--------------|----------------|------|-----|
| 16GB    | 4800 MT/s | 2Gx8 (16Gb)      | 2Gx64             | 8            | 1              | 1    | N   |

### Key timing parameters

| tCK<br>(ns) | tRCD<br>(ns) | tRP<br>(ns) | tRAS<br>(ns) | tRC<br>(ns) |
|-------------|--------------|-------------|--------------|-------------|
| 0.416       | 16.00        | 16.00       | 32           | 48.00       |

### tRFC parameter by IC Configuration

| Parameter  | IC Configuration |      |      |      | Unit |
|------------|------------------|------|------|------|------|
|            | 8Gb              | 16Gb | 24Gb | 32Gb |      |
| tRFC1,min  | 195              | 295  | TBD  | TBD  | ns   |
| tRFC2,min  | 130              | 160  | TBD  | TBD  | ns   |
| tRFCsb,min | 115              | 130  | TBD  | TBD  | ns   |

## 2. Pin Assignments

| 288-Pin DDR5 UDIMM Front |          |     |          |     |          |     |          | 288-Pin DDR5 UDIMM Back |          |     |          |     |          |     |          |
|--------------------------|----------|-----|----------|-----|----------|-----|----------|-------------------------|----------|-----|----------|-----|----------|-----|----------|
| Pin                      | Symbol   | Pin | Symbol   | Pin | Symbol   | Pin | Symbol   | Pin                     | Symbol   | Pin | Symbol   | Pin | Symbol   | Pin | Symbol   |
| 1                        | VIN_BULK | 37  | DQ20_A   | 73  | CK0_A_c  | 109 | Vss      | 145                     | VIN_BULK | 181 | DQ22_A   | 217 | CK1_A_c  | 253 | Vss      |
| 2                        | RFU      | 38  | Vss      | 74  | Vss      | 110 | DQ5_B    | 146                     | VIN_BULK | 182 | Vss      | 218 | Vss      | 254 | DQ7_B    |
| 3                        | RFU      | 39  | DQ21_A   | 75  | RFU      | 111 | Vss      | 147                     | PWR_GOOD | 183 | DQ23_A   | 219 | RFU      | 255 | Vss      |
| 4                        | HSCL     | 40  | Vss      | 76  | RFU      | 112 | DQ8_B    | 148                     | HAS      | 184 | Vss      | 220 | RFU      | 256 | DQ10_B   |
| 5                        | HSDA     | 41  | DQ24_A   | 77  | Vss      | 113 | Vss      | 149                     | RFU      | 185 | DQ26_A   | 221 | Vss      | 257 | Vss      |
| 6                        | Vss      | 42  | Vss      | 78  | CK0_B_t  | 114 | DQ9_B    | 150                     | Vss      | 186 | Vss      | 222 | CK1_B_t  | 258 | DQ11_B   |
| 7                        | RFU      | 43  | DQ25_A   | 79  | CK0_B_c  | 115 | Vss      | 151                     | PWR_EN   | 187 | DQ27_A   | 223 | CK1_B_c  | 259 | Vss      |
| 8                        | Vss      | 44  | Vss      | 80  | Vss      | 116 | DM1_B_n  | 152                     | RFU      | 188 | Vss      | 224 | Vss      | 260 | DQS1_B_c |
| 9                        | DQ0_A    | 45  | DM3_A_n  | 81  | RFU      | 117 | Vss      | 153                     | Vss      | 189 | DQS3_A_c | 225 | RFU      | 261 | DQS1_B_t |
| 10                       | Vss      | 46  | Vss      | 82  | CA12_B   | 118 | DQ12_B   | 154                     | DQ2_A    | 190 | DQS3_A_t | 226 | RFU      | 262 | Vss      |
| 11                       | DQ1_A    | 47  | DQ28_A   | 83  | Vss      | 119 | Vss      | 155                     | Vss      | 191 | Vss      | 227 | Vss      | 263 | DQ14_B   |
| 12                       | Vss      | 48  | Vss      | 84  | CA10_B   | 120 | DQ13_B   | 156                     | DQ3_A    | 192 | DQ30_A   | 228 | CA11_B   | 264 | Vss      |
| 13                       | DQS0_A_c | 49  | DQ29_A   | 85  | CA8_B    | 121 | Vss      | 157                     | Vss      | 193 | Vss      | 229 | CA9_B    | 265 | DQ15_B   |
| 14                       | DQS0_A_t | 50  | Vss      | 86  | Vss      | 122 | DQ16_B   | 158                     | DM0_A_n  | 194 | DQ31_A   | 230 | Vss      | 266 | Vss      |
| 15                       | Vss      | 51  | CB0_A    | 87  | CA6_B    | 123 | Vss      | 159                     | Vss      | 195 | Vss      | 231 | CA7_B    | 267 | DQ18_B   |
| 16                       | DQ4_A    | 52  | Vss      | 88  | CA4_B    | 124 | DQ17_B   | 160                     | DQ6_A    | 196 | CB2_A    | 232 | CA5_B    | 268 | Vss      |
| 17                       | Vss      | 53  | CB1_A    | 89  | Vss      | 125 | Vss      | 161                     | Vss      | 197 | Vss      | 233 | Vss      | 269 | DQ19_B   |
| 18                       | DQ5_A    | 54  | Vss      | 90  | CA2_B    | 126 | DQS2_B_c | 162                     | DQ7_A    | 198 | CB3_A    | 234 | CA3_B    | 270 | Vss      |
| 19                       | Vss      | 55  | DQS4_A_c | 91  | CA0_B    | 127 | DQS2_B_t | 163                     | Vss      | 199 | Vss      | 235 | CA1_B    | 271 | DM2_B_n  |
| 20                       | DQ8_A    | 56  | DQS4_A_t | 92  | Vss      | 128 | Vss      | 164                     | DQ10_A   | 200 | ALERT_n  | 236 | Vss      | 272 | Vss      |
| 21                       | Vss      | 57  | Vss      | 93  | CS0_B_n  | 129 | DQ20_B   | 165                     | Vss      | 201 | Vss      | 237 | CS1_B_n  | 273 | DQ22_B   |
| 22                       | DQ9_A    | 58  | CS0_A_n  | 94  | Vss      | 130 | Vss      | 166                     | DQ11_A   | 202 | CS1_A_n  | 238 | Vss      | 274 | Vss      |
| 23                       | Vss      | 59  | Vss      | 95  | RESET_n  | 131 | DQ21_B   | 167                     | Vss      | 203 | Vss      | 239 | DQS4_B_c | 275 | DQ23_B   |
| 24                       | DM1_A_n  | 60  | CA0_A    | 96  | Vss      | 132 | Vss      | 168                     | DQS1_A_c | 204 | CA1_A    | 240 | DQS4_B_t | 276 | Vss      |
| 25                       | Vss      | 61  | CA2_A    | 97  | CB0_B    | 133 | DQ24_B   | 169                     | DQS1_A_t | 205 | CA3_A    | 241 | Vss      | 277 | DQ26_B   |
| 26                       | DQ12_A   | 62  | Vss      | 98  | Vss      | 134 | Vss      | 170                     | Vss      | 206 | Vss      | 242 | CB2_B    | 278 | Vss      |
| 27                       | Vss      | 63  | CA4_A    | 99  | CB1_B    | 135 | DQ25_B   | 171                     | DQ14_A   | 207 | CA5_A    | 243 | Vss      | 279 | DQ27_B   |
| 28                       | DQ13_A   | 64  | CA6_A    | 100 | Vss      | 136 | Vss      | 172                     | Vss      | 208 | CA7_A    | 244 | CB3_B    | 280 | Vss      |
| 29                       | Vss      | 65  | Vss      | 101 | DQ0_B    | 137 | DM3_B_n  | 173                     | DQ15_A   | 209 | Vss      | 245 | Vss      | 281 | DQS3_B_c |
| 30                       | DQ16_A   | 66  | CA8_A    | 102 | Vss      | 138 | Vss      | 174                     | Vss      | 210 | CA9_A    | 246 | DQ2_B    | 282 | DQS3_B_t |
| 31                       | Vss      | 67  | CA10_A   | 103 | DQ1_B    | 139 | DQ28_B   | 175                     | DQ18_A   | 211 | CA11_A   | 247 | Vss      | 283 | Vss      |
| 32                       | DQ17_A   | 68  | Vss      | 104 | Vss      | 140 | Vss      | 176                     | Vss      | 212 | Vss      | 248 | DQ3_B    | 284 | DQ30_B   |
| 33                       | Vss      | 69  | CA12_A   | 105 | DQS0_B_c | 141 | DQ29_B   | 177                     | DQ19_A   | 213 | RFU      | 249 | Vss      | 285 | Vss      |
| 34                       | DQS2_A_c | 70  | RFU      | 106 | DQS0_B_t | 142 | Vss      | 178                     | Vss      | 214 | RFU      | 250 | DM0_B_n  | 286 | DQ31_B   |
| 35                       | DQS2_A_t | 71  | Vss      | 107 | Vss      | 143 | RFU      | 179                     | DM2_A_n  | 215 | Vss      | 251 | Vss      | 287 | Vss      |
| 36                       | Vss      | 72  | CK0_A_t  | 108 | DQ4_B    | 144 | RFU      | 180                     | Vss      | 216 | CK1_A_t  | 252 | DQ6_B    | 288 | RFU      |

### 3. Pin Descriptions

| Symbol                   | Type             | I/O Level | Description                   | Symbol                       | Type             | I/O Level | Description                 |
|--------------------------|------------------|-----------|-------------------------------|------------------------------|------------------|-----------|-----------------------------|
| CK_t, CK_c               | Input            | VDDQ      | Clock                         | DQ[31:0]_A<br>DQ[31:0]_B     | Input/<br>Output | VDDQ      | Data Input/Output           |
| CA[12:0]_A<br>CA[12:0]_B | Input            | VDDQ      | Command/Address Inputs        | CB[3:0]_A<br>CB[3:0]_B       | Input/<br>Output | VDDQ      | ECC Check Bits Input/Output |
| CS[1:0]_A<br>CS[1:0]_B   | Input            | VDDQ      | Chip Select                   | DQS[4:0]_A_t<br>DQS[4:0]_B_t | Input/<br>Output | VDDQ      | Data Strobe                 |
| ALERT_n                  | Output           | VDDQ      | Alert                         | DQS[4:0]_A_c<br>DQS[4:0]_B_c | Input/<br>Output | VDDQ      | Data Strobe                 |
| RESET_n                  | CMOS<br>Input    | VDDQ      | Active Low Asynchronous Reset | DM[3:0]_A_n<br>DM[3:0]_B_n   | Input            | VDDQ      | Input Data Mask             |
| PWR_GOOD                 | Input/<br>Output | VDDQ      | Power Good Indicator          | VIN_BULK                     | Supply           |           | External Power Supply       |
| HSCL                     | Input            | VOUT      | Host Sideband Bus Clock       | PWR_EN                       | Input            |           | PMIC Enable                 |
| HSDA                     | Input/<br>Output | VOUT      | Host Sideband Bus Data        | VSS                          | Supply           |           | Ground                      |
| HSA                      | Input            | GND       | Host Sideband Bus Device ID   | RFU                          |                  |           | Reserved for future use     |

[illegible]

## 5. Thermal Characteristics

| Symbol           | Parameter             |                        | Rating     | Units | Note    |
|------------------|-----------------------|------------------------|------------|-------|---------|
| T <sub>C</sub>   | Operation Temperature | Normal Operating Temp. | -40 to 85  | °C    | 1,2,3   |
|                  |                       | Extended Temp.         | 85 to 105  | °C    | 1,2,3,4 |
| T <sub>STG</sub> | Storage Temperature   |                        | -55 to 100 | °C    | 5       |

**Note:**

- Maximum operating case temperature; T<sub>C</sub> is measured in the center of the package.
- A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T<sub>C</sub> during operation.
- Device functionality is not guaranteed if the DRAM device exceeds the maximum T<sub>C</sub> during operation.
- If T<sub>C</sub> exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95μs interval refresh rate.
- Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

## 6. IDD, IDDQ and IPP Specifications

| Symbol | Description                                    | Value    |          | Units |
|--------|------------------------------------------------|----------|----------|-------|
|        |                                                | IDD Max. | IPP Max. |       |
| IDD0   | Operating One Bank Active-Precharge Current    | 872      | 72       | mA    |
| IDD0F  | Operating Four Bank Active-Precharge Current   | 272      | 88       | mA    |
| IDD2N  | Precharge Standby Current                      | 792      | 56       | mA    |
| IDD2P  | Precharge Power-Down Current                   | 760      | 56       | mA    |
| IDD3N  | Active Standby Current                         | 1224     | 64       | mA    |
| IDD3P  | Active Power-Down Current                      | 1208     | 64       | mA    |
| IDD4R  | Operating Burst Read Current                   | 3104     | 80       | mA    |
| IDD4W  | Operating Burst Write Current                  | 2880     | 304      | mA    |
| IDD5B  | Burst Refresh Current (Normal Refresh Mode)    | 2304     | 232      | mA    |
| IDD5C  | Burst Refresh Current (Same Bank Refresh Mode) | 1144     | 104      | mA    |
| IDD6E  | Self Refresh Current                           | 2072     | 256      | mA    |
| IDD7   | Operating Bank Interleave Read Current         | 4088     | 192      | mA    |
| IDD8   | Maximum Power Saving Deep Power Down Current   | 696      | 56       | mA    |

## 7. Timing Parameters

| Parameter                                                                               | Symbol     | 4400                    |     | 4800                    |     | 5200                    |     | Unit |
|-----------------------------------------------------------------------------------------|------------|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|
|                                                                                         |            | Min                     | Max | Min                     | Max | Min                     | Max |      |
| Clock Timing                                                                            |            |                         |     |                         |     |                         |     |      |
| Average clock period                                                                    | tCK,AVG    | 0.454                   |     | 0.416                   |     | 0.384                   |     | ns   |
| Command and Address Timing                                                              |            |                         |     |                         |     |                         |     |      |
| Read to Read command delay for same bank group                                          | tCCD_L     | 8nCK,5ns<br>(MAX)       |     | 8nCK,5ns<br>(MAX)       |     | 8nCK,5ns<br>(MAX)       |     | nCK  |
| WRITE to WRITE command delay for same bank group                                        | tCCD_L_WR  | 32nCK,<br>20ns<br>(MAX) |     | 32nCK,<br>20ns<br>(MAX) |     | 32nCK,<br>20ns<br>(MAX) |     | nCK  |
| WRITE to WRITE command delay for same bank group, second WRITE not RMW                  | tCCD_L_WR2 | 16nCK,<br>10ns<br>(MAX) |     | 16nCK,<br>10ns<br>(MAX) |     | 16nCK,<br>10ns<br>(MAX) |     | nCK  |
| Read to Read or Write to Write command delay for different bank group for BL16, BC8 OTF | tCCD_S     | 8                       |     | 8                       |     | 8                       |     | nCK  |
| ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size            | tRRD_S,2K  | 8                       |     | 8                       |     | 8                       |     | nCK  |
| ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size            | tRRD_S,1K  | 8                       |     | 8                       |     | 8                       |     | nCK  |
| ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size                 | tRRD_L,2K  | 8nCK,5ns<br>(MAX)       |     | 8nCK,5ns<br>(MAX)       |     | 8nCK,5ns<br>(MAX)       |     | nCK  |
| ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size                 | tRRD_L,1K  | 8nCK,5ns<br>(MAX)       |     | 8nCK,5ns<br>(MAX)       |     | 8nCK,5ns<br>(MAX)       |     | nCK  |
| Four activate window for                                                                | tFAW,2K    | 40nCK,                  |     | 40nCK,                  |     | 40nCK,                  |     | ns   |

|                                                                                                                       |         |                             |  |                             |  |                             |  |     |
|-----------------------------------------------------------------------------------------------------------------------|---------|-----------------------------|--|-----------------------------|--|-----------------------------|--|-----|
| 2KB page size                                                                                                         |         | 18.160ns<br>(MAX)           |  | 16.640ns<br>(MAX)           |  | 15.360ns<br>(MAX)           |  |     |
| Four activate window for<br>1KB page size                                                                             | tFAW,1K | 32nCK,<br>14.528ns<br>(MAX) |  | 32nCK,<br>13.312ns<br>(MAX) |  | 32nCK,<br>12.288ns<br>(MAX) |  | ns  |
| Delay from start of internal<br>WRITE transaction to<br>internal READ command<br>for different bank group             | tWTR_S  | 4nCK,<br>2.5ns<br>(MAX)     |  | 4nCK,<br>2.5ns<br>(MAX)     |  | 4nCK,<br>2.5ns<br>(MAX)     |  | ns  |
| Delay from start of internal<br>WRITE transaction to<br>internal READ command<br>for same bank group                  | tWTR_L  | 16nCK,<br>10ns<br>(MAX)     |  | 16nCK,<br>10ns<br>(MAX)     |  | 16nCK,<br>10ns<br>(MAX)     |  | ns  |
| Delay from start of internal<br>WRITE transaction to<br>internal READ with AUTO<br>PRECHARGE command for<br>same bank | tWTRA   | tWR-tRTP                    |  | tWR-tRTP                    |  | tWR-tRTP                    |  | ns  |
| Internal READ command<br>to PRECHARGE command<br>delay                                                                | tRTP    | 12nCK,<br>7.5ns<br>(MAX)    |  | 12nCK,<br>7.5ns<br>(MAX)    |  | 12nCK,<br>7.5ns<br>(MAX)    |  | ns  |
| PRECHARGE to PRECHARGE<br>delay                                                                                       | tPPD    | 2                           |  | 2                           |  | 2                           |  | nCK |
| WRITE recovery time                                                                                                   | tWR     | 29.964                      |  | 29.952                      |  | 29.952                      |  | ns  |
| DLL locking time                                                                                                      | tDLLK   | 1280                        |  | 1536                        |  | 1536                        |  | nCK |
| <b>Mode Register Read/Write Timing</b>                                                                                |         |                             |  |                             |  |                             |  |     |
| Mode register READ command<br>period                                                                                  | tMRR    | 14ns,<br>16nCK<br>(MAX)     |  | 14ns,<br>16nCK<br>(MAX)     |  | 14ns,<br>16nCK<br>(MAX)     |  |     |
| Mode register READ pattern<br>to mode register<br>READ pattern command<br>spacing                                     | tMRR_p  | 8                           |  | 8                           |  | 8                           |  | nCK |
| Mode register WRITE command<br>period                                                                                 | tMRW    | 5ns,8nCK<br>(MAX)           |  | 5ns,8nCK<br>(MAX)           |  | 5ns,8nCK<br>(MAX)           |  |     |
| Mode register SET command<br>delay                                                                                    | tMRD    | 14ns,<br>16nCK              |  | 14ns,<br>16nCK              |  | 14ns,<br>16nCK              |  |     |

|                                                                                                                             |                   |                              |                             |                              |                             |                              |                             |     |
|-----------------------------------------------------------------------------------------------------------------------------|-------------------|------------------------------|-----------------------------|------------------------------|-----------------------------|------------------------------|-----------------------------|-----|
|                                                                                                                             |                   | (MAX)                        |                             | (MAX)                        |                             | (MAX)                        |                             |     |
| DFE mode register WRITE<br>update delay time                                                                                | tDFE              | 80                           |                             | 80                           |                             | 80                           |                             | ns  |
| <b>Data Strobe Timing</b>                                                                                                   |                   |                              |                             |                              |                             |                              |                             |     |
| DQS_t, DQS_c differential<br>READ preamble                                                                                  | tRPRE             | TBD                          |                             | TBD                          |                             | TBD                          |                             | tCK |
| DQS_t, DQS_c differential<br>READ postamble                                                                                 | tRPST             | TBD                          |                             | TBD                          |                             | TBD                          |                             | tCK |
| DQS_t, DQS_c rising edge<br>output timing location<br>from rising CK_t, CK_c                                                | tDQSCK            | -0.286                       | 0.286                       | -0.3                         | 0.3                         | TBD                          | TBD                         | tCK |
| DQS_t, DQS_c rising edge<br>output variance window                                                                          | tDQSCKI           |                              | 0.475                       |                              | 0.49                        |                              | TBD                         | tCK |
| <b>Data Strobe Timing</b>                                                                                                   |                   |                              |                             |                              |                             |                              |                             |     |
| 2-tCK WRITE preamble enable<br>window                                                                                       | tWPRE_EN_2<br>tCK | 1.5                          |                             | 1.5                          |                             | 1.5                          |                             | tCK |
| 3-tCK WRITE preamble enable<br>window                                                                                       | tWPRE_EN_3<br>tCK | 2.5                          |                             | 2.5                          |                             | 2.5                          |                             | tCK |
| 4-tCK WRITE preamble enable<br>window                                                                                       | tWPRE_EN_4<br>tCK | 2.5                          |                             | 2.5                          |                             | 2.5                          |                             | tCK |
| DQS_t, DQS_c differential<br>WRITE postamble                                                                                | tWPST             | TBD                          |                             | TBD                          |                             | TBD                          |                             | tCK |
| Final trained value of host<br>DQS_t-DQS_c timing relative<br>to CWL CK_t-CK_c<br>edge                                      | tDQSoffset        | -0.5                         | 0.5                         | -0.5                         | 0.5                         | -0.5                         | 0.5                         | tCK |
| Write leveling setup time                                                                                                   | tWLS              | -80                          | 80                          | -80                          | 80                          | -80                          | 80                          | ps  |
| Write leveling hold time                                                                                                    | tWLH              | -80                          | 80                          | -80                          | 80                          | -80                          | 80                          | ps  |
| Voltage/temperature drift<br>window of first rising<br>DQS_t preamble edge relative<br>to CWL CK_t-CK_c<br>edge (x4/x8/x16) | tDQSD             | -0.25 x<br>tWPRE_E<br>N_ntCK | 0.25 x<br>tWPRE_E<br>N_ntCK | -0.25 x<br>tWPRE_E<br>N_ntCK | 0.25 x<br>tWPRE_E<br>N_ntCK | -0.25 x<br>tWPRE_E<br>N_ntCK | 0.25 x<br>tWPRE_E<br>N_ntCK | tCK |
| Host and system voltage/<br>temperature drift window<br>of first rising DQS_t preamble<br>edge relative to                  | tDQSS             | -0.25 x tWPRE_EN_ntCK        |                             |                              |                             |                              |                             | tCK |

|                                                                    |                  |                         |      |                         |      |                         |      |     |
|--------------------------------------------------------------------|------------------|-------------------------|------|-------------------------|------|-------------------------|------|-----|
| CWL CK_t-CK_c edge<br>(x4/x8/x16)                                  |                  |                         |      |                         |      |                         |      |     |
| <b>MPSM Timing</b>                                                 |                  |                         |      |                         |      |                         |      |     |
| MPSM exit to first valid<br>command delay                          | tMPSMX           | tMRD                    |      | tMRD                    |      | tMRD                    |      | ns  |
| <b>ZQ Calibration Timing</b>                                       |                  |                         |      |                         |      |                         |      |     |
| ZQ calibration time                                                | tZQCAL           | 1                       |      | 1                       |      | 1                       |      | μs  |
| ZQ calibration latch time                                          | tZQLAT           | 30ns,<br>8nCK<br>(MIN)  |      | 30ns,<br>8nCK<br>(MIN)  |      | 30ns,<br>8nCK<br>(MIN)  |      |     |
| <b>Reset Timing</b>                                                |                  |                         |      |                         |      |                         |      |     |
| RESET_n low time for reset<br>initialization with stable<br>power  | tPW_RESET        | 1                       |      | 1                       |      | 1                       |      | μs  |
| Time after RESET_n assertion<br>to ODT off                         | tRST_ADC         |                         | 50   |                         | 50   |                         | 50   | ns  |
| <b>Self Refresh Timing</b>                                         |                  |                         |      |                         |      |                         |      |     |
| Command pass disable delay                                         | tCPDED           | 5ns,8nCK<br>(MAX)       |      | 5ns,8nCK<br>(MAX)       |      | 5ns,8nCK<br>(MAX)       |      |     |
| Self refresh CS_n low pulse<br>width                               | tCSL             | 10                      |      | 10                      |      | 10                      |      | ns  |
| Self refresh exit CS_n high<br>pulse width                         | tCSH_Srexit      | 13                      | 30   | 13                      | 30   | 13                      | 30   | ns  |
| Self refresh exit CS_n low<br>pulse width                          | tCSL_Srexit      | 3nCK                    | 30ns | 3nCK                    | 30ns | 3nCK                    | 30ns |     |
| Self refresh exit CS_n low<br>pulse width with frequency<br>change | tCSL_FreqCh<br>g | VREFCA_<br>time         |      | VREFCA_<br>time         |      | VREFCA_<br>time         |      | ns  |
| Valid clock requirement<br>before SRX                              | tCKSRX           | 3.5ns,<br>8nCK<br>(MAX) |      | 3.5ns,<br>8nCK<br>(MAX) |      | 3.5ns,<br>8nCK<br>(MAX) |      | ns  |
| Valid clock requirement after<br>SRE                               | tCKLCS           | tCPDED +<br>1nCK        |      | tCPDED +<br>1nCK        |      | tCPDED +<br>1nCK        |      | nCK |
| Self refresh exit CS_n HIGH                                        | tCASRX           | 0                       |      | 0                       |      | 0                       |      | ns  |
| Exit self refresh to commands<br>not requiring a                   | tXS              | tRFC1                   |      | tRFC1                   |      | tRFC1                   |      | ns  |

|                                                                           |          |                                                     |                                           |                                                     |                                           |                                                     |                                           |     |
|---------------------------------------------------------------------------|----------|-----------------------------------------------------|-------------------------------------------|-----------------------------------------------------|-------------------------------------------|-----------------------------------------------------|-------------------------------------------|-----|
| locked DLL                                                                |          |                                                     |                                           |                                                     |                                           |                                                     |                                           |     |
| Exit self refresh to commands<br>requiring a locked<br>DLL                | tXS_DLL  | tDLLK                                               |                                           | tDLLK                                               |                                           | tDLLK                                               |                                           | ns  |
| <b>Power-Down Timing</b>                                                  |          |                                                     |                                           |                                                     |                                           |                                                     |                                           |     |
| Command pass disable delay                                                | tCPDED   | 5ns,8nCK<br>(MAX)                                   |                                           | 5ns,8nCK<br>(MAX)                                   |                                           | 5ns,8nCK<br>(MAX)                                   |                                           | ns  |
| Power-down time                                                           | tPD      | 7.5ns,<br>8nCK<br>(MAX)                             | 5*tREFI1<br>(normal)<br>9*tREFI2<br>(FGR) | 7.5ns,<br>8nCK<br>(MAX)                             | 5*tREFI1<br>(normal)<br>9*tREFI2<br>(FGR) | 7.5ns,<br>8nCK<br>(MAX)                             | 5*tREFI1<br>(normal)<br>9*tREFI2<br>(FGR) | ns  |
| Exit power-down to next<br>valid command                                  | tXP      | 7.5ns,<br>8nCK<br>(MAX)                             |                                           | 7.5ns,<br>8nCK<br>(MAX)                             |                                           | 7.5ns,<br>8nCK<br>(MAX)                             |                                           | ns  |
| Timing of ACT command<br>to POWER DOWN ENTRY<br>command                   | tACTPDEN | 2                                                   |                                           | 2                                                   |                                           | 2                                                   |                                           | nCK |
| Timing of PREab, PREsb or<br>PREpb command to POWER<br>DOWN ENTRY command | tPRPDEN  | 2                                                   |                                           | 2                                                   |                                           | 2                                                   |                                           | nCK |
| Timing of READ or READ<br>w/ AP command to POWER<br>DOWN ENTRY command    | tRDPDEN  | CL<br>+RBL/2+1                                      |                                           | CL<br>+RBL/2+1                                      |                                           | CL<br>+RBL/2+1                                      |                                           | nCK |
| Timing of WRITE command<br>to POWER DOWN ENTRY<br>command                 | tWRPDEN  | CWL<br>+WBL/ 2+<br>(tWR/<br>tCK(avg))<br>+1         |                                           | CWL<br>+WBL/ 2+<br>(tWR/<br>tCK(avg))<br>+1         |                                           | CWL<br>+WBL/ 2+<br>(tWR/<br>tCK(avg))<br>+1         |                                           | nCK |
| Timing of WRITE w/ AP<br>command to POWER<br>DOWN ENTRY command           | tWRAPDEN | CWL<br>+WBL/<br>2+-0.25 x<br>tWPRES_EN_n<br>tCKWR+1 |                                           | CWL<br>+WBL/<br>2+-0.25 x<br>tWPRES_EN_n<br>tCKWR+1 |                                           | CWL<br>+WBL/<br>2+-0.25 x<br>tWPRES_EN_n<br>tCKWR+1 |                                           | nCK |
| Timing of REFab or REFSb<br>command to POWER<br>DOWN ENTRY command        | tREFPDEN | 2                                                   |                                           | 2                                                   |                                           | 2                                                   |                                           | nCK |
| Timing of MRR command                                                     | tMRPDEN  | CL+8+1                                              |                                           | CL+8+1                                              |                                           | CL+8+1                                              |                                           | nCK |

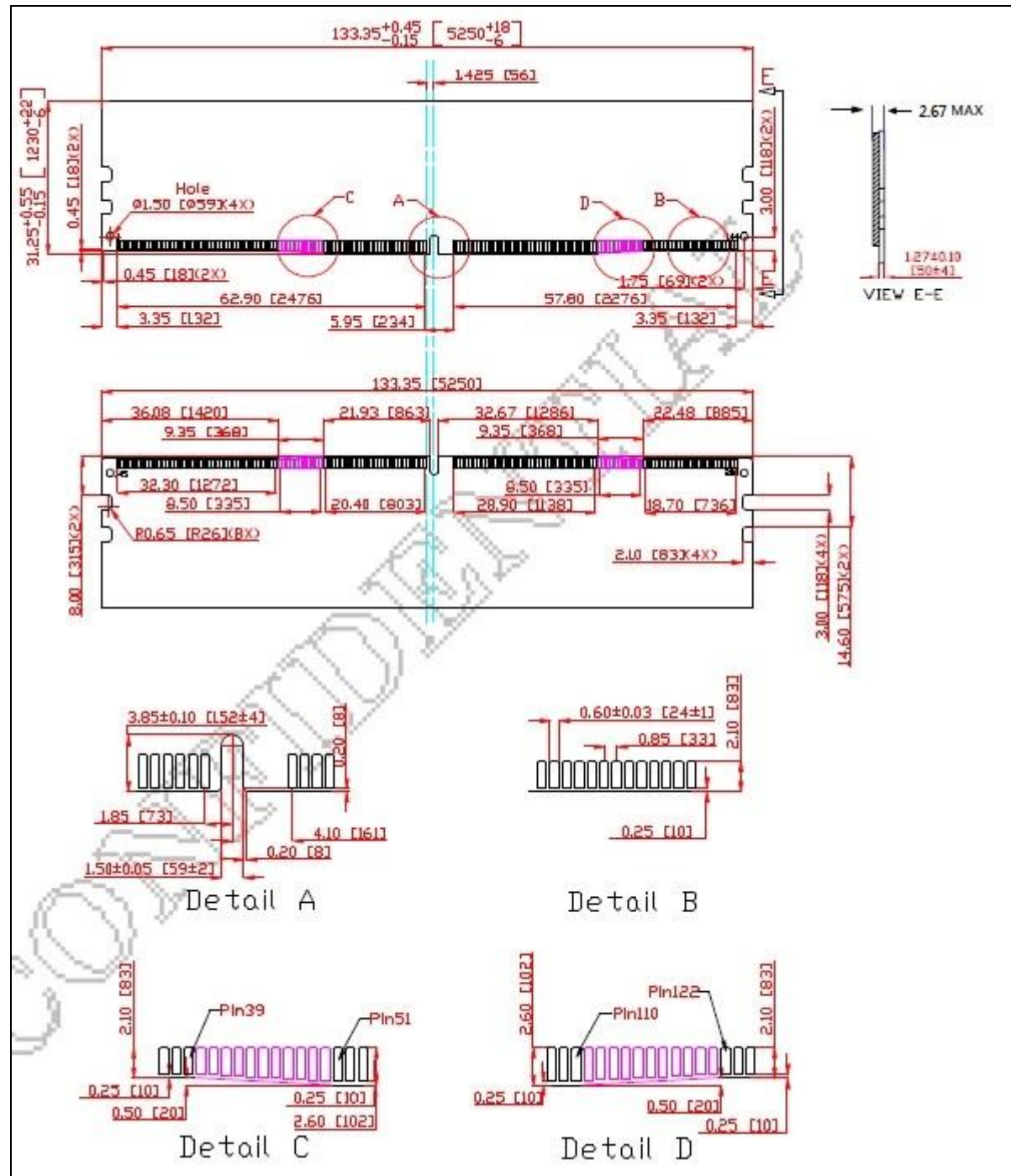
|                                                                                  |                      |                                                 |                         |                                                 |                         |               |                         |     |
|----------------------------------------------------------------------------------|----------------------|-------------------------------------------------|-------------------------|-------------------------------------------------|-------------------------|---------------|-------------------------|-----|
| to POWER DOWN ENTRY<br>command                                                   |                      |                                                 |                         |                                                 |                         |               |                         |     |
| Timing of MRW command<br>to POWER DOWN ENTRY<br>command                          | tMRWPDEN             | tMRD<br>(MIN)                                   |                         | tMRD<br>(MIN)                                   |                         | tMRD<br>(MIN) |                         | nCK |
| Timing of MPC command<br>to POWER DOWN ENTRY<br>command                          | tMPCPDEN             | tMPC_delay                                      |                         | tMPC_delay                                      |                         | tMPC_delay    |                         | nCK |
| <b>MPC Command Timing</b>                                                        |                      |                                                 |                         |                                                 |                         |               |                         |     |
| MPC to any other valid<br>command                                                | tMPC_Delay           | tMRD                                            |                         | tMRD                                            |                         | tMRD          |                         | nCK |
| Time between stable MPC<br>command and first falling<br>CS edge (setup)          | tMC_MPC_Se<br>tup    | 3                                               |                         | 3                                               |                         | 3             |                         | nCK |
| Time between first rising<br>CS edge and stable MPC<br>command (HOLD)            | tMC_MPC_H<br>old     | 3                                               |                         | 3                                               |                         | 3             |                         | nCK |
| Time CS_n is held LOW to<br>register MPC command                                 | tMPC_CS              | 3.5                                             | 8                       | 3.5                                             | 8                       | 3.5           | 8                       | nCK |
| <b>PDA Timing</b>                                                                |                      |                                                 |                         |                                                 |                         |               |                         |     |
| PDA ENUMERATE ID command<br>to any other command<br>cycle                        | tPDA_DELAY           | tPDA_DQ<br>S_DELAY<br>(MAX) +<br>BL/2 +<br>19ns |                         | tPDA_DQ<br>S_DELAY<br>(MAX) +<br>BL/2 +<br>19ns |                         | TBD           |                         | ns  |
| Delay to rising strobe edge<br>used for sampling DQ during<br>PDA operation      | tPDA_DQS_D<br>ELAY   | 5                                               | 18                      | 5                                               | 18                      | TBD           | TBD                     | ns  |
| DQS setup time during<br>PDA operation                                           | tPDA_S               | 3                                               |                         | 3                                               |                         | TBD           |                         | nCK |
| DQS hold time during PDA<br>operation                                            | tPDA_H               | 3                                               |                         | 3                                               |                         | TBD           |                         | nCK |
| <b>Read Training Timing</b>                                                      |                      |                                                 |                         |                                                 |                         |               |                         |     |
| Registration of MRW continuous<br>burst mode exit to<br>next valid command delay | tCont_Exit_<br>Delay |                                                 | tCont_Exit<br>+<br>tMRW |                                                 | tCont_Exit<br>+<br>tMRW |               | tCont_Exit<br>+<br>tMRW | ns  |
| Registration of MRW continuous                                                   | tCont_Exit           |                                                 | CL+BL/                  |                                                 | CL+BL/                  |               | CL+BL/                  | ns  |

|                                                                                                                           |                           |    |                         |    |                         |    |                         |     |
|---------------------------------------------------------------------------------------------------------------------------|---------------------------|----|-------------------------|----|-------------------------|----|-------------------------|-----|
| burst mode exit to                                                                                                        |                           |    | 2+10nCK                 |    | 2+10nCK                 |    | 2+10nCK                 |     |
| end of training mode                                                                                                      |                           |    |                         |    |                         |    |                         |     |
| <b>Read Preamble Timing</b>                                                                                               |                           |    |                         |    |                         |    |                         |     |
| Delay from MRW command<br>to DQS driven                                                                                   | tSDOn                     |    | 12nCK,<br>20ns<br>(MAX) |    | 12nCK,<br>20ns<br>(MAX) |    | 12nCK,<br>20ns<br>(MAX) |     |
| Delay from MRW command<br>to DQS disabled                                                                                 | tSDOff                    |    | 12nCK,<br>20ns<br>(MAX) |    | 12nCK,<br>20ns<br>(MAX) |    | 12nCK,<br>20ns<br>(MAX) |     |
| <b>CA Training Mode Timing</b>                                                                                            |                           |    |                         |    |                         |    |                         |     |
| Registration of CATM entry<br>command to start of<br>training samples time                                                | tCATM_Entry               | 20 |                         | 20 |                         | 20 |                         | ns  |
| Registration of CATM exit<br>CS_n assertion to end of<br>training mode (when DQ is<br>no longer driven by the<br>device). | tCATM_Exit                |    | 14                      |    | 14                      |    | 14                      | ns  |
| Registration of CATM exit<br>to next valid command delay                                                                  | tCATM_Exit_<br>Delay      | 20 |                         | 20 |                         | 20 |                         | ns  |
| Time from sample evaluation<br>to output on DQ bus                                                                        | tCATM_Valid               |    | 20                      |    | 20                      |    | 20                      | ns  |
| Time output is available on<br>DQ bus                                                                                     | tCATM_DQ_<br>Window       | 2  |                         | 2  |                         | 2  |                         | nCK |
| CS_n assertion duration to<br>exit CATM                                                                                   | tCATM_CS_E<br>xit         | 2  | 8                       | 2  | 8                       | 2  | 8                       | nCK |
| Registration of CSTM entry<br>command to start of training<br>samples time                                                | tCSTM_Entry               | 20 |                         | 20 |                         | 20 |                         | ns  |
| Min time between last<br>CS_n pulse and first pulse<br>of MPC command to exit<br>CSTM                                     | tCSTM_Min_<br>to_MPC_exit | 4  |                         | 4  |                         | 4  |                         | nCK |
| Registration of CSTM exit<br>command to end of training<br>mode                                                           | tCSTM_Exit                |    | 20                      |    | 20                      |    | 20                      | ns  |
| Time from sample evaluation                                                                                               | tCSTM_Valid               |    | 20                      |    | 20                      |    | 20                      | ns  |

|                                                                                                                                      |                            |                |     |                |     |                |     |     |
|--------------------------------------------------------------------------------------------------------------------------------------|----------------------------|----------------|-----|----------------|-----|----------------|-----|-----|
| to output on DQ bus                                                                                                                  |                            |                |     |                |     |                |     |     |
| Time output is available on DQ bus                                                                                                   | tCSTM_DQ_ Window           | 2              |     | 2              |     | 2              |     | nCK |
| Registration of CSTM exit to next valid command delay                                                                                | tCSTM_Exit_ Delay          | 20             |     | 20             |     | 20             |     | ns  |
| <b>Write Leveling Timing</b>                                                                                                         |                            |                |     |                |     |                |     |     |
| Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid | tWLPEN                     | 0              | 15  | 0              | 15  | 0              | 15  | ns  |
| Write leveling output delay                                                                                                          | tWLO                       | 0              | 9.5 | 0              | 9.5 | 0              | 9.5 | ns  |
| Write leveling output error                                                                                                          | tWLOE                      | 0              | 2   | 0              | 2   | 0              | 2   | ns  |
| Width of write leveling internal pulse                                                                                               | tWL_Pulse_ Width           | 2              |     | 2              |     | 2              |     | tCK |
| <b>VREFO/VREFC Timing</b>                                                                                                            |                            |                |     |                |     |                |     |     |
| VREFO/VREFC command to any other valid command delay                                                                                 | tVREFO_Delay/ tVREFC_Delay | tMRD           |     | tMRD           |     | tMRD           |     | nCK |
| Time CS_n is held LOW to register VREFO/VREFC command                                                                                | tVREFO_CS/ tVREFC_CS       | 3.5            | 8   | 3.5            | 8   | 3.5            | 8   | nCK |
| <b>hPPR/sPPR Timing</b>                                                                                                              |                            |                |     |                |     |                |     |     |
| hPPR programming time (x4/x8)                                                                                                        | tPGMa                      | 1000           |     | 1000           |     | 1000           |     | ms  |
| hPPR programming time (x16)                                                                                                          | tPGMb                      | 2000           |     | 2000           |     | 2000           |     | ms  |
| sPPR programming time                                                                                                                | tPGM_sPPR                  | CWL +8tCK +tWR |     | CWL +8tCK +tWR |     | CWL +8tCK +tWR |     | tCK |
| hPPR/sPPR recognition time                                                                                                           | tPGM_Exit                  | tRP            |     | tRP            |     | tRP            |     | ns  |
| hPPR program exit and new address setting time                                                                                       | tPGMPST                    | 50             |     | 50             |     | 50             |     | μs  |
| sPPR program exit and new address setting time                                                                                       | tPGMPST_sP PR              | tMRD           |     | tMRD           |     | tMRD           |     | ns  |

| DQS Interval Oscillator Readout Timing                                |                  |                                         |    |                           |    |                           |    |     |
|-----------------------------------------------------------------------|------------------|-----------------------------------------|----|---------------------------|----|---------------------------|----|-----|
| Delay time from DQS interval oscillator stop to mode register readout | tOSCO            | tMPC_De<br>lay                          |    | tMPC_De<br>lay            |    | tMPC_De<br>lay            |    | nCK |
| DQS interval oscillator start gap in automatic stop mode              | tOSCS            | tMPC_Delay + DQS interval timer runtime |    |                           |    |                           |    | nCK |
| ECS Timing                                                            |                  |                                         |    |                           |    |                           |    |     |
| ECS operation time                                                    | tECSc            | 176nCK,<br>110ns<br>(MAX)               |    | 176nCK,<br>110ns<br>(MAX) |    | 176nCK,<br>110ns<br>(MAX) |    |     |
| CRC Error Reporting Timing                                            |                  |                                         |    |                           |    |                           |    |     |
| CRC error to ALERT_n_latency                                          | tCRC_ALERT       | 3                                       | 13 | 3                         | 13 | 3                         | 13 | ns  |
| CRC ALERT_n pulse width                                               | CRC_ALERT_<br>PW | 12                                      | 20 | 12                        | 20 | 12                        | 20 | nCK |

## 8. Module Dimensions



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of  $\pm 0.15$  (6), unless otherwise specified.

## 9. RoHS Declaration

|                                                                                                                                                                                                                                                         |                                           |          |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|----------|
| innodisk                                                                                                                                                                                                                                                | 宜鼎國際股份有限公司<br><b>Innodisk Corporation</b> | Page 1/2 |
| Tel:(02)7703-3000 Internet: <a href="https://www.innodisk.com/">https://www.innodisk.com/</a>                                                                                                                                                           |                                           |          |
| <b>RoHS 自我宣告書 (RoHS Declaration of Conformity)</b>                                                                                                                                                                                                      |                                           |          |
| <b>Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products</b>                                                                                                                                                                               |                                           |          |
| 一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及 (EU) 2015/863 關於 RoHS 之規範要求。<br>Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement. |                                           |          |
| 二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。<br>Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.                                        |                                           |          |
| 三、 本公司聲明我們的產品符合 RoHS 指令的附件中 7(a)、7(c)-I、6(c) 允許豁免。<br>We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.                                                                                      |                                           |          |
| ※ 7(a) Lead in high melting temperature type solders (i.e. lead-based alloys containing 85% by weight or more lead).                                                                                                                                    |                                           |          |
| ※ 7(c)-I Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.                                                  |                                           |          |
| ※ 6(c) Copper alloy containing up to 4% lead by weight.<br>(This exemption applies to products that use antennas)                                                                                                                                       |                                           |          |
| Name of hazardous substance                                                                                                                                                                                                                             | Limited of RoHS ppm (mg/kg)               |          |
| 鉛 (Pb)                                                                                                                                                                                                                                                  | < 1000 ppm                                |          |
| 汞 (Hg)                                                                                                                                                                                                                                                  | < 1000 ppm                                |          |
| 鎘 (Cd)                                                                                                                                                                                                                                                  | < 100 ppm                                 |          |
| 六價鉻 (Cr 6+)                                                                                                                                                                                                                                             | < 1000 ppm                                |          |
| 多溴聯苯 (PBBs)                                                                                                                                                                                                                                             | < 1000 ppm                                |          |
| 多溴二苯醚 (PBDEs)                                                                                                                                                                                                                                           | < 1000 ppm                                |          |
| 鄰苯二甲酸二(2-乙基己基)酯 (DEHP)                                                                                                                                                                                                                                  | < 1000 ppm                                |          |
| 鄰苯二甲酸丁酯苯甲酯 (BBP)                                                                                                                                                                                                                                        | < 1000 ppm                                |          |
| 鄰苯二甲酸二丁酯 (DBP)                                                                                                                                                                                                                                          | < 1000 ppm                                |          |

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Page 2/2

|                  |            |
|------------------|------------|
| 鄰苯二甲酸二異丁酯 (DIBP) | < 1000 ppm |
|------------------|------------|

## 立 保 證 書 人 (Guarantor)

Company name 公司名稱: Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人: Randy Chien 簡川勝

Company Representative Title 公司代表人職稱: Chairman 董事長

Date 日期: 2021 / 06 / 09



## 10. REACH Declaration

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宜鼎國際股份有限公司  
Innodisk Corporation  
REACH DeclarationTel: (02) 7703-3000 Fax: (02) 7703-3555 Internet: <https://www.innodisk.com/>

Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006). We hereby confirm that the product(s),

**Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.**

- The standard products of **not listed in the Appendix2** meet the requirements of REACH SVHC regulations (SVHCs < 0.1% in Article), as described in the candidate list table currently including 224 substances and shown on the ECHA website. (<http://echa.europa.eu/de/candidate-list-table>).
- The standard products listed in the **Appendix2** contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table.  
Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs > 0.1% in Article).
- Comply with REACH Annex XVII.

## Guarantor

Company name 公司名稱: Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人:  陳怡全

Company Representative Title 公司代表人職稱: QA Manager 品保經理

Date 日期: 2022 / 06 / 14



## Revision Log

| Rev | Date                      | Modification        |
|-----|---------------------------|---------------------|
| 0.1 | 23 <sup>th</sup> May 2023 | Preliminary Edition |
| 1.0 | 23 <sup>th</sup> May 2023 | Official released   |

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