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EXCEED YOUR VISION

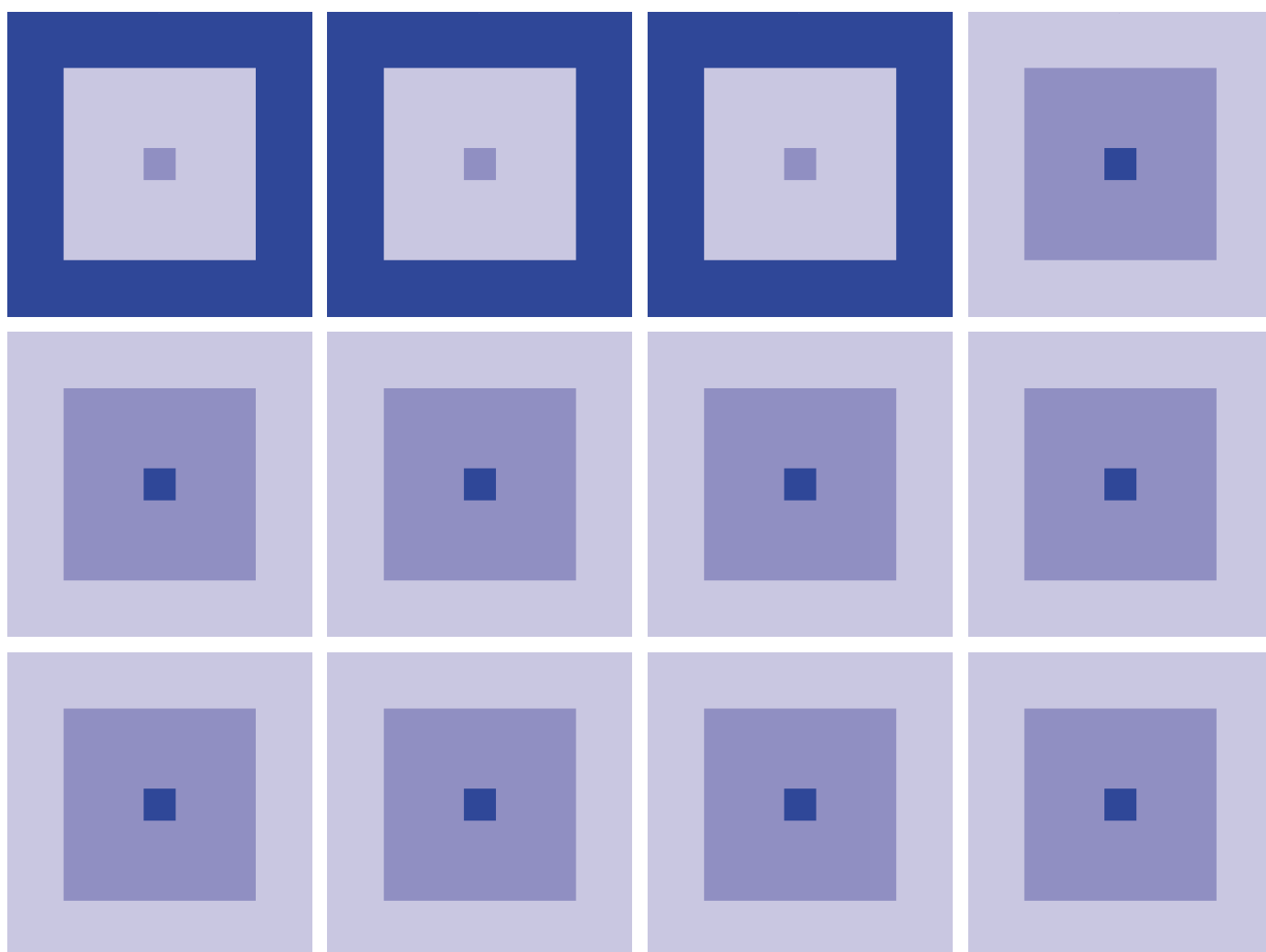# S1D15710 Series
Technical Manual

NOTICE

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S1D15710 Series
Technical Manual

Configuration of product number

●DEVICES

S1　D　15710　D　00B0　00

- Packing specification
- Specifications
- Shape (D:Chip, T:TCP, F:QFP)
- Model number
- Model name (D:LCD Driver)
- Product classification (S1:Semiconductors)

Contents

1. DESCRIPTION

The S1D15710 Series is a single-chip dot matrix liquid crystal display driver that can be connected directly to a microprocessor bus. Eight-bit parallel or serial display data transmitted from the microprocessor is stored in the internal display data RAM, and the chip generates liquid crystal drive signals, independently of the microprocessor.

It has a on-chip 65×256-bit display data RAM, and there is a one-to-one correspondence between the dot pixel on the liquid crystal panel pixels and internal RAM bit. This feature ensures implementation of highly free display.

The S1D15710 Series incorporate 65 common output circuits and 224 segment output circuits. A single chip can drive a 65×224 dot display (capable of displaying 14 columns $\times$ 4 rows with 16×16-dot kanji font). Further, display capacity can be extended by designing two chips in a master/display configuration.

Since both the S1D15710∗10∗∗ and S1D15710∗11∗∗ have built-in analog temperature sensor circuits, systems can be build that can maintain appropriate liquid crystal contrast over a wide temperature range with microcomputer control without requiring such parts as thermostats.

The S1D15710 Series can read and write RAM data with the minimum current consumption because it does not require any external operation clock. Also it incorporates a LCD power supply featuring a very low current consumption, a LCD drive power voltage regulator resistor and a display clock CR oscillator circuit. This allows the display system of a high-performance for handy equipment to be realized at the minimum power consumption and minimum component configuration.

2. FEATURES

- Direct display of RAM data using the display data RAM
  RAM bit data "1" .... goes on.
  "0" .... goes off (at display normal rotation).
- RAM capacity
  $65 \times 256 = 16,640$ bits
- Liquid crystal drive circuit
  65 circuits for the common output and 224 circuits for the segment output
- High-speed 8-bit MPU interface (Both the 80 and 68 series MUPs can directly be connected.)/serial interface enabled
- Abundant command functions
  Display Data Read/Write, Display ON/OFF, Display Normal Rotation/Reversal, Page Address Set, Display Start Line Set, column address set, Status Read, Power Supply Save Display All Lighting ON/OFF, LCD Bias Set, Read Modify Write, Segment Driver Direction Select, Electronic Control, V_5 Voltage Adjusting Built-in Resistance Ratio Set, Static Indicator, n Line Alternating Current Reversal Drive, Common Output State Selection, and Built-in Oscillator Circuit ON
- Built-in static drive circuit for indicators (One set, blinking speed variable)
- Built-in power supply circuit for low power supply liquid crystal drive
  Booster circuit (Boosting magnification - double, triple, quadruple, boosting reference power supply external input enabled)
- 3% high accuracy alternating current voltage adjusting circuit (Temperature gradient: –0.05%/°C)
  Built-in V_5 voltage adjusting resistor, built-in V_1 to V_4 voltage generation split resistors, built-in electronic control function, and voltage follower
- Built-in CR oscillator circuit (external clock input enabled)
- Low power consumption
- Built-in temperature sensor circuit (S1D15710D10B∗ and S1D15710D11B∗)
- Power supplies
  Logic power supply: $V_{DD} - V_{SS} = 1.8$ to 5.5 V
  Boosting reference power supply: $V_{DD} - V_{SS} = 1.8$ to 6.0 V
  Liquid crystal drive power supply: $V_5 - V_{DD} = -4.5$ to –18.0 V
- Wide operating temperature range –40 to +85°C
- CMOS process
- Shipping form Bare chip, TCP
- No light-resistant and radiation-resistant design are provided.

Series specification

Product name	Duty	Bias	SEG Dr	COM Dr	V_{REG} temperature gradient	Shipping form
S1D15710D00B∗	1/65	1/9, 1/7	224	65	–0.05%/°C	Bare chip
S1D15710D10B∗(*1)	1/65	1/9, 1/7	224	65	–0.05%/°C	Bare chip
S1D15710D11B∗(*2)	1/65	1/9, 1/7	224	65	–0.05%/°C	Bare chip
S1D15710T00∗∗	1/65	1/9, 1/7	224	65	–0.05%/°C	TCP

*1: The built-in power circuit has been upgraded so that liquid crystal displays having big load capacities can be driven. Check the display and select if the display quality is inadequate even in high power mode of S1D15710D00B∗. There are no methods for supplying liquid crystal drive power externally without using the built-in power circuit. In that case, select either the S1D15710D00B∗ or the S1D15710D11B∗.

*2: All specificationa are same as those of the S1D15710D00B∗ except for the temperature sensor circuit.

3. BLOCK DIAGRAM
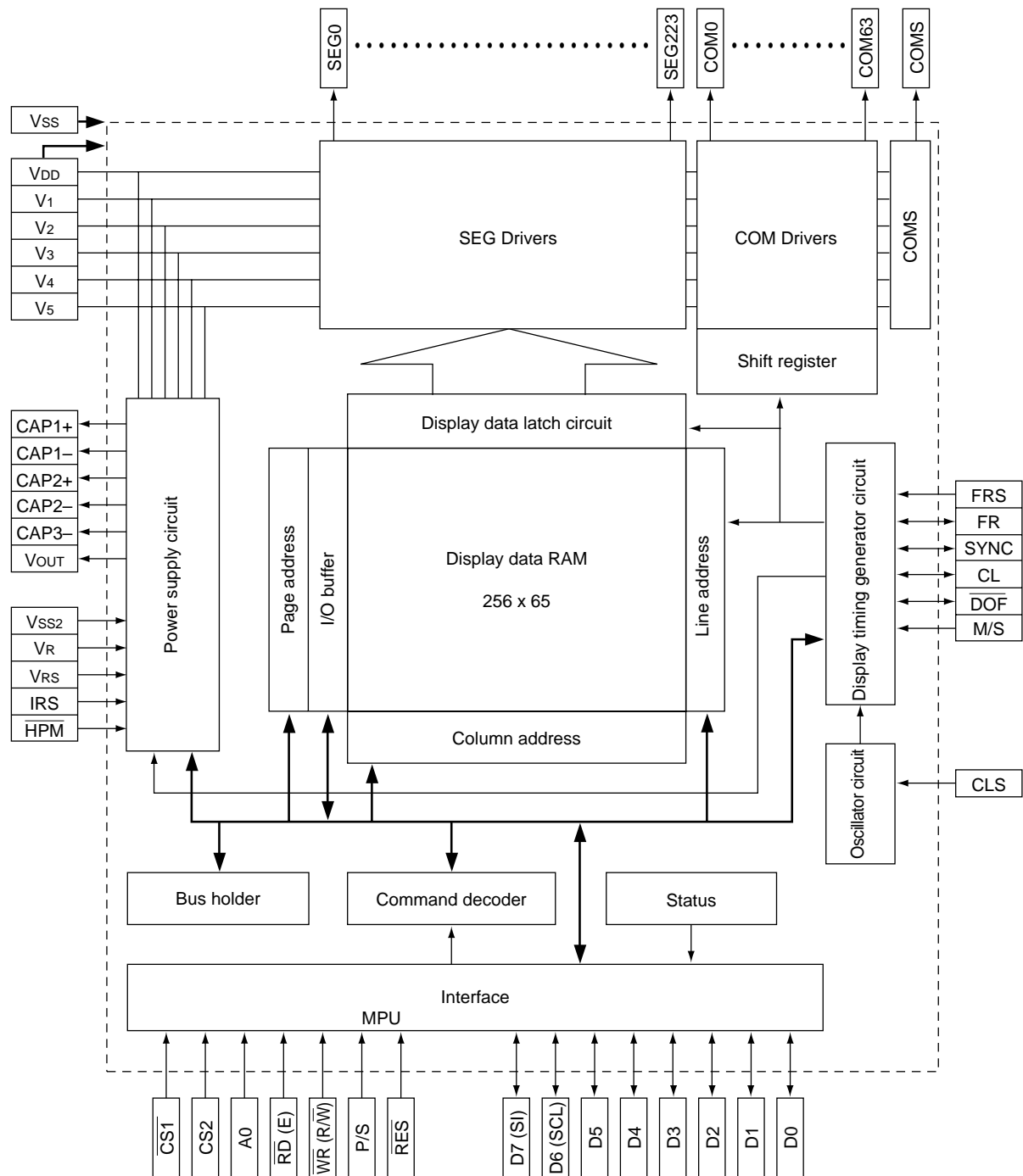
4. PIN LAYOUT

Chip Specification
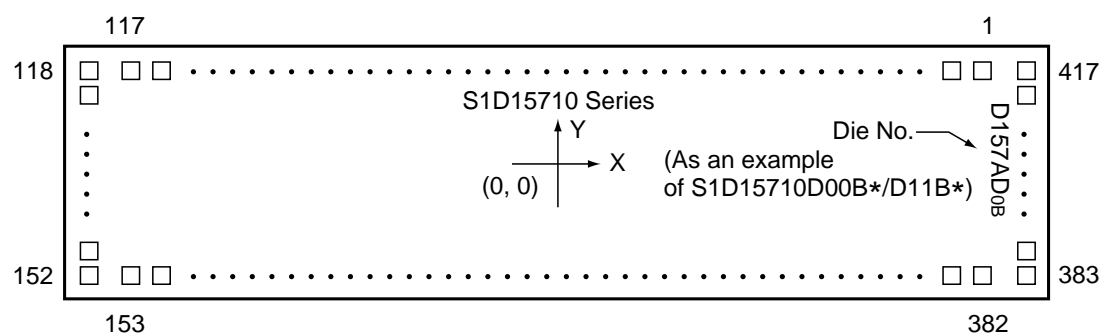
Item		Size		Unit
		X	Y	
Chip size		16.65 ×	2.90	mm
Chip thickness		0.625		mm
Bump pitch		69 (Min.)		μm
Bump size	PAD No.1 to 117	85 ×	85	μm
	PAD No.118	85 ×	73	μm
	PAD No.119 to 151	85 ×	47	μm
	PAD No.152	85 ×	73	μm
	PAD No.153	73 ×	85	μm
	PAD No.154 to 381	47 ×	85	μm
	PAD No.382	73 ×	85	μm
	PAD No.383	85 ×	73	μm
	PAD No.384 to 416	85 ×	47	μm
	PAD No.417	85 ×	73	μm
Bump height		17 (Typ.)		μm

PAD Central Coordinates

Unit: μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	(NC)	7814	1293	51	V_{DD}	972	1293	101	V_{DD}	−5723	1293
2	SYNC	7677		52	V_{DD}	838		102	M/S	−5859	
3	FRS	7541		53	V_{DD}	704		103	CLS	−5996	
4	TEST1	7404		54	V_{DD}	571		104	V_{SS}	−6132	
5	V_{DD}	7268		55	V_{DD}	437		105	C86	−6269	
6	TEST2	7131		56	V_{SS}	303		106	P/S	−6405	
7	V_{SS}	6995		57	V_{SS}	169		107	$\overline{V_{DD}}$	−6542	
8	TEST3	6855		58	V_{SS}	35		108	$\overline{HPM}$	−6678	
9	V_{DD}	6718		59	V_{SS2}	−99		109	V_{SS}	−6815	
10	TEST4	6582		60	V_{SS2}	−233		110	IRS	−6951	
11	V_{SS}	6445		61	V_{SS2}	−367		111	V_{DD}	−7088	
12	V_{SS}	6309		62	V_{SS2}	−501		112	TEST12	−7224	
13	V_{SS}	6169		63	V_{SS2}	−635		113	TEST13	−7361	
14	V_{DD}	6033		64	(NC)	−768		114	TEST14	−7510	
15	V_{DD}	5896		65	V_{OUT}	−902		115	TEST15	−7630	
16	V_{DD}	5760		66	V_{OUT}	−1036		116	TEST16	−7750	
17	V_{DD}	5623		67	CAP3−	−1170		117	(NC)	−7869	↓
18	TEST5	5483		68	CAP3−	−1304		118	(NC)	−8148	1295
19	TEST5	5347		69	(NC)	−1438		119	COM31		1209
20	TEST6	5210		70	CAP1+	−1572		120	COM30		1137
21	TEST6	5074		71	CAP1+	−1706		121	COM29		1064
22	TEST7	4937		72	CAP1−	−1840		122	COM28		991
23	TEST7	4798		73	CAP1−	−1974		123	COM27		919
24	TEST8	4661		74	CAP2−	−2107		124	COM26		846
25	TEST8	4525		75	CAP2−	−2241		125	COM25		773
26	TEST9	4388		76	CAP2+	−2375		126	COM24		701
27	TEST9	4252		77	CAP2+	−2509		127	COM23		628
28	SYNC	4112		78	V_{SS}	−2643		128	COM22		555
29	FRS	3975		79	V_{SS}	−2777		129	COM21		483
30	FR	3839		80	V_{RS}	−2911		130	COM20		410
31	$\overline{CL}$	3702		81	V_{RS}	−3045		131	COM19		337
32	$\overline{DOF}$	3566		82	V_{DD}	−3179		132	COM18		265
33	$\overline{V_{SS}}$	3429		83	V_{DD}	−3313		133	COM17		192
34	$\overline{CS1}$	3293		84	V_1	−3446		134	COM16		119
35	CS2	3156		85	V_1	−3580		135	COM15		47
36	$\overline{V_{DD}}$	3020		86	V_2	−3714		136	COM14		−26
37	$\overline{RES}$	2883		87	V_2	−3848		137	COM13		−99
38	A0	2747		88	(NC)	−3982		138	COM12		−171
39	$\overline{V_{SS}}$	2610		89	V_3	−4116		139	COM11		−244
40	$\overline{WR}, R/\overline{W}$	2474		90	V_3	−4250		140	COM10		−317
41	$\overline{RD},E$	2337		91	V_4	−4384		141	COM9		−389
42	V_{DD}	2201		92	V_4	−4518		142	COM8		−462
43	D0	2064		93	V_5	−4652		143	COM7		−535
44	D1	1928		94	V_5	−4785		144	COM6		−607
45	D2	1791		95	(NC)	−4919		145	COM5		−680
46	D3	1655		96	V_R	−5053		146	COM4		−753
47	D4	1518		97	V_{DD}	−5187		147	COM3		−825
48	D5	1382		98	TEST10	−5321		148	COM2		−898
49	D6 (SCL)	1245		99	V_{SS}	−5455		149	COM1		−971
50	D7 (SI)	1109	↓	100	TEST11	−5589	↓	150	COM0	↓	−1043

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Unit: μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
151	COMS	−8148	−1116	201	SEG45	−4579	−1293	251	SEG95	−1127	−1293
152	(NC)	↓	−1201	202	SEG46	−4510		252	SEG96	−1058	
153	(NC)	−7906	−1293	203	SEG47	−4441		253	SEG97	−989	
154	(NC)	−7823		204	SEG48	−4372		254	SEG98	−920	
155	(NC)	−7754		205	SEG49	−4303		255	SEG99	−851	
156	SEG0	−7685		206	SEG50	−4234		256	SEG100	−782	
157	SEG1	−7616		207	SEG51	−4164		257	SEG101	−713	
158	SEG2	−7547		208	SEG52	−4095		258	SEG102	−644	
159	SEG3	−7478		209	SEG53	−4026		259	SEG103	−575	
160	SEG4	−7409		210	SEG54	−3957		260	SEG104	−506	
161	SEG5	−7340		211	SEG55	−3888		261	SEG105	−437	
162	SEG6	−7271		212	SEG56	−3819		262	SEG106	−368	
163	SEG7	−7202		213	SEG57	−3750		263	SEG107	−299	
164	SEG8	−7133		214	SEG58	−3681		264	SEG108	−230	
165	SEG9	−7064		215	SEG59	−3612		265	SEG109	−161	
166	SEG10	−6995		216	SEG60	−3543		266	SEG110	−92	
167	SEG11	−6926		217	SEG61	−3474		267	SEG111	−23	
168	SEG12	−6857		218	SEG62	−3405		268	SEG112	46	
169	SEG13	−6788		219	SEG63	−3336		269	SEG113	115	
170	SEG14	−6719		220	SEG64	−3267		270	SEG114	184	
171	SEG15	−6650		221	SEG65	−3198		271	SEG115	253	
172	SEG16	−6581		222	SEG66	−3129		272	SEG116	322	
173	SEG17	−6512		223	SEG67	−3060		273	SEG117	391	
174	SEG18	−6442		224	SEG68	−2991		274	SEG118	461	
175	SEG19	−6373		225	SEG69	−2922		275	SEG119	530	
176	SEG20	−6304		226	SEG70	−2853		276	SEG120	599	
177	SEG21	−6235		227	SEG71	−2784		277	SEG121	668	
178	SEG22	−6166		228	SEG72	−2715		278	SEG122	737	
179	SEG23	−6097		229	SEG73	−2646		279	SEG123	806	
180	SEG24	−6028		230	SEG74	−2577		280	SEG124	875	
181	SEG25	−5959		231	SEG75	−2508		281	SEG125	944	
182	SEG26	−5890		232	SEG76	−2439		282	SEG126	1013	
183	SEG27	−5821		233	SEG77	−2370		283	SEG127	1082	
184	SEG28	−5752		234	SEG78	−2301		284	SEG128	1151	
185	SEG29	−5683		235	SEG79	−2232		285	SEG129	1220	
186	SEG30	−5614		236	SEG80	−2163		286	SEG130	1289	
187	SEG31	−5545		237	SEG81	−2094		287	SEG131	1358	
188	SEG32	−5476		238	SEG82	−2025		288	SEG132	1427	
189	SEG33	−5407		239	SEG83	−1956		289	SEG133	1496	
190	SEG34	−5338		240	SEG84	−1886		290	SEG134	1565	
191	SEG35	−5269		241	SEG85	−1817		291	SEG135	1634	
192	SEG36	−5200		242	SEG86	−1748		292	SEG136	1703	
193	SEG37	−5131		243	SEG87	−1679		293	SEG137	1772	
194	SEG38	−5062		244	SEG88	−1610		294	SEG138	1841	
195	SEG39	−4993		245	SEG89	−1541		295	SEG139	1910	
196	SEG40	−4924		246	SEG90	−1472		296	SEG140	1979	
197	SEG41	−4855		247	SEG91	−1403		297	SEG141	2048	
198	SEG42	−4786		248	SEG92	−1334		298	SEG142	2117	
199	SEG43	−4717		249	SEG93	−1265		299	SEG143	2186	
200	SEG44	−4648	↓	250	SEG94	−1196	↓	300	SEG144	2255	↓

Unit: μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
301	SEG145	2324	−1293	351	SEG195	5776	−1293	401	COM49	8148	119
302	SEG146	2393		352	SEG196	5845		402	COM50		192
303	SEG147	2462		353	SEG197	5914		403	COM51		265
304	SEG148	2531		354	SEG198	5983		404	COM52		337
305	SEG149	2600		355	SEG199	6052		405	COM53		410
306	SEG150	2669		356	SEG200	6121		406	COM54		483
307	SEG151	2739		357	SEG201	6190		407	COM55		555
308	SEG152	2808		358	SEG202	6259		408	COM56		628
309	SEG153	2877		359	SEG203	6328		409	COM57		701
310	SEG154	2946		360	SEG204	6397		410	COM58		773
311	SEG155	3015		361	SEG205	6466		411	COM59		846
312	SEG156	3084		362	SEG206	6535		412	COM60		919
313	SEG157	3153		363	SEG207	6604		413	COM61		991
314	SEG158	3222		364	SEG208	6673		414	COM62		1064
315	SEG159	3291		365	SEG209	6742		415	COM63		1137
316	SEG160	3360		366	SEG210	6811		416	COMS		1209
317	SEG161	3429		367	SEG211	6880		417	(NC)	▼	1295
318	SEG162	3498		368	SEG212	6949					
319	SEG163	3567		369	SEG213	7018					
320	SEG164	3636		370	SEG214	7087					
321	SEG165	3705		371	SEG215	7156					
322	SEG166	3774		372	SEG216	7225					
323	SEG167	3843		373	SEG217	7294					
324	SEG168	3912		374	SEG218	7364					
325	SEG169	3981		375	SEG219	7433					
326	SEG170	4050		376	SEG220	7502					
327	SEG171	4119		377	SEG221	7571					
328	SEG172	4188		378	SEG222	7640					
329	SEG173	4257		379	SEG223	7709					
330	SEG174	4326		380	(NC)	7778					
331	SEG175	4395		381	(NC)	7847					
332	SEG176	4464		382	(NC)	7930	▼				
333	SEG177	4533		383	(NC)	8148	−1201				
334	SEG178	4602		384	COM32		−1116				
335	SEG179	4671		385	COM33		−1043				
336	SEG180	4740		386	COM34		−971				
337	SEG181	4809		387	COM35		−898				
338	SEG182	4878		388	COM36		−825				
339	SEG183	4947		389	COM37		−753				
340	SEG184	5017		390	COM38		−680				
341	SEG185	5086		391	COM39		−607				
342	SEG186	5155		392	COM40		−535				
343	SEG187	5224		393	COM41		−462				
344	SEG188	5293		394	COM42		−389				
345	SEG189	5362		395	COM43		−317				
346	SEG190	5431		396	COM44		−244				
347	SEG191	5500		397	COM45		−171				
348	SEG192	5569		398	COM46		−99				
349	SEG193	5638		399	COM47		−26				
350	SEG194	5707	▼	400	COM48	▼	47				

5. PIN DESCRIPTION

Power Supply Pin

Pin name	I/O	Description	Number of pins
V_{DD}	Power supply	Commonly used with the MPU power supply pin V_{CC}.	12
V_{SS}	Power supply	0 V pin connected to the system ground (GND)	9
V_{SS2}	Power supply	Boosting circuit reference power supply for liquid crystal drive	5
V_{RS}	Power supply	External input pin for liquid crystal power supply voltage adjusting circuit They are set to OPEN	2
V_1, V_2 V_3, V_4 V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operation amplifier (OP amp) and applied. The potential needs to be specified based on V_{DD} to establish the relationship of dimensions shown below: $V_{DD} (=V_0) \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ Master operation When the power supply is ON, the following voltages are applied to $V_1 \sim V_4$ from the built-in power supply circuit. The selection of the voltages is determined using the LCD bias set command. | V_1	$1/9 \cdot V_5$	$1/7 \cdot V_5$
V_2	$2/9 \cdot V_5$	$2/7 \cdot V_5$
V_3	$7/9 \cdot V_5$	$5/7 \cdot V_5$
V_4	$8/9 \cdot V_5$	$6/7 \cdot V_5$		10

LCD Power Supply Circuit Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP1– pin.	2
CAP1–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
CAP2+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP2– pin.	2
CAP2–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP2+ pin.	2
CAP3–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
V_{OUT}	I/O	Boosting output pin. Connects a capacitor between the pin and V_{SS2}.	2
V_R	I	Voltage adjusting pin. Applies voltage between V_{DD} and V_5 using a split resistor. Valid only when the V_5 voltage adjusting built-in resistor is not used (IRS=LOW) Do not use VR when the V_5 voltage adjusting built-in resistor is used (IRS=HIGH)	1

5. PIN DESCRIPTION

System Bus Connecting Pins

Pin name	I/O	Description	Number of pins
D7 to D0 (SI) (SCL)	I/O	An 8-bit bidirectional data bus is used to connect an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S=LOW), D7: Serial data entry pin (SI) D6: Serial clock input pin (SCL) In this case, D0 to D5 are set to high impedance. When Chip Select is in the non-active state, D0 to D7 are set to high impedance.	8
A0	I	Normally the lowest order bit of the MPU address bus is connected to discriminate data / commands. A0=HIGH: Indicates that D0 to D7 are display data. A0=LOW: Indicates that D0 to D7 are control data.	1
$\overline{\text{RES}}$	I	Initialized by setting $\overline{\text{RES}}$ to LOW. Reset operation is performed at the $\overline{\text{RES}}$ signal level.	1
$\overline{\text{CS1}}$ CS2	I	Chip Select signal. When $\overline{\text{CS1}}$=LOW and CS2=HIGH, this signal becomes active and the input/output of data/commands is enabled.	2
$\overline{\text{RD}}$ (E)	I	• When the 80 series MPU is connected, active LOW is set. Pin that connects the $\overline{\text{RD}}$ signal of the 80 series MPU. When this signal is LOW, the S1D15710 series data bus is set in the output state. • When the 68 series MPU is connected, active HIGH is set. 68 series MPU enable clock input pin	1
$\overline{\text{WR}}$ (R/$\overline{\text{W}}$)	I	• When the 80 series MPU is connected, active LOW is set. Pin that connects the $\overline{\text{WR}}$ signal of the 80 series MPU. The data bus signal is latched on the leading edge of the $\overline{\text{WR}}$ signal. • When the 68 series MPU is connected, Read/write control signal input pin R/$\overline{\text{W}}$=HIGH: Read operation R/$\overline{\text{W}}$=LOW: Write operation	1
FRS	O	Output pin for static drive Used together with the SYNC pin	1
C86	I	MPU interface switching pin C86=HIGH: 68 series MPU interface C86=LOW: 80 series MPU interface	1
P/S	I	Switching pin for parallel data entry/serial data entry P/S=HIGH: Parallel data entry P/S=LOW: Serial data entry According to the P/S state, the following table is given. | P/S	Data/command	Data	Read/write	Serial clock
---	---	---	---	---
HIGH	A0	D0 to D7	$\overline{\text{RD}}$, $\overline{\text{WR}}$	
LOW	A0	SI (D7)	Write-only	SCL (D6)	 When P/S=LOW, D0 to D5 are set to high impedance. D0 to D5 can be HIGH, LOW, or "OPEN". $\overline{\text{RD}}$(E) and $\overline{\text{WR}}$ (R/$\overline{\text{W}}$) are fixed to HIGH or LOW. For the serial data entry, RAM display data cannot be read.	1

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Pin name	I/O	Description	Number of pins

CLS	I	Pin that selects the validity/invalidity of the built-in oscillator circuit for display clocks.
		  CLS=HIGH: Built-in oscillator circuit valid
		  CLS=LOW: Built-in oscillator circuit invalid (external input)
		When CLS=LOW, display clocks are input from the CL pin.
		When the S1D15710 series is used for the master/slave configuration, each of the CLS pins is set to the same level together.
		
		      Display clock Master Slave
		      Built-in oscillator circuit used HIGH HIGH
		      External input LOW LOW
			1

M/S	I	Pin that selects the master/slave operation for the S1D15710 series. The liquid crystal display system is synchronized by outputting the timing signal required for the liquid crystal display for the master operation and inputting the timing signal required for the liquid crystal display for the slave operation.
		  M/S=HIGH: Master operation
		  M/S=LOW: Slave operation
		According to the M/S and CLS states, the following table is given.
		
		See table below.
			1

Table for M/S pin:

M/S	CLS	Oscillator circuit	Power supply circuit	CL	FR	SYNC	FRS	DOF
HIGH	HIGH	Valid	Valid	Output	Output	Output	Output	Output
	LOW	Invalid	Valid	Input	Output	Output	Output	Output
LOW	HIGH	Invalid	Invalid	Input	Input	Input	Output	Input
	LOW	Invalid	Invalid	Input	Input	Input	Output	Input

Pin name	I/O	Description	Number of pins
CL	I/O	Display clock I/O pin According to the M/S and CLS states, the following table is given. See table below. When the S1D15710 series is used for the master/slave configuration, each CL pin is connected.	1

Table for CL pin:

M/S	CLS	CL
HIGH	HIGH	Output
	LOW	Input
LOW	HIGH	Input
	LOW	Input

Pin name	I/O	Description	Number of pins

FR	I/O	Liquid crystal alternating current signal I/O pin
		  M/S=HIGH: Output
		  M/S=LOW: Input
		When the S1D15710 series is used for the master/slave configuration, each FR pin is connected.
			1

SYNC	I/O	Liquid crystal synchronizing current signal I/O pin
		  M/S=HIGH: Output
		  M/S=LOW: Input
		When the S1D15710 series is used for the master/slave configuration, each SYNC pin is connected.
			2

$\overline{\text{DOF}}$	I/O	Liquid crystal display blanking control pin
		  M/S=HIGH: Output
		  M/S=LOW: Input
		When the S1D15710 series is used for the master/slave configuration, each $\overline{\text{DOF}}$ pin is connected.
			1

IRS	I	V_5 voltage adjusting resistor selection pin
		  IRS=HIGH: Built-in resistor used
		  IRS=LOW: Built-in resistor not used. The V_5 voltage is adjusted by the V_R pin and stand-alone split resistor.
		Valid only at master operation. The pin is fixed to HIGH or LOW at slave operation.
			1

$\overline{\text{HPM}}$	I	Power supply control pin of the power supply circuit for liquid crystal drive
		  $\overline{\text{HPM}}$=HIGH: Normal mode
		  $\overline{\text{HPM}}$=LOW: High power supply mode
		Valid only at master operation. The pin is fixed to HIGH or LOW at slave operation.
			1

5. PIN DESCRIPTION

Liquid Crystal Drive Pin

Pin name	I/O	Description	Number of pins
SEG0 to SEG223	O	Output pins for the LCD segment drive. Contents of the display RAM and FR signal are combined to select a desired level among V_{DD}, V_2, V_3 and V_5.	224
COM0 to COM63		Output pins for the LCD common drive. Scan data and FR signal are combined to select a desired level among V_{DD}, V_1, V_4 and V_5.	64
COMS	O	Indicator dedicated COM output pin Set to OPEN when not used When COMS is used for the master/slave configuration, the same signal is output to both the master and slave.	2

SEG table:

RAM data	FR	Output voltage	
		Display normal operation	Display reversal
HIGH	HIGH	V_{DD}	V_2
HIGH	LOW	V_5	V_3
LOW	HIGH	V_2	V_{DD}
LOW	LOW	V_3	V_5
Power save	—	V_{DD}	

COM table:

Scanning data	FR	Output voltage
HIGH	HIGH	V_5
HIGH	LOW	V_{DD}
LOW	HIGH	V_1
LOW	LOW	V_4
Power save	—	V_{DD}

Test Pin

Pin name	I/O	Description	Number of pins
TEST1 to 4	I/O	Fix the pin to HIGH. To use a built-in temperature sensor circuit in the S1D15710∗00∗∗/S1D15710∗11∗∗, see 16, Temperature Sensor Circuit.	4
TEST10	I	Fix it to HIGH for the S1D15710∗00∗∗/S1D15710∗11∗∗; fix it to LOW for S1D15710∗10∗∗.	1
TEST11to13	I/O	IC chip test pin. Fix the pin to HIGH.	3
TEST5 to 9, 14 to 16	I/O	IC chip test pin. Take into consideration so that the capacity of lines cannot be exhausted by setting the pin to OPEN.	13

6. FUNCTION DESCRIPTION

MPU Interface

Selection of interface type

The S1D15710 series transfers data through 8-bit bidirectional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin to either HIGH or LOW, the 8-bit parallel data entry or serial data entry can be selected as listed in Table 1.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH: Parallel data entry	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW: Serial data entry	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	(HZ)

Fix — to HIGH or LOW . HZ indicates the high impedance state.

Parallel interface

When the parallel interface is selected (P/S=HIGH), the S1D15705 series can directly be connected to the MPU bus of either the 80 or 68 series MPU by setting the C86 pin to HIGH or LOW as listed in Table 2.

Table 2

C86	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH: 68 series MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7 to D0
LOW: 80 series MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

In addition, the data bus signal can be identified according to the combinations of the A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals as listed in Table 3.

Table 3

Common	68 series	80 series		
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	Function
1	1	0	1	Display data read
1	0	1	0	Display data write
0	1	0	1	Status read
0	0	1	0	Control data write (command)

Serial interface

When the serial interface is selected (P/S=LOW), the serial data entry (SI) and serial clock input(SCL) can be accepted with the chip in the non-active state (CS1=LOW or CS2=HIGH. The serial interface consists of an 8-bit shift register and a 3-bit counter. Serial data is fetched from the serial data entry pin in the order of D7, D6, ..., and D0 on the leading edge of the serial clock and converted into 8-bit parallel data on the leading edge of the 8th serial clock, then processed.

Whether to identify that the serial data entry is display data or command is judged by the A0 input, and A0=HIGH indicates display data and A0=LOW indicates the command. After the chip is set to the non-active state, the A0 input is read and identified at the timing on the $8 \times n$-th leading edge of the serial clock. Figure 1 shows the signal chart of the serial interface.
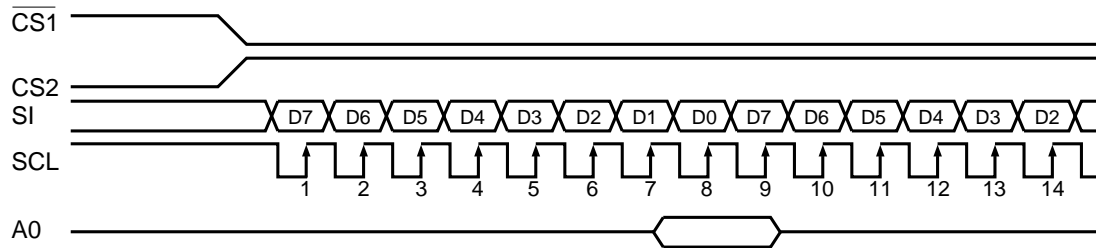
Figure 1

- When the chip is in the non-active state, both the shift register and counter are reset to the initial state.
- Cannot be read for the serial interface.
- For the SCL signal, pay careful attention to the terminating reflection of lines and external noise. The operation confirmation using actual equipment is recommended.

Chip select

The S1D15710 series has two chip select pins CS1 and CS2 and enables the MPU interface or serial interface only when CS1=LOW and CS2=HIGH.

When Chip Select is in the non-active state, D0 to D7 are in the high impedance state and the A0, RD, and WR inputs become invalid. When the serial interface is selected, the shift register and counter are reset.

Display data RAM and internal register access

Since the S1D15710 series access viewed from the MUP side satisfies the cycle time and does not require the wait time, high-speed data transfer is enabled.

The S1D15710 series performs a kind of inter-LSI pipeline processing through the bus holder attached to the internal data bus when it performs the data transfer with the MPU.

For example, when data is written on the display data RAM, the data is first held in the bus holder and written on the display data RAM up to the next data write cycle. Further, when the MPU reads the contents of display data RAM, the read data at the first data read cycle (dummy) is held in the bus holder and read on the system bus from the bus holder up to the next data read cycle. The read sequence of the display data RAM is restricted. When the address is set, note that the specified address data is not output to the subsequent read instruction and output at the second data read. Therefore single dummy read is required after the address set and write cycle. Figure 2 shows this relationship.

Busy flag

When the busy flag is "1", it indicates that the S1D15710 series is performing an internal operation, and only the status read instruction can be accepted. The busy flag is output to the D7 pin using the status read command. If the cycle time (t_{CYC}) is ensured, the MPU throughput can be improved greatly since this flag needs not be checked before each command.

• Write
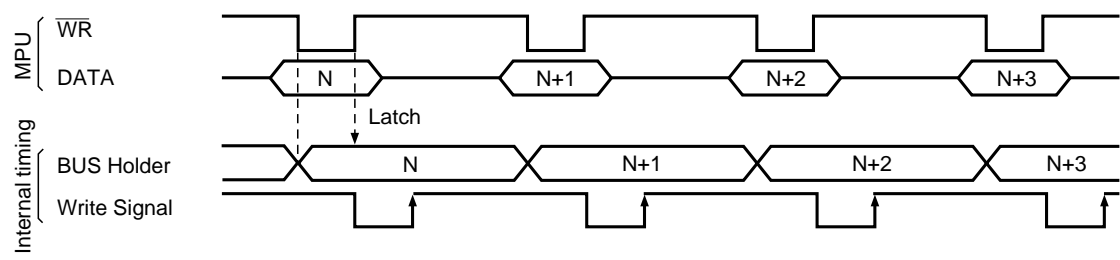
• Read
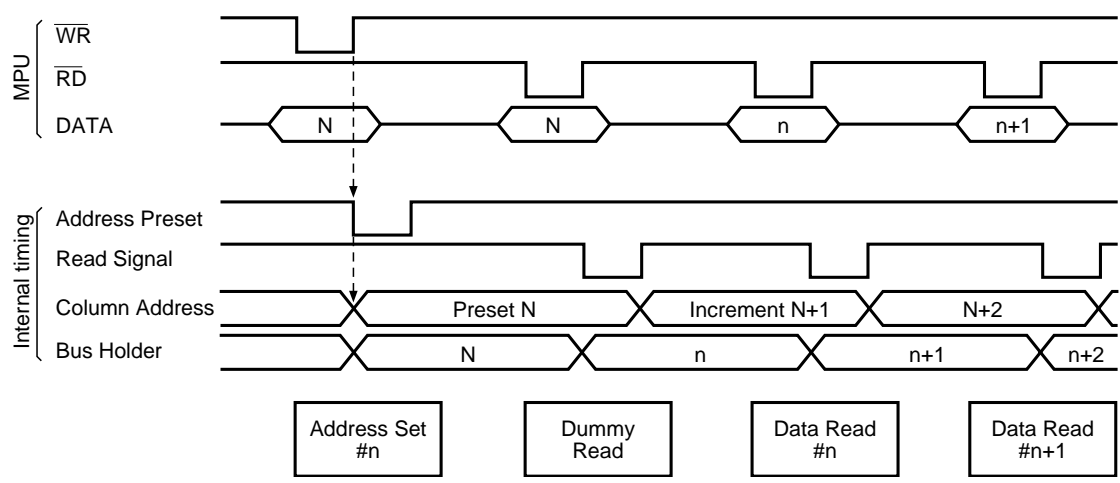
Figure 2

6. FUNCTION DESCRIPTION

Display Data RAM

Display data RAM

This display data RAM stores display dot data and consists of 65 (8 pages × one 8 bit + 1) × 256 bits. Desired bits can be accessed by specifying page and column addresses.

Since the MPU display data D7 to D0 correspond to the common direction of the liquid crystal display, the restrictions at display data transfer is reduced and the

display configuration with the high degree of freedom can easily be obtained when the S1D15710 series is used for the multiple chip configuration.

Besides, the read/write operation to the display data RAM is performed through the I/O buffer from the MPU side independently of the liquid crystal drive signal read. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.

D0	0	1	1	1		0	
D1	1	0	0	0		0	
D2	0	0	0	0		0	
D3	0	1	1	1		0	
D4	1	0	0	0		0	
—							

Display data RAM

Liquid crystal display

COM0, COM1, COM2, COM3, COM4, —

Figure 3

Page address circuit

As shown in Figure 4, the page address of the display data RAM is specified using the page address set command. To access the data using a new page, the page address is respecified.

The page address 8 (D3,D2,D1,D0=1,0,0,0) is an indicator dedicated RAM area and only the display data D0 is valid.

Column address circuit

As shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented by +1 at every input of display data read/write command. This allows the MPU to access the display data continuously.

Incrementation of the column address is stopped by FFH. When display data is accessed continuously, the column address continues to specify the FFH after access of the FFH. It should be noted that the column address FFH display data is accessed repeatedly. The column address and page address are independent of each other. Therefore, when shifting from the column of page 0 to the column of page 1, for example, it is necessary to specify each of the page address and column address again.

Furthermore, as shown in Table 4, the AD command (segment driver direction select command) can used to reverse the correspondence between the display data RAM column address and segment output. This allows constraints on IC layout to be minimized at the time of LCD module assembling.

Table 4

SEG output	SEG0 SEG223
ADC "0"	0 (H)→ Column Address→ DF (H)
(D0) "1"	FF (H)←Column Address← 20 (H)

Line address circuit

When displaying contents of the display data RAM, the line address circuit is used for specifying the corresponding addresses. See Figure 4. Using the display start line address set command, the top line is normally selected (when the common output state is normal, COM0 is output. And, when reversed outputs COM63). For the display area of 65 lines is secured starting from the specified display start line address in the address incrementing direction.

Dynamically changing the line address using the display start line address set command enables screen scrolling and page change.

EPSON

When setting the display start line to one channel

Page Address				Data		Line Address	Common output state: Normal rotation	COM Output
D3	D2	D1	D0					
0	0	0	0	D0–D7	Page 0	00H–07H		COM0–COM7
0	0	0	1	D0–D7	Page 1	08H–0FH		COM8–COM15
0	0	1	0	D0–D7	Page 2	10H–17H		COM16–COM23
0	0	1	1	D0–D7	Page 3	18H–1FH	Start	COM24–COM31
0	1	0	0	D0–D7	Page 4	20H–27H		COM32–COM39
0	1	0	1	D0–D7	Page 5	28H–2FH		COM40–COM47
0	1	1	0	D0–D7	Page 6	30H–37H		COM48–COM55
0	1	1	1	D0–D7	Page 7	38H–3FH		COM56–COM63
1	0	0	0	D0	Page 8			COMS

64 lines

SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	...	SEG218	SEG217	SEG218	SEG219	SEG220	SEG221	SEG222	SEG223		Column Address
00	01	02	03	04	05	06	07		D8	D9	DA	DB	DC	DD	DE	DF	0	D0
FF	FE	FD	FC	FB	FA	F9	F8		27	26	25	24	23	22	21	20	1	D0	ADC

LCD Out

The 65th line is accessed independently of the display start line address.

Figure 4

Display data latch circuit

The display data latch circuit is a latch that temporarily stores the display data output from the display data RAM to the liquid crystal drive circuit.

Since the Display Normal Rotation/Reversal, Display ON/OFF, and Display All Lighting ON/OFF commands control the data in this latch, the data within the display data RAM is not changed.

Oscillator Circuit

This oscillator circuit is a CR type oscillator and generates display clocks. The oscillator circuit is valid only when M/S=HIGH and CLS=HIGH and starts oscillation after the Built-in Oscillator Circuit ON command is entered. When CLS=LOW, the oscillation is stopped and the display clocks are entered from the CL pin.

Display Timing Generator Circuit

This display timing generator circuit generates timing signals from the display clocks to the line address circuit and the display latch circuit. It latches the display data to the display data latch circuit and outputs it to the segment drive output pin by synchronizing to the display clocks. The read operation of display data to the liquid crystal drive circuit is completely independent of the access to the display data RAM from the MPU. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.
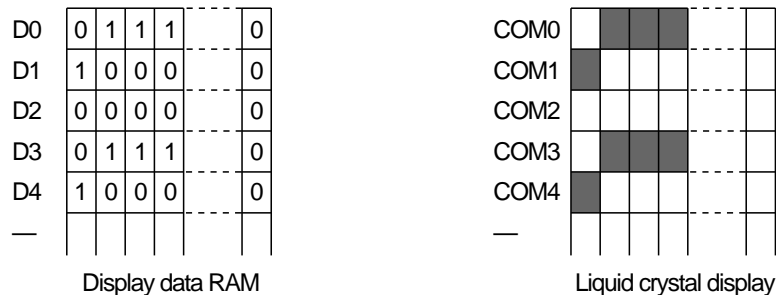
The circuit also generates the internal common timing, liquid crystal alternating current signal (FR), and synchronous signal (SYNC) from the display clocks.

As shown in Figure 5, the FR normally generates the drive waveforms in the 2-frame alternating current drive system to the liquid crystal drive circuit. It can generate n-line reversal alternating current drive waveforms by setting data (n-1) to the n-line reversal drive register. If a display quality problem such as crosstalk occurs, it can be improved by using the n-line reversal alternating current drive waveforms. Determine the number of lines (n) to which alternating current is applied by actually displaying the liquid crystal.

SNYC is a signal that synchronizes the line counter and common timing generator circuit to the SYNC signal output side IC. Therefore the SYNC signal becomes a waveform at a duty ratio of 50% that synchronizes to the frame synchronization.

When the S1D15710 series is used for the multiple chip configuration, the slave side needs to supply the display timing signals (FR, SYNC, CL, and $\overline{\text{DOF}}$) from the master side.

Table 5 shows the state of FR, SYNC, CL, or $\overline{\text{DOF}}$.

Table 5

Operation mode		FR	SYNC	CL	$\overline{\text{DOF}}$
Master	Built-in oscillator circuit valid (CLS=HIGH)	Output	Output	Output	Output
(M/S=HIGH)	Built-in oscillator circuit invalid (CLS=LOW)	Output	Output	Input	Output
Slave	Built-in oscillator circuit valid (CLS=HIGH)	Input	Input	Input	Input
(M/S=LOW)	Built-in oscillator circuit invalid (CLS=LOW)	Input	Input	Input	Input

2-frame alternating current drive waveforms
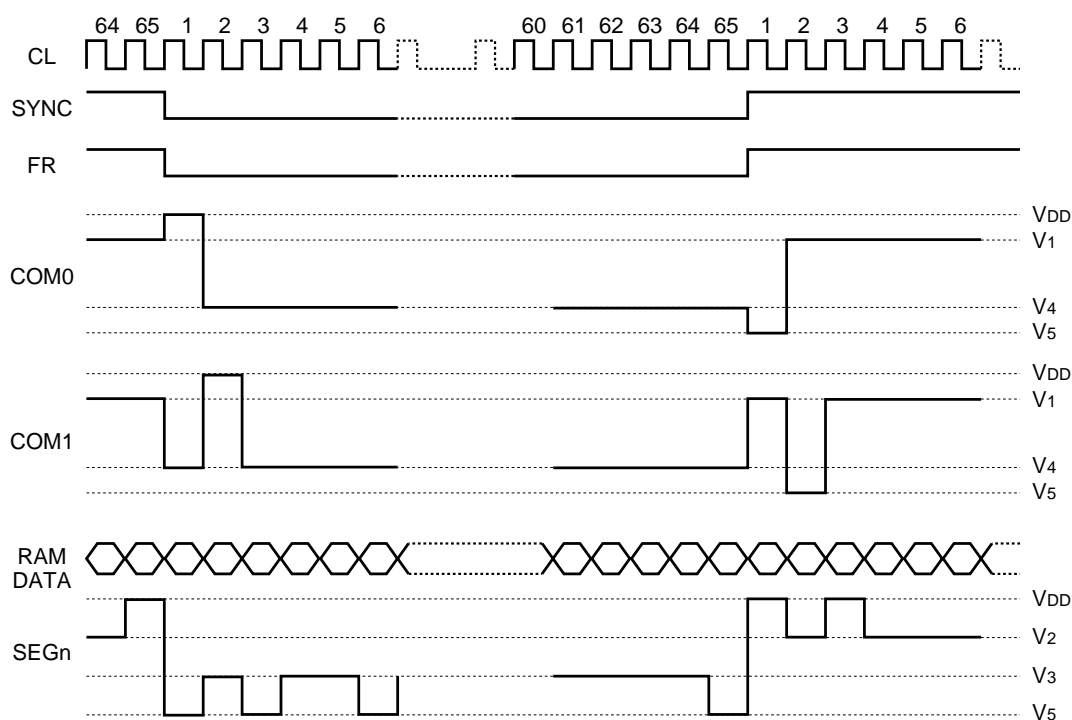
Figure 5

n-line reversal alternating current drive waveforms (Example of n=5: when the line reversal register is set to 4)
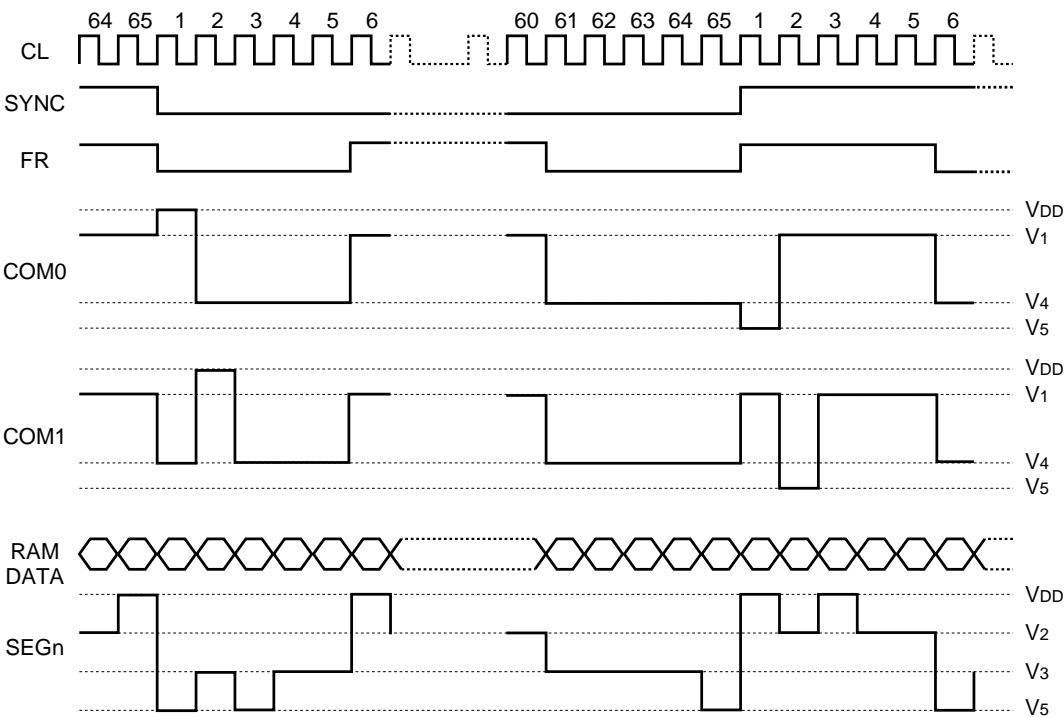
Figure 6

Common Output State Selection Circuit

The S1D15710 series can set the scanning direction of the COM output using the common output state selection command (see Figure 6). Therefore the IC assignment restrictions at LCD module assembly are reduced.

Table 6

State	COM scanning direction		
Normal rotation	COM 0	→	COM 63
Reversal	COM 63	→	COM 0

Liquid Crystal Drive Circuit

This liquid crystal drive circuit is 289 sets of mutiplexers that generate quadruple levels for liquid crystal drive. It outputs the liquid crystal drive voltage that corresponds to the combinations of the display data, COM scanning signal, and FR signal.
Figure 6 shows examples of the SEG and COM output waveforms.

6. FUNCTION DESCRIPTION

Figure 7

EPSON
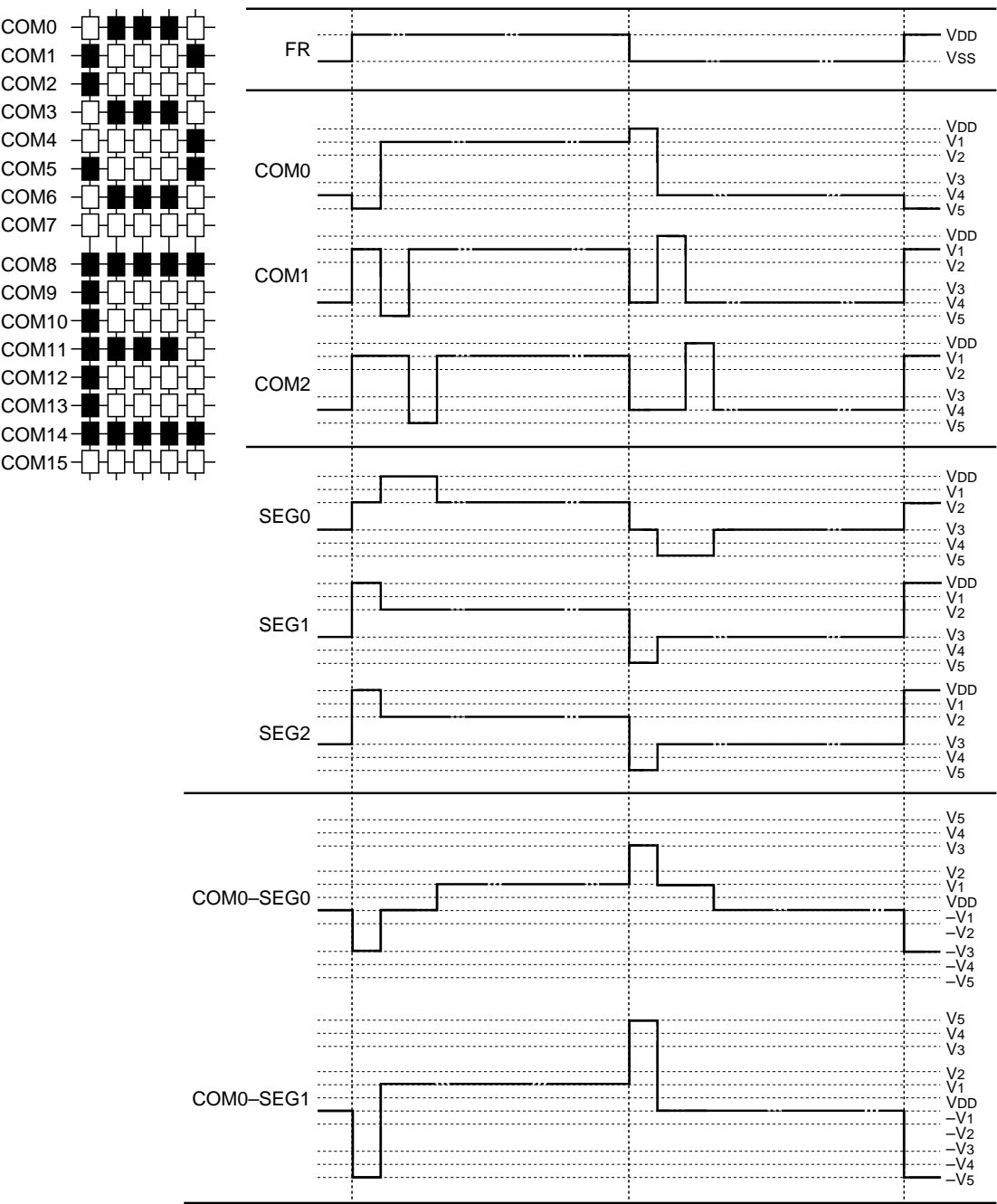
Power Supply Circuit

This power supply circuit is a low power supply consumption one that generates the voltage required for the liquid crystal drive and consists of a boosting circuit, voltage adjusting circuit, and voltage follower circuit. It is valid only at master operation.
The power supply circuit ON/OFF controls the boosting circuit, voltage adjusting circuit, and voltage follower circuit using the power supply control set command, respectively.
Therefore, it can also use the partial functions of the external power supply and built-in power supply together. Table 7 lists the functions that control 3-bit data using the power control set command and Table 8 lists the reference combinations.

Table 7 Description of controlling bits using the power control set command

Item	State "1"	"0"
D2 Boosting circuit control bit	ON	OFF
D1 Voltage adjusting circuit (V adjusting circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference combinations

Status of use	D2	D1	D0	Boosting circuit	V adjusting circuit	V/F circuit	External voltage input	Boosting system pin
① Built-in power supply used	1	1	1	O	O	O	V_{SS2}	Used
② V adjusting circuit and V/F circuit only	0	1	1	X	O	O	V_{OUT}, V_{SS2}	OPEN
③ V/F circuit only	0	0	1	X	X	O	V_5, V_{SS2}	OPEN
④ External power supply only	0	0	0	X	X	X	V_1 to V_5	OPEN

• The boosting system pin indicates the CAP1+, CAP1–, CAP2+, CAP2–, or CAP3– pin.
• Although the combinations other than those listed in the above table are also possible, they cannot be recommended because they are not actual use methods.

Boosting circuit

The boosting circuit incorporated in the S1D15710 series enables the quadruple boosting, triple boosting, and double boosting of the $V_{DD} – V_{SS2}$ potential.
For the quadruple boosting, the $V_{DD} \leftrightarrow V_{SS2}$ potential is quadruple-boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔and CAP1–, between CAP2+↔ and CAP2–, between CAP1+↔ and CAP3–, and between V_{SS2}↔ and V_{OUT}.
For the triple boosting, the $V_{DD} \leftrightarrow V_{SS2}$ potential is triple-boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔ and CAP1–, between CAP2+↔ and CAP2–, and between V_{SS2}↔ and V_{OUT} and strapping both CAP3– and V_{OUT} pins.
For the double boosting, the $V_{DD} \leftrightarrow V_{SS2}$ potential is doubly boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔ and CAP1–, and between V_{SS2}↔, setting CAP2+ to OPEN, and V_{OUT} and strapping CAP2–, CAP3–, and V_{OUT} pins.
Figure 8 shows the relationships of boosting potential.

6. FUNCTION DESCRIPTION

Quadruple boosting circuit   Triple boosting circuit   Double boosting circuit

Quadruple boosting
potential relationship

Triple boosting
potential relationship

Double boosting
potential relationship
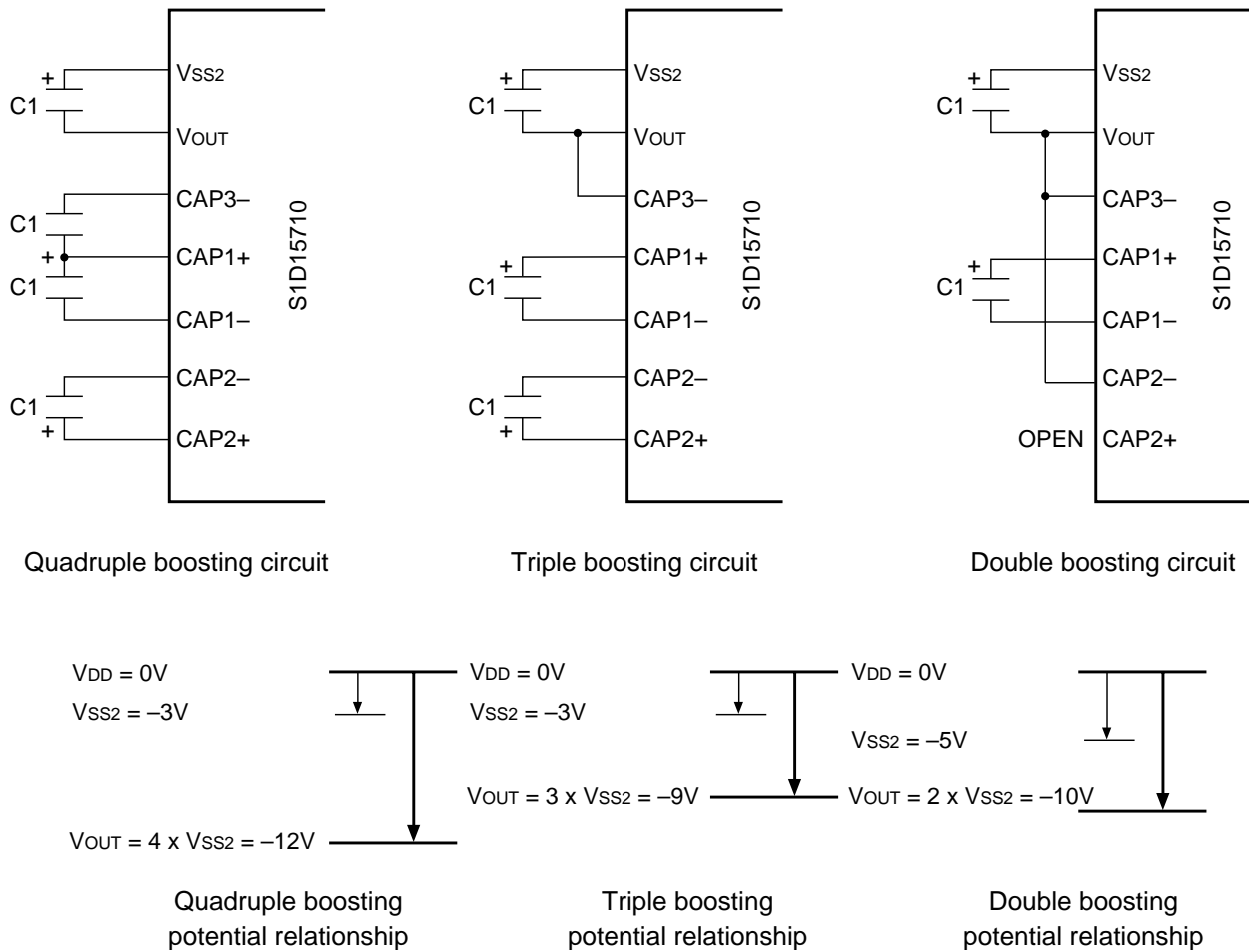
Figure 8

• Set the V_{SS2}" voltage range so that the voltage of the V_{OUT} pin cannot exceed the absolute maximum ratings.

Voltage adjusting circuit

The boosting voltage generated in V_{OUT} outputs the liquid crystal drive voltage V_5 through the voltage adjusting circuit.

Since the S1D15710 series incorporates a high-accuracy constant power supply, 64-step electronic control function, and V_5 voltage adjusting resistor, a high-accuracy voltage adjusting circuit can eliminate and save parts.

(A) When using the V_5 voltage adjusting built-in resistor
The liquid crystal power supply voltage V_5 can be controlled only using the command without an external resistor and the light and shade of liquid crystal display be adjusted by using the V_5 voltage adjusting built-in resistor and the electronic control function.
The V_5 voltage can be obtained according to Expression A-1 within the range of $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{Rb}{Ra}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG} \quad \text{(Expression A-1)}$$

$$\left[\Theta V_{EV} = \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}\right]$$

Figure 9

VREG is a constant voltage source within an IC, and the value at Ta=25°C is constant as listed in Table 9.

Table 9

Device	Temperature gradient	Unit	VREG	Unit
Internal power supply	−0.05	[%/°C]	−2.1	[V]

α indicates an electronic control command value. Setting data in a 6-bit electronic control register enters one state among 64 states. Table 10 lists the values of α based on the setup of the electronic control register.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			⋮			⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra indicates the V5 voltage adjusting built-in resistance ratio and can be adjusted into eight steps using the V5 voltage adjusting built-in resistance ratio set command. The reference values of the (1+Rb/Ra) ratio are obtained as listed in Table 11 by setting 3-bit data in the V5 voltage adjusting built-in resistance ratio register.

Table 11 (Reference values)

Register			Device per temperature gradient [Unit: %/°C]
D2	D1	D0	−0.05
0	0	0	4.5
0	0	1	5.0
0	1	0	5.5
0	1	1	6.0
1	0	0	6.5
1	0	1	7.0
1	1	0	7.6
1	1	1	8.1

For the internal resistance ratio, a manufacturing dispersion of up to ±7% should be taken into account. When not within the tolerance, adjust the V5 voltage by externally mounting Ra and Rb.

Figure 10 show the V5 voltage reference values per temperature gradient device based on the values of the V5 voltage adjusting built-in resistance ratio register and electronic control register at Ta=25°C.
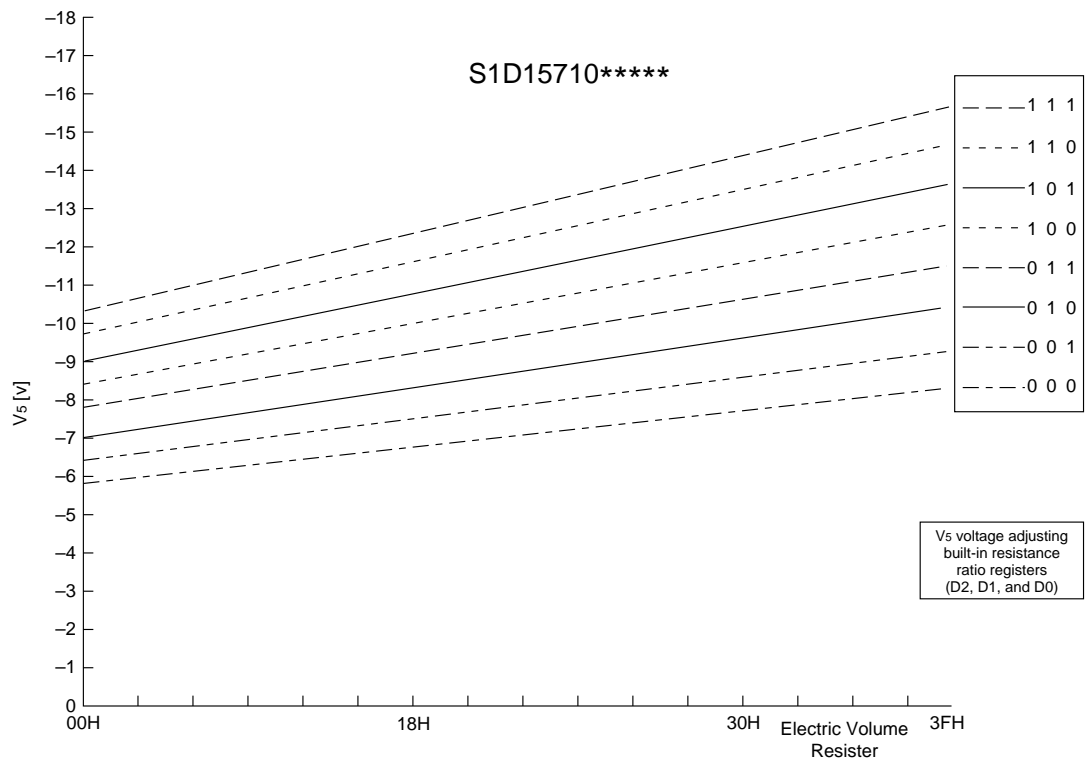
Figure 10 S1D15710***** Temperature gradient = −0.05%/°C

V5 voltage based on the values of V5 voltage adjusting built-in resistance ratio register and electronic control register

<Setting example: When setting V5 = –9 V at Ta=25°C>
From Figure 8 and Expression A-1.

Table 12

Description	Register					
	D5	D4	D3	D2	D1	D0
V5 voltage adjusting	–	–	–	0	1	0
electronic control	1	0	0	1	0	1

In this case, Table 13 lists the V5 voltage variable range and pitch width using the electronic control function.

Table 13

V5	Min.		Typ.		Max.	Unit
Variable range	−11.6	to	−9.3	to	−7.1	[V]
Pitch width			67			[mV]

(B) When using the external resistor (not using the V_5 voltage adjusting built-in resistor) ①
The liquid crystal power supply voltage V_5 can also be set by adding the resistors (Ra' and Rb') between V_{DD} and V_R and between V_R and V_5 without the V_5 voltage adjusting built-in resistor (IRS pin=LOW). Also in this case, the liquid crystal power supply voltage V_5 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic control function.

The V_5 voltage can be obtained from Expression B-1 by setting the external resistors Ra' and Rb' within the range of $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb'}{Ra'}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{Rb'}{Ra'}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$ (Expression B-1)

$$\left[\Theta V_{EV} = \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}\right]$$

Figure 11

<Setting example: When setting V_5=−9 V at Ta=25°C>

Set the value of the electronic control register as the intermediate value (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 31$$
$$V_{REG} = -2.1V$$

From Expression B-1, it follows that

$$V_5 = \left(1 + \frac{Rb'}{Ra'}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$ (Expression B-2)

$$-9V = \left(1 + \frac{Rb'}{Ra'}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

Also, suppose the current applied to Ra' and Rb' is 5µA.

$$Ra' + Rb' = 1.8M\Omega$$ (Expression B-2)

It follows that
Therefore from Expressions B-2 and B-3, we have

$$\frac{Rb'}{Ra'} = 4.3$$
$$Ra' = 340k\Omega$$
$$Rb' = 1460k\Omega$$

In this case, Table 14 lists the V_5 voltage variable range and pitch width using the electronic control function.

Table 14

V_5	Min.		Typ.		Max.	Unit
Variable range	−11.1	to	−9.0	to	−6.8	[V]
Pitch width			67			[mV]

(C) When using the external resistor (not using the V_5 voltage adjusting built-in resistor) ②
In the use of the above-mentioned external resistor, the liquid crystal power supply voltage V_5 can also be set by adding the resistors to finely adjust Ra' and Rb'. Also in this case, the liquid crystal power supply voltage V_5 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic control function.

The V_5 voltage can be obtained from the following expression C-1 by setting the external resistors R_1, R_2 (variable resistors), and R_3 within the range of $|V_5| < |V_{OUT}|$ and finely adjusting R_2 (ΔR_2).

$$V_5 = \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

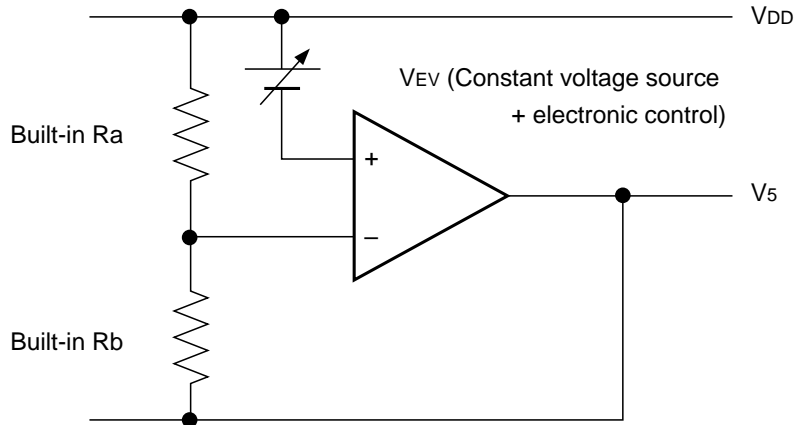$$\left[\Theta V_{EV} = \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}\right]$$ (Expression C-1)
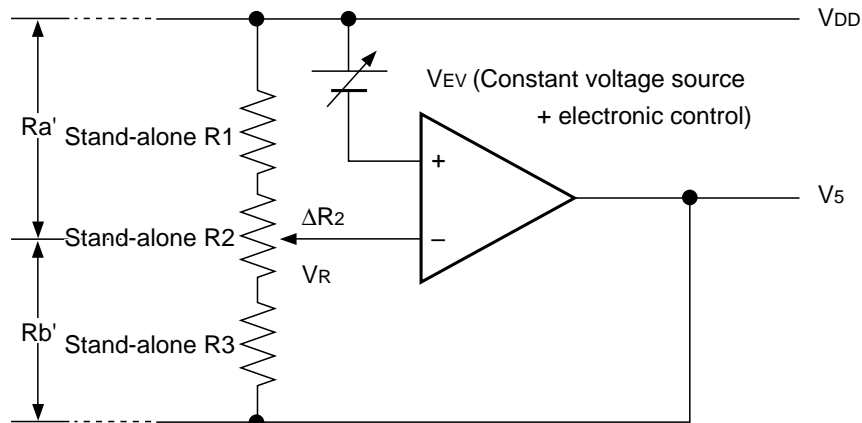
Figure 12

<Setting example: When setting V5=–7 to –11 V at Ta=25°C>

Set the value of the electronic control register as the intermediate value (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 31$$
$$V_{REG} = -2.1V$$

When ΔR2=0Ω, to obtain V5=–9 V from Expression C-1, it follows that

$$-11V = \left(1 + \frac{R_3 + R_2}{R_1}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Expression C-2)

When ΔR2=R2, to obtain V5=–7V, it follows that

$$-7V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Expression C-3)

Also, suppose the current applied between VDD and V5 is 5µA.

$$R_1 + R_2 + R_3 = 1.8M\Omega$$

(Expression C-4)

It follows that
Therefore from Expressions C-2, C-3, and C-4, we have

$$R_1 = 162k\Omega$$
$$R_2 = 278k\Omega$$
$$R_3 = 1363k\Omega$$

At this time, the V5 voltage variable range and notch width based on electronic volume function are given in the following Table when V5=–9 V by R2 is assumed:
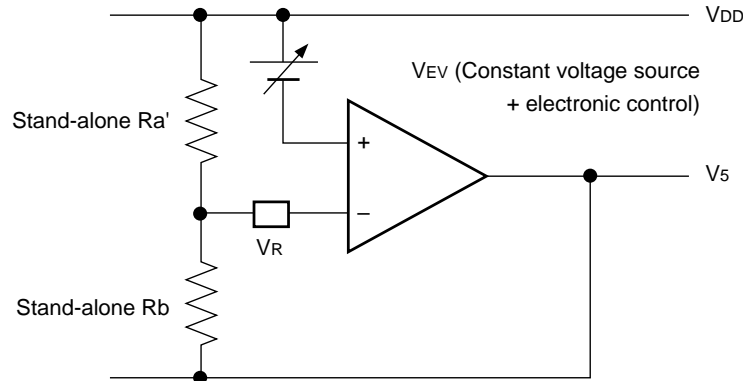
Table 15

V5	Min.		Typ.		Max.	Unit
Variable range	–11.1	to	–9.0	to	–6.8	[V]
Pitch width			67			[mV]

- When using the V5 voltage adjusting built-in resistor or electronic control function, the state where at least the V5 voltage adjusting circuit and voltage follower circuit are operated together needs to be set using the power control set command. Also when the boosting circuit is OFF, the voltage needs to be applied from VOUT.
- The VR pin is valid only when the V5 voltage adjusting built-in resistor (IRS pin=LOW). Set the VR pin to OPEN when using the V5 voltage adjusting built-in resistor (IRS pin=HIGH).
- Since the VR pin has high input impedance, noise must be taken into consideration such as for short and shielded lines.

Liquid crystal voltage generator circuit

The V5 voltage is resistor-split within an IC and generates the V1, V2, V3, and V4 potentials required for the liquid crystal drive.
Further, the V1, V2, V3, and V4 potentials are impedance-converted by the voltage follower and supplied to the liquid crystal drive circuit.

Using the bias set command allows you to select a desired bias ratio from 1/9 or 1/7.

High power mode

The power supply circuit incorporated in the S1D15710 series has the ultra-low power consumption (normal mode: $\overline{HPM}$=HIGH). Therefore the display quality

may be deteriorated in large load liquid crystal or panels. In this case, the display quality can be improved by setting HPM pin=LOW (high power mode). Whether to use the power supply circuit in this mode should need the display confirmation by actual equipment.
Also, if improvement is insufficient even for the high power mode setting, use either the S1D15710D10B∗ or supply liquid crystal drive power externally. In either case, be sure to check the display thoroughly.

Command sequence when the built-in power supply is turned off

To turn off the built-in power supply, set it in the power save state and then turn off the power supply according to the command sequence shown in Figure 13 (procedure).

Procedure	Description (Command, state)	Command address D7 D6 D5 D4 D3 D2 D1 D0	
Step1	Power save	1 0 1 0 1 0 0 0	Power save command
Step2	Turning off the built -in power supply	1	(Both stand-by and sleep can be useal)

Figure 13

① All the built-in power supply used

(1) When using the V5 voltage adjusting built-in resistor
(Example of VSS2=VSS, quadruple boosting)
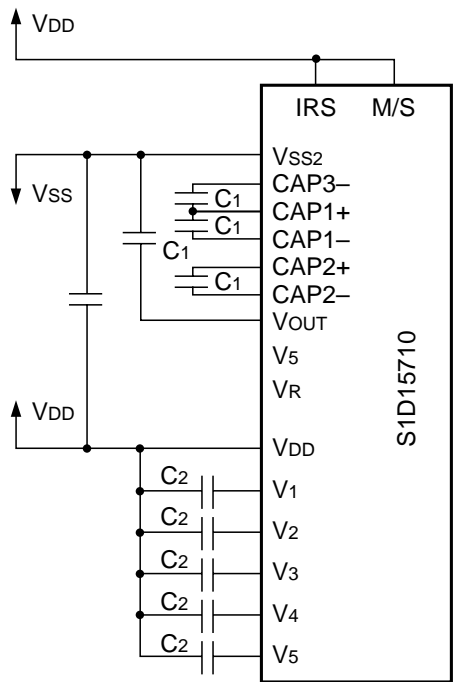
(2) When not using the V5 voltage adjusting built-in resistor
(Example of VSS2=VSS, quadruple boosting)
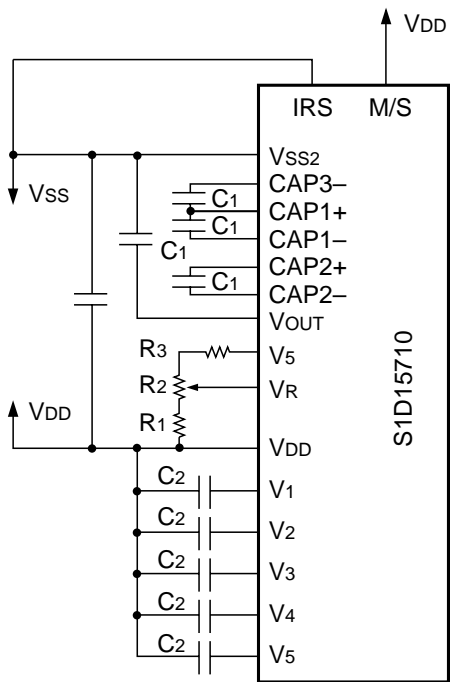
② Only the voltage adjusting circuit and V/F circuit used
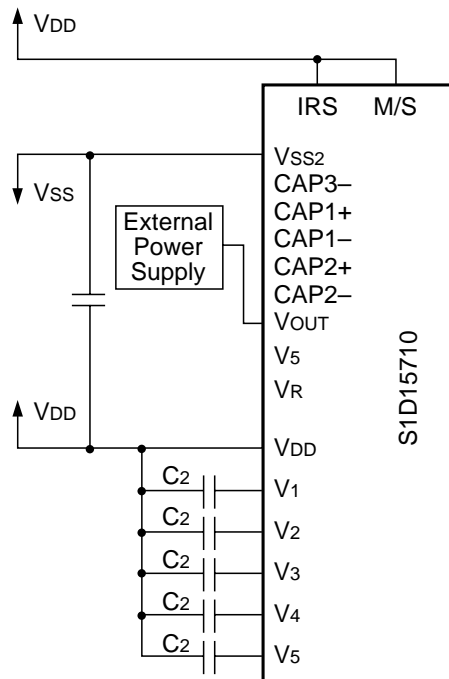
(1) When using the V5 voltage adjusting built-in resistor   (2) When not using the V5 voltage adjusting built-in resistor
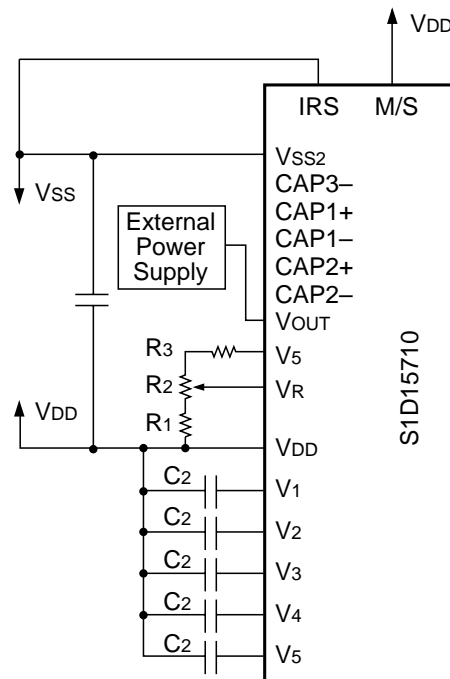
③ Only the V/F circuit used

④ Only the external power supply used
   Depending on all external power supplies
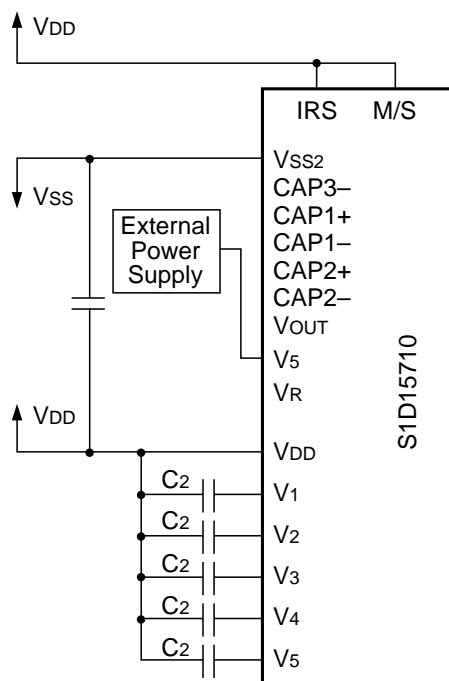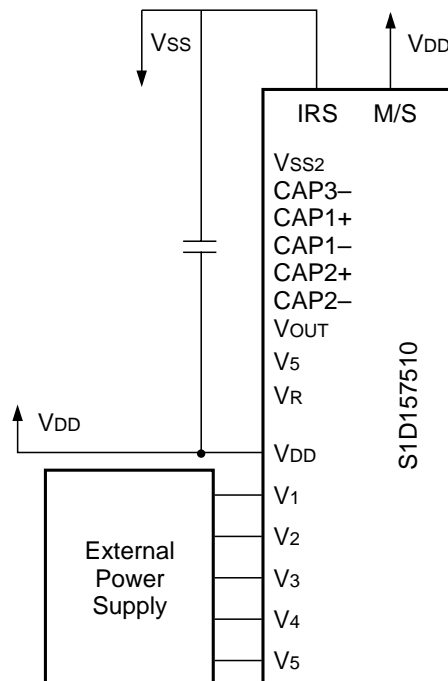
Common reference setting example
At V5=–8 to –12 V variable

Item	Setting value	Unit
C1	1.0 to 4.7	μF
C2	0.01 to 1.0	μF

Figure 14

*1 Since the V_R terminal input impedance is high, use short leads and shielded lines. When the V_R terminal is not used, means should be taken to prevent capacitance of the line or others from being applied.

*2 C_1 and C_2 are determined according to the size of the LCD panel. Set a value so that the liquid crystal drive voltage can be stable.

    [Setting example] • Turn on the V_5 adjusting circuit and the V/F circuit and apply external voltage.
                      • Display LCD heavy load patterns like lateral stripes and determine C_2 so that the liquid crystal drive voltages (V_1 to V_5) can be stable.
                      • Then turn on all built-in power supplies and determine C_1.

*3 Capacity is connected in order to stabilize voltage between V_{DD} and V_{SS} power supplies.

*4 When the built-in V/F circuit is used to drive an LCD panel with heavy alternating or direct current load, we recommend that external resistance be connected in order to stabilize V/F outputs, or electric potentials, V_1, V_2, V_3 and V_4.
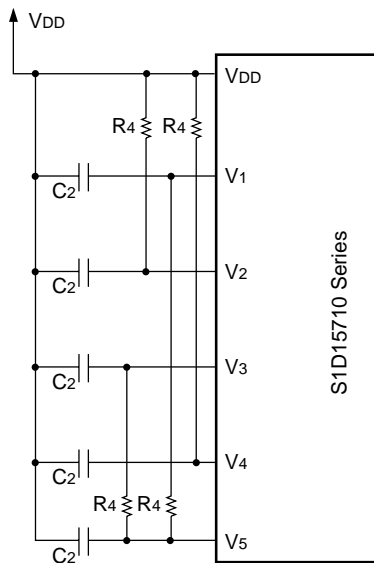
Figure 15

Adjust resistance value R_4 to the optimal level by checking driving waveform displayed on the LCD.

Reference setting: $R_4 = 0.1$ to 1.0 [MΩ]

*5 Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display. Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability.
Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.

2. Connection of the smoothing capacitors for the liquid crystal drive
The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally.
Reference value of the resistance is 100kΩ to 1MΩ. Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

6. FUNCTION DESCRIPTION

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.
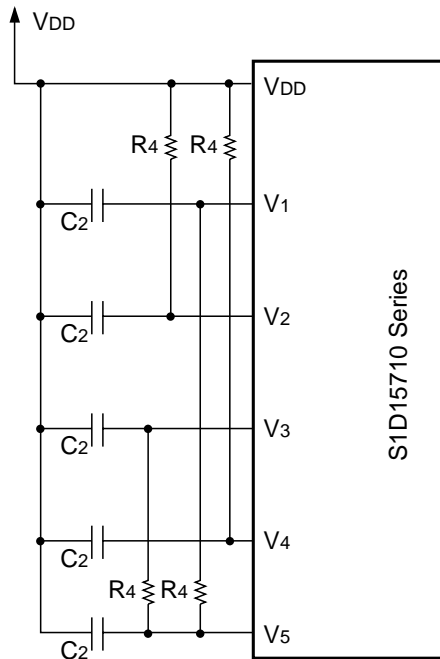
Exemplary connection diagram 2.
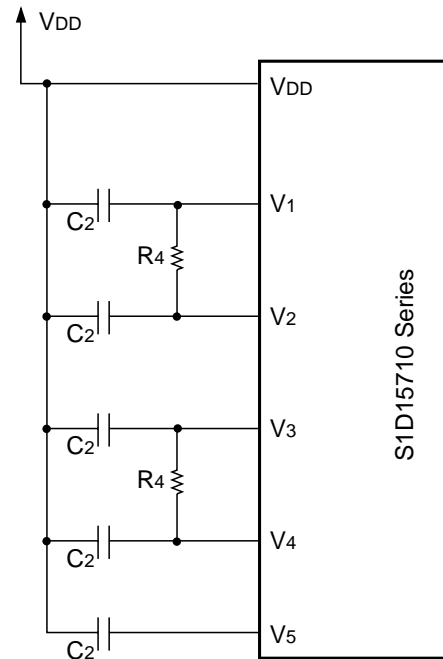
Reference circuit examples

Reset Circuit

When the $\overline{RES}$ input is set to the LOW level, this LSI enters each of the initial setting states

1. Display OFF
2. Display Normal Rotation
3. ADC Select: Normal rotation (ADC command D0=0)
4. Power Control Register: (D2,D1,D0)=(0,0,0)
5. Register Data Clear within Serial Interface
6. LCD Power Supply Bias Ratio: 1/9 bias
7. n-Line Alternating Current Reversal Drive Reset
8. Power saving clear
9. Display All Lighting OFF: (Display All Lighting ON/OFF command D0=LOW)
10. Built-in Oscillator Circuit stopped
11. Static Indicator OFF
    Static Indicator Register: (D1,D2)=(0,0)
12. Read Modify Write OFF
13. Display start line set to the first line
14. Column address set to address 0
15. Page address set to page 0
16. Common Output State   Normal rotation
17. V_5 Voltage Adjusting Built-in Resistance Ratio Register: (D2,D1,D0)=(0,0,0)
18. Electronic Control Register Set Mode Reset
    Electronic Control Register* (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0)
19. n-Line Alternating Current Reversal Register: (D3, D2, D1, D0) = (0, 0, 0, 0)

20. Test Mode Reset

On the other hand, when using the reset command, only the items 11 to 20 of the above-mentioned initial setting are executed.

When the power is turned on, the initialization using the $\overline{RES}$ pin is required. After the initialization using the $\overline{RES}$ pin, each input pin needs to be controlled normally. Besides, when the MPU control signal has high impedance, overcurrent may be applied to an IC. After turning on the power, take action so that the input pin cannot have high impedance.
The S1D15710 Series discharge electric charges of V_5 and V_{OUT} at $\overline{RES}$ pin is set to the LOW level. If external power supplies for driving LCD are used, do not input external power while the $\overline{RES}$ pin is set to the LOW level to prevent short-circuiting between the external power supplies and V_{DD}.

7. COMMAND DESCRIPTION

The S1D15710 series identifies data bus signals according to the combinations of A0, $\overline{RD}$(E), and $\overline{WR}$(R/$\overline{W}$). Since the interpretation and execution of commands are performed only by the internal timing independently of external clocks, the S1D15710 performs high-speed processing that does not require busy check normally.

The 80 series MPU interface starts commands by inputting low pulses to the $\overline{RD}$ pin at read and to the $\overline{WR}$ pin at write operation. The 68 series MPU interface enters the read state when HIGH is input to the R/$\overline{W}$ pin. It enters the write state when LOW is input to the same pin. It starts commands by inputting high pulses to the E pin (for the timing, see the Timing Characteristics of Chapter 10). Therefore the 68 series MPU interface differs from the 80 series MPU interface in that $\overline{RD}$(E) is set to "1 (H)" at status read and display data read in the Command Description and Command Table. The command description is given below by taking the 80 series MPU interface as an example.

When selecting the serial interface, enter sequential data from D7.

Command description

(1) Display ON/OFF

This command specifies display ON/OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

For display OFF, the segment and common drivers output the VDD level.

(2) Display Start Line Set

This command specifies the display start line address of the display data RAM shown in Figure 4. The display area is displayed for 65 lines from the specified line address to the line address increment direction. When this command is used to dynamically change the line address, the vertical smooth scroll and page change are enabled. For details, see the Line address circuit of "Function Description".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

7. COMMAND DESCRIPTION

(3) Page Address Set

This command specifies the page address that corresponds to the low address when accessing the display data RAM shown in Figure 4 from the MPU side. The display data RAM can access desired bits when the page address and column address are specified. Even when the page address is changed, the display state will not be changed. For details, see the Page address circuit of "Function Description".

A0	$\overline{\text{E}}$ $\overline{\text{RD}}$	$\overline{\text{R/W}}$ $\overline{\text{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

(4) Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (higher 4-bits and lower 4-bits) when it is set (set continuously in principle). Each time the display data RAM is accessed, the column address automatically increments (+), making it possible for the MPU to continuously read and write the display data. The column address increment is stopped at FFH, and the FFH is specified continuously. This must be noted when you want to access continuously. In this case, the page address is not changed continuously. For details, see "Column Address Circuit" in Function Description.

	A0	$\overline{\text{E}}$ $\overline{\text{RD}}$	$\overline{\text{R/W}}$ $\overline{\text{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
High-order bit →	0	1	0	0	0	0	1	A7	A6	A5	A4
Low-order bit →							0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
				↓				↓
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

(5) Status Read

A0	$\overline{\text{E}}$ $\overline{\text{RD}}$	$\overline{\text{R/W}}$ $\overline{\text{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY=1, indicates an internal operation being done or reset. The command cannot be accepted until BUSY=0 is reached. However, if the cycle time is satisfied, the command needs not be checked.
ADC	Indicates the correspondence relationship between the column address and segment driver. 0: Reversal (column address 199–n ↔ SEG n) 1: Normal rotation (column address n ↔ SEG n) (Reverses the polarity of ADC command.)
ON/OFF	ON/OFF: Specifies display ON/OFF 0: Display ON 1: Display OFF (Reverses the polarity of display ON/OFF command.)
RESET	Indicates the $\overline{RES}$ signal or that initial setting is being done using the reset command. 0: Operating state 1: Resetting

(6) Display Data Write

This command writes 8-bit data to the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively write the display data.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0				Write data				

(7) Display Data Read

This command reads the 8-bit data in the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively read the data consisting of multiple words.

Besides, immediately after the column address is set, dummy read is required one time. For details, see the description of the Display data RAM and internal register access of "Function Description".

When using the serial interface, the display cannot be read.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1				Read data				

(8) ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence relationship between the column address of the display RAM data shown in Figure 4 and the segment driver output. Therefore the order of the segment driver output pin can be reversed using the command. After the display data is written and read, the column address is incremented by 1 according to the column address of Figure 4. For details, see the Column address circuit of "Function Description".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Clockwise (normal rotation)
										1	Counterclockwise (reversal)

(9) Display Normal Rotation/Reversal

This command can reversal display lighting and non-lighting without overwriting the contents of display data RAM. In this case, the contents of display data RAM are held.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	LCD on potential (normal rotation) RAM data HIGH
										1	LCD on potential (reversal) RAM data LOW

(10) Display All Lighting ON/OFF

This command can forcedly make all display set in the lighting state irrespective of the contents of display data RAM. In this case, the contents of display data RAM are held.
This command has priority over the display normal rotation/reversal command.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display state
										1	Display all lighting

(11) LCD Bias Set

This command selects the bias ratio of the voltage required for liquid crystal drive. The command is valid when the V/F circuit of the power supply circuit is operated.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

(12) Read Modify Write

This command is used together with the end command. Once this command is entered, the column address can be incremented by 1 only using the display data write command instead of being changed using the display read command. This state is held until the end command is entered. When the end command is entered, the column address returns to the address when the read modify write command is entered. This function can reduce the load of the MPU when repeatedly changing data for a specific display area such as a blinking cursor.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* The commands other than Display Data Read/Write can be used even in Read Modify Write mode. However, the column address set command cannot be used.

• Sequence for cursor display
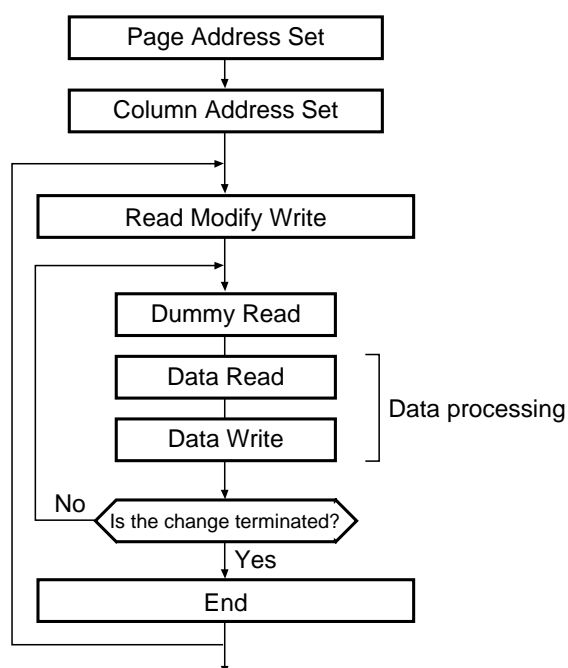
Figure 16

(13) End

This command resets the Read Modify Write mode and returns the column address to the mode initial address.

A0	$\overline{\text{E}}$ $\overline{\text{RD}}$	R/$\overline{\text{W}}$ $\overline{\text{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0
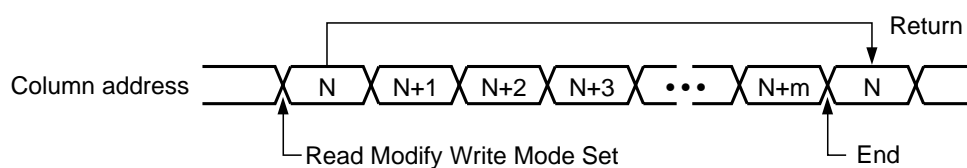
Figure 17

(14) Reset

This command initializes Display Start Line, Column Address, Page Address, Common Output State, V5 Voltage Adjusting Built-in Resistance Ratio, Electronic Control, and Static Indicator and resets the Read Modify Write mode and Test mode. This will not have any effect on the display data RAM. For details, see the Reset of " Function Description".

Reset operation is performed after the reset command is entered.

A0	$\overline{\text{E}}$ $\overline{\text{RD}}$	R/$\overline{\text{W}}$ $\overline{\text{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power is applied is performed using the reset signal to the $\overline{\text{RES}}$ pin. The reset command cannot be substituted for the signal.

7. COMMAND DESCRIPTION

(15) Common Output State Selection

This command can select the scanning direction of the COM output pin. For details, see the Common Output State Selection Circuit of "Function Description".

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
0	1	0	1	1	0	0	0	*	*	*	Normal rotation	COM0 → COM63
							1				Reversal	COM63 → COM0

*: Invalid bit

(16) Power Control Set

This command sets the function of the power supply circuit. For details, see the Power Supply Circuit of "Function Description".

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	0	1	0	1	0			Boosting circuit: OFF
								1			Boosting circuit: ON
									0		V adjusting circuit: OFF
									1		V adjusting circuit: ON
										0	V/F circuit: OFF
										1	V/F circuit: ON

(V/F circuit: Voltage follower circuit, V adjusting circuit: voltage adjusting circuit)

(17) V_5 Voltage Adjusting Built-in Resistance Ratio Set

This command sets the V_5 voltage adjusting built-in resistance ratio. For details, see the Power Supply Circuit of "Function Description".

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb to Ra ratio
0	1	0	0	0	1	0	0	0	0	0	Small
									0	0	1	
									0	1	0	
									↓			↓
									1	1	0	
									1	1	1	Large

(18) Electronic Control (2-Byte Command)

This command controls the liquid crystal drive voltage V_5 output from the voltage adjusting circuit of the built-in liquid crystal power supply and can adjust the light and shade of liquid crystal display.
Since this command is a 2-byte command that is used together with the electronic control mode set command and electronic control register set command, always use both the commands consecutively.

• Electronic Control Mode Set
Entering this command validates the electronic control register set command. Once the electronic control mode is set, the commands other than the electronic control register set command cannot be used. This state is reset after data is set in the register using the electronic control register set command.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

• Electronic Control Register Set
This command is used to set 6-bit data in the electronic volume register to allow the liquid crystal drive voltage V5 to enter one-state voltage value among 64-state voltage values.
After this command is entered and the electronic control register is set, the electronic control mode is reset.

A0	E RD	R/W̄ WR	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	*	*	0	0	0	0	0	0	Small
0	1	0	*	*	0	0	0	0	0	1	
0	1	0	*	*	0	0	0	0	1	0	
							↓				↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

*: Invalid bit

When not using the electronic control function, set (1,0,0,0,0,0).

• Sequence of the electronic control register set
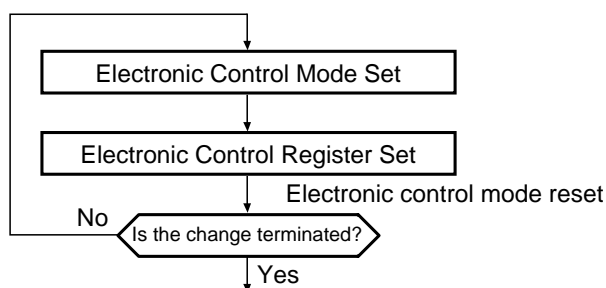
Figure 18

(19) Static Indicator (2-Byte Command)

This command controls the indicator display of the static drive system. The static indicator display is controlled only using this command, and this command is independent of other display control commands.
The static indicator is used to connect the SYNC pin to one of its liquid crystal drive electrodes and the FRS pin to the other. For the electrodes used for the static indicator, the pattern separated from the electrodes for dynamic drive are recommended. When this pattern is too adjacent, the deterioration of liquid crystal and electrodes may be caused.
Since the static indicator ON command is a 2-byte command that is used together with the static indicator register set command, always use both the commands consecutively. (The static indicator OFF command is a 1-byte command.)

• Static Indicator ON/OFF
Entering the static indicator ON command validates the static indicator register set command. Once the static indicator ON command is entered, the commands other than the static indicator register set command cannot be used. This state is reset after the data is set in the register using the static indicator register set command.

A0	E RD	R/W̄ WR	D7	D6	D5	D4	D3	D2	D1	D0	Static indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

7. COMMAND DESCRIPTION

• Static Indicator Register Set
This command sets data in the 2-bit static indicator register and sets the blinking state of the static indicator.

A0	$\overline{E}$ $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Indicator display state
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinks at an interval of approximately 0.5 second.)
									1	0	ON (blinks at an interval of approximately one second.)
									1	1	ON (goes on at all times.)

*: Invalid bit

• Sequence of Static Indicator Register Set
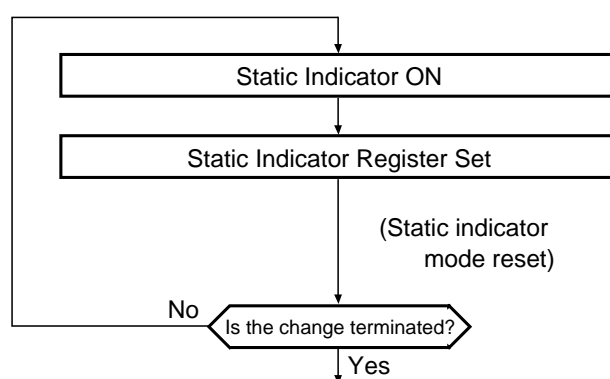
Figure 19

(20) Power Save

This command makes the static indicator enter the power save state and can greatly reduce the power consumption. The power save state consists of the sleep state and stand-by state.

A0	$\overline{E}$ $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Power save state
0	1	0	1	0	1	0	1	0	0	0	Stand-by state
										1	Sleep state

The operating state before the display data and power save activation is held in the sleep and stand-by states, and the display data RAM can also be accessed from the MPU.

• Sleep State
This command stops all the operations of LCD display systems, and can reduce the power consumption approximate to the static current when they are not accessed from the MPU. The internal state in the sleep state is as follows:
(1)   The oscillator circuit and the LCD power supply circuit are stopped.
(2)   All liquid crystal drive circuit is stopped and the segment and common drivers output the VDD level.

• Stand-by State

This command stops the operation of the duty LCD display system and operates only the static drive system for indicators. Consequently the minimum current consumption required for the static drive is obtained. The internal state in the stand-by state is as follows:

(1) The LCD power supply circuit is stopped. The oscillator circuit is operated.

(2) The duty drive system liquid crystal drive circuit is stopped and the segment and common drivers output the V$_{DD}$ level. The static drive system is operated.

  * When using external power supplies, it is recommended that the function of the external power supply circuit should be stopped at power save activation. For example, when providing each level of the liquid crystal drive voltage using a stand-alone split resistor circuit, it is recommended that the circuit which cuts off the current applied to the split resistor circuit should be added at power save activation. The S1D15710 series has the liquid crystal display blanking control pin $\overline{DOF}$ and is set to $\overline{LOW}$ at power save activation. The function of the external power supply circuit can be stopped using the $\overline{DOF}$ output.

(21) Power Save Reset

This command resets the power save state and returns the state before power save activation.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	1

(22) n-Line Reversal Drive Register Set

This command sets the number of reversal lines of the liquid crystal drive in the register. 2 to 16 lines can be set. For details, see the Display Timing Generator Circuit of "Function Description".

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line of reversal lines
0	1	0	0	0	1	1	0	0	0	0	—
							0	0	0	1	2
							0	0	1	0	3
							↓				↓
							1	1	1	0	15
							1	1	1	1	16

(23) n-Line Reversal Drive Reset

This command resets the n-line reversal alternating current drive and returns to the normal 2-frame reversal alternating current drive system. The value of the n-line reversal alternating current drive register is not changed.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	0	0

(24) Built-in Oscillator Circuit ON

This command starts the operation of the built-in CR oscillator circuit. This command is valid only for the master operation (M/S=HIGH) and built-in oscillator circuit valid (CLS=HIGH).

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	1

7. COMMAND DESCRIPTION

(25) NOP

Non-OPeration

A0	E̲ R̲D̲	R/W̄̄ W̄R̄	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(26) Test

IC chip test command. Do not use this command. If the test command is used incorrectly, it can be reset by setting the R̄ĒS̄ input to LOW or by using the reset command or NOP.

A0	E̲ R̲D̲	R/W̄̄ W̄R̄	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

(Note) Although the S1D15710 series holds the command operating state, it may change the internal state if excessive foreign noise is entered. Such action that suppresses the generation of noise and prevents the effect of noise needs to be taken on installation and systems. Besides, to prevent sudden noise, it is recommended that the operating state should periodically be refreshed.

Table 16 S1D15710 Series Commands

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
				Command code								
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 / 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display Start Line Set	0	1	0	0	1	Display start address						Sets the display start line address of the display RAM.
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				Sets the page address of the display RAM.
(4) Column Address Set High-Order Bit	0	1	0	0	0	0	1	High order Column address				Sets the high-order four bits of the column address of the display RAM.
Column Address Set Low-Order Bit	0	1	0	0	0	0	0	Low order Column address				Sets the low-order four bits of the column address of the display RAM.
(5) Status Read	0	0	1	Status				0	0	0	0	Reads the status information.
(6) Display Data Read	1	1	0	Write data								Writes data on the display RAM.
(7) Display Data Write	1	0	1	Read data								Reads data from the display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 / 1	Supports the SEG output of the display RAM address. 0: normal rotation, 1: Reversal
(9) Display Normal Rotation/Reversal	0	1	0	1	0	1	0	0	1	1	0 / 1	LCD display normal rotation/ reversal 0: normal rotation, 1: Reversal
(10) Display All Lighting ON/OFF	0	1	0	1	0	1	0	0	1	0	0 / 1	Display all lighting 0: normal display, 1: All ON
(11) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 / 1	Sets the LCD drive voltage bias ratio. 0: 1/9, 1: 1/7
(12) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. At write operation: By 1, at read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Resets Read Modify Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal resetting
(15) Common Output State Selection	0	1	0	1	1	0	0	0	*	*	*/1	Selects the scanning direction of the COM output. 0: Normal rotation, 1: Reversal
(16) Power Control Set	0	1	0	0	0	1	0	1	Operating state			Selects the state of the built-in power supply
(17) V5 Voltage Adjusting Internal Resistance Ratio Set	0	1	0	0	0	1	0	0	Resistance ratio setting			Selects the state of the built-in resistance ratio (Rb/Ra).
(18) Electronic Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	
Electronic Control Register Set	0	1	0	*	*	Electronic control value						Sets the V5 output voltage in the electronic register.
(19) Static Indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 / 1	0: OFF, 1: ON
Static Indicator Register Set	0	1	0	*	*	*	*	*	*	State		Sets the blinking state.
(20) Power Save	0	1	0	1	0	1	0	1	0	0	0 / 1	Moves to the power save state. 0: Stand-by, 1: Sleep
(21) Power Save Reset	0	1	0	1	1	1	0	0	0	0	1	Resets power save.
(22) n-Line Reversal Drive Register Set	0	1	0	0	0	1	1	Number of reversal Line				Sets the number of line reversal drive lines.
(23) n-Line Reversal Drive Reset	0	1	0	1	1	1	0	0	1	0	0	Resets the line reversal drive.
(24) Built-in Oscillator Circuit ON	0	1	0	1	0	1	0	1	0	1	1	Starts the operation of the built-in CR oscillator circuit.
(25) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation command
(26) Test	0	1	0	1	1	1	1	*	*	*	*	Do not use the IC chip test command.

*: Invalid bit

8. COMMAND SETTING

Instruction Setup: Reference

(1) Initial Setting

```
┌─────────────────────────────────────────────────────┐
│ Turn on the VDD - VSS power supply in the RES pin=LOW *1 │
└─────────────────────────────────────────────────────┘
                          │
┌─────────────────────────────────────────────────────┐
│              Power supply regulated                  │
└─────────────────────────────────────────────────────┘
                          │
┌─────────────────────────────────────────────────────┐
│        Reset the reset state (RES pin=HIGH)          │
└─────────────────────────────────────────────────────┘
                          │
┌─────────────────────────────────────────────────────┐
│            Initial setting state (default) *2        │
└─────────────────────────────────────────────────────┘
                          │
┌─────────────────────────────────────────────────────┐
│ Function setting by command input (set by user)      │
│ (24) Built-in Oscillator Circuit ON  *3              │
│  (The built-in CR oscillator circuit is used)        │
└─────────────────────────────────────────────────────┘
                          │
┌─────────────────────────────────────────────────────┐
│ Function setting by command input (set by user)      │
│ (11)  LCD Bias Set  *4                               │
│ (8)   ADC Select  *5                                 │
│ (15)  Common Output State Selection  *6              │
│ (22)  n-Line Reversal Register Set  *7               │
│  (When the n-line alternating current                │
│    reversal drive is used)                           │
└─────────────────────────────────────────────────────┘
                          │
┌─────────────────────────────────────────────────────┐
│ Function setting by command input (set by user)      │
│ (17)  V5 Voltage Adjusting Built-in Resistance       │
│        ratio Set  *8                                 │
│ (18)  Electronic Control  *9                         │
└─────────────────────────────────────────────────────┘
                          │
┌─────────────────────────────────────────────────────┐
│ Function setting by command input (set by user)      │
│ (16)  Power Control Set  *10                         │
└─────────────────────────────────────────────────────┘
                          │
┌─────────────────────────────────────────────────────┐
│              End of initial setting                  │
└─────────────────────────────────────────────────────┘
```

Notes: Reference items

*1: If external power supplies for driving LCD are used, do not supply voltage on V_{OUT} or V_5 pin during the period when $\overline{RES}$ = LOW. Instead, input voltage after releasing the reset state.
6. Function Description "Reset Circuit"

*2: The contents of DDRAM are not defined even in the initial setting state after resetting.
6. Function Description Section "Reset Circuit"

*3: 7. Command Description Item (24) "Built-in oscillator circuit ON"

*4: 7. Command Description Item (11) "LCD bias set"

*5: 7. Command description Item (8) "ADC select"

*6: 7. Command Description Item (15) "Common output state selection"

*7: 6. Function Description Section "Display Timing Generator Circuit", 7. Command Description Item (22) "n-Line Reversal Register Set"

*8: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (17) "V_5 Voltage Adjusting Built-in Resistance ratio Set"

*9: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (18) "Electronic Control"

*10: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (16) "Power Control Set"

(2) Data Display

```
┌─────────────────────────────────────────────┐
│              End of initial setting           │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ Function setting by command input (set by user)│
│   (2) Display Start Line Set  *11             │
│   (3) Page Address Set  *12                   │
│   (4) Column Address Set  *13                 │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ Function setting by command input (set by user)│
│   (6) Display Data Write  *14                 │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ Function setting by command input (set by user)│
│   (1) Display ON/OFF  *15                     │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│              End of data display              │
└─────────────────────────────────────────────┘
```
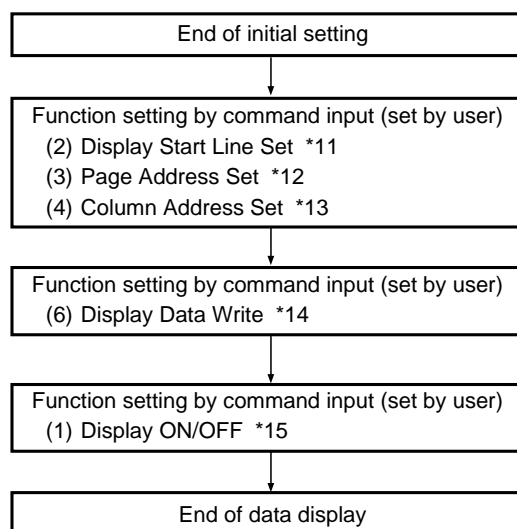
Notes: Reference items

    *11: 7. Command Description Item (2) "Display Start Line Set"

    *12: 7. Command Description Item (3) "Page Address Set"

    *13: 7. Command Description Item (4) "Column Address Set"

    *14: The contents of DDRAM is not defined after completing initial setting. Enter data in each DDRAM to be used for display.

           7. Command Description Item (6) "Display Data Write"

    *15: Avoid activating the display function with entering space characters as the data if possible.

           7. Command Description Item (1) "Display ON/OFF"

(3) Refresh *16

```
      ┌───→┌─────────────────────────────────────┐
      │    │            A desired mode             │
      │    └─────────────────────────────────────┘
      │                      ↓
      │    ┌─────────────────────────────────────┐
      │    │         Set all commands again.       │
      │    └─────────────────────────────────────┘
      │                      ↓
      │    ┌─────────────────────────────────────┐
      │    │    Write in the display data RAM again.│
      │    └─────────────────────────────────────┘
      └──────────────────────┘
```
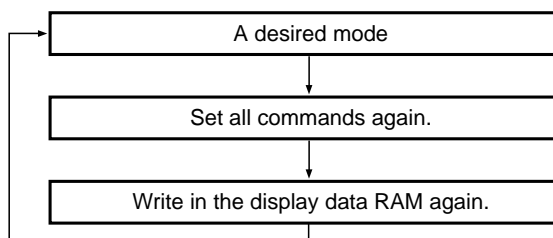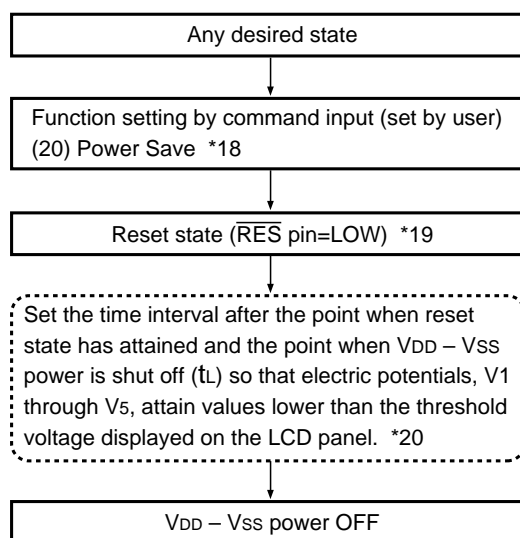
Notes: Reference items

    *16: It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.

(4) Power *17

```
┌─────────────────────────────────────┐
│          Any desired state           │
└─────────────────────────────────────┘
                    ↓
┌─────────────────────────────────────┐
│ Function setting by command input    │
│ (set by user)                        │
│ (20) Power Save  *18                 │
└─────────────────────────────────────┘
                    ↓
┌─────────────────────────────────────┐
│      Reset state (RES pin=LOW)  *19  │
└─────────────────────────────────────┘
                    ↓
┌ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┐
  Set the time interval after the point
  when reset state has attained and the
  point when $V_{DD} - V_{SS}$ power is shut
  off ($t_L$) so that electric potentials, V1
  through V5, attain values lower than the
  threshold voltage displayed on the LCD
  panel.  *20
└ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┘
                    ↓
┌─────────────────────────────────────┐
│        $V_{DD} - V_{SS}$ power OFF    │
└─────────────────────────────────────┘
```

Notes: Reference items

    *17: This IC is a $V_{DD} - V_{SS}$ power system circuit controlling the LCD driving circuit for the $V_{DD} - V5$ power system. Shutting of power with voltage remaining in the $V_{DD} - V5$ power system may cause uncontrolling voltage to be output from the SEG and COM pins. Follow the Power OFF sequence.

    *18: 7. Command Description Item (20) "Power Saving"

    *19: When external power supplies for driving LCD are used, turn all external power supplies off before entering reset state.
            6. Function Description Item "Reset Circuit"

    *20: The threshold voltage of the LCD panel is about 1 [V].
          When the internal power supply circuit is used, discharge time t_H from the start of resetting to the voltage between V_{DD} and $V5$ being reduced to 1 volt depends on capacitor C2 to be connected between $V1 - V5$ and V_{DD}. Figure 5 shows the reference values.
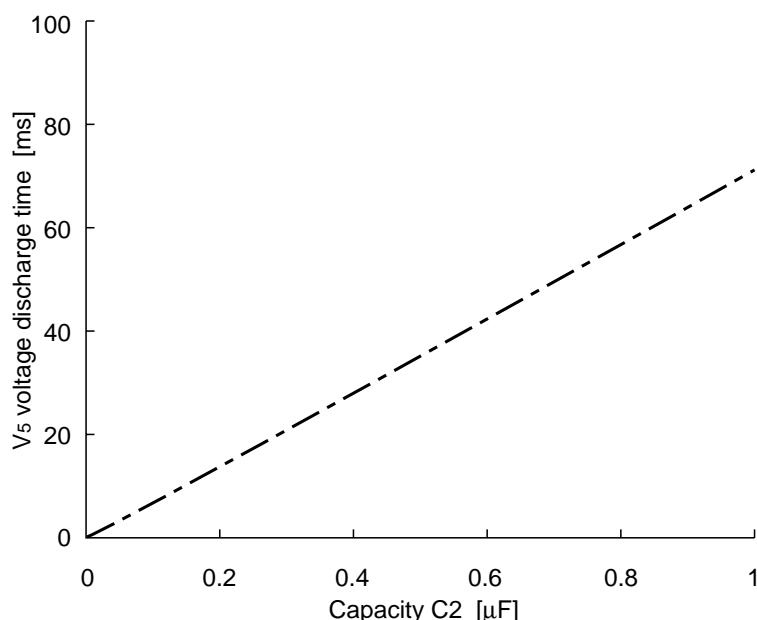
Figure 20

Set up t_L so that the relationship, $t_L > t_H$, is maintained. A state of $t_L < t_H$ may cause faulty display.
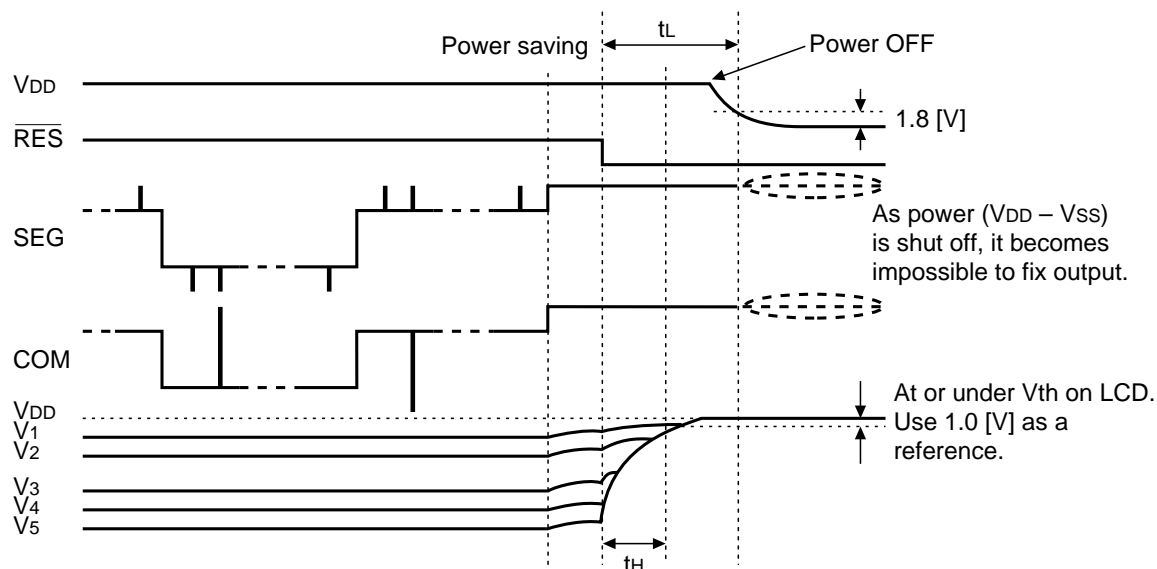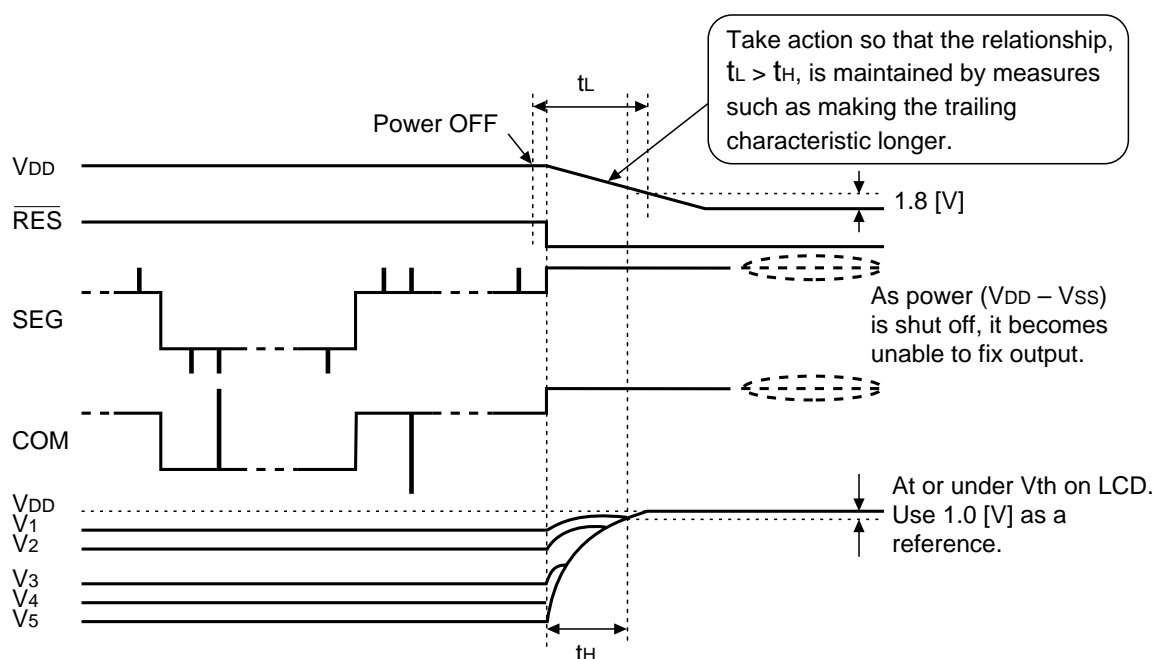
Figure 21

If command control is disabled when power is OFF, take action so that the relationship, $t_L > t_H$, is maintained by measures such as making the trailing characteristic of power ($V_{DD} - V_{SS}$) longer.

Figure 22

9. ABSOLUTE MAXIMUM RATINGS

Table 17

V_{SS}=0 V unless specified otherwise

Item		Symbol	Specification value			Unit
Power supply voltage		V_{DD}	−0.3	to	+7.0	V
Power supply voltage (2) (Based on V_{DD})		V_{SS2}	−7.0	to	+0.3	
	At triple boosting		−6.0	to	+0.3	
	At quadruple boosting		−4.5	to	+0.3	
Power supply voltage (3) (Based on V_{DD})		V_5, V_{OUT}	−22.0	to	+0.3	
Power supply voltage (4) (Based on V_{DD})		V_1, V_2, V_3, V_4	V_5	to	+0.3	
Input voltage		V_{IN}	−0.3	to	V_{DD}+0.3	
Output voltage		V_O	−0.3	to	V_{DD}+0.3	
Operating temperature		T_{OPR}	−40	to	+85	°C
Storage temperature	TCP	T_{STR}	−55	to	+100	
	Bare chip		−55	to	+125	

System (MPU) side   S1D15710 side
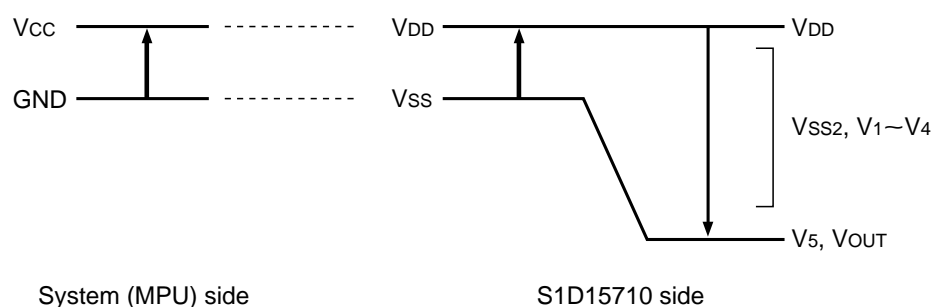
Figure 23

(Notes) 1. The values of the V_{SS2}, V_1 to V_5, and V_{OUT} voltages are based on V_{DD}=0 V.
2. The V_1, V_2, V_3, and V_4 voltages must always satisfy the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Insure that voltage levels V_{SS2} and V_{OUT} are always such that the relationship of $V_{DD} \geq V_{SS} \geq V_{SS2} \geq V_{OUT}$ is maintained.
4. When LSI is used exceeding the absolute maximum ratings, the LSI may be damaged permanently. Besides, it is desirable that the LSI should be used in the electrical characteristics condition for normal operation. If this condition is exceeded, the LSI may malfunction and have an adverse effect on the reliability of the LSI.

10. DC CHARACTERISTICS

Table 18

V_{SS}=0 V, V_{DD}=3.0 V $\pm$ 10%, and Ta=−40 to +85°C

Item		Symbol	Condition		Specification value			Unit	Applicable pin
					Min.	Typ.	Max.		
Operating voltage (1)	Recommended operation	V_{DD}			2.7	—	3.3	V	V_{DD} *1
	Operable	V_{DD}			1.8	—	5.5		V_{DD} *1
Operating voltage (2)	Recommended operation	V_{SS2}	(Based on V_{DD})		−3.3	—	−2.7		V_{SS2}
	Operable	V_{SS2}	(Based on V_{DD})		−6.0	—	−1.8		V_{SS2}
Operating voltage (3)	Operable	V_5	(Based on V_{DD})		−18.0	—	−4.5		V_5 *2
	Operable	V_1, V_2	(Based on V_{DD})		$0.4 \times V_5$	—	V_{DD}		V_1, V_2
	Operable	V_3, V_4	(Based on V_{DD})		V_5	—	$0.6 \times V_5$		V_3, V_4
High level input voltage		V_{IHC}			$0.8 \times V_{DD}$	—	V_{DD}		*3
Low level input voltage		V_{ILC}			V_{SS}	—	$0.2 \times V_{DD}$		*3
High level output voltage		V_{OHC}	I_{OH}=−0.5mA		$0.8 \times V_{DD}$	—	V_{DD}		*4
Low level output voltage		V_{OLC}	I_{OL}=0.5mA		V_{SS}	—	$0.2 \times V_{DD}$		*4
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}		−1.0	—	1.0	μA	*5
Output leak current		I_{LO}			−3.0	—	3.0		*6
Liquid crystal driver On resistance		R_{ON}	Ta=25°C (Based on V_{DD})	V_5=−14.0V	—	2.0	3.5	kΩ	SEGn COMn *7
				V_5=−8.0V	—	3.2	5.4		
Static current consumption		I_{SSQ}			—	0.01	5	μA	V_{SS}, V_{SS2}
Output leak current		I_{5Q}	V_5=−18.0V (Based on V_{DD})		—	0.01	15		V_5
Input pin capacity		C_{IN}	Ta=25°C, f=1MHz		—	5.0	8.0	pF	
Oscillating frequency	Built-in oscillation	f_{OSC}	Ta=25°C		18	22	26	kHz	*8
	External input	f_{CL}			4.5	5.5	6.5		CL *8

Table 19

	Item	Symbol	Condition		Specification value			Unit	Applicable pin
					Min.	Typ.	Max.		
Built-in power supply circuit	Input voltage	V_{SS2}	At triple boosting (Based on V_{DD})		−6.0	—	−1.8	V	V_{SS2}
		V_{SS2}	At quadruple boosting (Based on V_{DD})		−5.0	—	−1.8		V_{SS2}
	Boosting output voltage	V_{OUT}	(Based on V_{DD})		−20.0	—	—		V_{OUT}
	Voltage adjusting circuit operating voltage	V_{OUT}	(Based on V_{DD})		−20.0	—	−6.0		V_{OUT}
	V/F circuit operating voltage	V_5	(Based on V_{DD})		−18.0	—	−4.5		V_5 *9
	Reference voltage	V_{REG0}	Ta=25°C,	−0.05%/°C	−2.04	−2.10	−2.16		*10

[*: see Page 49.]

10. DC CHARACTERISTICS

Dynamic current consumption value (1) During display operation and built-in power supply OFF

Current values dissipated by the whole IC when the external power supply is used

Table 20 Display All White   Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15710D00B*	I_{DD}	V_{DD}=5.0V, V_5−V_{DD}=−11.0V	—	25	42	µA	*11
/D11B*	(1)	V_{DD}=3.0V, V_5−V_{DD}=−11.0V	—	25	42		

Table 21 Display Checker Pattern   Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15710D00B*	I_{DD}	V_{DD}=5.0V, V_5−V_{DD}=−11.0V	—	38	64	µA	*11
/D11B*	(1)	V_{DD}=3.0V, V_5−V_{DD}=−11.0V	—	38	64		

Dynamic current consumption value (2) During display operation and built-in power supply ON

Current values dissipated by the whole IC containing the built-in power supply circuit

Table 22 Display All White   Ta=25°C

Item	Symbol	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
S1D15710	I_{DD}	V_{DD}=5.0V, Triple boosting	Normal mode	—	92	154	µA	*12
D00B*/D11B*	(2)	V_5−V_{DD}=−11.0V	High power mode	—	242	405		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	129	216		
		V_5−V_{DD}=−11.0V	High power mode	—	310	518		
S1D15710D10B*		V_{DD}=5.0V, Triple boosting	Normal mode	—	135	225		
		V_5−V_{DD}=−11.0V	High power mode	—	288	480		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	176	294		
		V_5−V_{DD}=−11.0V	High power mode	—	363	605		

Table 23 Display Checker Pattern   Ta=25°C

Item	Symbol	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
S1D15710	I_{DD}	V_{DD}=5.0V, Triple boosting	Normal mode	—	132	221	µA	*12
D00B*/D11B*	(2)	V_5−V_{DD}=−11.0V	High power mode	—	280	468		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	167	279		
		V_5−V_{DD}=−11.0V	High power mode	—	350	585		
S1D15710D10B*		V_{DD}=5.0V, Triple boosting	Normal mode	—	178	297		
		V_5−V_{DD}=−11.0V	High power mode	—	330	550		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	220	367		
		V_5−V_{DD}=−11.0V	High power mode	—	406	677		

Current consumption at power save V_{SS}=0 V and V_{DD}=3.0 V ±10%

Table 24   Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}		—	0.01	5	µA	
Stand-by state	I_{DDS2}		—	4	8		

[*: see Page 49.]

[Reference data 1]
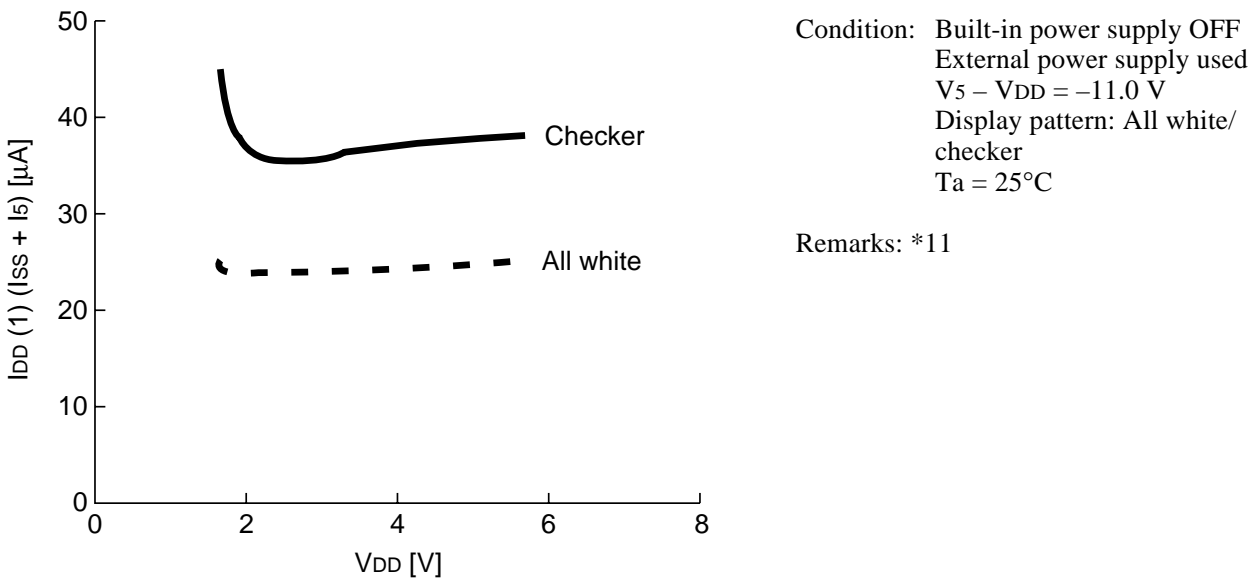• Dynamic current consumption (1) External power supply used and LCD being displayed

Condition: Built-in power supply OFF
External power supply used
$V_5 - V_{DD} = -11.0$ V
Display pattern: All white/
checker
$Ta = 25°C$

Remarks: *11

Figure 24

[Reference data 2]
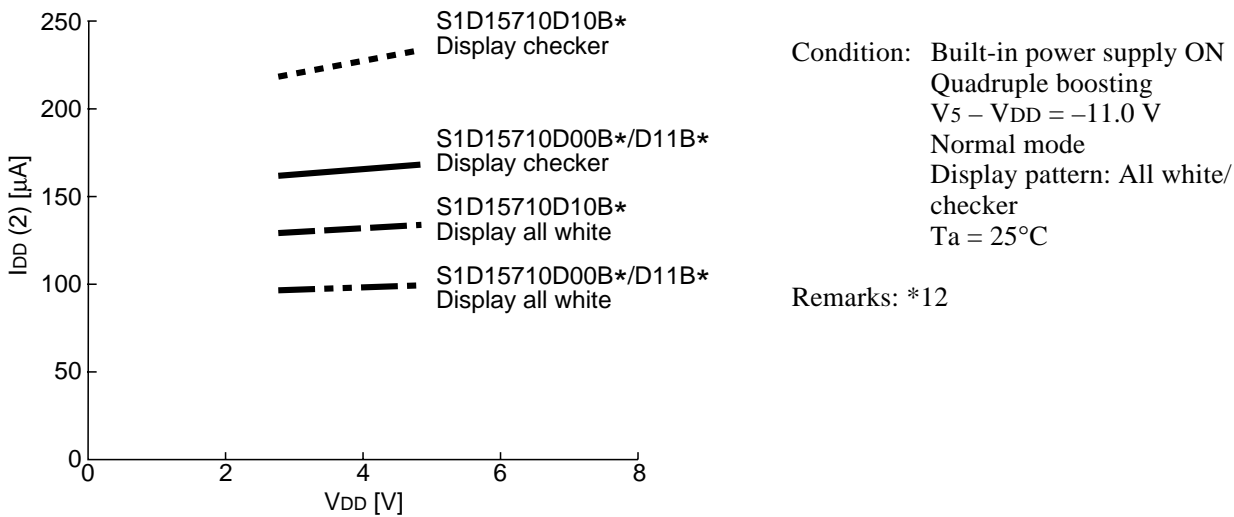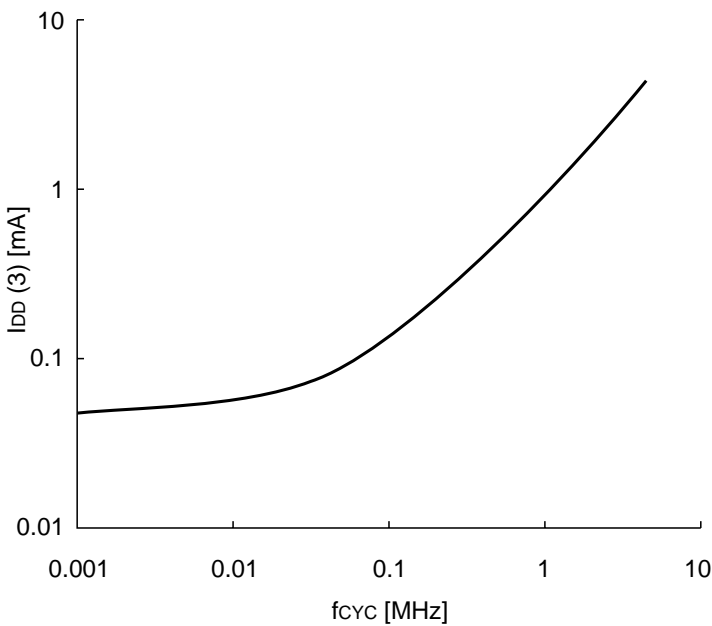• Dynamic current consumption (2) Built-in power supply used and LCD being displayed

S1D15710D10B*
Display checker

S1D15710D00B*/D11B*
Display checker

S1D15710D10B*
Display all white

S1D15710D00B*/D11B*
Display all white

Condition: Built-in power supply ON
Quadruple boosting
$V_5 - V_{DD} = -11.0$ V
Normal mode
Display pattern: All white/
checker
$Ta = 25°C$

Remarks: *12

Figure 25

[Reference data 3]
• Dynamic current consumption (3) During access

Indicates the current consumption when the checker pattern is always written at f_{CYC}.
Only I_{DD} (1) when not accessed
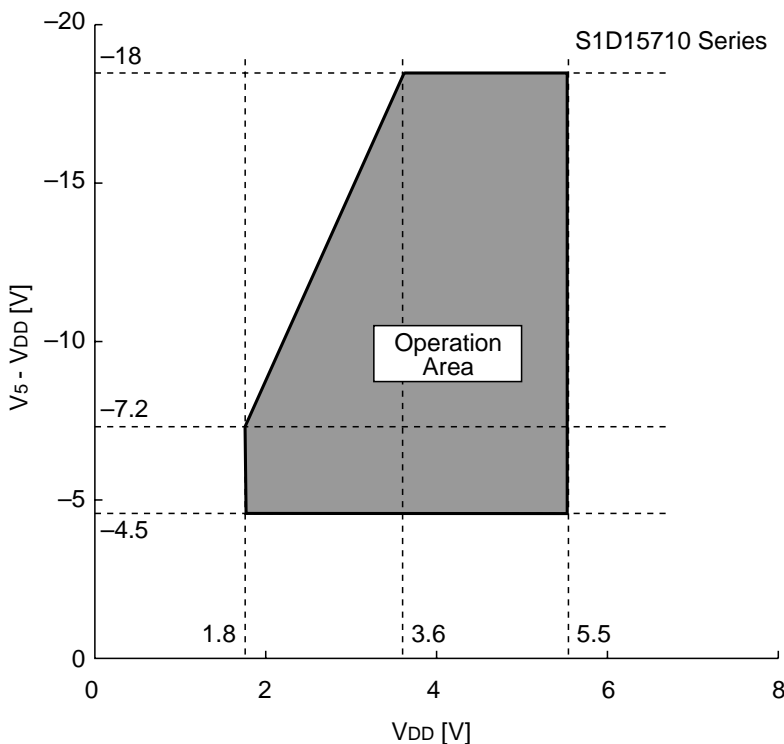Condition: Built-in power supply OFF and external power supply used
$V_{DD} – V_{SS} = 3.0$ V,
$V_5 – V_{DD} = –11.0$ V
$Ta = 25°C$

Figure 26

[Reference data 4]

V_{SS} and V_5 system operating voltage ranges

Remarks: *2

Figure 27

[*: see page 49.]

Relationships between the oscillating frequency f$_{OSC}$, display clock frequency f$_{CL}$, and liquid crystal frame frequency f$_{FR}$

Table 25

Item	f$_{CL}$	f$_{FR}$
When built-in oscillator circuit used	$\dfrac{f_{OSC}}{4}$	$\dfrac{f_{OSC}}{4*65}$
When built-in oscillator circuit not used	External input (f$_{CL}$)	$\dfrac{f_{CL}}{65}$

(f$_{FR}$ indicates the alternating current cycle of the liquid crystal and does not indicate that of the FR signal.)

[Reference items marked by *]

*1   The wide operating voltage range is not warranted. However, when there is a sudden voltage change during MPU access, it cannot be warranted.

*2   For the V$_{DD}$ and V$_5$ operating voltage ranges, see Figure 27. These ranges are applied when using the external power supply.

*3   A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, $\overline{IRS}$ and $\overline{HPM}$ pins

*4   D0 to D7, FR, FRS, $\overline{DOF}$ and CL pins

*5   A0, $\overline{RD}$ (E), $\overline{WR}$ (R/W), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, $\overline{RES}$, IRS and $\overline{HPM}$ pins

*6   Applied when D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ pins are in the high impedance state

*7   Resistance value when the 0.1 V voltage is applied between the output pin SEGn or COMn and power supply pins (V$_1$, V$_2$, V$_3$, and V$_4$). Specified within the range of operating voltage (3)
R$_{ON}$ = 0.1 V/ΔI (ΔI indicates the current applied when 0.1 V is applied between the power ON.)

*8   For the relationship between the oscillating frequency and frame frequency. The specification value of the external input item is a recommended value.

*9   The V$_5$ voltage adjusting circuit is adjusted within the voltage follower operating voltage range.

*10   This is the internal voltage reference supply for the V$_5$ voltage regulator circuit. The thermal slope V$_{REG}$ of the S1D15710 Series is about –0.05%/°C.

*11 and *12   Indicate the current dissipated by a single IC at built-in oscillator circuit used, 1/9 bias, and display ON.
Does not include the current due to the LCD panel capacity and wiring capacity.
Applicable only when there is no access from the MPU.

*12   When the V$_5$ voltage adjusting built-in resistor is used

10. DC CHARACTERISTICS

Timing Characteristics

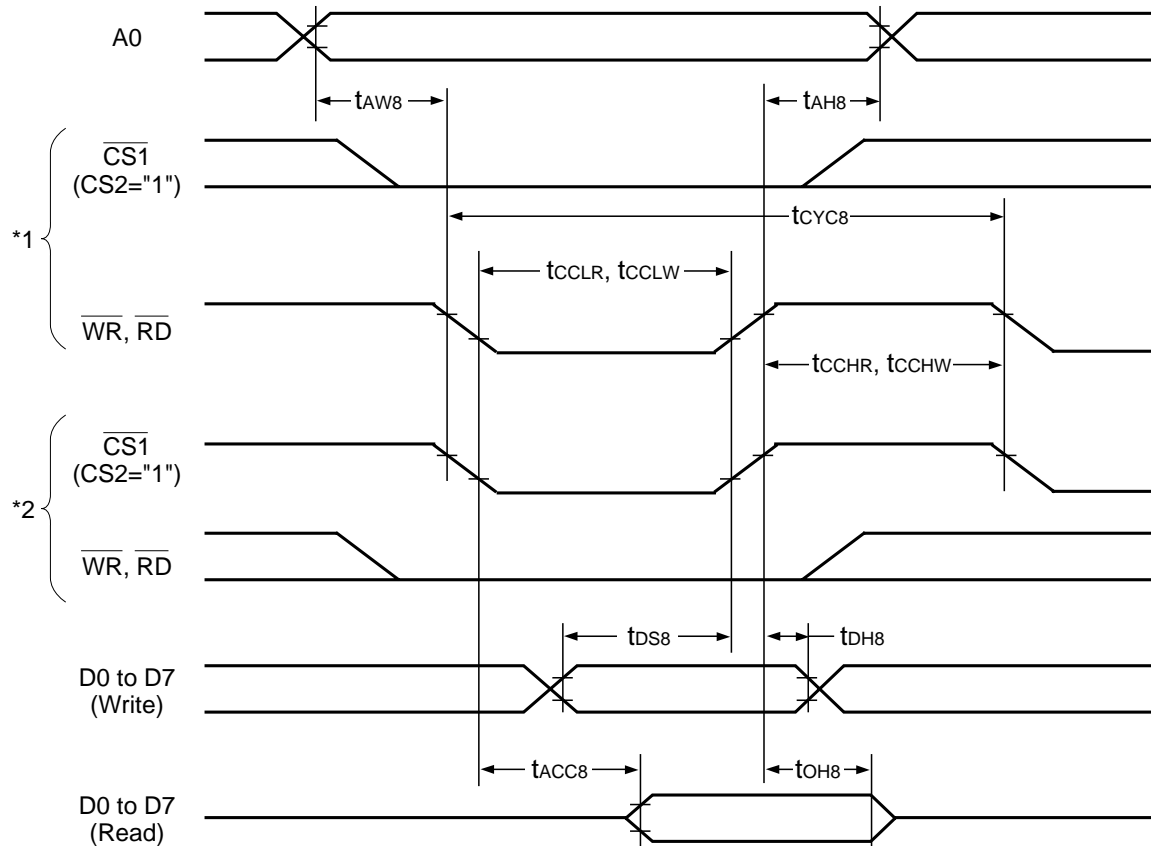**System bus read/write characteristics 1 (80 series MPU)**

Figure 28

*1 is set when $\overline{CS}$ is LOW and access is made with $\overline{WR}$ and $\overline{RD}$.
*2 is used when $\overline{WR}$ and $\overline{RD}$ are LOW and accessed with $\overline{CS}$.

Table 26

[V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		333	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		30	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		70	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		30	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		30	—	
Data setup time	D0 to D7	t_{DS8}		30	—	
Data hold time		t_{DH8}		10	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	70	
Output disable time		t_{OH8}		5	50	

Table 27

[V$_{DD}$=2.7V to 4.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t$_{AH8}$		0	—	ns
Address setup time		t$_{AW8}$		0	—	
System cycle time	A0	t$_{CYC8}$		500	—	
Control LOW pulse width (Write)	$\overline{WR}$	t$_{CCLW}$		60	—	
Control LOW pulse width (Read)	$\overline{RD}$	t$_{CCLR}$		120	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t$_{CCHW}$		60	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t$_{CCHR}$		60	—	
Data setup time	D0 to D7	t$_{DS8}$		40	—	
Data hold time		t$_{DH8}$		15	—	
$\overline{RD}$ access time		t$_{ACC8}$	C$_L$=100pF	—	140	
Output disable time		t$_{OH8}$		10	100	

Table 28

[V$_{DD}$=1.8V to 2.7V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t$_{AH8}$		0	—	ns
Address setup time		t$_{AW8}$		0	—	
System cycle time	A0	t$_{CYC8}$		1000	—	
Control LOW pulse width (Write)	$\overline{WR}$	t$_{CCLW}$		120	—	
Control LOW pulse width (Read)	$\overline{RD}$	t$_{CCLR}$		240	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t$_{CCHW}$		120	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t$_{CCHR}$		120	—	
Data setup time	D0 to D7	t$_{DS8}$		80	—	
Data hold time		t$_{DH8}$		30	—	
$\overline{RD}$ access time		t$_{ACC8}$	C$_L$=100pF	—	280	
Output disable time		t$_{OH8}$		10	200	

*1.   This is the case of accessing by $\overline{WR}$ and $\overline{RD}$ when $\overline{CS1}$ = LOW.
*2.   This is the case of accessing by $\overline{CS1}$ when $\overline{WR}$ and $\overline{RD}$ = LOW.
*3   The rise and fall times (t$_r$ and t$_f$) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t$_r$+t$_f$) ≤ (t$_{CYC8}$–t$_{CCLW}$–t$_{CCHW}$) or (t$_r$+t$_f$) ≤ (t$_{CYC8}$–t$_{CCLR}$–t$_{CCHR}$).
*4   All timings are specified based on the 20 and 80% of V$_{DD}$.
*5   t$_{CCLW}$ and t$_{CCLR}$ are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2= HIGH) level and $\overline{WR}$, $\overline{RD}$ are at the LOW level.

10. DC CHARACTERISTICS

System bus read/write characteristics 2 (68 series MPU)
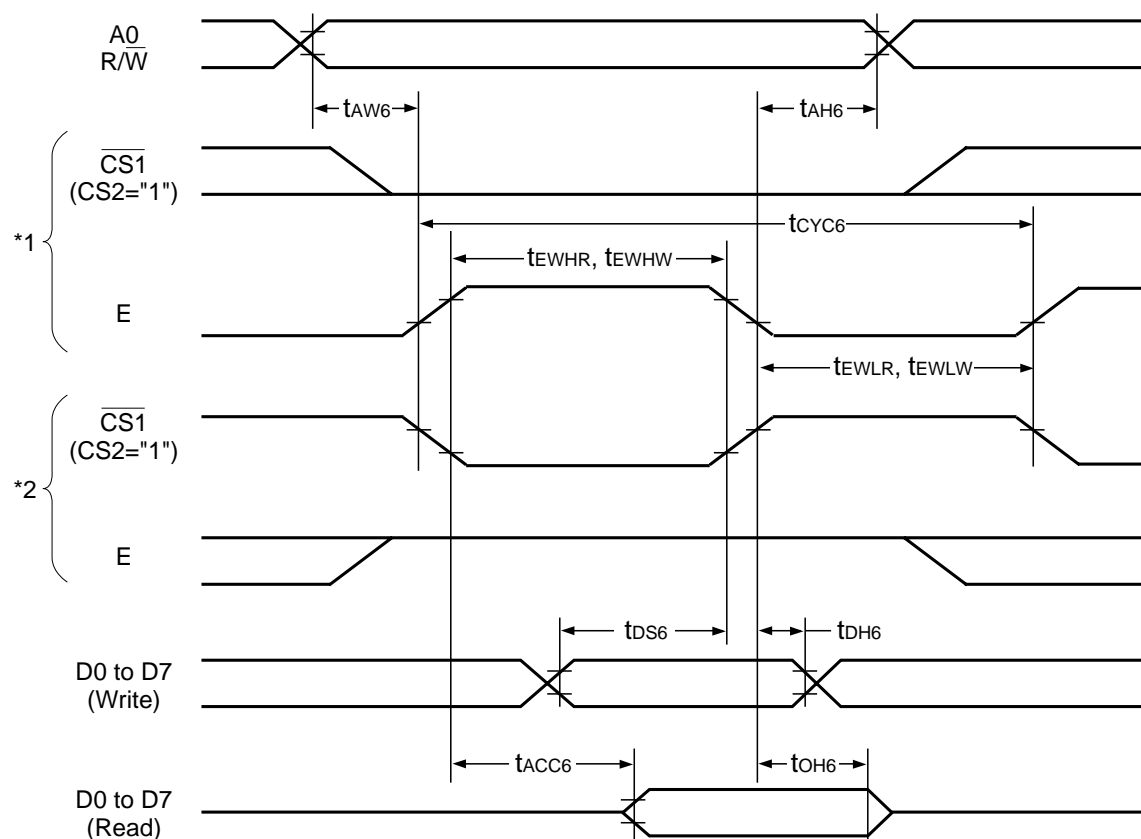

Figure 29

*1 is set when $\overline{CS}$ is LOW and access is made with E.
*2 is used when E is HIGH and access is made with $\overline{CS}$.

Table 29

[VDD=4.5V to 5.5V, Ta=–40 to +85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	tAH6		0	—	ns
Address setup time			tAW6		0	—	
System cycle time			tCYC6		333	—	
Data setup time		D0 to D7	tDS6		30	—	
Data hold time			tDH6		10	—	
Access time			tACC6	CL=100pF	—	70	
Output disable time			tOH6		10	50	
Enable HIGH pulse width	Read	E	tEWHR		70	—	
	Write		tEWHW		30	—	
Enable LOW pulse width	Read	E	tEWLR		30	—	
	Write		tEWLW		30	—	

Table 30

[V$_{DD}$=2.7V to 4.5V, Ta=–40 to +85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t$_{AH6}$		0	—	ns
Address setup time			t$_{AW6}$		0	—	
System cycle time			t$_{CYC6}$		500	—	
Data setup time		D0 to D7	t$_{DS6}$		40	—	
Data hold time			t$_{DH6}$		15	—	
Access time			t$_{ACC6}$	C$_L$=100pF	—	140	
Output disable time			t$_{OH6}$		10	100	
Enable HIGH pulse width	Read	E	t$_{EWHR}$		120	—	
	Write		t$_{EWHW}$		60	—	
Enable LOW pulse width	Read	E	t$_{EWLR}$		60	—	
	Write		t$_{EWLW}$		60	—	

Table 31

[V$_{DD}$=1.8V to 2.7V, Ta=–40 to +85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t$_{AH6}$		0	—	ns
Address setup time			t$_{AW6}$		0	—	
System cycle time			t$_{CYC6}$		1000	—	
Data setup time		D0 to D7	t$_{DS6}$		80	—	
Data hold time			t$_{DH6}$		30	—	
Access time			t$_{ACC6}$	C$_L$=100pF	—	280	
Output disable time			t$_{OH6}$		10	200	
Enable HIGH pulse width	Read	E	t$_{EWHR}$		240	—	
	Write		t$_{EWHW}$		120	—	
Enable LOW pulse width	Read	E	t$_{EWLR}$		120	—	
	Write		t$_{EWLW}$		120	—	

*1   This is the case of accessing by E when $\overline{CS1}$ = LOW.
*2   This is the case of accessing by $\overline{CS1}$ when E = HIGH.
*3   The rise and fall times (t$_r$ and t$_f$) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t$_r$+t$_f$) $\leq$ (t$_{CYC6}$–t$_{EWLW}$–t$_{EWHW}$) or (t$_r$+t$_f$) $\leq$ (t$_{CYC6}$–t$_{EWLR}$–t$_{EWHR}$).
*4   All timings are specified based on the 20 and 80% of V$_{DD}$.
*5   t$_{EWLW}$ and t$_{EWLR}$ are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2 = HIGH) level and E is at the HIGH level.
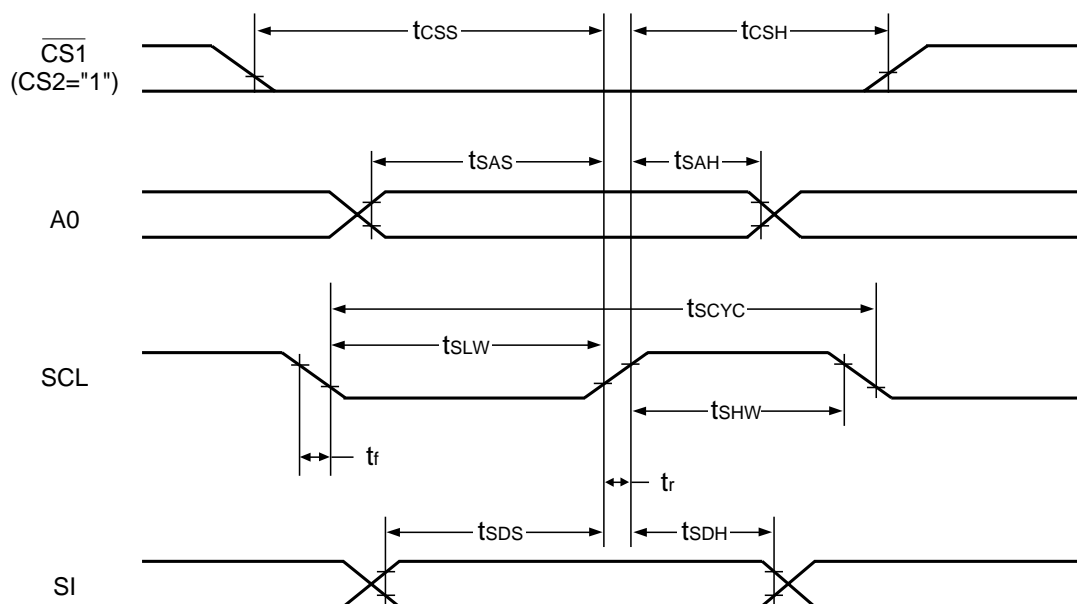
10. DC CHARACTERISTICS

Serial interface

Figure 30

Table 32

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	tSCYC		200	—	ns
SCL HIGH pulse width		tSHW		75	—	
SCL LOW pulse width		tSLW		75	—	
Address setup time	A0	tSAS		50	—	
Address hold time		tSAH		100	—	
Data setup time	SI	tSDS		50	—	
Data hold time		tSDH		50	—	
CS-SCL time	CS	tCSS		100	—	
		tCSH		100	—	

Table 33

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	tSCYC		250	—	ns
SCL HIGH pulse width		tSHW		100	—	
SCL LOW pulse width		tSLW		100	—	
Address setup time	A0	tSAS		150	—	
Address hold time		tSAH		150	—	
Data setup time	SI	tSDS		100	—	
Data hold time		tSDH		100	—	
CS-SCL time	CS	tCSS		150	—	
		tCSH		150	—	

Table 34

[V$_{DD}$=1.8V to 2.7V, Ta=−40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t$_{SCYC}$		400	—	ns
SCL HIGH pulse width		t$_{SHW}$		150	—	
SCL LOW pulse width		t$_{SLW}$		150	—	
Address setup time	A0	t$_{SAS}$		250	—	
Address hold time		t$_{SAH}$		250	—	
Data setup time	SI	t$_{SDS}$		150	—	
Data hold time		t$_{SDH}$		150	—	
CS-SCL time	CS	t$_{CSS}$		250	—	
		t$_{CSH}$		250	—	

*1 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns.
*2 All timings are specified based on the 20 and 80% of V$_{DD}$.

Display control output timing
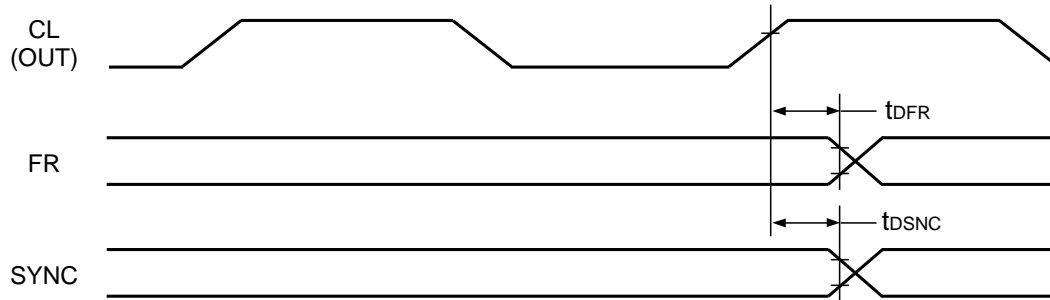
Figure 31

Table 35

[V$_{DD}$=4.5V to 5.5V, Ta=−40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t$_{DFR}$	C$_L$=50pF	—	10	40	ns
SYNC delay time	SYNC	t$_{DSNC}$	C$_L$=50pF	—	10	40	ns

Table 36

[V$_{DD}$=2.7V to 4.5V, Ta=−40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t$_{DFR}$	C$_L$=50pF	—	20	80	ns
SYNC delay time	SYNC	t$_{DSNC}$	C$_L$=50pF	—	20	80	ns

Table 37

[V$_{DD}$=1.8V to 2.7V, Ta=−40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t$_{DFR}$	C$_L$=50pF	—	50	200	ns
SYNC delay time	SYNC	t$_{DSNC}$	C$_L$=50pF	—	50	200	ns

*1 Valid only when the master mode is selected.
*2 All timings are specified based on the 20 and 80% of V$_{DD}$.
*3 Pay attention not to cause delays of the timing signals CL, FR and SYNC to the salve side by wiring resistance, etc., while master/slave operations are in progress. If these delays occur, indication failures such as flickering may occur.
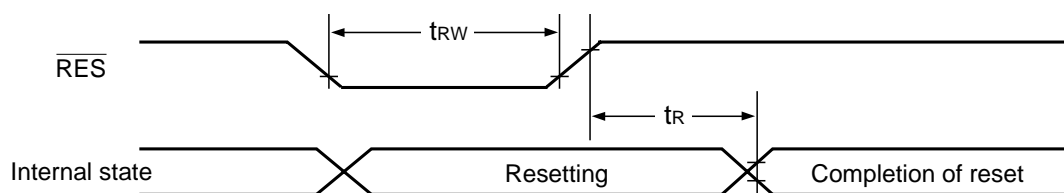
10. DC CHARACTERISTICS

Reset input timing

Figure 32

Table 38

[VDD=4.5V to 5.5V, Ta=−40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		tR		—	—	0.5	μs
Reset LOW pulse width	$\overline{RES}$	tRW		0.5	—	—	

Table 39

[VDD=2.7V to 4.5V, Ta=−40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	μs
Reset LOW pulse width	$\overline{RES}$	tRW		1	—	—	

Table 40

[VDD=1.8V to 2.7V, Ta=−40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	μs
Reset LOW pulse width	$\overline{RES}$	tRW		1.5	—	—	

*1   All timings are specified based on the 20 and 80% of VDD.

11. MICROPROCESSOR (MPU) INTERFACE: REFERENCE

The S1D15710 series can directly be connected to the 80 system MPU and 68 series MUP. It can also be operated with a fewer signal lines by using the serial interface.

The S1D15710 series is used for the multiple chip configuration to expand the display area. In this case, it can select the ICs that are accessed individually using the Chip Select signal.

After the initialization using the $\overline{RES}$ pin, the respective input pins of the S1D15710 series need to be controlled normally.

80 series MPU
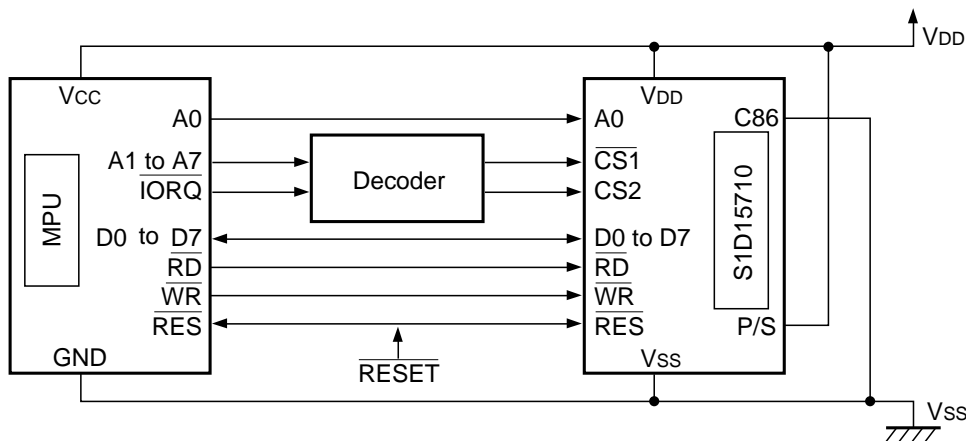
Figure 33-1

68 series MPU
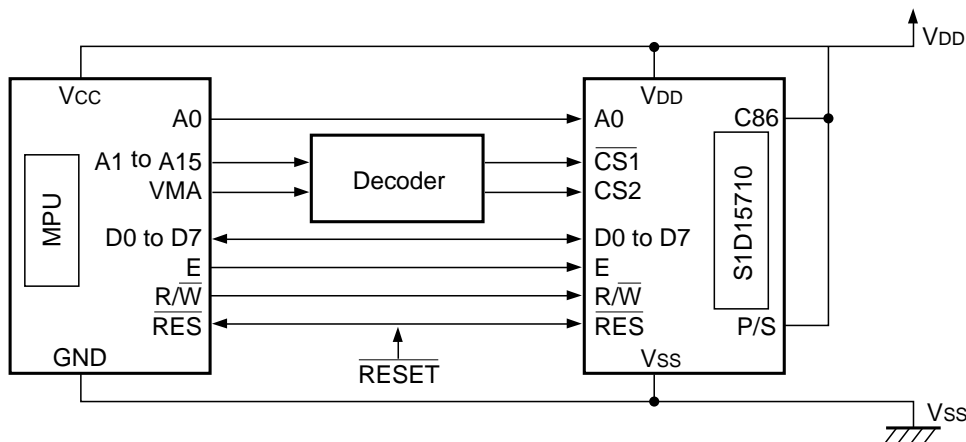
Figure 33-2

Serial interface
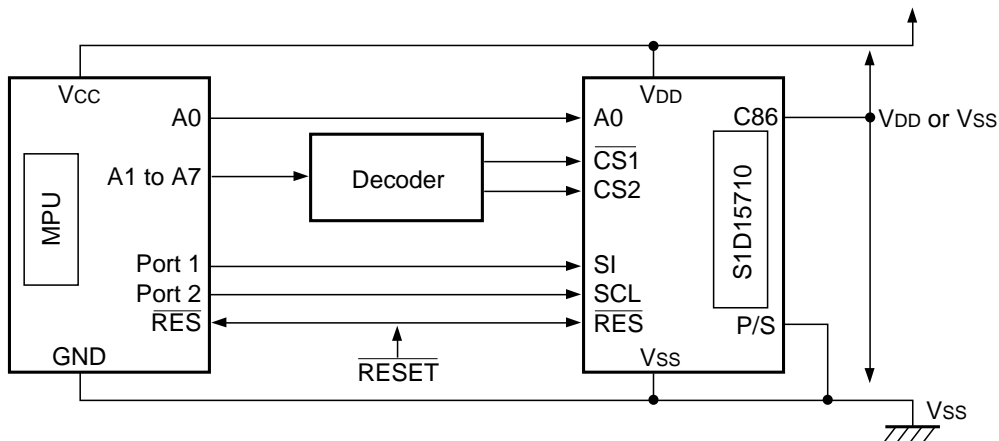
Figure 33-3

12. CONNECTION BETWEEN LCD DRIVERS: REFERENCE

The S1D15710 series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15710∗∗∗∗/S1D15710∗∗∗∗) for the master/slave.

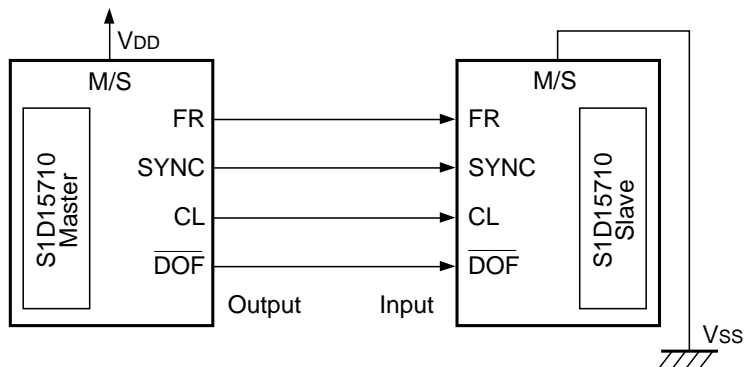**S1D15710 (master) ↔ S1D15710 (slave)**

Figure 34

13. LCD PANEL WIRING: REFERENCE

The S1D15710 series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15710∗∗∗∗/S1D15710∗∗∗∗) for the multiple chip configuration.

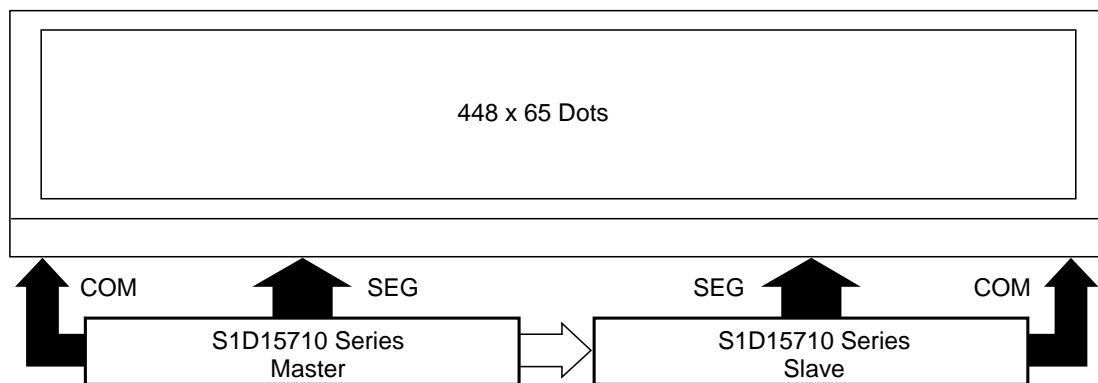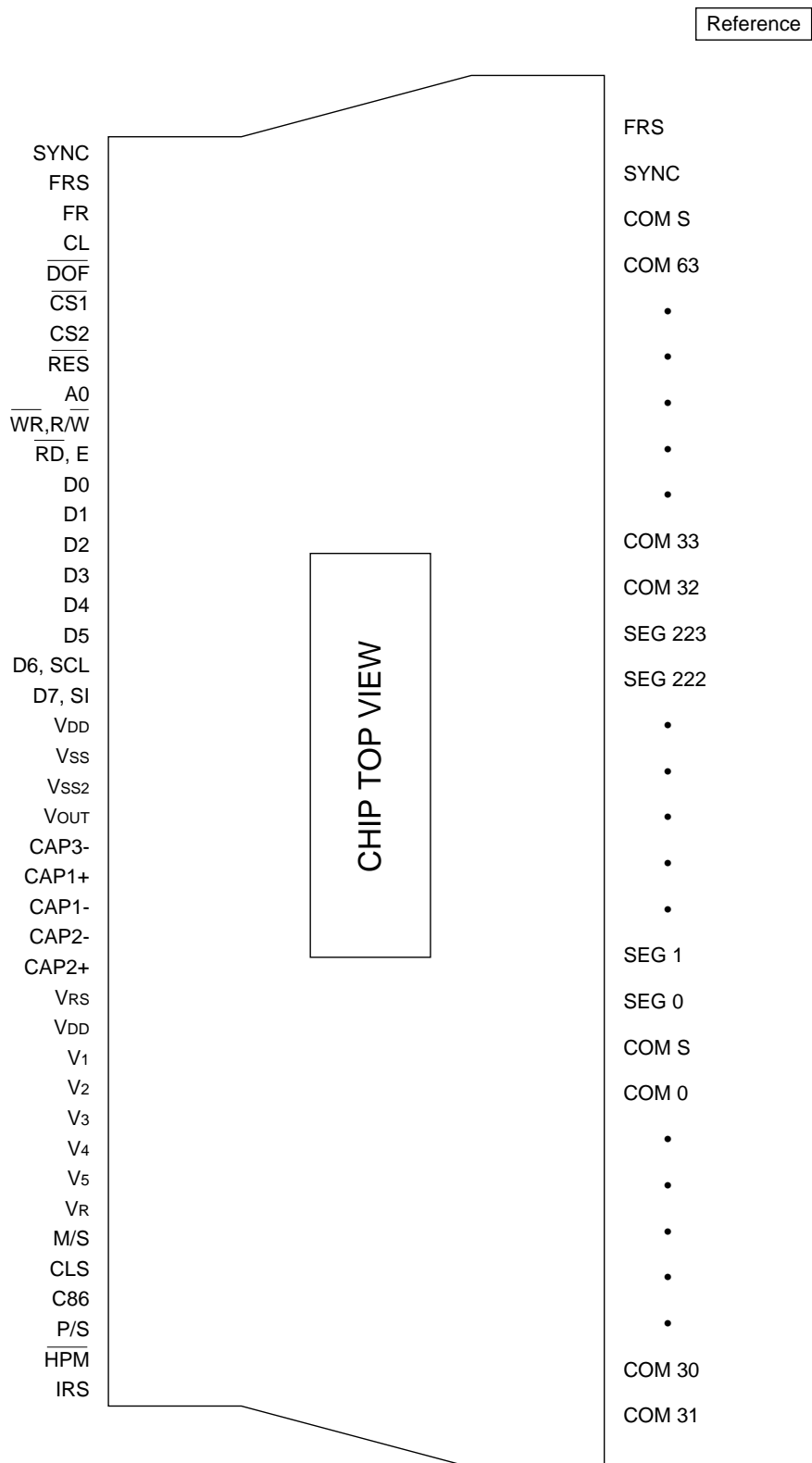### 1-chip configuration
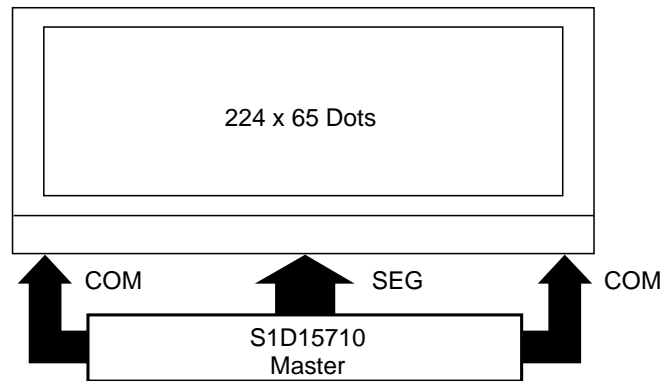
Figure 35-1

2-chip configuration

Figure 35-2

14. TCP PIN LAYOUT

Reference

Left pins	Right pins
SYNC	FRS
FRS	SYNC
FR	COM S
CL	COM 63
$\overline{\text{DOF}}$	•
$\overline{\text{CS1}}$	•
CS2	•
$\overline{\text{RES}}$	•
A0	•
$\overline{\text{WR}},\text{R}/\overline{\text{W}}$	COM 33
$\overline{\text{RD}}$, E	COM 32
D0	SEG 223
D1	SEG 222
D2	•
D3	•
D4	•
D5	•
D6, SCL	•
D7, SI	SEG 1
V_{DD}	SEG 0
V_{SS}	COM S
V_{SS2}	COM 0
V_{OUT}	•
CAP3-	•
CAP1+	•
CAP1-	•
CAP2-	•
CAP2+	COM 30
V_{RS}	COM 31
V_{DD}	
V_1	
V_2	
V_3	
V_4	
V_5	
V_R	
M/S	
CLS	
C86	
P/S	
$\overline{\text{HPM}}$	
IRS	

CHIP TOP VIEW

Note) This TCP pin layout does not specify the TCP dimensions.

15. TCP DIMENSIONS
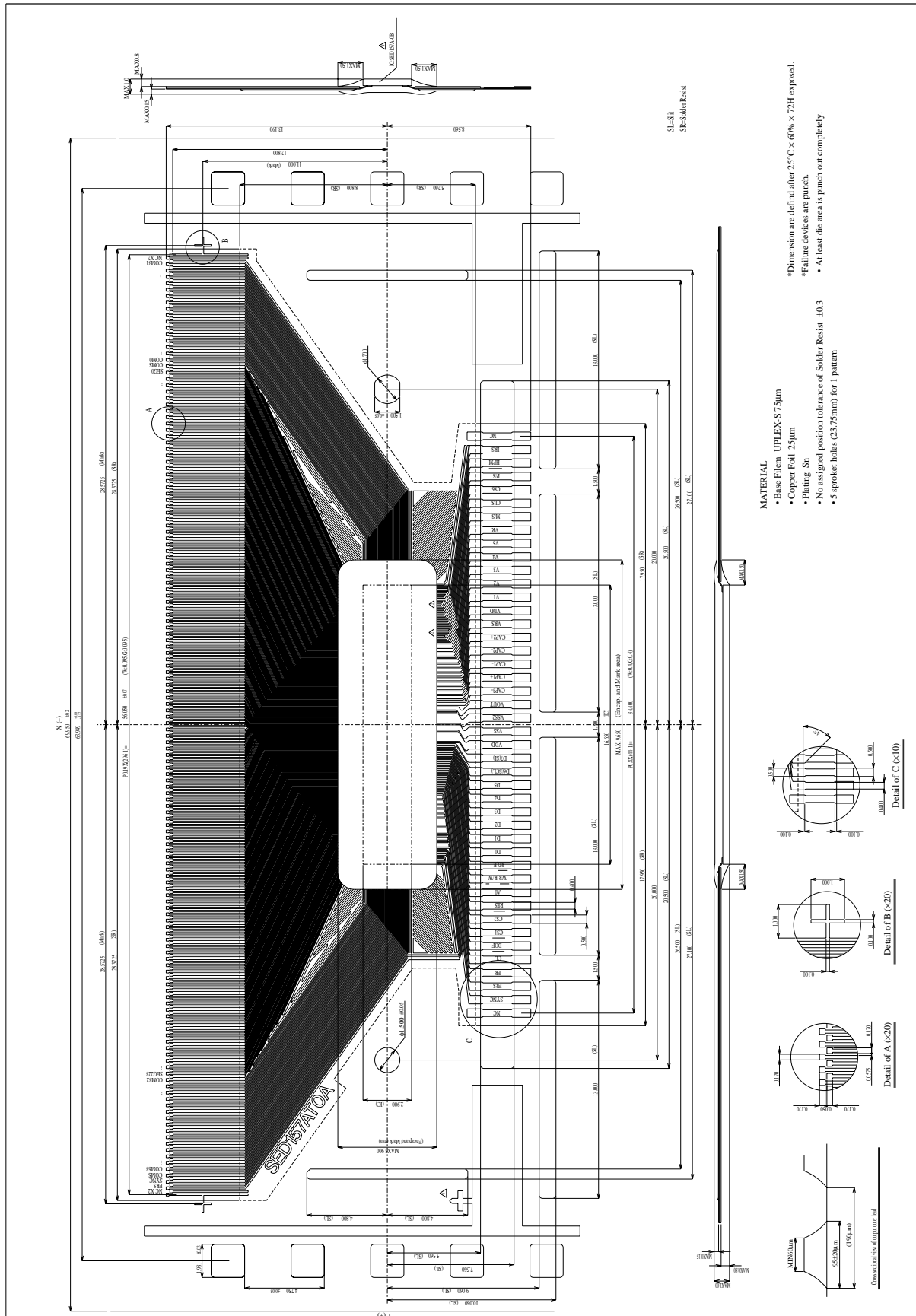
16. TEMPERATURE SENSOR CIRCUIT

Both the S1D15710∗10∗∗ and S1D15710∗11∗∗ have built-in temperature sensor circuits with analog voltage output terminals having a temperature gradient of 11.4mV/°C (Typ.). By controlling the liquid crystal drive voltage at V_5 by inputting an electric volume register value corresponding to the temperature sensor output value from the MPU enables liquid crystal to display appropriate light and shade over a wide range of temperatures.

Build a system to compensate for variations in the output voltage by feeding back the output voltage value sampled at a constant temperature to the MPU and store it as the standard voltage in order to achieve higher control of the liquid crystal drive voltage.

1. Terminal description

*Terminals related to the temperature sensor circuit are allocated to TEST 1 and 2, and are named V_{SEN1} for TEST1 and SVS1 for TEST2. Use the temperature sensor as indicated in the table below. When not in use, fix each terminal at HIGH.

Pin name	I/O	Description	Number of pins
SVS1	Power	Power terminal of the temperature sensor. Apply compulsory operation voltage to V_{DD}.	1
V_{SEN1}	O	Analog voltage output terminal of temperature sensor. Monitor the output voltage to V_{DD}.	1

2. Electrical characteristics

| Item	Symbol	Condition	Specification value			Unit	Applicable PIN
			Min.	Typ.	Max.		
Operating voltage	SVS	(V_{DD} standard)	−5.5	−5.0	−4.5	V	SVS1
Output voltage	V_{SEN}	(V_{DD} standard) Ta=−40°C	−4.35	−3.62	−2.89	V	V_{SEN1}
		(V_{DD} standard) Ta=25°C	−3.48	−2.88	−2.28		
		(V_{DD} standard) Ta=85°C	−2.92	−2.20	−1.47		
Output voltage temperature gradient	V_{GRA}	*1	9.4	11.4	13.4	mV/°C	V_{SEN1}
Output voltage linearity	ΔVL	*2	−1.5	−	1.5	%	V_{SEN1}
Output voltage setup time	tSEN	*3	100	−	−	mS	V_{SEN1}
Operating current	ISEN	Ta=25°C	−	40	150	μA	SVS1

*Notes:
  *1: Slope of approximate line of Typ. output voltage.
 *2: Maximum deviation of output voltage curve and approximate line.
When the output voltage difference between –40°C and 85°C is ΔVSEN, the difference between the approximate line and the output voltage value is ΔDIFF and the maximum value is ΔDIFF(Max.), output voltage linearity ΔVL will be expressed using the following formula:

$$\Delta V_L = \frac{\Delta DIFF(Max.)}{\Delta V_{SEN}} \times 100$$
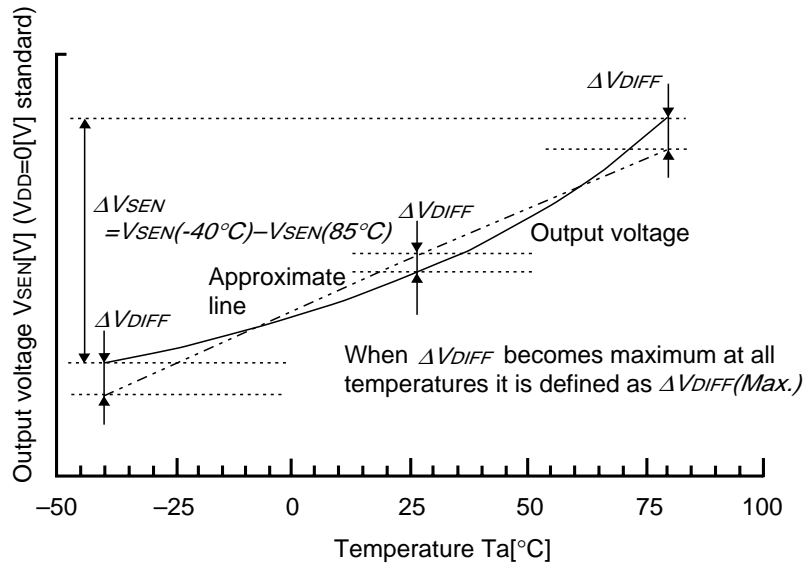
  *3: Waiting time until monitoring is enabled with stable output voltage after applying power voltage SVS to terminal SVS1. The output voltage needs to be sampled after a longer than standard waiting time.
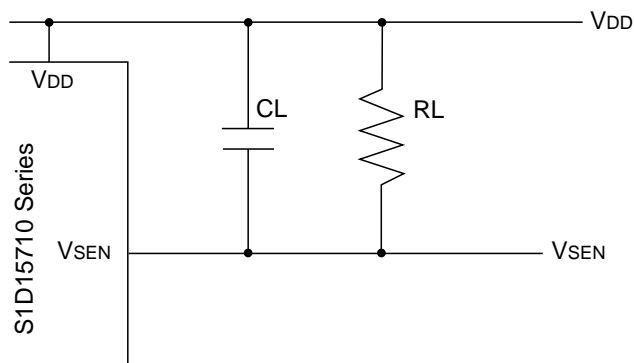
■ Output voltage characteristics
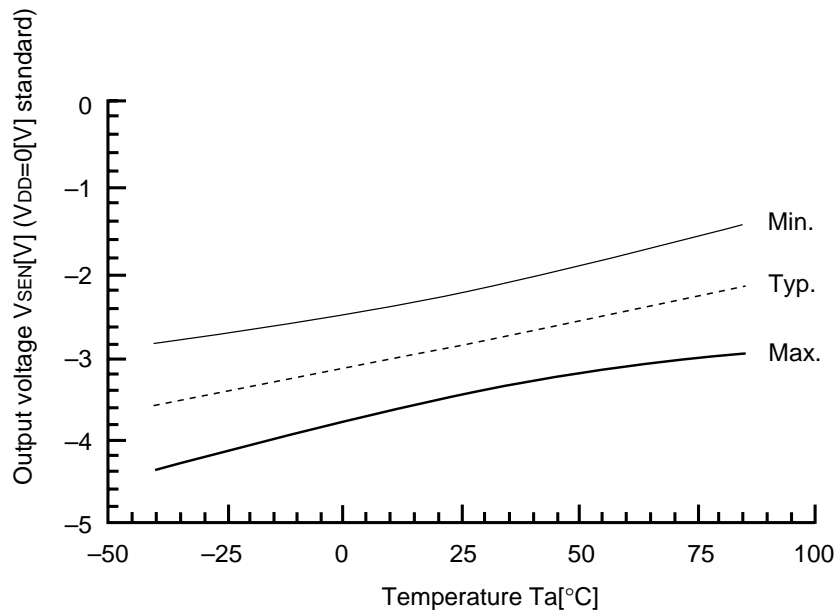
3. Output terminal load

Load capacity CL of VSEN output terminal VSEN1 should be under 100pF and load resistance RL higher than 1MΩ. Be careful not to build a current path between VSS in order to obtain an accurate output voltage value.

17. NOTES

The following points should be noted when this development specification is used:
Please be advised on the following points in use of this development specification.
1. This development Specification is subject to change without previous notice.
2. This development Specification does not guarantee or furnish the industrial property right not its execution. Application examples in this development specification are intended to ensure your better understanding of the product. Thus the manufacturer shall not be liable for any trouble arising in your circuits from using such application example.
   Numerical values provided in the property table of this manual are represented with their magnitude on the numerical line.
3. No part of this development specification may not be reproduced, copied or used for commercial purpose without a written permission from the manufacturer.

In handling of semiconductor devices, your attention is required to following points.
[Precaution on light]
Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in malfunctioning of the ICs. To prevent such malfunctioning of the ICs mounted on the boards or products, make sure that:
   (1) Your design and mounting layout done are so that the IC is not exposed to light in actual use.
   (2) The IC is protected from light in the inspection process.
   (3) The IC is protected from light in its front, rear and side faces.

Attention to COG module
When this IC is used as chip on glass (COG) module, it needs the greatest care as follows, because the resistance of ITO wire inserted between IC and external input / output pins may influence the display quality.
   (1) The resistance of ITO wire connected to external capacitor must be as low as possible.
   (2) The resistance of ITO wire connected to power source must be as low as possible.

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