EPSON
EXCEED YOUR VISION

S1D15721 Series
Technical Manual

SEIKO EPSON CORPORATION

Rev.2.1

NOTICE

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1. DESCRIPTION

The S1D15721 Series is a single chip MLS driver for dot matrix liquid crystal displays which can be directly connected to the microcomputer bus. It accepts the 8-bit parallel or serial display data from the microcomputer to store the data in the on-chip display data RAM, and issues liquid crystal drive signals independently of the microcomputer.

The S1D15721 Series provides both 4 gray-scale display and binary display. It incorporates a display data RAM (81 × 256 × 2 bits). In the case of 4 gray-scale display, 2 bits of the on-chip RAM respond to one-dot pixels, while in the case of binary display, 1 bit of the on-chip RAM respond to one-dot pixels.

The S1D15721 Series features 81 common output circuits and 256 segment output circuits. A single chip provides a display of 16 characters by 5 lines with 81 × 256 dots (16 × 16 dots) and display of 21 characters by 6 lines by the 12 × 12 dot-character font.

S1D15721 Series can be used to constitute a system to provide optimum LCD contrast throughout a wide temperature range without need for use of supplementary parts such as the thermistor, under controls of a microcomputer.

2. FEATURES

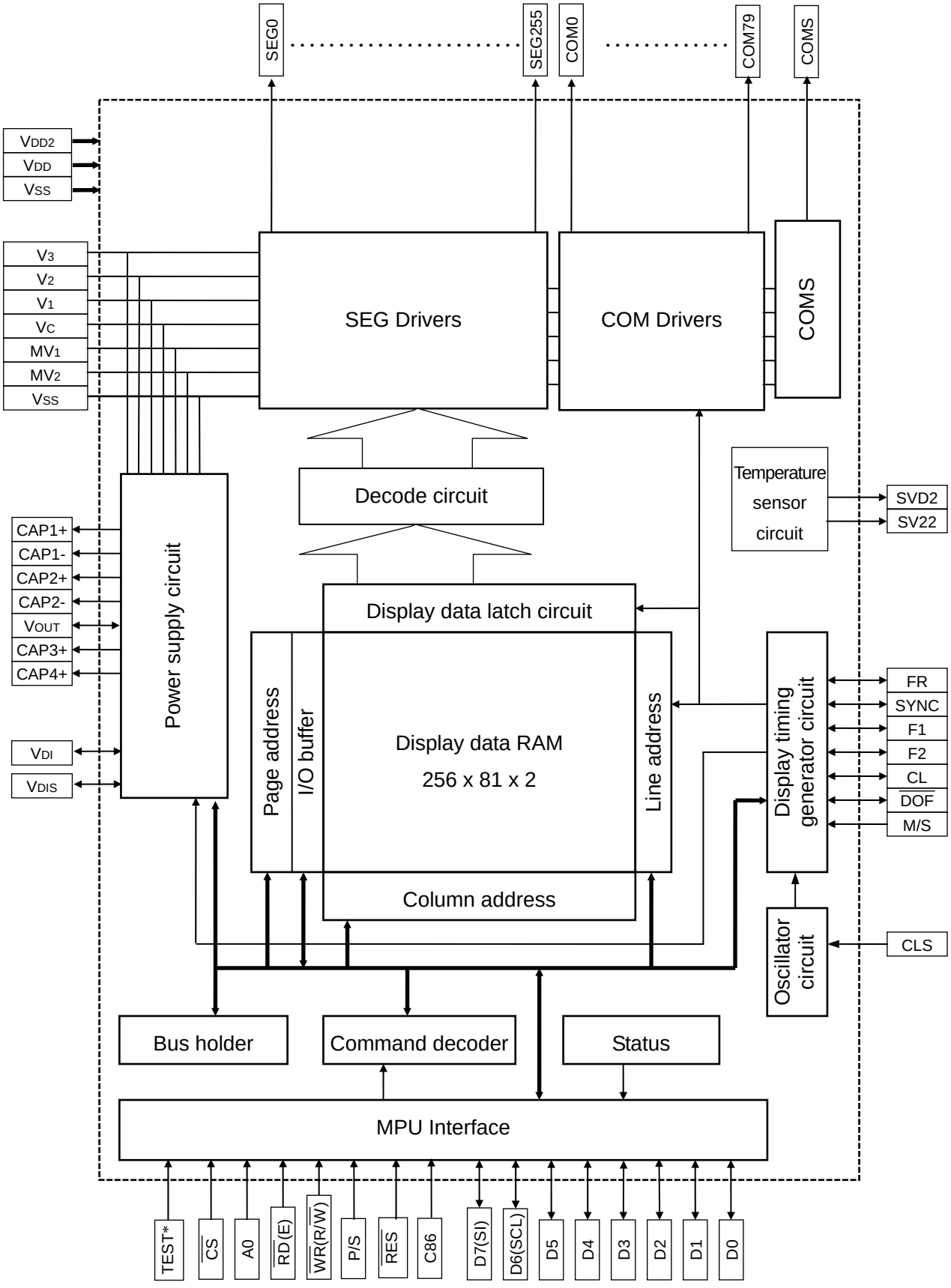
- Direct RAM data display by display data RAM
  - 4 gray-scale display
  (Normally white in normal display mode)
    RAM bit data (high order and low order)
      (1,1): gray-scale 3, black
      (1,0): gray-scale 2
      (0,1): gray-scale 1
      (0,0): gray-scale 0, white
  - Binary display
  (Normally white display is in normal mode)
    RAM bit data
      "1": On and black
      "0": Off and white
- RAM capacity
  $81 \times 256 \times 2 = 41{,}472$ bits
- Liquid crystal drive circuit
  81 common outputs and 256 segment outputs
- High-speed 8-bit MPU interface (directly connectable to the MPUs of both 80/68 series) / serial interface possible
- A variety of command functions
  Display Line Number set, n-line reversal, display data RAM address control, contrast control, display ON/OFF, display normal/reverse rotation, display all lighting ON/OFF, liquid crystal drive power supply circuit control, display clock built-in oscillator circuit control
- MLS drive technology
  Built-in high precision voltage regulation function
- High precision CR oscillator circuit incorporated
- Low power consumption
- Built-in temperature sensor circuit
- Power supply
  Logic power supply 1: V_{DI}-V_{SS}= 2.7 to 3.3V
  Logic power supply 2: V_{DD}-V_{SS}= 2.7 to 5.5V
  Liquid crystal drive power supply: V_3-V_{SS}= 5.6 to 17.0V
  Boosting power supply: V_{DD2}-V_{SS}= V_{DI} to 5.5V
- Wide operation temperature range:
  -40 to +85°C: S1D15721D00B000, -40 to +95°C: S1D15721D01B000
- CMOS process
- Shipping form: Bare chips, TCP
- Light and radiation proof measures are not taken in designing.

Series Specifications

Product name	Form of shipping	Chip thickness	Schmidt trigger input	Noise filter circuit	Operating temperature
S1D15721D00B000	Bare chip	0.625mm	—	$\overline{RES}$	-40 to +85 °C
S1D15721D01B000			*1	*1	-40 to +95°C

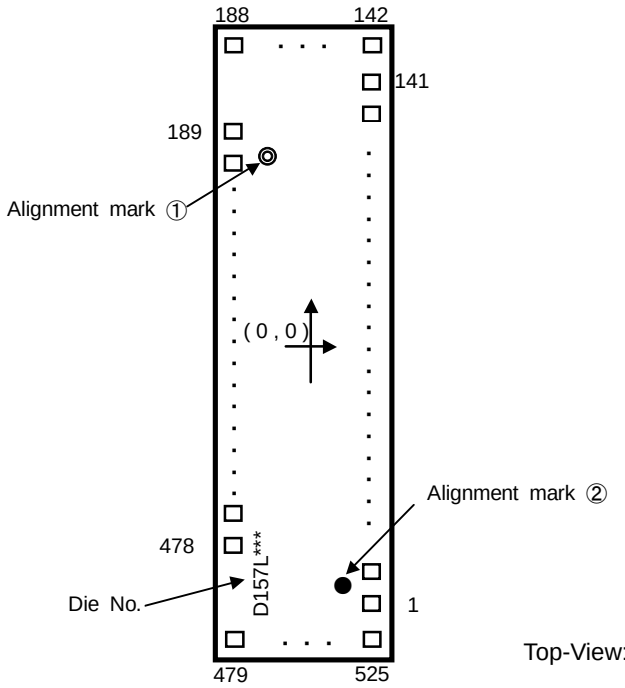
*1: Apply to $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, $\overline{RES}$, A0, D6(SCL), D7(SI) and CL pins.

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT

4.1 Chip Assignment



Top-View: from bump side

Die No.	Parts number
D157LD0B	S1D15721D00B000
D157LD1B	S1D15721D01B000

Item		Size X		Size Y	Unit
Chip size		2.66	×	18.95	mm
Chip thickness		0.625			mm
Bump pitch		50 (Min.)			μm
Bump size	PAD No.1 to 3, 6, 9, 20, 23, 38, 140, 141	84	×	36	μm
	PAD No.4, 5, 7, 8, 10 to 19, 21, 22, 24 to 37, 39 to 139	84	×	81	μm
	PAD No.142 to 188, 479 to 525	33	×	113	μm
	PAD No. 189 to 478	113	×	33	μm
Bump height		17 (Typ.)			μm

4.2 Alignment mark

Alignment coordinate

① (-645, 7013)

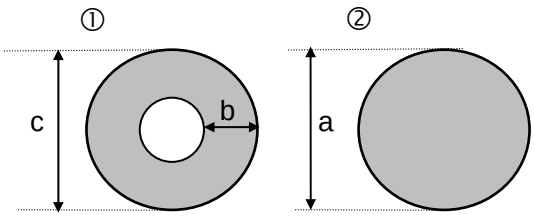
② (918, -8889)

Mark size

a = 80 μm

b = 30 μm

c = 71 μm



4.3 Pad Center Coordinates

Unit: μm

PAD No.	Pin Name	X	Y
1	NC	1174	-9077
2	NC		-9026
3	V_{DD}		-8921
4	TESTA		-8843
5	TESTB		-8614
6	V_{DI}		-8535
7	TEST1		-8402
8	TEST2		-8073
9	V_{DD}		-7994
10	VDIS		-7748
11	SYNC		-7641
12	FR		-7312
13	CL		-7206
14	$\overline{DOF}$		-6877
15	F1		-6771
16	F2		-6442
17	$\overline{CS}$		-6335
18	$\overline{RES}$		-6007
19	A0		-5900
20	V_{SS}		-5648
21	$\overline{WR}$,R/$\overline{W}$		-5569
22	$\overline{RD}$, E		-5240
23	V_{DD}		-5161
24	D0		-4914
25	D1		-4808
26	D2		-4479
27	D3		-4373
28	D4		-4044
29	D5		-3937
30	D6, SCL		-3609
31	D7, SI		-3502
32	V_{DI}		-3273
33	V_{DI}		-3166
34	V_{DI}		-3060
35	V_{DI}		-2953
36	V_{DI}		-2847
37	V_{DI}		-2740
38	V_{DD}		-2662
39	M/S		-2529
40	CLS		-2200
41	V_{SS}		-2094
42	V_{SS}		-1987
43	V_{SS}		-1881
44	V_{SS}		-1774
45	V_{SS}		-1668
46	V_{SS}		-1561
47	TEST3		-1455
48	C86		-1126
49	P/S		-1019
50	V_{DD}	↓	-790

PAD No.	Pin Name	X	Y
51	V_{DD}	1174	-684
52	V_{DD}		-577
53	V_{DD}		-471
54	V_{DD}		-364
55	V_{DD}		-258
56	V_{DD}		-151
57	V_{DD}		-45
58	V_{DD}		62
59	V_{DD2}		428
60	V_{DD2}		534
61	V_{DD2}		641
62	V_{DD2}		747
63	V_{DD2}		854
64	V_{DD2}		960
65	V_{DD2}		1067
66	V_{DD2}		1173
67	V_{OUT}		1280
68	V_{OUT}		1386
69	V_{OUT}		1493
70	V_{OUT}		1599
71	V_{OUT}		1706
72	V_{OUT}		1812
73	CAP1+		1919
74	CAP1+		2025
75	CAP1+		2132
76	CAP1+		2238
77	CAP1+		2345
78	CAP1+		2451
79	CAP1-		2558
80	CAP1-		2664
81	CAP1-		2771
82	CAP1-		2877
83	CAP1-		2984
84	CAP1-		3090
85	CAP3+		3197
86	CAP3+		3303
87	CAP3+		3410
88	CAP3+		3516
89	CAP3+		3623
90	CAP3+		3729
91	V_{OUT}		3836
92	CAP4+		3942
93	CAP4+		4049
94	CAP4+		4155
95	CAP4+		4262
96	CAP4+		4368
97	CAP4+		4475
98	CAP2-		4581
99	CAP2-		4688
100	CAP2-	↓	4794

PAD No.	Pin Name	X	Y
101	CAP2-	1174	4901
102	CAP2-		5007
103	CAP2-		5114
104	CAP2+		5220
105	CAP2+		5327
106	CAP2+		5433
107	CAP2+		5540
108	CAP2+		5646
109	CAP2+		5753
110	V_3		5859
111	V_3		5966
112	V_3		6072
113	V_3		6179
114	V_2		6285
115	V_2		6392
116	V_2		6498
117	V_2		6605
118	V_1		6711
119	V_1		6818
120	V_1		6924
121	V_1		7031
122	V_C		7137
123	V_C		7244
124	V_C		7350
125	V_C		7457
126	MV_1		7563
127	MV_1		7670
128	MV_1		7776
129	MV_1		7883
130	MV_2		7989
131	MV_2		8096
132	MV_2		8202
133	MV_2		8309
134	V_{SS}		8415
135	V_{SS}		8522
136	V_{SS}		8628
137	V_{SS}		8735
138	SVD2		8841
139	SV22		8948
140	NC		9026
141	NC	↓	9077
142	NC	1149	9309
143	NC	1099	
144	NC	1049	
145	COM39	999	
146	COM38	949	
147	COM37	899	
148	COM36	849	
149	COM35	799	
150	COM34	749	↓

4. PIN ASSIGNMENT

Unit: μm

PAD No.	Pin Name	X	Y
151	COM33	699	9309
152	COM32	649	
153	COM31	599	
154	COM30	549	
155	COM29	500	
156	COM28	450	
157	COM27	400	
158	COM26	350	
159	COM25	300	
160	COM24	250	
161	COM23	200	
162	COM22	150	
163	COM21	100	
164	COM20	50	
165	COM19	0	
166	COM18	-50	
167	COM17	-100	
168	COM16	-150	
169	COM15	-200	
170	COM14	-250	
171	COM13	-300	
172	COM12	-350	
173	COM11	-400	
174	COM10	-450	
175	COM9	-500	
176	COM8	-549	
177	COM7	-599	
178	COM6	-649	
179	COM5	-699	
180	COM4	-749	
181	COM3	-799	
182	COM2	-849	
183	COM1	-899	
184	COM0	-949	
185	COMS	-999	
186	NC	-1049	
187	NC	-1099	
188	NC	-1149	↓
189	NC	-1163	7218
190	NC		7168
191	NC		7118
192	NC		7068
193	NC		7018
194	NC		6968
195	NC		6918
196	NC		6868
197	NC		6818
198	NC		6768
199	NC		6718
200	NC	↓	6668

PAD No.	Pin Name	X	Y
201	NC	-1163	6618
202	NC		6568
203	NC		6518
204	NC		6469
205	NC		6419
206	SEG0		6369
207	SEG1		6319
208	SEG2		6269
209	SEG3		6219
210	SEG4		6169
211	SEG5		6119
212	SEG6		6069
213	SEG7		6019
214	SEG8		5969
215	SEG9		5919
216	SEG10		5869
217	SEG11		5819
218	SEG12		5769
219	SEG13		5719
220	SEG14		5669
221	SEG15		5619
222	SEG16		5569
223	SEG17		5519
224	SEG18		5470
225	SEG19		5420
226	SEG20		5370
227	SEG21		5320
228	SEG22		5270
229	SEG23		5220
230	SEG24		5170
231	SEG25		5120
232	SEG26		5070
233	SEG27		5020
234	SEG28		4970
235	SEG29		4920
236	SEG30		4870
237	SEG31		4820
238	SEG32		4770
239	SEG33		4720
240	SEG34		4670
241	SEG35		4620
242	SEG36		4570
243	SEG37		4520
244	SEG38		4471
245	SEG39		4421
246	SEG40		4371
247	SEG41		4321
248	SEG42		4271
249	SEG43		4221
250	SEG44	↓	4171

PAD No.	Pin Name	X	Y
251	SEG45	-1163	4121
252	SEG46		4071
253	SEG47		4021
254	SEG48		3971
255	SEG49		3921
256	SEG50		3871
257	SEG51		3821
258	SEG52		3771
259	SEG53		3721
260	SEG54		3671
261	SEG55		3621
262	SEG56		3571
263	SEG57		3521
264	SEG58		3472
265	SEG59		3422
266	SEG60		3372
267	SEG61		3322
268	SEG62		3272
269	SEG63		3222
270	SEG64		3172
271	SEG65		3122
272	SEG66		3072
273	SEG67		3022
274	SEG68		2972
275	SEG69		2922
276	SEG70		2872
277	SEG71		2822
278	SEG72		2772
279	SEG73		2722
280	SEG74		2672
281	SEG75		2622
282	SEG76		2572
283	SEG77		2522
284	SEG78		2473
285	SEG79		2423
286	SEG80		2373
287	SEG81		2323
288	SEG82		2273
289	SEG83		2223
290	SEG84		2173
291	SEG85		2123
292	SEG86		2073
293	SEG87		2023
294	SEG88		1973
295	SEG89		1923
296	SEG90		1873
297	SEG91		1823
298	SEG92		1773
299	SEG93		1723
300	SEG94	↓	1673

Unit: μm

PAD No.	Pin Name	X	Y
301	SEG95	-1163	1623
302	SEG96		1573
303	SEG97		1523
304	SEG98		1474
305	SEG99		1424
306	SEG100		1374
307	SEG101		1324
308	SEG102		1274
309	SEG103		1224
310	SEG104		1174
311	SEG105		1124
312	SEG106		1074
313	SEG107		1024
314	SEG108		974
315	SEG109		924
316	SEG110		874
317	SEG111		824
318	SEG112		774
319	SEG113		724
320	SEG114		674
321	SEG115		624
322	SEG116		574
323	SEG117		524
324	SEG118		475
325	SEG119		425
326	SEG120		375
327	SEG121		325
328	SEG122		275
329	SEG123		225
330	SEG124		175
331	SEG125		125
332	SEG126		75
333	SEG127		25
334	SEG128		-25
335	SEG129		-75
336	SEG130		-125
337	SEG131		-175
338	SEG132		-225
339	SEG133		-275
340	SEG134		-325
341	SEG135		-375
342	SEG136		-425
343	SEG137		-475
344	SEG138		-524
345	SEG139		-574
346	SEG140		-624
347	SEG141		-674
348	SEG142		-724
349	SEG143		-774
350	SEG144		-824

PAD No.	Pin Name	X	Y
351	SEG145	-1163	-874
352	SEG146		-924
353	SEG147		-974
354	SEG148		-1024
355	SEG149		-1074
356	SEG150		-1124
357	SEG151		-1174
358	SEG152		-1224
359	SEG153		-1274
360	SEG154		-1324
361	SEG155		-1374
362	SEG156		-1424
363	SEG157		-1474
364	SEG158		-1523
365	SEG159		-1573
366	SEG160		-1623
367	SEG161		-1673
368	SEG162		-1723
369	SEG163		-1773
370	SEG164		-1823
371	SEG165		-1873
372	SEG166		-1923
373	SEG167		-1973
374	SEG168		-2023
375	SEG169		-2073
376	SEG170		-2123
377	SEG171		-2173
378	SEG172		-2223
379	SEG173		-2273
380	SEG174		-2323
381	SEG175		-2373
382	SEG176		-2423
383	SEG177		-2473
384	SEG178		-2522
385	SEG179		-2572
386	SEG180		-2622
387	SEG181		-2672
388	SEG182		-2722
389	SEG183		-2772
390	SEG184		-2822
391	SEG185		-2872
392	SEG186		-2922
393	SEG187		-2972
394	SEG188		-3022
395	SEG189		-3072
396	SEG190		-3122
397	SEG191		-3172
398	SEG192		-3222
399	SEG193		-3272
400	SEG194		-3322

PAD No.	Pin Name	X	Y
401	SEG195	-1163	-3372
402	SEG196		-3422
403	SEG197		-3472
404	SEG198		-3521
405	SEG199		-3571
406	SEG200		-3621
407	SEG201		-3671
408	SEG202		-3721
409	SEG203		-3771
410	SEG204		-3821
411	SEG205		-3871
412	SEG206		-3921
413	SEG207		-3971
414	SEG208		-4021
415	SEG209		-4071
416	SEG210		-4121
417	SEG211		-4171
418	SEG212		-4221
419	SEG213		-4271
420	SEG214		-4321
421	SEG215		-4371
422	SEG216		-4421
423	SEG217		-4471
424	SEG218		-4520
425	SEG219		-4570
426	SEG220		-4620
427	SEG221		-4670
428	SEG222		-4720
429	SEG223		-4770
430	SEG224		-4820
431	SEG225		-4870
432	SEG226		-4920
433	SEG227		-4970
434	SEG228		-5020
435	SEG229		-5070
436	SEG230		-5120
437	SEG231		-5170
438	SEG232		-5220
439	SEG233		-5270
440	SEG234		-5320
441	SEG235		-5370
442	SEG236		-5420
443	SEG237		-5470
444	SEG238		-5519
445	SEG239		-5569
446	SEG240		-5619
447	SEG241		-5669
448	SEG242		-5719
449	SEG243		-5769
450	SEG244		-5819

Unit: μm

PAD No.	Pin Name	X	Y
451	SEG245	-1163	-5869
452	SEG246		-5919
453	SEG247		-5969
454	SEG248		-6019
455	SEG249		-6069
456	SEG250		-6119
457	SEG251		-6169
458	SEG252		-6219
459	SEG253		-6269
460	SEG254		-6319
461	SEG255		-6369
462	NC		-6419
463	NC		-6469
464	NC		-6518
465	NC		-6568
466	NC		-6618
467	NC		-6668
468	NC		-6718
469	NC		-6768
470	NC		-6818
471	NC		-6868
472	NC		-6918
473	NC		-6968
474	NC		-7018
475	NC		-7068
476	NC		-7118
477	NC		-7168
478	NC		-7218
479	NC	-1149	-9309
480	NC	-1099	
481	NC	-1049	
482	COM40	-999	
483	COM41	-949	
484	COM42	-899	
485	COM43	-849	
486	COM44	-799	
487	COM45	-749	
488	COM46	-699	
489	COM47	-649	
490	COM48	-599	
491	COM49	-549	
492	COM50	-500	
493	COM51	-450	
494	COM52	-400	
495	COM53	-350	
496	COM54	-300	
497	COM55	-250	
498	COM56	-200	
499	COM57	-150	
500	COM58	-100	

PAD No.	Pin Name	X	Y
501	COM59	-50	-9309
502	COM60	0	
503	COM61	50	
504	COM62	100	
505	COM63	150	
506	COM64	200	
507	COM65	250	
508	COM66	300	
509	COM67	350	
510	COM68	400	
511	COM69	450	
512	COM70	500	
513	COM71	549	
514	COM72	599	
515	COM73	649	
516	COM74	699	
517	COM75	749	
518	COM76	799	
519	COM77	849	
520	COM78	899	
521	COM79	949	
522	COMS	999	
523	NC	1049	
524	NC	1099	
525	NC	1149	

5. PIN DESCRIPTION

5.1 Power Pin

Pin name	I/O	Description	Number of pins
V_{DD}	Power supply	Connect to system MPU power supply pin V_{CC}.	13
V_{SS}	Power supply	Connect to the system GND.	11
V_{DD2}	Power supply	Boosting power supply pin. When using the built-in boosting circuit, supply the supply voltage, which becomes a boosting source, to this pin. When not using the built-in boosting circuit, make $V_{DD2} = V_{DD}$ (or short-circuit V_{DD2} to the V_{DD} pin).	8
V_{DI}	Power supply	Power supply pin for internal logic The relations of $V_{DD} \geq V_{DI}$ and $3.3V \geq V_{DI} \geq 2.7V$ should be observed. Series S1D15721 has the built-in V_{DI} generating circuit. In view of the potential relations between V_{DD} and V_{DI}, make them valid or invalid with the V_{DIS} pin. 1. When making the V_{DI} generating circuit valid (V_{DIS} = HIGH) with V_{DD}max.>3.3V, Supply power for the internal logic circuit from the internal V_{DI} generating circuit. Connect a capacitor between the V_{DI} pin and the V_{SS} pin. 2. When making the V_{DI} generating circuit invalid (V_{DIS} = LOW) with V_{DD}max.>3.3V, Input power for the internal logic circuit externally from the V_{DI} pin. Input power for the logic circuit externally in the ranges of $V_{DD} \geq V_{DI}$ and $3.3V \geq V_{DI} \geq 2.7V$. 3. In case of V_{DD}max$\leq$3.3V, Make V_{DIS} = LOW (invalid V_{DI} generating circuit) and short-circuit the V_{DI} pin to the V_{DD} pin ($V_{DI}=V_{DD}$). When using this IC in multi-chip (master and slave) configuration, keep the same V_{DI} voltage on each chip. When using the built-in V_{DI} generating circuit, set V_{DIS} = HIGH for the master chip and set V_{DIS} = LOW for master chip to provide V_{DI} voltage from the master chip to the slave chip. Another way is that both VDIs connect together with VDIS of both chips set to HIGH. It is recommended in case to be concerned power line swinging by big panel load, high wiring resistance, high speed MPU accessing etc.	7
V_{DIS}	I	This pin is for making the V_{DI} generating circuit valid or invalid. V_{DIS} = HIGH: The V_{DI} generating circuit is valid. V_{DIS} = LOW: The V_{DI} generating circuit is invalid. When the V_{DIS} pin is changed from LOW to HIGH for use, it should be initialized by the $\overline{RES}$ pin after changing it. The V_{DIS} pin only control operation of the V_{DI} generating circuit, and the circuit operates independent from the power save command.	1

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>V_3, V_2, V_1, V_C, MV_1, MV_2</td><td>Power supply</td><td>A liquid crystal drive multi-level power supply. The voltages determined by the liquid crystal cell are impedance-converted by resistive divider and operational amplifier for application.
The following order must be maintained:
$V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq V_{SS}$
MV_3 is short circuited with V_{SS} inside the IC chip.
Master operation: When power supply is turned on, the following voltage is applied to each pin by the built-in power supply circuit.
<table>
<tr><td>V_2</td><td>6/8・V_3</td><td>16/20・V_3</td><td>14/16・V_3</td></tr>
<tr><td>V_1</td><td>5/8・V_3</td><td>13/20・V_3</td><td>11/16・V_3</td></tr>
<tr><td>V_C</td><td>4/8・V_3</td><td>10/20・V_3</td><td>8/16・V_3</td></tr>
<tr><td>MV_1</td><td>3/8・V_3</td><td>7/20・V_3</td><td>5/16・V_3</td></tr>
<tr><td>MV_2</td><td>2/8・V_3</td><td>4/20・V_3</td><td>2/16・V_3</td></tr>
</table>
</td><td>24</td></tr>
</table>

5.2 LCD Power Supply Current Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP1- pin.	6
CAP1-	O	Pin connected to the negative side of the step-up capacitor. Connect the capacitor between this pin and CAP1+ pin.	6
CAP2+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP2- pin.	6
CAP2-	O	Pin connected to the negative side of the step-up capacitor. Connect the capacitor between this pin and CAP2+ pin.	6
V_{OUT}	O	Output pin for step-up. Connect the capacitor between this pin and V_{DD2}.	7
CAP3+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP1- pin.	6
CAP4+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP2- pin.	6

5.3 System Bus Connection Pin

Pin name	I/O	Description	Number of pins
D7 to D0 (SI) (SCL)	I/O	Connects to the 8-bit or 16-bit MPU data bus via the 8-bit bi-directional data bus. When the serial interface is selected (P/S = LOW), D7 serves as the serial data input (SI) and D6 serves as the serial clock input (SCL), In this case, D0 through D5 go to a high impedance state. In case of inactive chip select, D0 to D7 turn into high impedance. In case of active chip select, fix the data bus to HIGH or LOW even in other operation than reading and writing and control it so that it does not turn into high impedance.	8
A0	I	Normally, the least significant bit MPU address bus is connected to distinguish between data and command. A0 = HIGH : indicates that D0 to D7 are display data or command parameters. A0 = LOW : indicates that D0 to D7 are control commands.	1

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>When the $\overline{RES}$ is LOW, in initialization is achieved.
Resetting operation is done on the level of the $\overline{RES}$ signal.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>A chip select signal. When $\overline{CS}$ = LOW, signals are active, and data/command input/output are enabled.
When $\overline{CS}$ = High, the data bus is caused to high impedance.</td><td>1</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When the 80 series MPU is connected. (active LOW)
A pin for connection of the $\overline{RD}$ signal of the 80 series MPU.
When this signal is LOW, the data bus of the S1D15721 Series is in the output state.
• When the 68 series MPU is connected. (active HIGH)
Serves as a 68 series MPU enable clock input pin.
Signals on the data bus are latched at the falling edge of Signal E.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When the 80 series MPU is connected. (active LOW)
A pin for connection of the $\overline{WR}$ signal of the 80 series MPU.
Signals on the data bus are latched at the leading edge of the $\overline{WR}$ signal.
• Serves as a read/write control signal input pin when the 68 series MPU is connected. (active HIGH)
R/$\overline{W}$ = HIGH : Read
R/$\overline{W}$ = LOW : Write</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>A MPU interface switching pin.
C86 = HIGH : 68 series MPU interface
C86 = LOW : 80 series MPU interface
In case of serial interface (P/S= LOW), fix C68 to LOW</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel data input/serial data input select pin
P/S = HIGH : Parallel data input
P/S = LOW : Serial data input
The following Table shows the summary:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = LOW, D0 to D5 high impedance.
D0 to D5 can be HIGH, LOW or open.
$\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) are locked to HIGH or LOW. Fix C86 to LOW.
The serial data input does not allow the RAM display data to be read.</td><td>1</td></tr>
<tr><td>CLS</td><td>I</td><td>A pin used to select Enable/Disable state of the built-in oscillator circuit for display clock.
CLS = HIGH : Built-in oscillator circuit Enabled
CLS = LOW : Built-in oscillator circuit Disabled (External input)
When CLS is LOW, display clock is input from the CL pin. When the S1D15721 Series is used in the master/slave mode, each CLS pins must be set to the same level.
<table>
<tr><th>Display clock</th><th>Master</th><th>Slave</th></tr>
<tr><td>Built-in oscillator circuit used</td><td>HIGH</td><td>HIGH</td></tr>
<tr><td>External input</td><td>LOW</td><td>LOW</td></tr>
</table></td><td>1</td></tr>
</table>

5. PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>M/S</td><td>I</td><td>A pin used to select the master/slave operation for S1D15721 Series.
Liquid crystal display system is synchronized when the master operation outputs the timing signal required for liquid crystal display, while the slave operation inputs the timing signal required for liquid crystal display.
M/S = HIGH : Master operation
M/S = LOW : Slave operation
The following Table shows the relation in conformance to the M/S and CLS :
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillation circuit</th><th>Power circuit</th><th>Temperature Sensor circuit</th><th>CL</th><th>FR, $\overline{\text{DOF}}$, F1, F2, SYNC</th></tr>
<tr><td rowspan="2">HIGH</td><td>HIGH</td><td>Enabled</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td></tr>
<tr><td>LOW</td><td>Disabled</td><td>Enabled</td><td>Enabled</td><td>Input</td><td>Output</td></tr>
<tr><td rowspan="2">LOW</td><td>HIGH</td><td>Disabled</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td></tr>
<tr><td>LOW</td><td>Disabled</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin.
The following Table shows the relation in conformance to the M/S and CLS state:
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td rowspan="2">HIGH</td><td>HIGH</td><td>Output</td></tr>
<tr><td>LOW</td><td>Input</td></tr>
<tr><td rowspan="2">LOW</td><td>HIGH</td><td>Input</td></tr>
<tr><td>LOW</td><td>Input</td></tr>
</table>When you want to use the S1D15721 Series in the master/slave mode, connect each CL pin. In case of using external clock, the external clock must be stopped at LOW when you stop it.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>A liquid crystal alternating current input/output pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15721 Series in the master/slave mode, connect each FR pin.</td><td>1</td></tr>
<tr><td>F1, F2, SYNC</td><td>I/O</td><td>A liquid crystal sync signal input/output pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15721 Series in the master/slave mode, connect each F1, F2 and SYNC pins.</td><td>Each 1</td></tr>
<tr><td>$\overline{\text{DOF}}$</td><td>I/O</td><td>A liquid crystal blanking control pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15721 Series in the master/slave mode, connect each $\overline{\text{DOF}}$ pin.</td><td>1</td></tr>
</table>

5.4 Liquid Crystal drive pin

Pin name	I/O	Description	Number of pins
SEG0 to SEG255	O	Liquid crystal segment drive output pins. One of the V_2, V_1, V_C, MV_1, and MV_2 levels is selected by a combination of the display RAM content and FR/F1/F2 signals.	256
COM0 to COM79	O	Liquid crystal common drive output pins. One of the V_3, V_C, V_{SS} levels is selected by a combination of the scan data and FR/F1/F2 signals.	80
COMS	O	COM output pins for icon line. These pins outputted the same signal. Set to OPEN not used. When COMS is used for the master/ slave configuration, the same signal is output to both the master and slave.	2

5.5 Temperature sensor pins

Pin name	I/O	Description	Number of pins
SVD2	O	Analog voltage output pin for temperature sensor.	1
SV22	O	Temperature sensor test pin. Set to OPEN.	1

5.6 Test pins

Pin name	I/O	Description	Number of pins
TEST 1,2	I	IC chip test pin. Fix the pin HIGH.	2
TEST 3	I	IC chip test pin. Fix these pins LOW.	1
TEST A	I	IC chip test pin. Fix the pin HIGH.	1
TEST B	I/O	Connect this to the V_{DI} pin.	1

6. FUNCTIONAL DESCRIPTION

6.1 MPU interface

6.1.1 Selection of Interface Type

S1D15721 Series allows data to be sent via the 8-bit bi-directional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin to HIGH or LOW, you can select either 8-bit parallel data input or serial data input, as shown in Table 6.1.

Table 6.1

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH : Parallel input	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW : Serial input	$\overline{CS}$	A0	—	—	LOW	SI	SCL	(HZ)

— : Fixed to HIGH or LOW HZ: High impedance state

6.1.2 Parallel Interface

When the parallel interface is selected (P/S = HIGH), direction connection to the MPU bus of either 80 series MPU or 68 series MPU is performed by setting the 86 pin to either HIGH or LOW, as shown in Table 6.2.

Table 6.2

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH : 68 series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7 to D0
LOW : 80 series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

The data bus signals are identified by a combination of A0, $\overline{RD}$ (E), and $\overline{WR}$ (R/$\overline{W}$) signals as shown in Table 6.3.

Table 6.3

Common	68 series	80 series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Display data read, status read
1	0	1	0	Display data write, command parameter
0	0	1	0	Command write

6.1.3 Serial Interface

When the serial interface is selected (P/S=LOW), the chip is active ($\overline{CS}$=LOW), and reception of serial data input (SI) and serial clock input (SCL) is enabled. Serial interface comprises a 8-bit shift register and 3-bit counter. The serial data are latched by the rising edge of serial clock signals in the order of D7, D6, …. and D0 starting from the serial data input pin. On the rising edge of 8th serial clock signal, they are converted into 8-bit parallel data to be processed. Whether serial data input is a display data or command is identified by A0 input. A0 = HIGH indicates display data or command parameter, while A0 = LOW shows command data. The A0 input is read and identified at every 8 × n-th rising edge of the serial clock after the chip has turned active.

Fig.6.1 shows the serial interface signal chart.

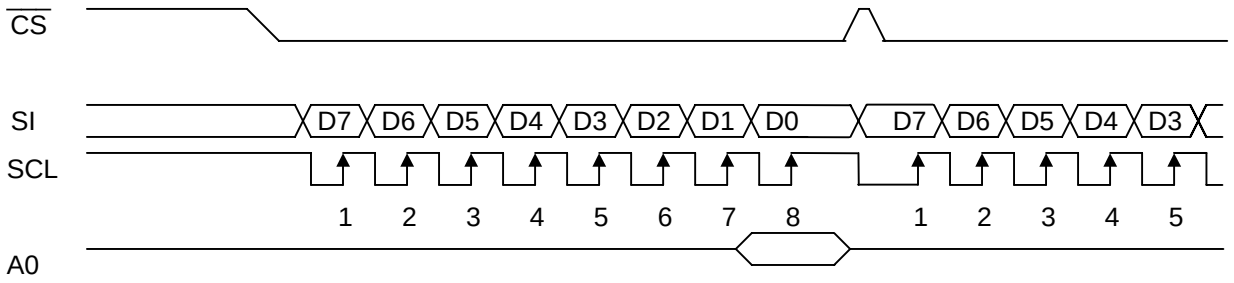


Fig.6.1

* It is recommended to set the $\overline{CS}$ pin to the HIGH level for every 8 bits of serial clocks to clear malfunction of the serial clock counter caused by external noise. When the chip is inactive, the counter is reset to the initial state.
* Reading is not performed in the case of serial interface.
* For the SCL signal, a sufficient care must be taken against terminal reflection of the wiring and external noise. Recommend to use an actual equipment to verify the operation.

6.1.4 Chip Selection

The S1D15721 Series has chip select pin. MPU interface or serial interface is enabled only when $\overline{CS}$ = LOW.

When the chip select pin is inactive, D0 to D5 are in the state of high impedance, while A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled. When serial interface is selected, the shift register and counter are reset.

6.1.5 Access to display data RAM and Internal register

Access to S1D15721 Series viewed from the MPU side is enabled only if the cycle time requirements are kept. This does not required waiting time; hence, high-speed data transfer is allowed.

Furthermore, at the time of data transfer with the MPU, S1D15721 Series provides a kind of inter-LSI pipe line processing via the bus holder accompanying the internal data bus.

For example, when data is written to the display data RAM by the MPU, the data is once held by the bus holder. It is written to the display data RAM before the next data write cycle comes.

On the other hand, when the MPU reads the content of the display data RAM, it is read in the first data read cycle (dummy), and the data is held in the bus holder. Then it is read onto on the system bus from the bus holder in the next data read cycle. Restrictions are imposed on the display data RAM read sequence. When the address has been set, specified address data is not output to the Read command immediately after that. The specified address data is output in the second data reading. This must be carefully noted. Therefore, one dummy read operation is mandatory subsequent to address setting or write cycle. Fig.6.2 illustrates this relationship.

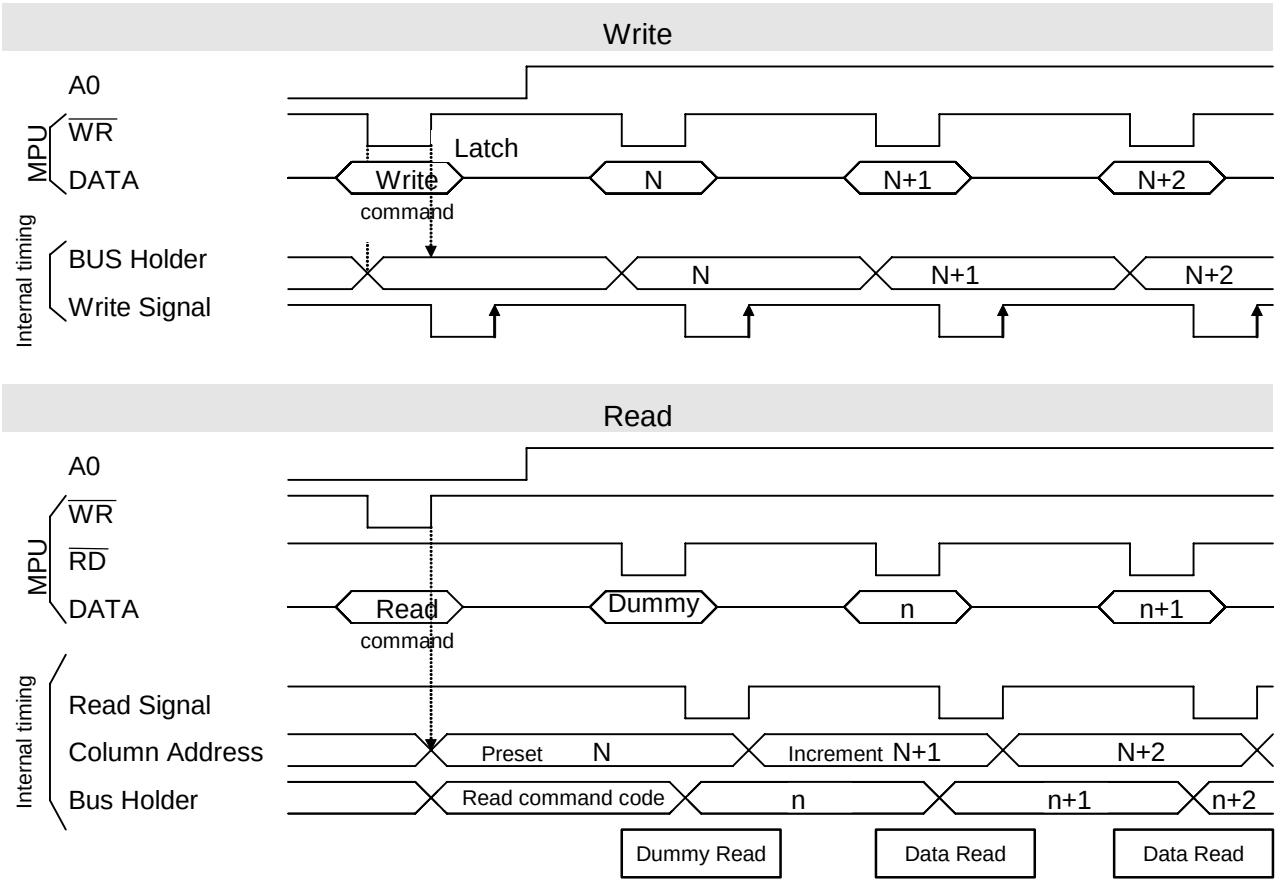


Fig.6.2

6.2 Display data RAM

6.2.1 Display data RAM

This is a RAM to store the display dot data, and comprises 81 × 256 × 2 bits. Access to the desired bit is enabled by specifying the page address and column address. When the 4 gray-scale is selected by the Display Mode Set command, display data input for gray-scale display are processed as a two-bit pair. Combination is as follows:

(MSB, LSB) = (D1, D0), (D3, D2), (DS, D4), (D7, D6)

When the RAM bit data is gray-scale 1 and 2, gray-scale display is realized according to the parameter of the Gray-scale Pattern Set command. (Normality and white are displayed.)

RAM bit data (high order and low order)

(1,1): gray-scale 3 Black (when display is in normal mode)
(1,0): gray-scale 2
(0,1): gray-scale 1
(0,0): gray-scale 0 White (when display is in normal mode)

When binary display is selected by the Display Mode Set command, the RAM 1 bit built in the one-dot pixel responds to it. When the RAM bit data is “1”, the display is black. If it is “0”, the display is given in white.

RAM bit data

“1”: Light On Black (when display is in normal mode)
“0”: Light Off White (when display is in normal mode)

Display data D7 to D0 from the MPU correspond to LCD common direction, as shown in Fig.6.3 and 6.4. Therefore, less restrictions when multi-chip usage.

Furthermore, read/write operations from the MPU to the RAM are carried out via the input/output buffer. The read operation from Display data RAM is designed as an independent operation. Accordingly, even if the MPU accesses the RAM asynchronously during LCD display, no adverse effect is given to display.

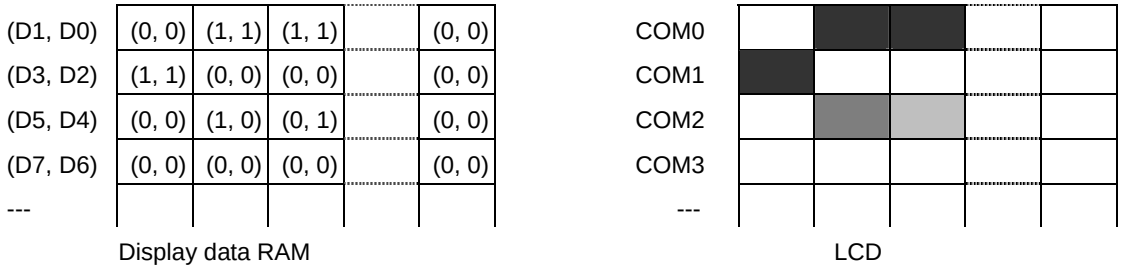


Fig.6.3 4 gray-scale

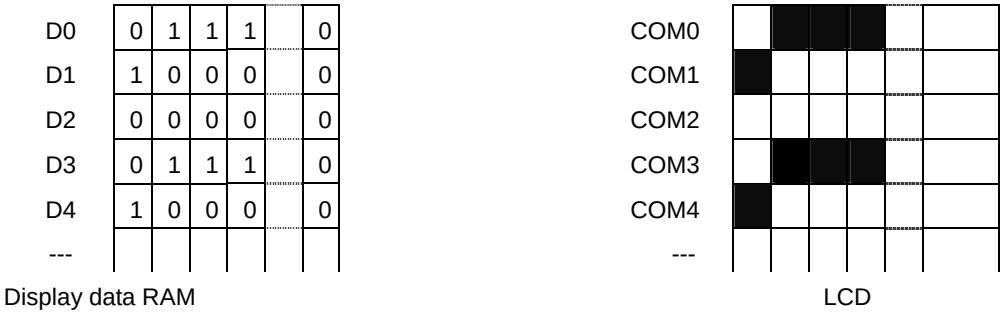


Fig.6.4 Binary

6.2.2 Gray-scale display

When the 4 gray-scale is selected by the Display Mode Set command, gray-scale is represented carried out according to the gray-scale data written in the display data RAM.

On the 4 gray-scale, 2 gray-scale of halftones (gray-scale 2 and 1) has its level of contrast specified by the Gray-scale Set command. Gray-scale can be Selected from 5 levels of contrast.

6.2.3 Page address circuit and column address circuit

The address of the display data RAM to be accessed is specified by the Page Address Set command and Column Address Set command, as shown in Fig.6.5 and Fig.6.6.

For address incremental direction, either the column direction or page direction can be selected by the Display Data Input Direction Select command. Whichever direction is chosen, increment is carried out by positive one (+1) after write or read operation.

When the column direction is selected for address increment, the column address is increased by +1 for every write or read operation. After the column address has accessed up to FFH, the page address is incremented by +1 and the column address shifts to 0H.

When the page direction is selected for address increment, the page address is increased with the column address locked in position. When the page address has accessed up to Page 20, the column address is incremented by +1, and the page address goes to Page 0.

Whichever direction is selected for address increment, the page address goes back to Page 0 and the column address to 0H after access up to the column address FFH of page address Page 20.

As shown in Fig.6.4, relationship between the display data RAM column address and segment output can be reversed by the Column Address Set Direction command. This will reduce restrictions on IC layout during LCD module assembling.

Page 20 is a RAM domain only for indicators, and when display data D0 - D1 chooses two values after four-gradation being chosen by the Display Mode Set command, only D0 of its display data is effective.

Table 6.4

SEG output		SEG0		SEG255
Column Address Set Direction	"0"	0(H)	Column Adress	→FF(H)
(D0)	"1"	FF(H)	Column Adress	←0(H)

6.2.4 Line address circuit

The line address circuit specifies the line address corresponding to COM output when the contents of the display data RAM is displayed, as shown in Fig.6.5 and 6.6. Normally, the top line of the display (COM0 output in the case of normal rotation of the common output status and COM79 output in the case of reverse rotation) is specified by the Display Start Line Address Set command. The display area starts from the specified display start line address to cover the area corresponding to the lines specified by the DUTY Set command in the direction where the line address increments. If the display start line set command is used for dynamic modification of the line address, screen scroll and page change are enabled.

6.2.5 Display data latch circuit

The display data larch circuit is a latch to temporarily latch the display data output from then display data RAM to the liquid crystal drive circuit. Display normal/reverse, display ON/OFF, and display all lighting ON/OFF commands control the data in this latch, without the data in the display data RAM being controlled.

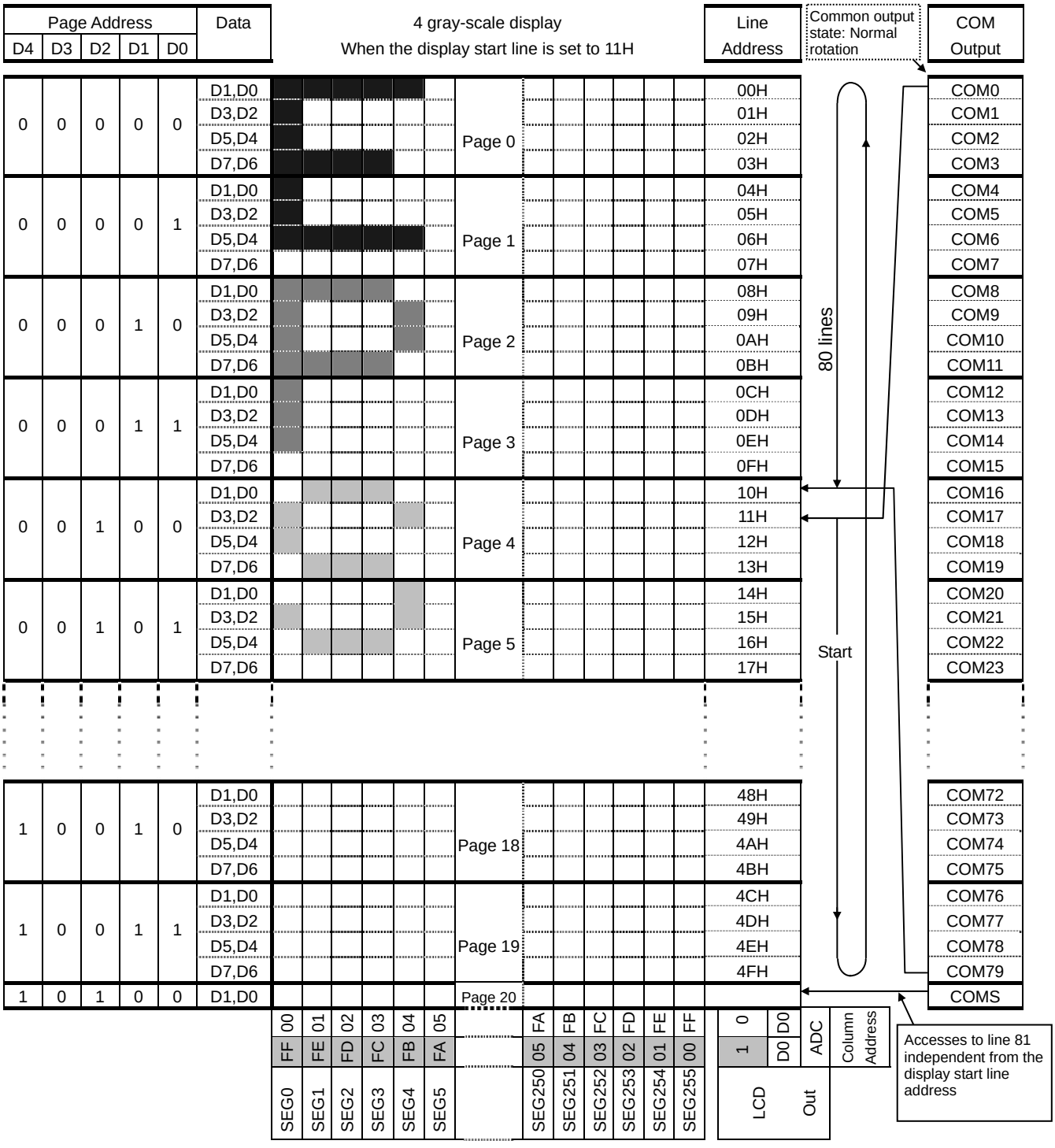


Fig.6.5 4 Gray-scale Display

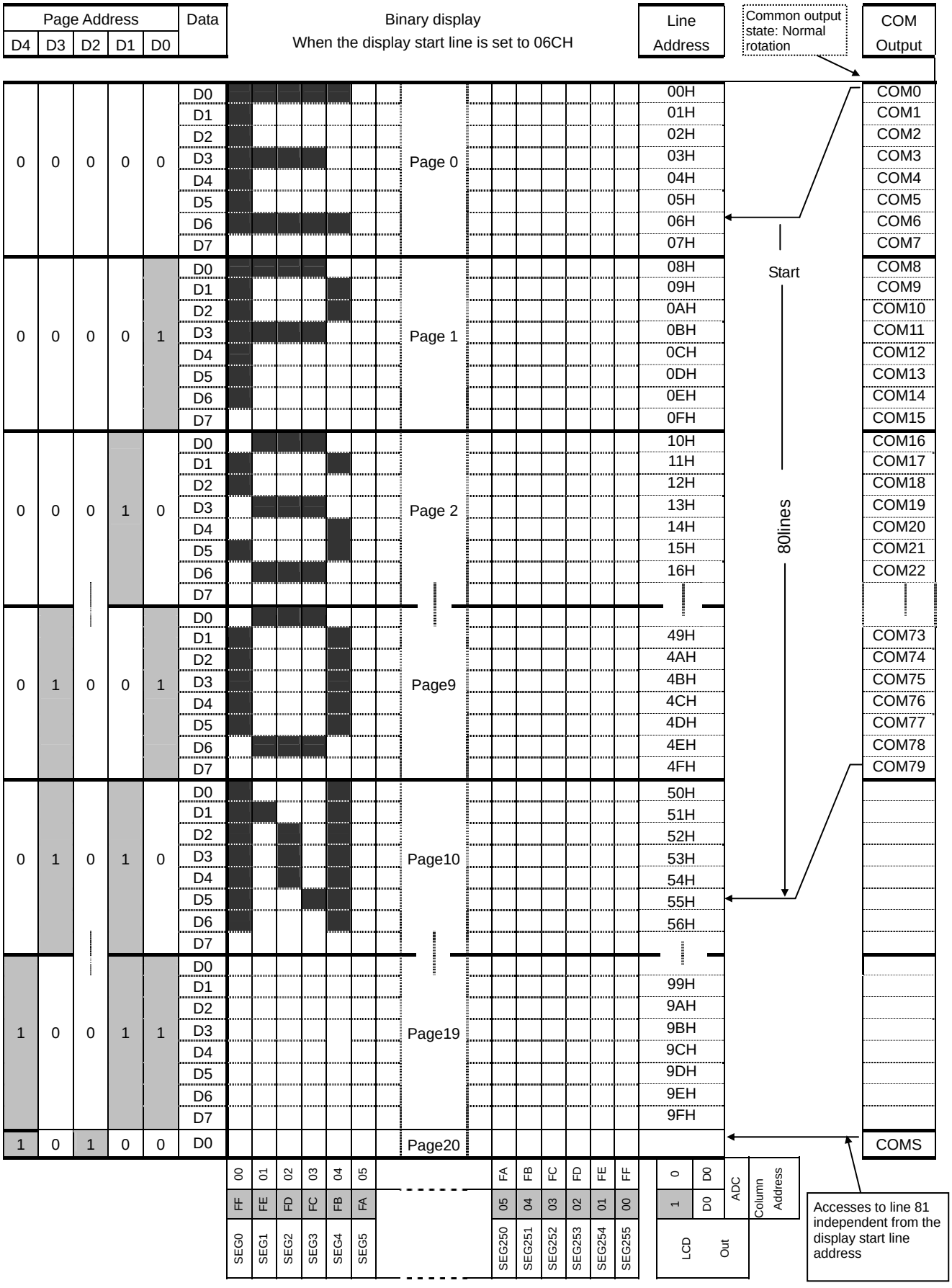


Fig.6.6 Binary display

6.3 Oscillator circuit

A display clock is generated by the CR oscillator. The oscillator circuit is enabled only when M/S = HIGH and CLS = HIGH. Oscillation starts after input of the built-in oscillator circuit ON command input.

When CLS = LOW, oscillation stops, and display clock is input from the CL pin.

In case of using external clock, the external clock must be stopped at LOW when you stop it.

6.4 Display timing generation circuit

Timing signals are generated from the display clock to the line address circuit and display data latch circuit. Synchronized with display clock, display data is latched in display data latch circuit, and is output to the segment drive output pin. Reading of the display data into the LCD drive circuit is completely independent of access from the MPU to the display data RAM. Accordingly, asynchronous access to the display data RAM during LCD display does not give any adverse effect; like as flicker.

Furthermore, the display clock generates internal common timing, liquid crystal alternating signal (FR), field start signal (SYNC) and drive pattern signal (F1 and F2).

The FR, after initialized by the RES pin, normally generates 2-frame alternating drive system drive waveform to the liquid crystal drive circuit. The n-line reverse alternating drive waveform is generated for each 4 × (a+1) line by setting data on the n-line reverse drive register. When there is a display quality problem including crosstalk, the problem may be solved using the n-line reverse alternating drive.

Execute liquid crystal display to determine the number of lines "n" for alternation.

When you want to use the S1D15721 Series in multi-chip configuration, supply display timing signal (FR, SYNC, F1, F2, CL, DOF) to the slave side from the master side. Table 6.5 shows the statuses or FR, SYNC, F1, F2, CL, DOF.

Table 6.5

Operating mode		CL	FR, SYNC, F1, F2, $\overline{DOF}$
Master (M/S = HIGH)	Built-in oscillator circuit enabled (CLS = HIGH)	Output	Output
	Built-in oscillator circuit disabled (CLS = LOW)	Input	Output
Slave (M/S = LOW)	Built-in oscillator circuit enabled (CLS = HIGH)	Input	Input
	Built-in oscillator circuit disabled (CLS = LOW)	Input	Input

6.5 Liquid crystal drive circuit

6.5.1 SEG Drivers

Select and output one level out of the five levels of V_2, V_1, V_C, MV_1 and MV_2.

6.5.2 COM Drivers

Select and output one level out of the three levels of V_3, V_C and V_{SS}.

For Series S1D15721, the COM output scanning direction can be set by the Select Common Output Status command. (See Table 6.6.) Therefore, IC arrangement comes to be less restricted when the LCD module is assembled.

Table 6.6

Status	COM scanning direction				
Normal	COM 0	→	COM 79	→	COMS
Reverse	COM 79	→	COM 0	→	COMS

6.5.3 COMS

This is the common output circuit for icon line. Select and output one level out of the three-value levels of V_3, V_C and V_{SS} according to the driver control signal decided by the decoder.

Common outputs are made not by the Set Display Duty command and the Select Display Start Line command immediately before a screen is changed.

For this IC, the 4-line simultaneous selection drive system (MLS) has been adopted, and the selection period equivalent to Display 4 lines is necessary even for COMS 1 Line.

6.5.4 Dummy Selection Period

Immediately after COMS has been selected, the selection period equivalent to Display 4 lines is provided as dummy. Therefore, the relationship between the number of display lines l (including COMS) set up by the set the number of display line command and display duty (1 selection period length of liquid crystal line sequential drive for frame cycle) is

$$duty = 1/(l + 3 + 4) = 1/(l + 7)$$

Some liquid crystal display patterns allow reduction of cross talk by changing the SEG output during dummy selection period using the the set thedisplay mode command

6.6 Power supply circuit

This is a power supply circuit to generate voltage required for liquid crystal drive, and is characterized by a low power consumption. It consists of a step-up circuit, V_3 voltage regulating circuit and liquid crystal drive voltage generating circuit, and is enabled only during master operation. During slave operation, following 3 control bits should be LOW. The power supply circuit uses the power control set command to provide an on/off control of step-up circuit, V_3 voltage regulating circuit and liquid crystal drive potential generating circuit. This allows a combined use of the external power supply and part of built-in power supply functions. Table 6.7 shows functions controlled by the 3-bit data of the control set command, and Table 6.8 shows reference combinations. Also, by use of the magnification of amplification changing over command, it is possible to select the amplifying magnification from five different steps. The power supply circuit is enabled only during master operation.

Enabled only in master operation.

Table 6.7 Control by 3-bit data of the control set command

Item		State	
		"1"	"0"
D2	Step-out circuit control bit	ON	OFF
D1	V_3 voltage regulator circuit (V_3 regulator circuit) control bit	ON	OFF
D0	LCD driving voltage generating circuit (LCDV circuit) control bit	ON	OFF

Table 6.8 Reference combination

Circuits used	D2	D1	D0	Step-up circuit	V_3 regulator circuit	LCDV circuit	Eternal input power supply
① Use of all built-in power supplies	1	1	1	Enable	Enable	Enable	—
② V_3 regulating circuit and LCDV circuit only	0	1	1	Disable	Enable	Enable	V_{OUT} *2
③ LCDV circuit only	0	0	1	Disable	Disable	Enable	V_3
④ External power supply only	0	0	0	Disable	Disable	Disable	V_3,V_2,V_1,V_C,MV_1, MV_2

*1 Any combinations other than the above are not available.

*2 In case of ②, the V_3 voltage is generated from V_{OUT}. Input the V_{OUT} voltage that allows you to secure stable V_3 voltage continuously.

6.6.1 Amplification circuit

By use of the amplification circuit being built into the S1D15721 Series, it is possible to make amplification of the electric potential between V_{DD2} - V_{SS} onto quintuple amplification, quadruple amplification, triple amplification or double amplification. Also, by use of the relevant command, it is possible to select either one from the quintuple amplification, quadruple amplification, triple amplification, double amplification and equal amplification.

① When using the quintuple-boosting, connect the capacitor C1 between CAP1+ ⇔ CAP1-, between CAP2+ ⇔ CAP2-, between CAP3 ⇔ CAP1-, between CAP4+ ⇔ CAP2- and between V_{DD2} ⇔ V_{OUT} before use.

② When using the quadruple-boosting, connect the capacitor C1 between CAP1+ ⇔ CAP1-, between CAP2+ ⇔ CAP2-, between CAP3+ ⇔ CAP1- and between V_{DD2} ⇔ V_{OUT} and short-circuit the CAP4+ pin and the V_{OUT} pin before use.

③ When using the triple-boosting, connect the capacitor C1 between CAP1+ ⇔ CAP1-, between CAP2+ ⇔ CAP2- and between V_{DD2} ⇔ V_{OUT} and short-circuit the CAP4+ pin, CAP3+ pin and the V_{OUT} pin before use.

④ When using the double-boosting, connect the capacitor C1 between CAP1+ ⇔ CAP1- and between V_{DD2} ⇔ V_{OUT}, open the CAP2- pin and short-circuit the CAP4+ pin, CAP3+ pin, CAP2+ pin and the V_{OUT} pin before use.

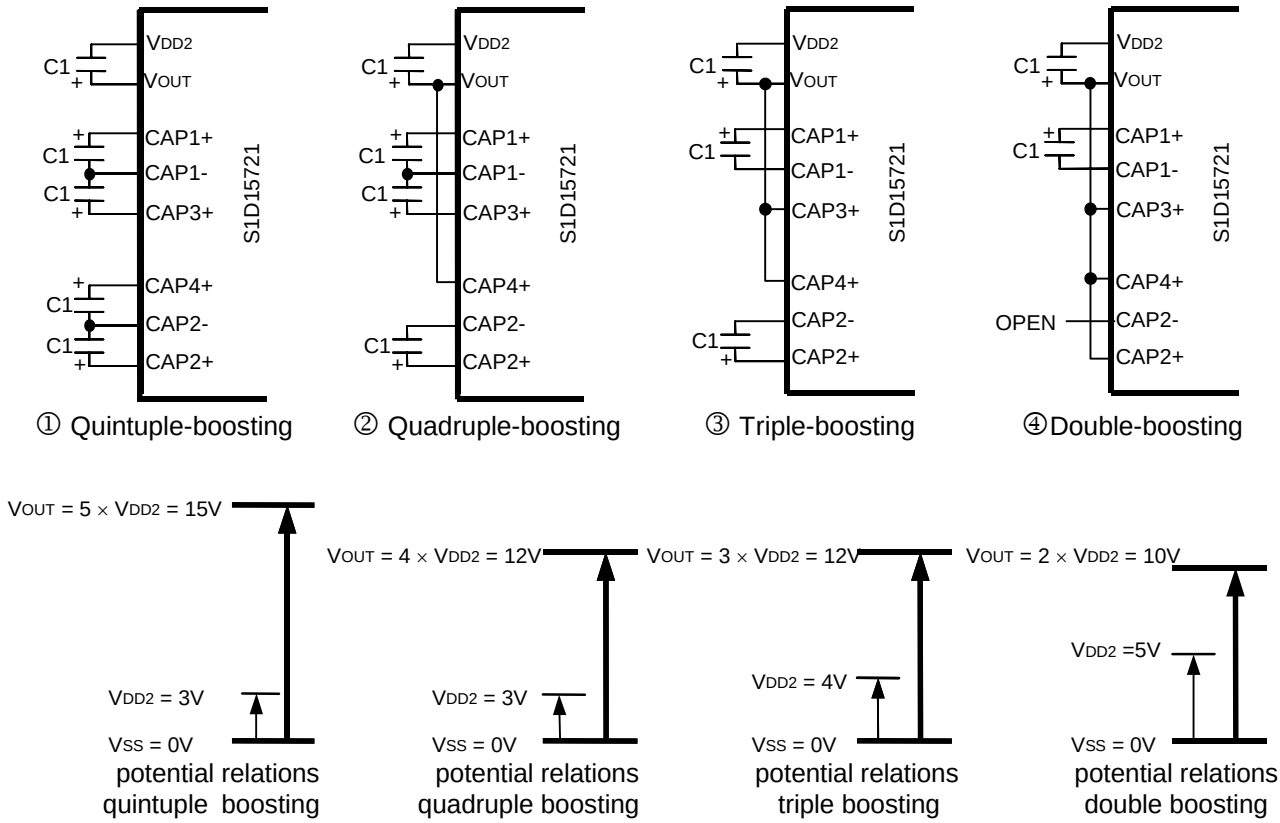


Fig.6.7

* Set the voltage range of the V_{DD2} so that the voltage of the V_{OUT} pin may not exceed the absolute maximum rating.

6.6.2 V_3 Voltage Regulating Circuit

V_{OUT} generated from the step-up circuit or V_{OUT} input from the outside produces liquid crystal drive voltage V_C via the voltage regulating circuit.

The S1D15721 series has high accuracy constant voltage source and allows adjustment of the V_3 voltage, using the 8-level V_3 adjust voltage command and 128-level electronic volume command. The liquid crystal drive voltage can be adjusted with high accuracy, using command only, without additional external parts. This makes it possible to provide a high precision liquid crystal drive voltage regulation only by the command without adding any external parts.

6.6.2.1 Electronic volume

Setting data in the 7-bit electronic volume register using the electronic volume command takes 1 state out of 128 states.

Table 6.9 shows the value of α by setting the data in the electronic volume register.

Table 6.9

D6	D5	D4	D3	D2	D1	D0	α	Voltage V_3
0	0	0	0	0	0	0	0	Small
0	0	0	0	0	0	1	1	↑
0	0	0	0	0	1	0	2	↑
				.			.	↑
				.			.	↑
				.			.	↑
1	1	1	1	1	0	1	125	↑
1	1	1	1	1	1	0	126	↑
1	1	1	1	1	1	1	127	Large

6.6.2.2 Adjust V_3 voltage

The 3-bit register of the V_3 adjust voltage command allows selection of the V_3 voltage range from eight states. Table 6.10 shows the V_3 voltage output range at 25°C. The V_3 voltage can be set in a wide range according to register value. Set it to more than 5.6V, the minimum operating voltage.

Table 6.10

D2	D1	D0	V_3 voltage output range
0	0	0	4.20V to 6.95V
0	0	1	4.71V to 7.81V
0	1	0	5.36V to 8.89V
0	1	1	6.03V to 10.00V
1	0	0	6.89V to 11.43V
1	0	1	7.72V to 12.80V
1	1	0	8.77V to 14.55V
1	1	1	9.65V to 16.00V

Since the V_3 voltage adjusting circuit has temperature characteristics, calculation of the V_3 voltage at a certain temperature requires correction for the voltage value at 25°C. Set temperature characteristics of the V_3 voltage, using the set temperature gradient command.

Example: When V_3 = 10.0[V] at 25°C, the amount of correction at 35°C with the temperature gradient set at 0.06%/°C is 10[V] × {35-25}[℃] × (-0.06[%/°C]/100[%])=-0.06[V].
Therefore, the calculated value of the V_3 voltage output at 35°C becomes 9.94[V].

The expression A.1 shows the V3 output voltage at 25°C using the register value of the V3 adjust voltage command and the setting α of the electronic volume register. Variations in manufacuture at 25°C is ± 3 %,

Formula A.1

Unit [V]

Adjust V3 voltage Register value			V3 output voltage
D2	D1	D0	
0	0	0	4.196+0.0217 × α
0	0	1	4.707+0.0244 × α
0	1	0	5.361+0.0278 × α
0	1	1	6.031+0.0313 × α
1	0	0	6.893+0.0357 × α
1	0	1	7.720+0.0400 × α
1	1	0	8.773+0.0455 × α
1	1	1	9.650+0.0500 × α

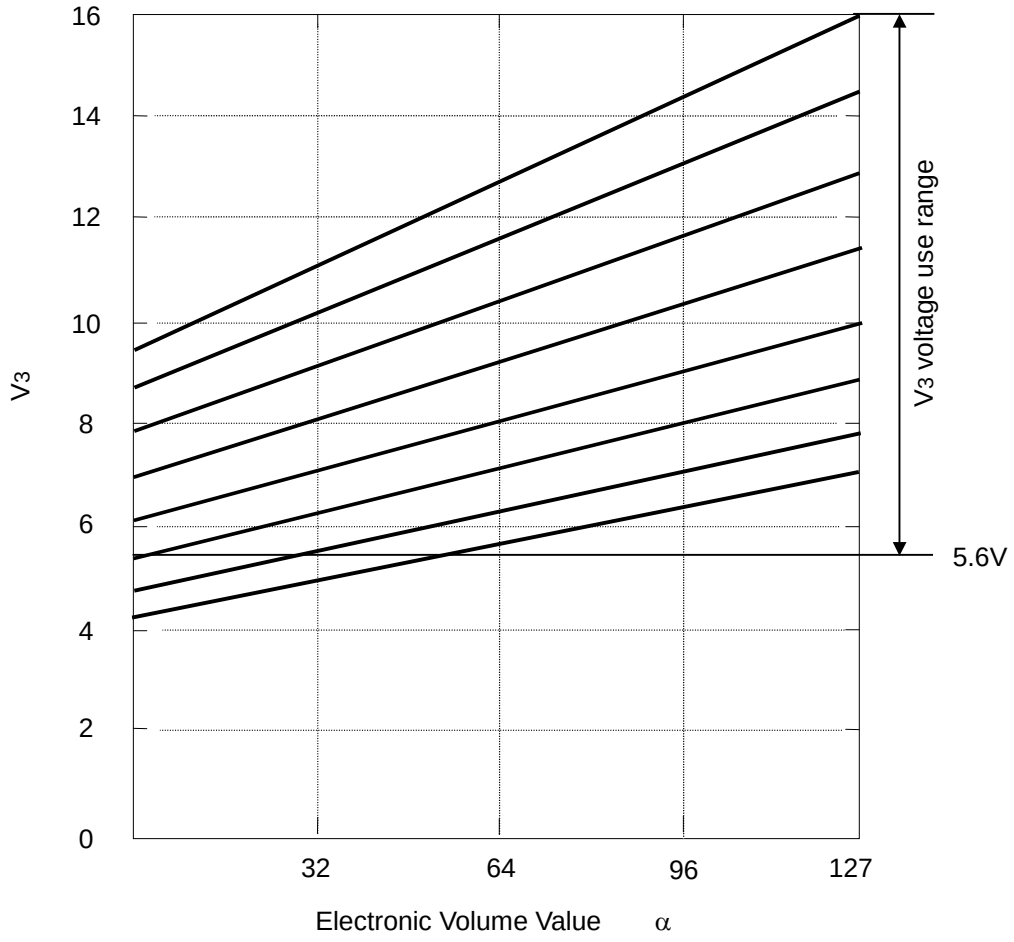


Fig.6.8

6.6.3 Liquid crystal drive voltage circuit

Voltages V_3 is converted by resistive divider to produce V_2, V_1, V_C, MV_1 and MV_2 voltages. V_2, V_1, V_C, MV_1 and MV_2 voltages are impedance - converted by the voltage follower, and is supplied to the liquid crystal drive circuit. A bias ratio is chosen by the bias set command.

Table 6.11 LCD bias set command register contents

	D1	D0	D1	D0	D1	D0
	0	0	0	1	1	0
V_2	6/8•V_3		16/20•V_3		14/16•V_3	
V_1	5/8•V_3		13/20•V_3		11/16•V_3	
V_C	4/8•V_3		10/20•V_3		8/16•V_3	
MV_1	3/8•V_3		7/20•V_3		5/16•V_3	
MV_2	2/8•V_3		4/20•V_3		2/16•V_3	

6.6.4 Temperature Gradient Selection Circuit

This circuit is used for selecting the temperature gradient characteristics of the liquid crystal drive supply voltage. The set temperature gradient command allows selection of temperature gradient characteristics from eight states. See Setting Temperature Gradient in 7.1 Command Description (27). Selecting temperature gradient characteristics matching temperature characteristics of the liquid crystal to be used enables you to configure the system without an external add-on device for correcting temperature characteristics.

6.6.5 Discharge

$\overline{RES}$ Setting LOW level for the pin input or inputting the discharge command discharges the capacitor connected externally. This command short-circuits each liquid crystal drive voltage to V_{SS} with switching elements of low impedance. Perform external circuit control to prevent external power supply to V_{OUT} and liquid crystal drive voltage during discharging by referring to 7.3 Setup Example of Instructions. The voltage of the power supply system shorted with V_{DD2} and V_{DD2} increases due to the charge flowing in from the capacitor for boosting. Design the external circuit not to permit these voltages to exceed the absolute maximum ratings, using 6.7 Example of Power Supply Circuit Peripheral Circuitry as reference.

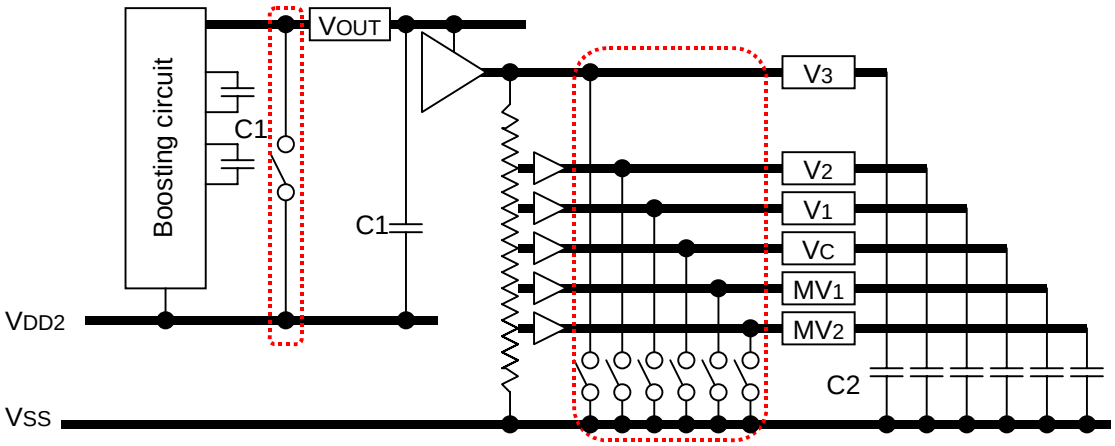
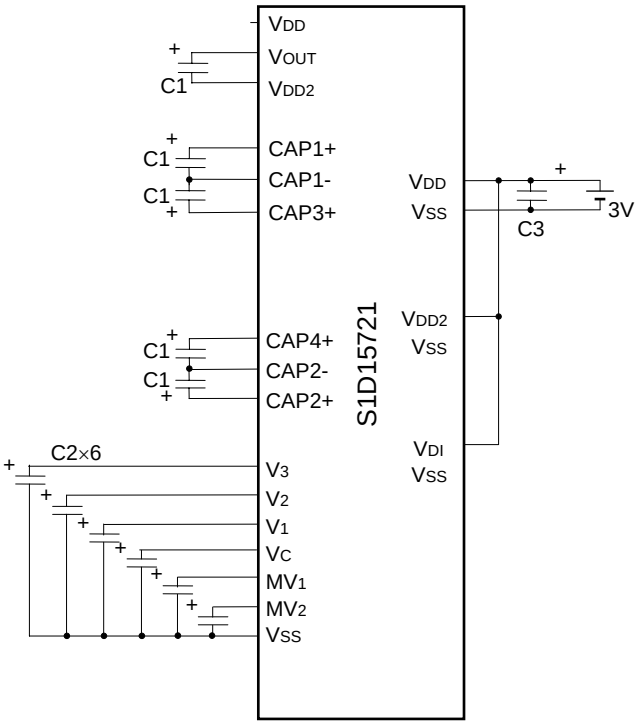


Fig.6.9 Location of Switching Elements for Discharge

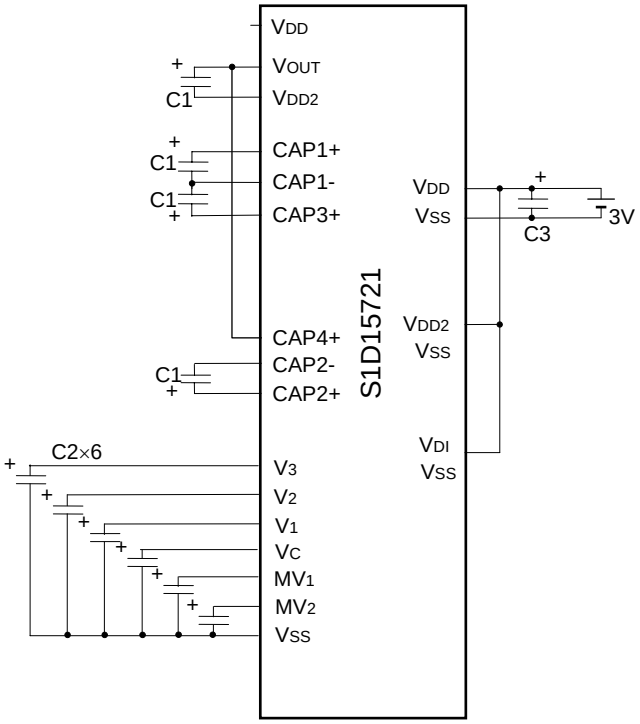
6.7 Examples of the peripheral circuits of the power circuit

① All the built-in power supplies are used

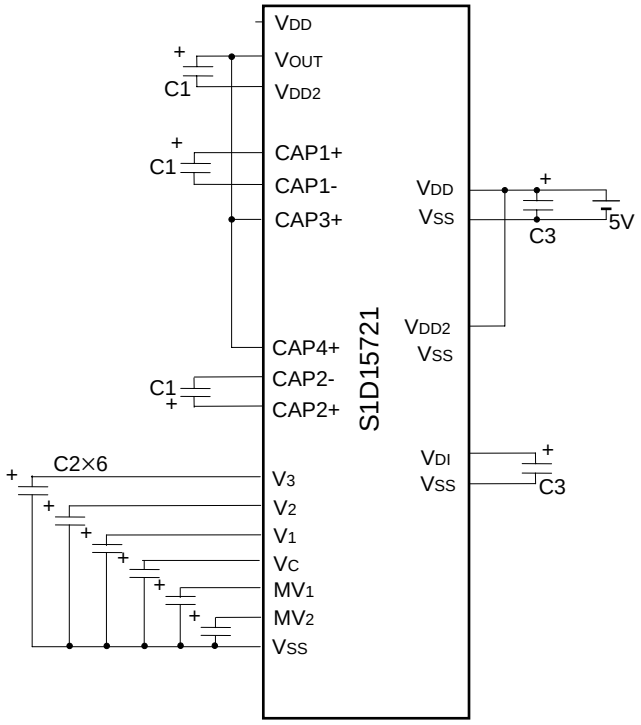
When using quintuple boosting
(external input of V_{DI})



When using quadruple boosting
(external input of V_{DI})



When using triple boosting
(internal generation of V_{DI})



When using double boosting
(internal generation of V_{DI})

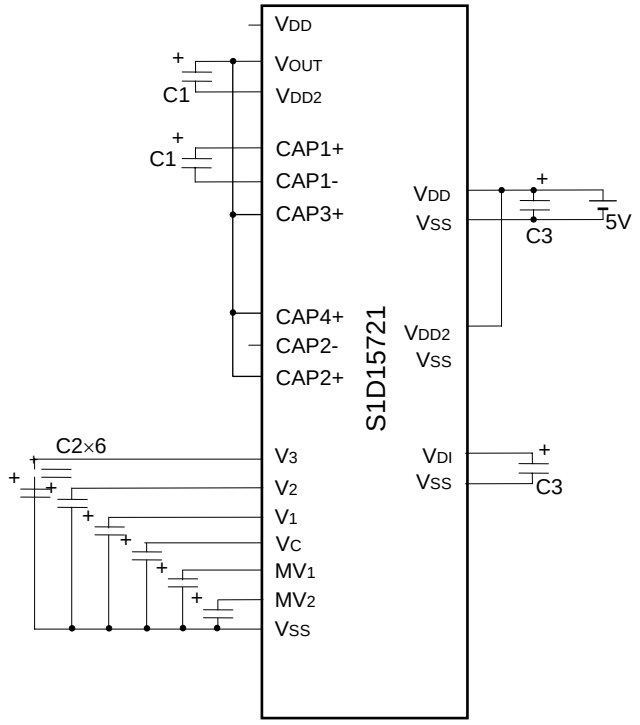
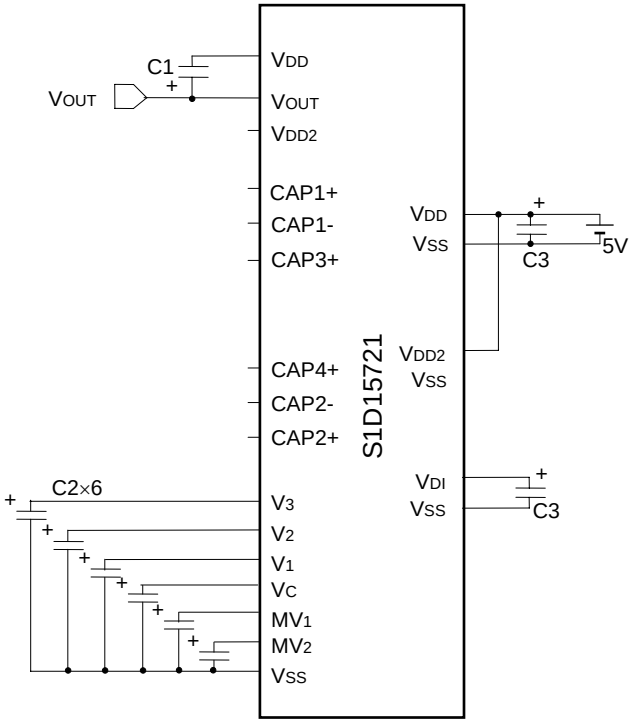
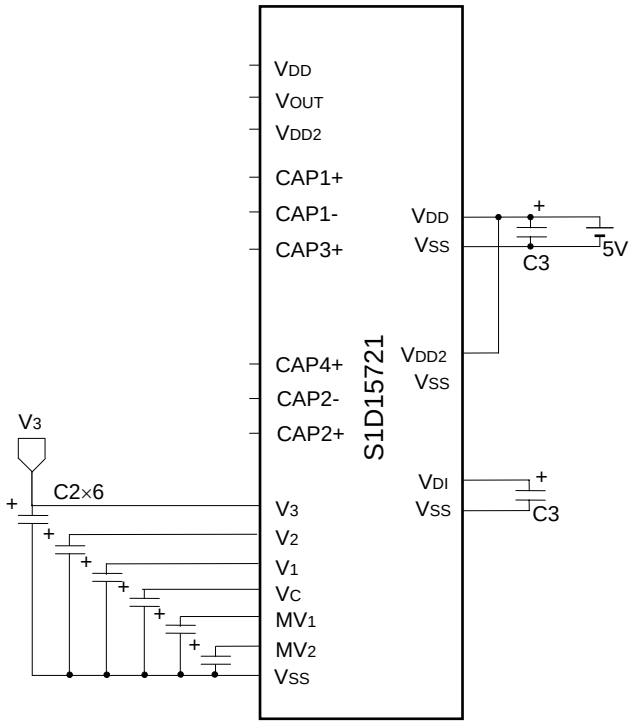


Fig.6.10

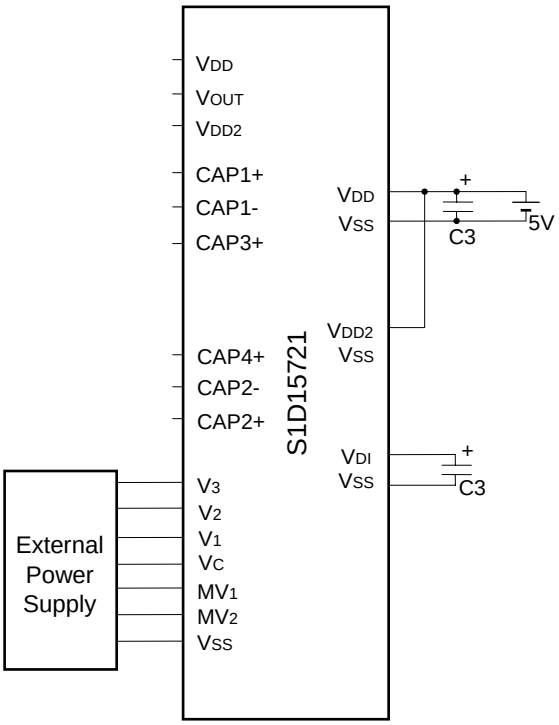
② V_3 adjusting circuit and LCDV circuit
V_{OUT} external input
(internal generation of V_{DI})



③ LCDV circuit only
V_3 external input
(internal generation of V_{DI})



④ External power supply only
External input (internal generation of V_{DI})



⑤ Connection example of smoothing capacitor for liquid crystal drive voltage
In addition to connections in ① - ③ above, the following connection is also possible.

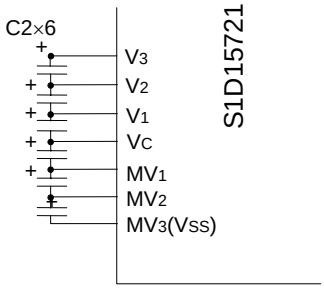


Fig.6.11

Table 6.12 Examples of common reference settings

Descriptions	Symbol	Reference setting value [μF]
Capacity for supply voltage regulation	C1	1.0 to 4.7
Capacity for step-up circuits	C2	1.0 to 4.7
Liquid crystal drive voltage retaining (smoothing) capacitor	C3	0.47 to 4.7

*1: The optimal values of C1 and C2 vary depending on the liquid crystal panel to be driven. Using the above values as reference, display the pattern of high load in the actual equipment and carefully evaluate it before determining it. (Non-polarity capacitance can be applicable.)

*2: If appropriate display quality is not obtained even after driving the built-in power supply circuit because the display panel is large, externally supply liquid crystal drive voltage without using the built-in power supply.

*3: Connection of the liquid crystal drive voltage stabilizing capacitor C2 can be made by the method shown in Fig.6.11 ⑤, however, the capacity value and the connection method may affect the display quality. Display the pattern of high load in the actual equipment and carefully evaluate it before determining it.

*4. While Discharge Command or $\overline{RES}$ is LOW, this IC discharges the charge on a capacitor connected to the outside of the IC to V_{DD2} in case of V_{OUT} or to V_{SS} in cases of V_3 to MV_2.

Fully examine that a charge flown in from the V_{OUT} system does not make the V_{DD2} potential exceed the maximum rating by all means,

Carefully evaluate not to allow the voltage of the power supply shorted with V_{DD2} and V_{DD2} due to the charge flowing in from the V_{OUT} power to exceed the absolute maximum rating and consider

- Connecting the zener diode between V_{DD2} and V_{SS} (Fig.6.12)
- Using the power supply circuit that can absor the charge flowing in
- Reducing the capacity value for the capacitor and decreasing quantity of charge.

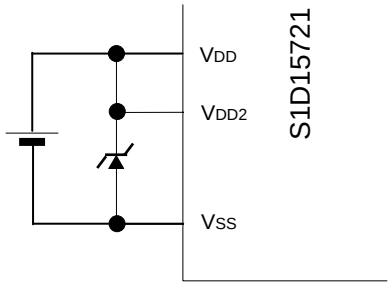


Fig.6.12 The example made into V_{DD}=V_{DD2}

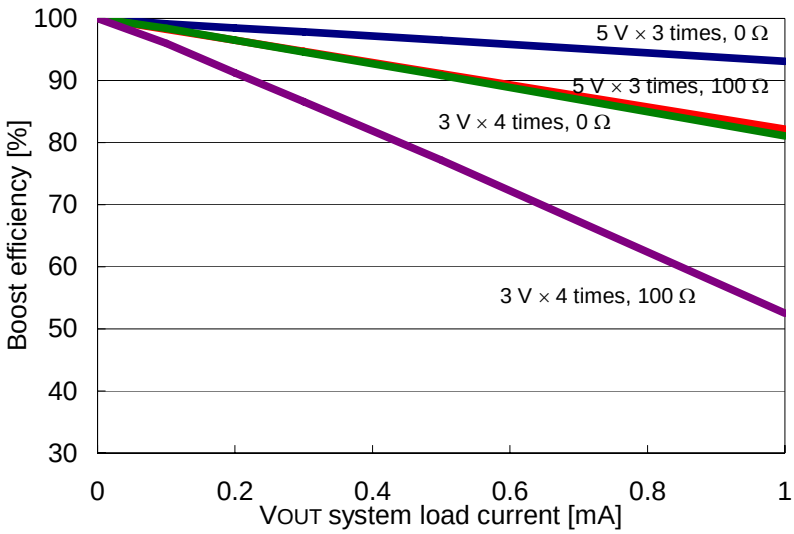
6.8 Precautions in Mounting COG

When mounting the COG, there is a resistance component generated between the IC chip and external connection devices (capacitor and resistor) due to ITO wiring. This effect may cause deterioration in the quality of the liquid crystal display, leading to malfunction of the IC chip. When designing the module, consider the following three points and carefully conduct evaluations under actual use conditions.

6.8.1 Wiring Resistance of Boosting Pin

The booster circuit of this IC chip performs switching with the transistor of extremely low ON resistance. In COG mounting, wiring resistance of ITO enters the switching transistor serially, which controls the boost ability. Carefully consider wiring to each boost capacitor by making the ITO wiring as thick as possible.

[Load Current Characteristics of Built-in Booster Circuit (Reference Value)]



Conditions
V_{DD}=V_{DD2}=5V, 3V
triple boosting, quadruple boosting
The capacitor for boosting 1 μF, V_{DD} and V_{SS} serially add 50 Ω to power supply.

Fig.6.13

Load current characteristics of built-in booster circuit when there is no resistance or resistance of 100 Ω between each CAP pin and capacitor.

When the current I_{OUT} is drawn from the V_{OUT} pin, changes of boost efficiency at I_{OUT} = 0 mA with the V_{OUT} voltage set to 100% are shown.

6.8.2 Wiring Resistance of Power Supply Pin

Power supply voltage may drop instantaneously in synchronization with the timing of generating instantaneous current as in the time when the display clock is switched. If the ITO wiring resistance of the power supply pin is high at this time, power supply voltage in the IC chip may vary greatly, leading to malfunction. To supply stable power to the IC, decrease the wiring impedance of the power line as low as possible.

6.8.3 Creation of Module Sample by Changing the Sheet Resistance

Evaluate the sample of which ITO power resistance has been changed and use the one with sufficient operation margin.

6.9 Temperature sensor circuit

The S1D15721 Series IC has the built-in temperature sensor circuit equipped with the pin to output the analog voltage, which represents the -4.70 mV/°C (Typ.) temperature gradient. The suitable tone LCD display is enabled in a wide temperature range by inputting the electronic control resistor value sent from the MPU for the temperature sensor output value to control the LCD drive voltage V_3. To perform master / slave operation, only master IC is enabled.

6.9.1 Analog Voltage Output

Inputting the temperature sensor ON command causes the analog voltage to be output from the SVD2 pin, which varies according to the temperature. To control liquid crystal drive voltage with higher accuracy, configure the system which can reduce variations in output voltage by allowing the MPU to give the feedback of values of the output voltage sampled under certain temperature and store them as reference voltage.

6.9.2 Precautions

(1) Noise influence

The temperature sensor circuit is operating depending on IC's logic operating voltage, i.e., SV22 voltage generated by the regulator operating in the V_{DI} power supply system. This circuit is composed so that it is not affected by regular fluctuations in the V_{DI} power supply system, but when a power noise occurs to the V_{DI} supply voltage in a high-speed logic operation like writing in the RAM, the SV22 voltage is also affected by the noise sometimes.

To detect temperatures accurately. stop accessing from the MPU and observe the operating conditions stipulated at the AC timing when receiving outputs from the temperature sensor.

(2) Influence of mounting

The output SVD2 from the temperature sensor circuit is stipulated as the output voltage value to the IC's substrate potential V_{SS}. When measuring the SVD2 potential in an actual system, you are requested to pay attention to the potential relations between the IC's substrate and the system GND.

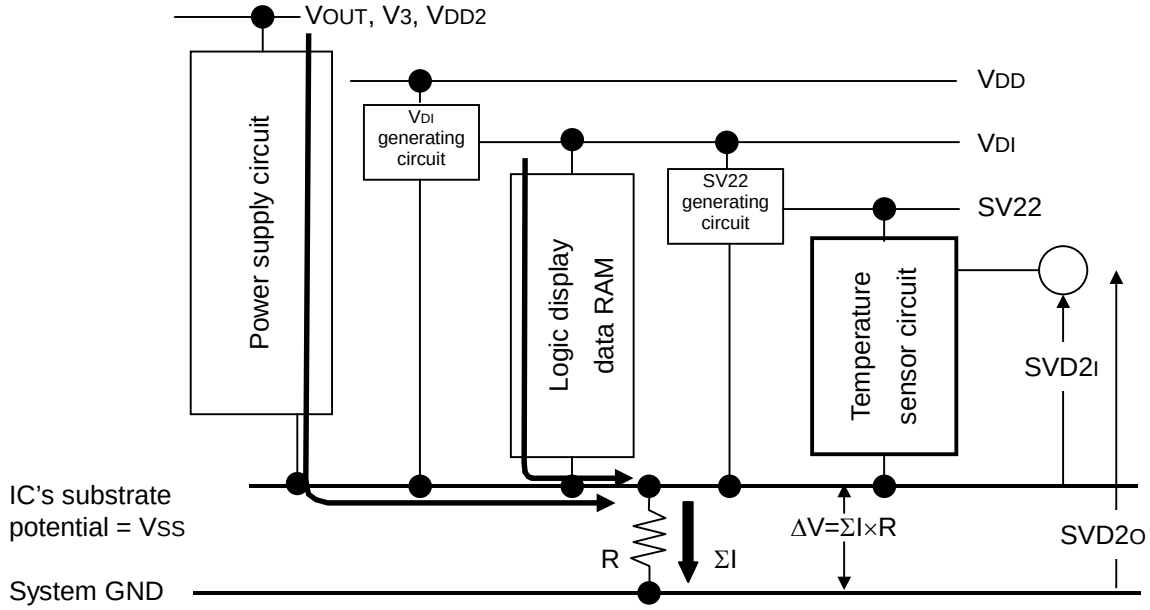


Fig.6.14 Influence of Resistance R between System GND and V_{SS}

When the resistance component R exists between the system GND and the IC's V_{SS} pin, the IC's substrate potential V_{SS} viewed from the system GND drops as follows:

$\Delta V = \Sigma I \times R$ (ΣI: The total current consumed by the IC.)

Therefore, the temperature sensor output viewed from the system GND (SVD2O in Fig.6.14) is affected by ΔV to the temperature sensor output viewed from the IC's VSS (SVD2I in Fig.6.14).

To eliminate the affect of ΔV as much as possible, you are requested to design and use the temperature sensor circuit taking the following three points into account:

- When mounting the COG, reduce resistances such as ITO resistance between the system GND and the IC's VSS pin as much as possible.
- Reduce influences of external circuits on the IC as much as possible by storing the SVD2 voltage measured when the system is operated under a certain temperature as the reference voltage.

6.10 Reset circuit

When the $\overline{RES}$ input becomes LOW, this LSI is set to the initialized state.
The following shows the initially set state:

1. Display : OFF
2. Display : normal mode
3. Display all lighting : OFF
4. Common output status : normal
5. Display start line: Set to 1st line
6. Page address: Set to 0 page
7. Column address: Set to 0 address
8. Display data input direction: Column direction
9. Column address direction : forward
10. n-line a.c. reverse drive: OFF (reverse drive for each frame)
11. n-line reverse drive register: (D4, D3, D2, D1, D0)=(0, 0, 0, 0, 0)
12. Display mode: 4 gray-scale display
13. Dummy select period display status: Display All lighting ON
14. Gray-scale pattern register: (D7, D6, D5, D4, D3, D2, D1, D0) = (*, 1, 0, 1, *, 0, 1, 0)
15. Display line number register: (D4, D3, D2, D1, D0) = (1, 0, 0, 1, 1) (display of 81 line)
16. Start spot (block) register: (D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0) (COM0)
17. Read modify write: OFF
18. Built-in oscillation circuit: stop
19. Oscillation frequency register: (D3, D2, D1, D0) = (0, 0, 0, 0)
20. Power control register: (D2, D1, D0) = (0, 0, 0)
21. LCD drive voltage selection register: (D2, D1, D0) = (0, 0, 0)
22. LCD bias set register: (D1, D0) = (0, 0)
23. Electronic volume register: (D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0)
24. Discharge: ON (only for when $\overline{RES}$ = LOW)
25. Power save: OFF
26. Temperature gradient register: (D2, D1, D0) = (0, 0, 0) (-0.06/°C)
27. Register data in the serial interface: Clear
28. Temperature sensor OFF.
29. MLS AC driving method select register: (D4, D3) = (0,1)

When power is turned on, initialization by the $\overline{RES}$ pin is necessary. After initialization by the $\overline{RES}$ pin, each input pin must be controlled correctly.

Furthermore, when control signals from the MPU have a high impedance, the excessive current may flow to the IC.

The S1D15721 series discharges V_{OUT} to V_{DD2} and liquid crystal drive voltage to V_{SS} at $\overline{RES}$ the pin = LOW level. When using the external power supply for liquid crystal drive, do not supply external power $\overline{RES}$ during pin = LOW to prevent external power supply from shorting with V_{DD2} and V_{SS}. At this time, in some power supply peripheral circuitry, the charge flowing in from the V_{OUT} power increases the power voltage shorted with the V_{DD2} and V_{DD2}. Using 6.6.5 Power Supply Peripheral Circuitry as reference, adopt the power supply peripheral circuitry that does not allow these power supplies to exceed the absolute maximum ratings.

7. COMMAND

The S1D15721 Series identifies data bus signals by a combination of A0, $\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$). Interpretation and execution of the command are executed by the internal timing alone which is independent of the external clock. This allows high-speed processing.

The 80 series MPU interface allows the command to be started by entering the low pulse in the $\overline{RD}$ pin during reading and by entering the low pulse in the $\overline{WR}$ pin during writing.

The 68 series MPU interface allows a read state to occur by entering HIGH in the R/$\overline{W}$ pin, and permits a write state to occur by entering LOW. It also allows the command to be started by entering the high pulse in the pin E. (For timing, see the description of "10. Timing characteristics").

Accordingly, the 68 series MPU interface is different from 80 series MPU interface in that $\overline{RD}$(E) is "1(H)" in the case of display data/read shown in the Command Description and Command Table. The following describes the commands, based on the example of the 80 series MPU interface:

When the serial interface is selected, enter data sequentially starting from D7.

7.1 Command Description

(1) Display ON/OFF

This command sets the display ON/OFF.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Output level
0	1	0	1	0	1	0	1	1	1	0	Display OFF
										1	Display ON

After reset is done from the reset pin, the display is set to OFF.

(2) Display Normal/Reverse

This command allows the display ON/OFF state to be reversed, without having to rewrite the contents of the display data RAM. In this case, contents of the display data RAM are maintained.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM data = HIGH LCD ON Voltage (normal)
										1	RAM data = LOW LCD ON Voltage (reverse)

After reset is done from the reset pin, the display is set to NORMAL.

(3) Display All Lighting ON/OFF

This command forces all the displays to be turned on independently of the contents of the display data RAM. In this case, the contents of the display data RAM are maintained. In combination with the invert the display command, non-lighting display is also available.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display status
										1	Display all lighting

After reset is done from the reset pin, the display is set to normal rotation.

(4) Common Output Status Select

This command allows the scanning direction of the COM output pin to be selected. For details, see the description of "6.5.2 COM Drivers" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
0	1	0	1	1	0	0	0	1	0	0	Normal	COM0 → COM79 → COMS
										1	Reverse	COM79 → COM0 → COMS

After reset is done from the reset pin, the display is set to NORMAL.

(5) Display Start Line Set

The parameter following this command specifies the display start line address of the display data RAM shown in Fig.6.5 and 6.6.

The display area is indicated in the direction where line address numbers are incremented, starting from the specified line address. If a dynamic change of the line address is made by this command, smooth scrolling in the longitudinal direction and page breaking are enabled. For details, see the description of "6.2.4 Line address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	0	0	1	0	1	0	Mode setting
1	1	0	L7	L6	L5	L4	L3	L2	L1	L0	Address set

Set to the mode setting 00H at the time of resetting.

The setting range of the address parameter of the set display start line command in the 4-gray scale display differs from that in the binary display. The set display mode command allows selection between the 4-gray scale display and the binary display.

(i) When the display mode is a 4 gray-scale mode:

L7	L6	L5	L4	L3	L2	L1	L0	Line address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
				↓				↓
0	1	0	0	1	1	1	0	4EH
0	1	0	0	1	1	1	1	4FH

Register setting at 50H or higher is not allowed.

(ii) When the display mode is binary:

L7	L6	L5	L4	L3	L2	L1	L0	Line address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
				↓				↓
1	0	0	1	1	1	1	0	9EH
1	0	0	1	1	1	1	1	9FH

Register setting at A0H or higher is not allowed.

(6) Page Address Set

This command specifies the page address corresponding to row address when MPU access to the display data RAM shown in Fig.6.5 and 6.6. For details, see the description of "6.2.3 Page address circuit and column address circuit" in the Function Description.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	1	1	0	0	0	1	Mode setting
1	1	0	*	*	*	P4	P3	P2	P1	P0	Address setting

*: denote invalid bits.

P4	P3	P2	P1	P0	Page address
0	0	0	0	0	Page 0
0	0	0	0	1	Page 1
			↓		↓
1	0	0	1	0	Page 18
1	0	0	1	1	Page 19
1	0	1	0	0	Page 20

Set to the page address 00H at the time of resetting.
Register setting at 15H or higher is not allowed.

(7) Column Address Set

This command sets the display data RAM column address given in Fig.6.5 and 6.6. For details, see the description of "6.2.3 Column address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	0	1	0	0	1	1	Mode setting
1	1	0	C7	C6	C5	C4	C3	C2	C1	C0	Address setting

C7	C6	C5	C4	C3	C2	C1	C0	Column address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
				↓				↓
1	1	1	1	1	1	1	0	FEH
1	1	1	1	1	1	1	1	FFH

Set to the column address 00H at the time of resetting.

(8) Display Data Write

This command allows the 8-bit data to be written to the address specified by the display data RAM. After writing, column address or page address is automatically incremented +1 by the Display Data Input Direction Select command.

This enables the MPU to write the display data continuously.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	1	1	0	1
1	1	0	Write Data							

(9) Display Data Read

This command allows the 8-bit data to be read from the address specified by the display data RAM. After reading, column address or page address is automatically incremented +1 by the Display Data Input Direction select command. This enables the MPU to read multiple word data continuously.

It should be noted that one dummy reading is essential immediately after the column address or page address has been set. For details, see the description of "6.1.5 Access to display data RAM and internal register" in the Function Description. When the serial interface is used, display data cannot be read.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	1	1	0	0
1	0	1	Read Data							

(10) Display Data Input Direction Select

This command sets the direction where the display RAM address number is automatically incremented. For details, see the description of "6.2.3 Column address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	0	0	0	1	0	0	Column
										1	Page

After reset is done from the reset pin, the display is set to column address direction.

(11) Column Address Set Direction

This command can reverse the relationship between the display RAM data column address and segment driver output shown in Fig.6.5 and 6.6. So you can reverse the sequence of segment driver output pins using this command. When the display data is written or read, the column address is incremented by (+1) according to the column address given in Fig.6.4 and 6.5. For details, see the description of "6.2.3 Page address circuit and Column address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

After reset is done from the reset pin, the display is set to NORMAL.

(12) n-line Inversion Drive Register Set

This command sets the liquid crystal alternating drive reverse line count in the register. The line count to be set is 4 to 76 (19 states for each 4 lines). For details, see the description of "6.4 Display timing generation circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	1	0	1	1	0	Mode setting
1	1	0	*	*	0	N4	N3	N2	N1	N0	Line count setting

*: denote invalid bits.

N4	N3	N2	N1	N0	Reverse line count
0	0	0	0	0	4 (1 × 4)
0	0	0	0	1	8 (2 × 4)
			↓		↓
1	0	0	0	1	72 (18 × 4)
1	0	0	1	0	76 (19 × 4)

After resetting, the number of inverted lines is set to 4. Register value setting at 20 (13H) or higher is not allowed.

(13) n-line Inverting Drive ON/OFF

This command provides ON/OFF control of n-line inverting drive.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	1	0	0	1	0	0	OFF
										1	ON

Set to OFF after resetting.

(14) Display Mode Set

This command allows selection between the 4-gray scale display and the binary display and setting of the SEG output state during dummy selection period.

Structure of display data RAM in the 4-gray scale display differs from that in the binary display. For more information, see 6.2.1 Display RAM in Functional Description.

When the dummy selection period and full display lighting are selected, the same level as in full display lighting is output from all SEG during dummy selection. When the dummy selection period and full display lighting shut off are selected, the same level as in full display lighting shut off is output. Determine after adjusting to the display pattern of the liquid crystal panel and comparing the display quality.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	1	0	0	1	1	0	Mode set
1	1	0	*	*	*	*	*	*	K1	K0	State set

*: denote invalid bits.

K1	K0	State of selection
0		Dummy Selection Period Full display lighting
1		Dummy Selection Period Full display lighting shutoff
	0	4-gray scale mode
	1	Binary mode

Set to (K1, K0) = (0, 0) at the time of resetting.

(15) Gray-scale Pattern Set

This command sets the level of gray-scale.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	1	1	0	0	1	Mode set
1	1	0	*	G6	G5	G4	*	G2	G1	G0	Selection of gray-scale level

*: denote invalid bits.

Set the gray scale bit (1, 0) with G6 to G4.

	G6	G5	G4		G2	G1	G0	Level of gray-scale select
—	0	1	0	—	—	—	—	White
—	0	1	1	—	—	—	—	
		↓				↓		↓
—	1	1	0	—	—	—	—	Black

Set the gray scale bit (0, 1) with G2 to G0.

	G6	G5	G4		G2	G1	G0	Level of gray-scale select
—	—	—	—	—	0	0	1	White
—	—	—	—	—	0	1	0	
		↓				↓		↓
—	—	—	—	—	1	0	1	Black

(16) Display Line Number Set

This command allows change of the number of display lines. Driving the number of lines required for display provides liquid crystal drive at lower power consumption. Display is provided in the desired location on the panel (continuous COM pin + COMS pin in 4 lines).

This command is used with a pair of the display line number set parameter and start point (block) parameter, so be sure to set both parameters so that one of them will immediately follow the other.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	1	0	1	1	0	1	Mode set
1	1	0	*	*	*	U4	U3	U2	U1	U0	Display Line Number Set
1	1	0	*	*	*	S4	S3	S2	S1	S0	Start point set

*: denote invalid bits.

- Set number of display line register

The number of display lines can be set from 5 (4 lines + COMS) to 81 lines (80 lines + COMS) in steps of 4 lines.

The relationship between the number of display lines and display duty (1 selection period length of liquid crystal line sequential drive for fram cycle) is

$$duty = 1 \Big/ (l + 7)$$

U4	U3	U2	U1	U0	Number of display lines	Display duty
0	0	0	0	0	5	1/12
0	0	0	0	1	9	1/16
		↓				
1	0	0	1	0	77	1/84
1	0	0	1	1	81	1/88

After resetting, the range is set to (U4, U3, U2, U1, U0) = (1, 0, 0, 1, 1) 81-line display.
Register value setting at (1, 0, 1, 0, 0) (14H) or higher is not allowed.

- Start point (block) register set parameter

Use this parameter to set 5-bit data in the start point (block) register. Then one of 20 start point blocks will be determined.

Use the Display Start Line Set command (5) for display scroll. Do not use this command for display scroll.

S4	S3	S2	S1	S0	Start point set	
					Common output status select = normal	Common output status select = reverse
0	0	0	0	0	0 (COM0 to 3)	19 (COM79 to 76)
0	0	0	0	1	1 (COM4 to 7)	18 (COM75 to 72)
0	0	0	1	0	2 (COM8 to 11)	17 (COM71 to 68)
		↓			↓	↓
1	0	0	1	0	18 (COM72 to 75)	1 (COM7 to 4)
1	0	0	1	1	19 (COM75 to 79)	0 (COM3 to 0)

Set to 0 block (S4, S3, S2, S1, S0) = (0, 0, 0, 0, 0) at the time of resetting.
Register value setting at (1, 0, 1, 0, 0) (14H) or higher is not allowed.

[Setup example of set the number of display line command] (in case of "common output status select" = Normal)

Setup example 1: When the display is set to 45 lines (1/52 duty) and the start point is to 1 (COM4 to 7), the display of 45 lines appears from COM4-47 + COMS

Setup example 2: When the display is set to 65 lines (1/72 duty) and the start point is to 16 (COM64 to 7), the display of 65 lines appears from COM64-79, COM60-47 + COMS. Following COM79, COM0 is selected and COMS is selected at the end.

As the most suitable voltage for liquid crystal drive changes by changing the number of display lines, reset to the voltage that makes the display most suitable with the electronic volume.

If the COM pin is not used in common to master and slave in operation of multiple chips of master/slave (top and bottom two-screen drive of SEG 256 lines, COM 81 lines + 81 lines), the difference in the number of display lines between master and slave causes a difference in the density of display, depending on the display area. Be sure to set to the same number of display lines.

(17) Read Modify Write

This command is paired with end command for use. If this command is entered, the column address is not changed by the Display Data Read command. It can be incremented +1 by the Display Data Read command alone. This states retained until the End command is input. If the End command is input, the column address goes back to the address when the Read Modify Write command is input. This function reduces the MPU loads when changing the data repeated in the specific display area such as blinking cursor.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

After reset, read modify write mode is not available.

A command other than display data Read/Write command can be used in the Read Modify Write mode. However, you cannot use the column address set command.

- Sequence for cursor display

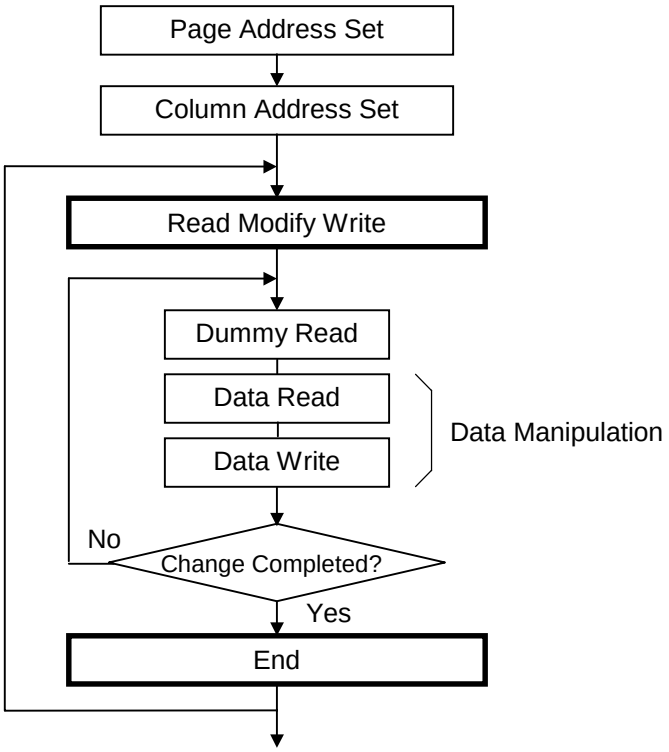


Fig.7.1

(18) End

This command releases the read modify write mode and gets column address back to the initial address of the mode.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

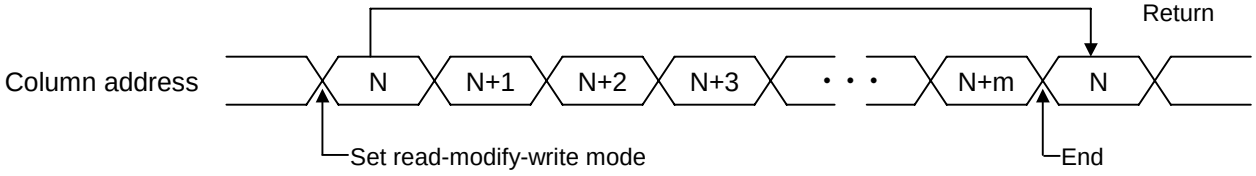


Fig.7.2

(19) Built-in Oscillator Circuit ON/OFF

This command starts the built-in oscillator circuit operation. It is enabled only in the master operation mode (M/S=HIGH) when built-in oscillator circuit is valid (CLS=HIGH).

An internal clock is required to operate the built-in power supply. To use the built-in oscillation circuit, execute the built-in oscillation circuit ON command before the set power control command. To turn off the internal oscillation circuit, it is necessary to shut off the built-in power, using the set power control command, and discharge the capacitor connected externally, using the discharge command, beforehand.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Built-in oscillator circuit
0	1	0	1	0	1	0	1	0	1	0	OFF
										1	ON

Set to OFF after resetting.

(20) Built-in Oscillator Circuit Frequency Select

This command sets the built-in oscillator circuit frequency.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	0	1	1	1	1	1	Mode setting
1	1	0	*	*	*	*	F3	F2	F1	F0	CL frequency

F3	F2	F1	F0	Built-in oscillation circuit frequency f_{CL} [kHz]			Frame frequency f_{FR} [Hz]		
				Min.	Typ.	Max.	81-line display	65-line display	33-line display
0	0	0	0	386	420	454	199	243	438
0	0	0	1	317	345	374	164	200	360
0	0	1	0	278	303	328	143	175	315
0	0	1	1	243	264	286	125	153	275
0	1	0	0	225	248	271	117	143	258
0	1	0	1	202	223	243	105	129	232
0	1	1	0	187	206	225	98	119	215
0	1	1	1	172	189	207	89	109	197
1	0	0	0	165	184	203	87	107	192
1	0	0	1	153	171	188	81	99	178
1	0	1	0	145	162	178	77	94	168
1	0	1	1	136	152	167	72	88	158
1	1	0	0	130	146	163	69	85	153
1	1	0	1	123	138	154	65	80	144
1	1	1	0	117	133	148	63	77	138
1	1	1	1	111	126	140	60	73	131

*: (F3, F2, F1, F0) = (0, 0, 0, 0) is set after resetting.

* The table above shows the values at 25°C and Min. and Max. indicate manufacturing variations in the built-in oscillation cirucuit frequency.
* The f_{FR} indicates frame frequency when the built-in oscillation circuit frequency is a typical value, not the frequency of the FR signal. For the relationship between f_{CL} and f_{FR}, see 9. DC Characteristics and Table 9.9.

(21) Power Control Set

This command sets the built-in power supply circuit function. For details, see the description of "6.6 Power supply circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	0	0	1	0	1	Mode set
1	1	0	0	0	0	0	0	W2	W1	W0	Set state

W2	W1	W0	Selected state
0			Step-up circuit: OFF
1			Step-up circuit: ON
	0		V_3 adjusting circuit: OFF
	1		V_3 adjusting circuit: ON
		0	LCDV circuit: OFF
		1	LCDV circuit: ON

V_3 adjusting circuit: V_3 voltage adjusting ciruit,
LCDV circuit: liquid crystal drive voltage generation circuit
Set to (W2, W1, W0) = (0, 0, 0) after resetting.

An internal clock is required to operate the built-in power supply circuit. If the built-in oscillation circuit is used, execute the built-in oscillation circuit ON command before the set power control command. To use the built-in oscillation circuit, operate the built-in oscillation circuit and input to the CL pin before the set power control command. When the clock stopped during built-in power circuit operating, abnormal display may appear. Therefore don't stop built-in oscillator or external clock during built-in power circuit operation.

To operate the IC on master-slave configuration, the built-in power supply circuit cannot be used. Set the parameter (0, 0, 0), using the set power control command.

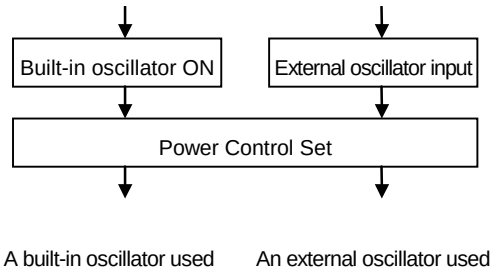


Fig.7.3

(22) Adjust V_3 voltage

Select the V_3 voltage range out of 8 states, using this command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	0	1	0	1	1	Mode setting
1	1	0	*	*	*	*	*	V2	V1	V0	Set the adjustable range

*: denote invalid bits.

V2	V1	V0	V_3 voltage output range
0	0	0	4.20V to 6.95V
0	0	1	4.71V to 7.81V
0	1	0	5.36V to 8.89V
0	1	1	6.03V to 10.00V
1	0	0	6.89V to 11.43V
1	0	1	7.72V to 12.80V
1	1	0	8.77V to 14.55V
1	1	1	9.65V to 16.00V

Output voltage value at 25°C (V2, V1, V0) = (0, 0, 0) is set after performing reset.

(23) LCD Bias Set

With this command, the bias ratio of voltage required for a liquid crystal drive is chosen.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	1	0	0	0	1	0	Mode setting
1	1	0	0	0	0	0	0	0	B1	B0	Bias ratio setting

B1	B0	Bias ratio
0	0	1/8
0	1	1/6.7
1	0	1/5.3

(B1, B0)=(0, 0) are setup after reset.
Register setting at 03H is not allowed.

(24) Electronic Volume

This command controls liquid crystal drive voltage V3 issued from the built-in liquid crystal power supply V3 voltage regulating circuit, and adjusts the liquid crystal display density. For details, see the description of "6.6.2 V3 Voltage Regulating Circuit" in the Function Description.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	0	0	0	0	0	1	Mode setting
1	1	0	*	R6	R5	R4	R3	R2	R1	R0	Electronic Volume setting

*: denote invalid bits.

When a 7-bit data to the electronic volume register is set by this command, V3 assumes one state out of voltage values in 128 states.

R6	R5	R4	R3	R2	R1	R0	V3
0	0	0	0	0	0	0	Smaller
0	0	0	0	0	0	1	
0	0	0	0	0	1	0	
				↓			↓
1	1	1	1	1	1	0	
1	1	1	1	1	1	1	Larger

After resetting, (R6, R5, R4, R3, R2, R1, R0) are set to 00H.

(25) Discharge ON/OFF

This command is discharges the capacitors connected to the power supply circuit. This command is used when the system power of this IC is turned off, and the display line number is changed. See the description of 7.3.3 Power Supply OFF and 7.3.4 Changing the Number of Line in the 7.3 Instruction Setup: Reference.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	1	0	1	0	1	0	Discharge OFF
										1	Discharge ON

After resetting, discharge OFF is set.
However, Discharge is operated for the $\overline{RES}$=LOW period.

When power is externally supplied to any of V_{OUT}, V_3, V_2, V_1, V_C, MV_1, or MV_2, be sure to execute this command after setting the external power supply to the state of high impedance.

(26) Power Saving

When the IC is placed in the power-saving mode with this command and there is no access from the MPU, current consumption can be reduced to the value close to static current.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Power save mode
0	1	0	1	0	1	0	1	0	0	0	OFF
										1	ON

In the power save mode, display data and operation before power saving are maintained. Access to the display data RAM from the MPU is also possible.

In the power save mode, the following occurs:
Stop of oscillator circuit
Stop of LCD power supply circuit
Stop of all liquid crystal drive circuit (V_{SS} level output is issued as the segment and common driver output).

The power save OFF command releases the power save mode. The system goes back to the state before the power save mode.

If external oscillator circuit is used, the built-in booster circuit operates even in the power save mode. To reduce the current consumption during power saving by turning off the built-in booster circuit, either as following operations is required after entry to the power save mode.
(1) external clock is stopped
(2) built-in booster circuit is stopped by power control set command
To quit from power save state, either as following operations is required before power save OFF command.
(1) external clock is started.
(2) built-in booster circuit is started by power control set command

When the external power supply is used, it is recommended to stop the external power supply circuit function when the power save mode is started. For example, when each level of the liquid crystal drive voltage is given from the external resistive divider circuit, it is recommended to add a circuit to cut off the current flowing to the resistive divider circuit when power save function is started. The S1D15721 Series has a liquid crystal display blanking control control pin $\overline{DOF}$, and the level goes LOW when power save function is started. You can use the $\overline{DOF}$ output to stop the external power supply circuit function.

(27) Temperature Gradient Set

The 3-bit data of this command is used to set the temperature gradient characteristics of the liquid crystal drive voltage output from the built-in power supply circuit from eight states. The temperature gradient of the liquid crystal drive voltage can be set according to the liquid crystal temperature gradient to be used. This eliminates the need of a temperature characteristics regulating circuit to be installed outside this IC (S1D15721 Series).

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	0	0	1	1	1	0	Mode setting
1	1	0	*	*	*	*	*	T2	T1	T0	Temperature gradient setting

*: denote invalid bits.

T2	T1	T0	Temperature gradient [%/°C] (for reference)
0	0	0	-0.06
0	0	1	-0.08
0	1	0	-0.10
0	1	1	-0.11
1	0	0	-0.13
1	0	1	-0.15
1	1	0	-0.17
1	1	1	-0.18

(T2, T1, T0)= (0,0,0) is set after resetting.

(28) Status Read

This command reads out the temperature gradient select bit set on the register.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	0	0	1	1	1	0	Mode setting
1	0	1	*	*	*	*	*	T2	T1	T0	Value of temperature gradient read

*: denote invalid bits.

T2	T1	T0	Temperature gradient [%/°C] (for reference)
0	0	0	-0.06
0	0	1	-0.08
0	1	0	-0.10
0	1	1	-0.11
1	0	0	-0.13
1	0	1	-0.15
1	1	0	-0.17
1	1	1	-0.18

(29) Temperature sensor ON/OFF

The ON/OFF of the temperature sensor is set by this command.

Turning on the temperature sensor does causes no problem even when output from the temperature sensor circuit is not used, however, operating current of the temperature sensor circuit is steadily consumed.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	0	1	0	1	0	0	0	Temperature sensor OFF
										1	Temperature sensor ON

The temperature sensor is set to OFF after performing reset.

(30) MLS drive selection

This command is used to select MLS drive method and liquid crystal AC drive method. Select the most suitable drive method for the display pattern.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	1	1	0	0	1	1	1	Mode setting
1	1	0	*	*	*	P4	P3	0	1	1	Driving method set

* denote invalid bits.

P4	P3	—	P1	P0	Drive method
0		—			n-line inversion Frame inversion overlap ON
1		—			n-line inversion Frame inversion overlap OFF
	0	—			MLS dispersion drive
	1	—			MLS non-dispersion drive

After resetting, (P4, P3) is set to (0, 1).

- n line inversion
  Frame inversion overlap OFF
  Controlled by the parameter P4. Enabled only when n line inversion drive is ON.
  Deviation can be produced in liquid crystal AC drive, depending on combination of the number of display lines and the number of lines of n line inversion, which could cause dark and light streaks. This function reduces deviation in liquid crystal AC drive and dark and light streaks of display by overlapping the n line inversion with the frame inversion.

- MLS dispersion drive / non-dispersion drive
  Controlled by the parameter P3.
  For this IC, the 4-line simultaneous selection MLS dispersion drive method has been adopted. The common output pin outputs a signal at the same time when the display lines are selected four times in 1 frame in 4 lines.
  For non-dispersion drive, the common output pin outputs a signall by selecting four times continuously. It is recommended to use this drive if the display is frequently changed.
  For dispersion drive, the common output pin outputs a signall by selecting four times at equal intervals in a frame. Compared to non-dispersion drive, higher contrast can be obtained basically, however, the display flicker may be caused in the drive in which animation is displayed.

In either function, determine to turn ON/OFF after evaluating the display quality in a comprehensive manner, including actual display pattern flicker and cross talk. The frame frequency from which optimal frequency can be obtained may be switched when the function is turned ON/OFF. Use the select builit-in oscillation circuit command or change the clock frequency supplied externally to drive at an appropriate frame frequency.

(31) NOP
This is a Non-Operation command.

	$\overline{E}$	$R/\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	0	0	0	1	1

7.2 Command Table

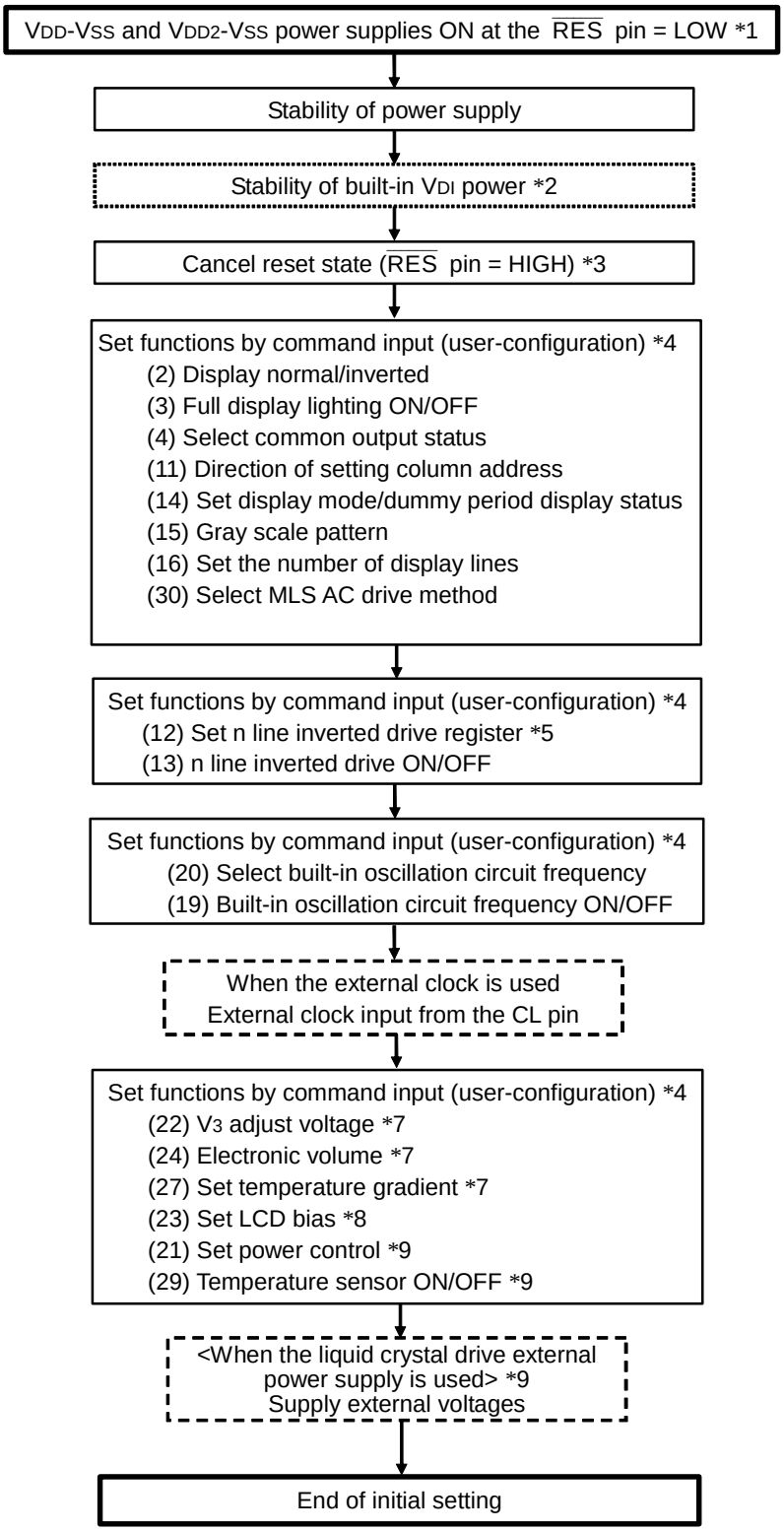
Table 7.1 Table of commands in S1D15721 series

Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF control. 0:OFF, 1:ON
(2) Display Normal/Reverse	0	1	0	1	0	1	0	0	1	1	0 1	LCD display normal/reverse 0: Normal, 1: Reverse
(3) Display All Lighting ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display All Lighting 0: Normal display, 1: All ON
(4) Common Output Status Select	0	1	0	1	1	0	0	0	1	0	0 1	Selects COM output scan direction. 0: Normal, 1: Reverse
(5) Display Start Line Set	0 1	1 1	0 0	1	0 Display start line address	0	0	1	0	1	0	Sets display start line.
(6) Page Address Set	0 1	1 1	0 0	1 *	0 *	1 *	1	0 Page address	0	0	1	Sets the display RAM page address.
(7) Column Address Set	0 1	1 1	0 0	0	0 Column Address Set	0	1	0	0	1	1	Sets the display RAM column address.
(8) Display Data Write	0 1	1 1	0 0	0	0 Writes data	0	1	1	1	0	1	Writes data to the display RAM.
(9) Display Data Read	0 1	1 0	0 1	0	0 Reads data	0	1	1	1	0	0	Reads data to the display RAM.
(10) Display Data Input Direction Select	0	1	0	1	0	0	0	0	1	0	0 1	Display RAM data input direction 0: Column direction, 1: Page direction
(11) Column Address Set Direction	0	1	0	1	0	1	0	0	0	0	0 1	Compatible with display RAM address SEG output 0: Normal, 1: Reverse
(12) n-line Inversion Drive Register Set	0 1	1 1	0 0	0 *	0 *	1 0	1	0 Invert line count	1	1	0	n-line invert drive. Sets the line count.
(13) n-line Inversion Drive Resister ON/OFF	0	1	0	1	1	1	0	0	1	0	0 1	Resets the line invert drive. 0: n-line OFF, 1: n-line ON
(14) Display Mode	0 1	1 1	0 0	0 *	1 *	1 *	0 *	0 *	1 *	1 Mode	0	Switches between dummy selection in the state of display and 4-gray scale display/ binary display
(15) Gray-scale Pattern Set	0 1	1 1	0 0	0	0 Gray-scale pattern	1	1	1	0	0	1	Selects the contrast of gray-scale bit (1,0),(0,1)
(16) Display Line Number Set	0 1 1	1 1 1	0 0 0	0 * *	1 * *	1 * *	0	1 Display line Start spot	1	0	1	Line Number set Start spot set
(17) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. Increments +1 in the write mode. Does not increment in the read mode.
(18) End	0	1	0	1	1	1	0	1	1	1	0	Resets read modify write functions.

Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(19) Built-in Oscillator Circuit ON/OFF	0	1	0	1	0	1	0	1	0	1	0 1	Built-in oscillator circuit operation 0: OFF, 1: ON
(20) Built-in Oscillator Circuit Frequency Select	0 1	1 1	0 0	0 *	1 *	0 *	1 *	1	1 Frequency	1	1	Changes frequency of a built-in oscillation circuit
(21) Power Control Set	0	1	0	0	0	1	0	0	1	0	1	Selects built-in power supply operation state
(22) Adjust V_3 voltage	0 1	1 1	0 0	0 *	0 *	1 *	0 *	1 *	0 V_3 range	1	1	Sets the voltage range output from the V_3 adjusting circuit.
(23) LCD bias set	0 1	1 1	0 0	1 *	0 *	1 *	0 *	0 *	0 *	1 bias	0	Selects the bias ratio of the liquid crystal drive voltage.
(24) Electronic Volume	0 1	1 1	0 0	1 *	0	0 Electronic volume	0	0	0	0	1	Electronic volume 128 states
(25) Discharge ON/OFF	0	1	0	1	1	1	0	1	0	1	0 1	Discharges Power supply circuit connection capacitor. 0: OFF (normal), 1:ON
(26) Power Save ON/OFF	0	1	0	1	0	1	0	1	0	0	0 1	Power Save 0: OFF, 1: ON
(27) Temperature Gradient Set	0 1	1 1	0 0	0 *	1 *	0 *	0 *	1 *	1 Temperature gradient	1	0	Sets the temperature gradient of the liquid crystal drive voltage 8 levels
(28) Status Read	0 1	1 0	0 1	1 *	0 *	0 *	0 *	1 *	1 Temperature gradient	1	0	Issues the temperature gradient select bit.
(29) Temperature sensor ON/OFF	0	1	0	0	0	1	0	1	0	0	0 1	Operation of the temperature sensor circuit 0: OFF (normal), 1: ON
(30) MLS drive selection	0 1	1 1	0 0	1 *	1 *	1 *	0 Status	0	1 0	1 1	1 1	Sets the MLS drive method and liquid crystal AC drive method
(31) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-operation command

7.3 Instruction Setup Example (Reference)

7.3.1 Initial setup



Notes: Numbers in parentheses correspond to those in the item of command description.

*1: When supplying V_{OUT} or V_3 - MV_2 voltages externally, set them to the state of high impedance and turn on V_{DD} and V_{DD2} power. When supplying V_{DI} voltage externally, input at the same timing as V_{DD} and V_{DD2}.

*2: When using the built-in V_{DI} generaion circuit, cancel the state of reset after V_{DI} voltage is started and stabilized. The wait time is proportional to the capacity value between V_{DI} and V_{SS}. Secure the wait time of 30 ms or more when V_{SS} = V_{DD2} = 5.0V and the capacity value is 4.7μF.

*3: The contents of the display data RAM are undefined even in the state of initial setting following reset.

*4: Set the state when performing initial setting and periodical command resetting (refreshing) even if default values after resetting are used, a recovery can be made from a sudden change of internal state resulted from excessive external noise.

*5: It is not necessary to set if n line inverted drive is not used.

*6: It is not necessary to set if the built-in oscillation circuit is not used.

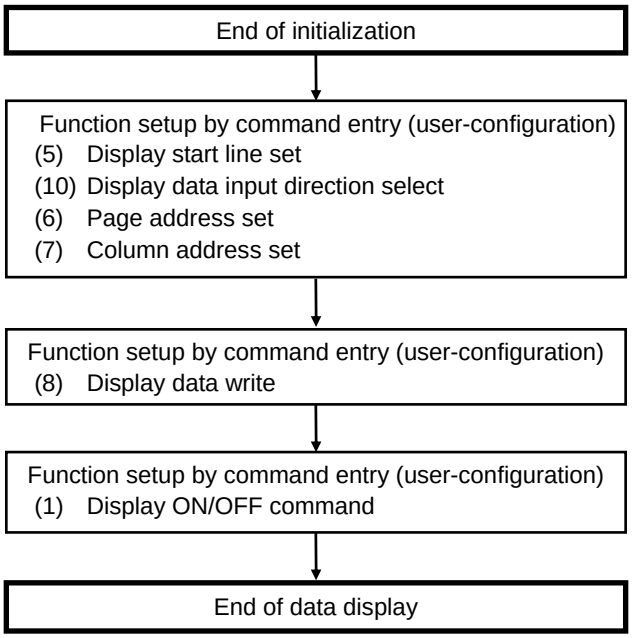
*7: It is not necessary to set if the built-in V_3 voltage adjusting circuit is not used.

*8: It is not necessary to set if the built-in liquid crystal drive voltage generation circuit (voltage follower) is not used.

*9: When supplying external power from V_{OUT} or V_3 and using the built-in V_3 voltage adjusting circuit or built-in liquid crystal drive voltage generation circuit, externally supply power before issuing the set power control command.

When the external power supply is started abruptly, the system power voltage may be changed due to capacity coupling of the bypass capacitor. To avoid a problem such as false recognition of a command, do not issue the command until charging of the bypass capacitor after turning on the external power supply is completed and each power voltage is stabilized.

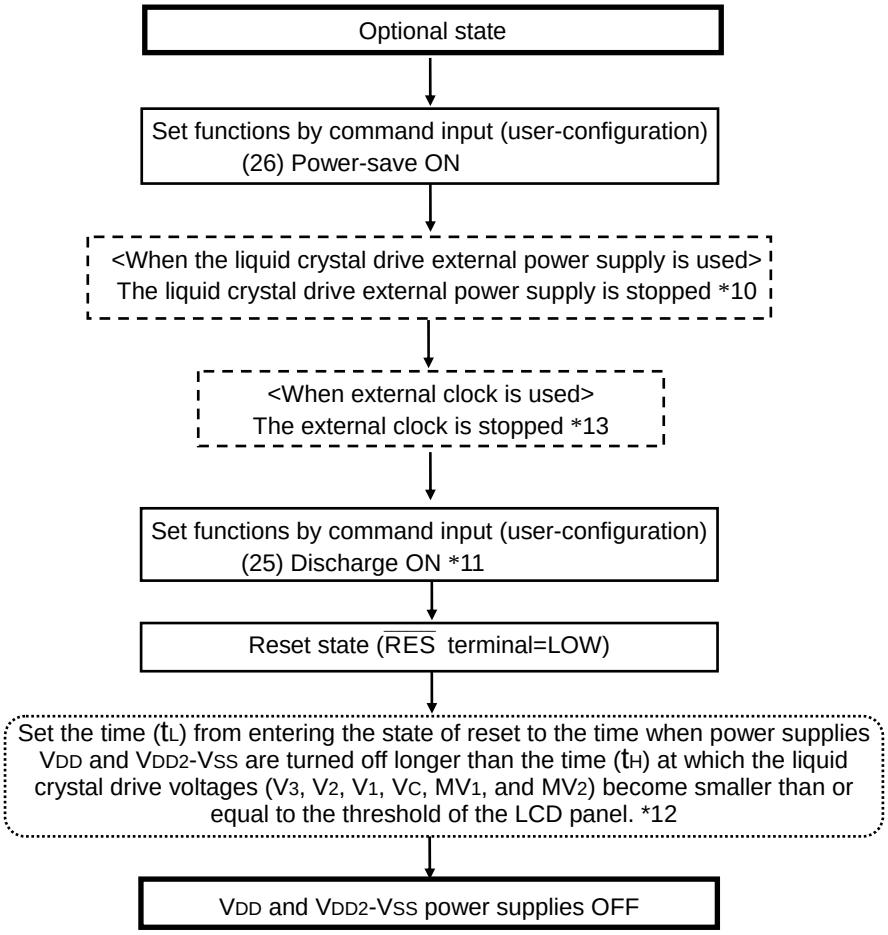
7.3.2 Data display



Note:

* DDRAM contents are not determined after end of initialization. Write data to all the DDRAM used for display <All area which is set by "(5) Display start line set" and"(16) Display Line Number Set" command, and Page20 (correspond to COMS)>. See “(8) Display data write” in the “7.1 Command Description”.

7.3.3 Power OFF



Notes: This IC controls the circuits of the liquid crystal drive power supply system in the V_{DD2}-V_{SSL} power supply circuits. If V_{DD2}-V_{SSL} power supplies are cut off with the voltage remaining in the liquid crystal drive power supply system, the voltage that is not controlled will be output from the SEG and COM pins, which could cause display problem. Be sure to follow the above power supply OFF sequence.

*10: Set to the state of high impedance.

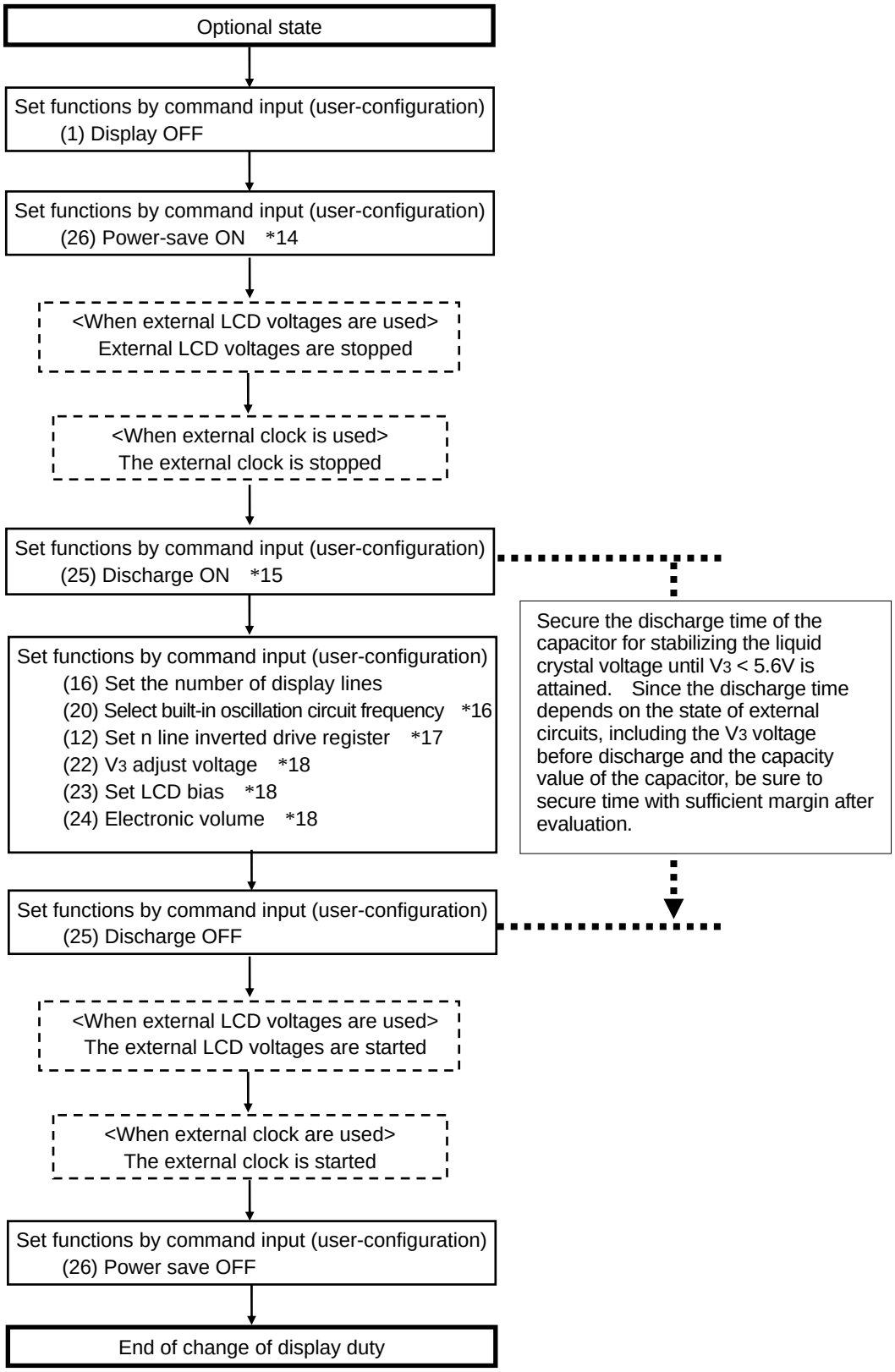
*11: Turning ON the discharge discharges the IC external capacitor connected to the V_{OUT}, each CAP pin, V_3, V_2, V_1, V_C, MV_1 and MV_2 pins to the V_{DD2} and V_{SS}. At this time, in some power supply peripheral circuitry, the discharge intensity flowing in increases the power potential shorted with the V_{DD2} and V_{DD2}. To make sure that the potential of the V_{DD2} and power supply shorted with the V_{DD2} do not exceed its absolute maximum rating, take the following measures.

- Use the power supply circuit that can absorb the discharge intensity to the V_{DD2} pin
- Connect the zener diode between V_{DD2} and V_{SS};
- Adjust the capacity value of each capacitor;
- Add the external resistor for discharge between V_{OUT} and V_{SS} and between V_3 and V_{SS} to discharge by switching the external resistor; Following completion of discharge, disconnect the external resistor and turn off power after setting $\overline{RES}$=LOW.

*12: The threshold voltage of the liquid crystal 1[V] serves as an index.

*13: In case of using external clock, the external clock must be stopped at LOW when you stop it.

7.3.4 Change the Number of Line



Notes:

*14: When the number of liquid crystal display lines is changed, the liquid crystal drive voltage from which optimal contrast is obtained changes. To avoid the problem of the display, for example, the display turns black for an instant, place in the power save mode in the above sequence and turn off the display once. Then set to obtain the optimal liquid crystal drive voltage before displaying again.

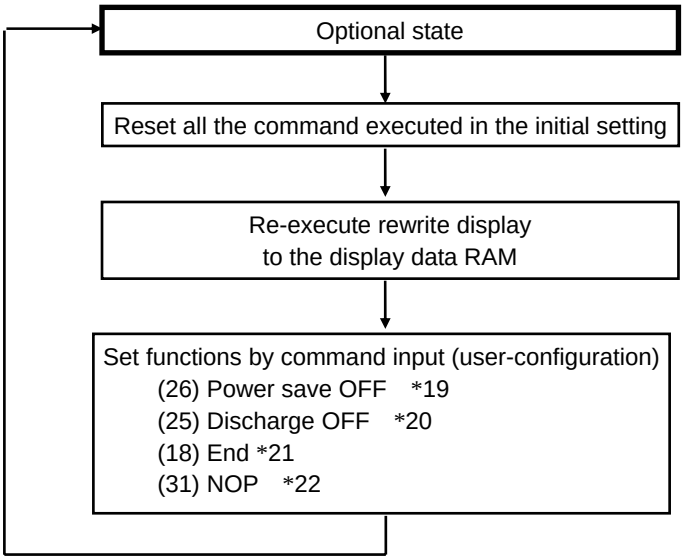
*15: To change the liquid crystal drive voltage, discharge the capacitor for holding the voltage once. For discharge, see 7.3.3 Sequence for Turning OFF Power

*16: Set to frame frequency with evaluating display quality.

*17: Set to the number of n line inversion with evaluating display quality.

*18: When power supply voltage for liquid crystal drive is supplied externally, set the necessary items in conformity to the functions of the built-in power supply used.

7.3.5 Refresh



Note: This IC holds the operating state by a command, however, it may change the internal state when excessive external noise enters. Measures are required to prevent noise generation or influence in terms of mounting and the system itself. To provide for a sudden, excessive external noise, it is recommended to refresh the operating state and the contents of display regularly.

*19: When the IC chip enters the power-saving mode, the power save OFF command can be used to exit.

*20: When the IC chip enters discharge state, the Discharge OFF command can be used to exit.

*21: When the IC chip enters Read Modify Write state, the END command can be used to exit.

*22: In case of S1D15721D01B000, when the IC chip enters Test mode, the NOP command can be used to exit.

8. ABSOLUTE MAXIMUM RATINGS

Table 8.1

V_{SS} = 0V unless otherwise specified.

Item		Symbol	Specified value	Unit
Power voltage (1)		V_{DD}	-0.3 to +6.0	V
Power voltage (2)		V_{DD2}	V_{DI} to +6.0	
Power voltage (3) (requires external input)		V_{DI}	-0.3 to +3.6	
Power voltage (4)		V_3, V_{OUT}	-0.3 to +18.0	
Power voltage (5)		V_2, V_1, V_C, MV_1, MV_2	-0.3 to V_3	
Input voltage		V_{IN}	-0.3 to V_{DD}+0.3	
Output voltage		V_O	-0.3 to V_{DD}+0.3	
Operating temperature (S1D15721D00B000)		T_{OPR}	-40 to +85	°C
Operating temperature (S1D15721D01B000)		T_{OPR}	-40 to +95	
Storage temperature	bare chip	T_{STR}	-55 to +125	

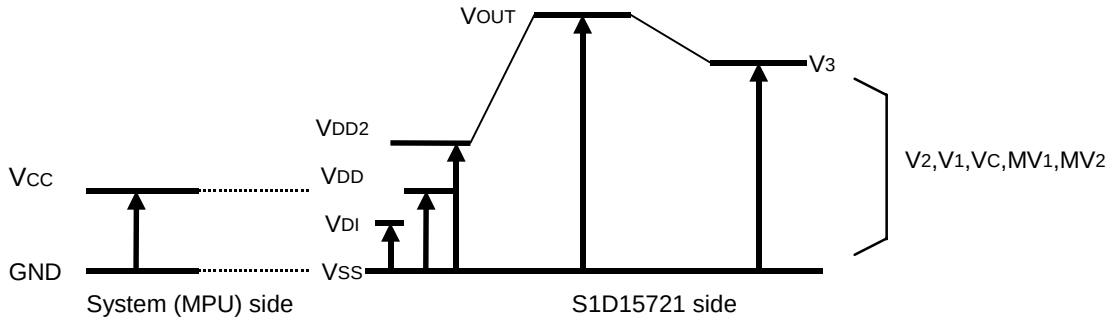


Fig.8.1

Notes: 1. Always keep the voltages of V_3, V_2, V_1, V_C, MV_1 and MV_2 in the following condition: $V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq V_{SS}$. When inputting these voltages from outside, bring them to the high impedance status during resetting by RES pin and input voltages that satisfy the above condition after releasing the reset.

2. For voltage of V_{OUT}, always keep $V_{OUT} \geq V_{DD2}$. When inputting V_{OUT} from outside, bring it to the high impedance status during resetting by RES pin and input a voltage that satisfies $V_{OUT} \geq V_3$+0.2V after releasing the reset. When V_{OUT} is supplied externally, the V_{OUT} should be High impedance state from V_{DD} and V_{DD2} ON to the V_{OUT} ON.

3. If the LSI has been used in excess of the absolute maximum rating, it may be subjected to permanent breakdown. So in the normal operation, the LSI preferred to be used under the condition of electrical characteristics. If this condition is not met, LSI operation error may occur and LSI reliability may be deteriorated.

9. DC CHARACTERISTICS

9.1 DC Characteristics

V_{SS}=0V, V_{DD}=5.0V ±10% and T_a=-40 to +85°C unless otherwise specified.
T_a=-40 to +85°C (S1D15721D00B000)
T_a=-40 to +95°C (S1D15721D01B000)

Table 9.1

Item		Symbol	Conditions		Specified value Min.	Typ.	Max.	Unit	Applicable pin
Operating voltage (1)		V_{DD}	—		2.7	—	5.5	V	V_{DD} *1
Operating voltage (2)		V_{DD2}	—		V_{DI}	—	5.5		V_{DD2}
Operating voltage (3)		V_{DI}	requires external input		2.7	—	3.3		V_{DI}
Operating voltage (4)		V_{OUT}	—		V_{DD2}	—	17.0		V_{OUT}
Operating voltage (5)		V_3	—		5.6	—	17.0		V_3 *2
High-level input voltage (1)		V_{IHC1}	V_{DD}=2.7V to 5.5V		0.8xV_{DD}	—	V_{DD}		*3
Low-level input voltage (1)		V_{ILC1}			V_{SS}	—	0.2xV_{DD}		*3
High-level input voltage (2)		V_{IHC2}	V_{DI}=2.7V to 3.3V		0.8xV_{DD}	—	V_{DI}		*7
Low-level input voltage (2)		V_{ILC2}			V_{SS}	—	0.2xV_{DI}		*7
Hysteresis voltage		V_H	V_{DD}=5.0V		1.0	1.4	—		*4
High-level output voltage (1)		V_{OHC1}	V_{DD}=2.7V	I_{OH}=-25µA	0.8xV_{DD}	—	V_{DD}		*5
Low-level output voltage (1)		V_{OLC1}	to 5.5V	I_{OL}= 25µA	V_{SS}	—	0.2xV_{DD}		*5
High-level output voltage (2)		V_{OHC2}	V_{DD}=2.7V	I_{OH}=-100µA	0.8xV_{DD}	—	V_{DD}		*6
Low-level output voltage (2)		V_{OLC2}	to 5.5V	I_{OL}= 100µA	V_{SS}	—	0.2xV_{DD}		*6
High-level output voltage (3)		V_{OHC3}	V_{DD}=2.7V	I_{OH}=-100µA	0.8xV_{DI}	—	V_{DI}		*7
Low-level output voltage (3)		V_{OLC3}	to 3.3V	I_{OL}= 100µA	V_{SS}	—	0.2xV_{DI}		*7
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}		-1.0	—	1.0	µA	*8
Output leak current		I_{LO}			-3.0	—	3.0		*9
LCD driver ON resistance		R_{ON}	T_a=25°C	V_3= 7.2V	—	3.5	7.0	kΩ	SEGn
				V_3= 14.0V	—	1.8	3.6		COMn *10
Static current consumption		I_{DDQ}	T_a=25°C	V_{DD} = 3.0V	—	0.3	1	µA	V_{DD} *11
		I_{DIQ}		V_{DI} = 3.0V	—	0.3	1	µA	V_{DI}
		I_{3Q}		V_3 = 16.0V	—	5	20		V_3
Input pin capacity		C_{IN}	T_a=25°C, f=1MHz		—	8	16	pF	—
Oscillation frequency	Built-in oscillation	f_{OSC}	T_a=25°C		386	420	454	kHz	*12
	External input		Max. frequency		—	420	500		

[Asterisked references]

*1. Does not guarantee if there is an abrupt voltage variation during MPU access.

*2. For V_{DI} and V_3 system operating voltage range, see Fig.9.6.
Applicable when the external power supply is used.

*3. A0, D0 to D5, D6(SCL), D7(SI), RD(E), WR(R/W), CS, CLS, CL, FR, M/S, C86, P/S, RES, VDIS, TEST1, TEST2, TEST3, TESTA pins.

*4. A0, D6(SCL), D7(SI), RD(E), WR(R/W), CS, CL, RES pins of S1D15721D01B000.

*5. D0 to D7 pins.

*6. CL pins

*7. FR, DOF, F1, F2 and SYNC pins

*8. A0, RD(E), WR(R/W), CS, CLS, M/S, C86, P/S, RES, VDIS, TEST1, TEST2, TEST3, TESTA, TESTB pins.

*9. Applicable when D0 to D5, D6(SCL), D7(S1), CL, FR, DOF, F1, F2 and SYNC pins have a high impedance.

*10. Indicates the resistance when 0.1V voltage is applied between the output pin SEGn or COMn and each power supply (V_2, V_1, V_C, MV_1, MV_2).
R_{ON} = 0.1V/ΔI (where ΔI denotes current when 0.1V is applied when power is on).

*11. Current values when VDIS = LOW.

*12. For relations between the oscillation frequency and the frame frequency, see Table 9.9. Min. and max. of the built-in oscillation circuit indicate manufacturing variations in oscillation frequency, the typ. at the external input indicates the equal value of frame frequency and the built-in oscillation circuit frequency is a typ. value, and the max. value indicates the maximum operability.

Table 9.2

Item		Symbol	Conditions	Specified value			Unit	Applicable pin
				Min.	Typ.	Max.		
Built-in power circuit	Input voltage	V_{DD2}	double boosting	2.7	—	5.5	V	V_{DD2}
		V_{DD2}	triple boosting	2.7	—	5.5		
		V_{DD2}	quadruple boosting	2.7	—	4.2		
		V_{DD2}	quintuple boosting	2.7	—	3.4		
	Boosting output voltage	V_{OUT}	—	—	—	17.0		V_{OUT}
	Voltage adjusting circuit operating voltage	V_3	—	5.6	—	17.0		V_3 *13

*13 V_3 voltage adjustment circuit is adjusted in the electronic volume range of motion.

9.1.1 Dynamic current consumption value

While the indication operation is in progress and when the built-in power supply being turned on:
The current value being consumed by the whole IC including the built-in power supply.

Indication mode: 4 gradations, f_{FR}=144Hz, $V_{DD} = V_{DD2}$, n-line reversion 1/8 bias, When built-in oscillation is used

Table 9.3 Indications: All white indications *14

Symbol: ISS(1)

V_{DD}	Boosting	V_3 voltage	1/81 Duty		1/65 Duty		Unit	Remark
			Typ.	Max.	Typ.	Max.		
5V	Triple	14V	398	664	363	605	μA	
		10V	392	654	357	595		
3V	Quintuple	14V	531	885	494	824		
	Quadruple	10V	429	715	398	663		

*14 When normally white liquid crystal panel is used. In normally black, all black.

Table 9.4 Indications: Heavy load indications *15

Symbol: ISS(1)

V_{DD}	Boosting	V_3 voltage	1/81 Duty		1/65 Duty		Unit	Remark
			Typ.	Max.	Typ.	Max.		
5V	Triple	14V	503	838	442	737	μA	*14
		10V	469	782	417	695		
3V	Quintuple	14V	684	1140	611	1018		
	Quadruple	10V	519	866	469	782		

*15 "Under heavy load conditions" indicates the state in which maximum current is consumed as a display pattern.

Display mode in binary at f_{FR}=75Hz, $V_{DD} = V_{DD2}$, No line reversion, 1/8 bias

Table 9.5 Display: entirely in white *14 Code: ISS (1)

V_{DD}	Boosting	V_3 voltage	1/81 Duty		1/65 Duty		Unit	Remark
			Typ.	Max.	Typ.	Max.		
5V	Triple	14V	308	514	290	484	μA	*13
		10V	302	504	285	474		
3V	Quintuple	14V	437	729	418	696		
	Quadruple	10V	350	584	333	555		

Table 9.6 Display: Heavy load display *15 Code: ISS (1)

V_{DD}	Boosting	V_3 voltage	1/81 Duty		1/65 Duty		Unit	Remark
			Typ.	Max.	Typ.	Max.		
5V	Triple	14V	360	601	331	552	μA	*14
		10V	340	567	314	524		
3V	Quintuple	14V	512	854	478	796		
	Quadruple	10V	395	658	369	615		

9.1.2 Current consumption under power saving mode (1)

V_{SS} = 0V, V_{DD} = 5.0V, V_{DIS} = HIGH, T_a = 25°C.

Table 9.7

Item	Symbol	Condition	Specified value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}	—	—	11	22	μA	—

9.1.3 Current consumption under power saving mode (2)

V_{SS} = 0V, V_{DD} = V_{DI} = 3.0V, V_{DIS} = LOW, T_a = 25°C.

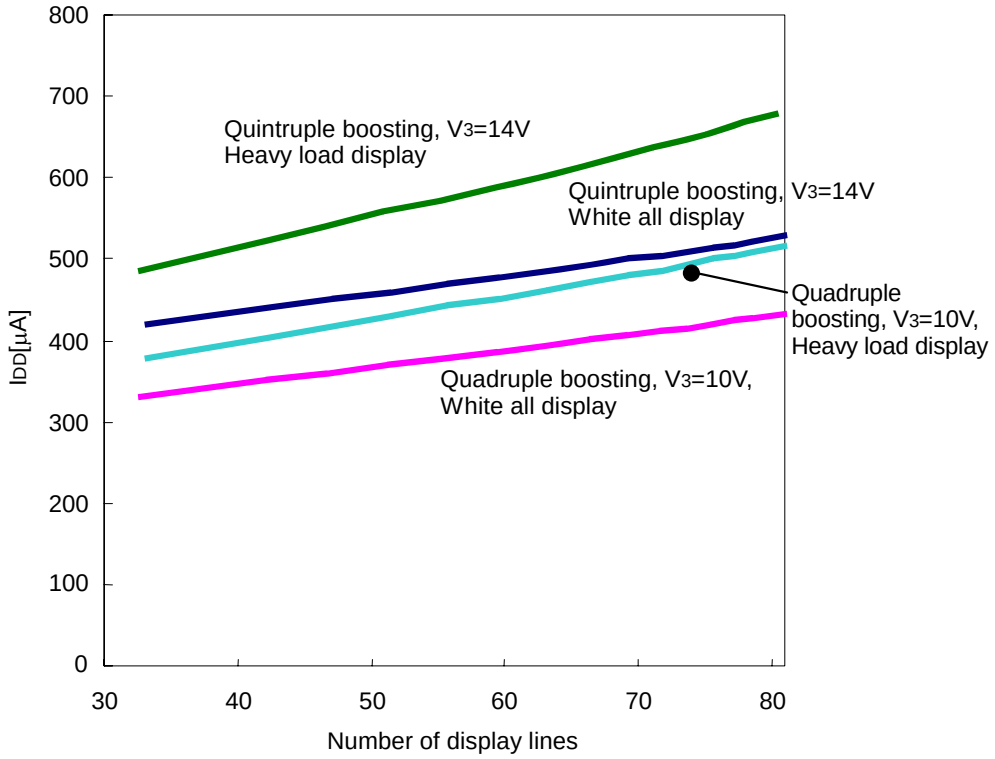
Table 9.8

Item	Symbol	Condition	Specified value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS2}	—	—	0.1	3	μA	—

9.1.4 Reference Data

- Dynamic current consumption When the LCD is indicating that the built in power supply is being used

$V_{DD} = V_{DD2} = 3.0V$, $f_{FR} = 144Hz$, internal oscillation circuit, 4-gray scale display, 1/8 bias



$V_{DD} = V_{DD2} = 5.0V$, $f_{FR} = 144Hz$, internal oscillation circuit, 4-gray scale display, 1/8 bias

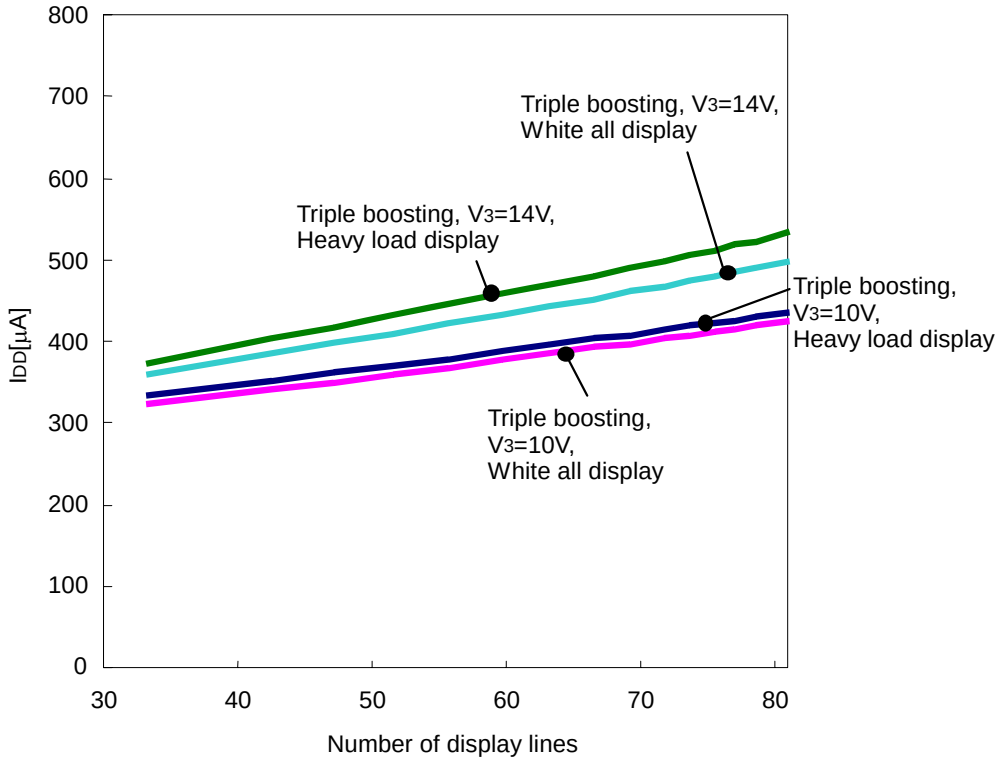
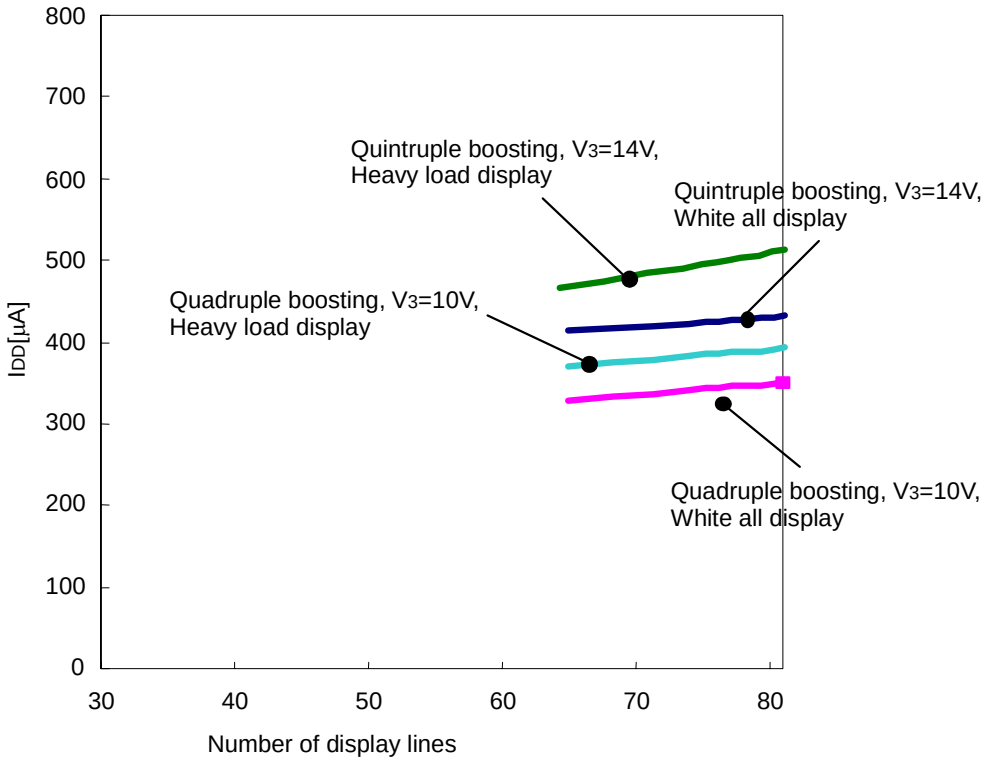


Fig.9.1

$V_{DD} = V_{DD2} = 3.0V$, $f_{FR} = 75Hz$, internal oscillation circuit, binary display, 1/8 bias



$V_{DD} = V_{DD2} = 5.0V$, $f_{FR} = 75Hz$, internal oscillation circuit, binary display, 1/8 bias

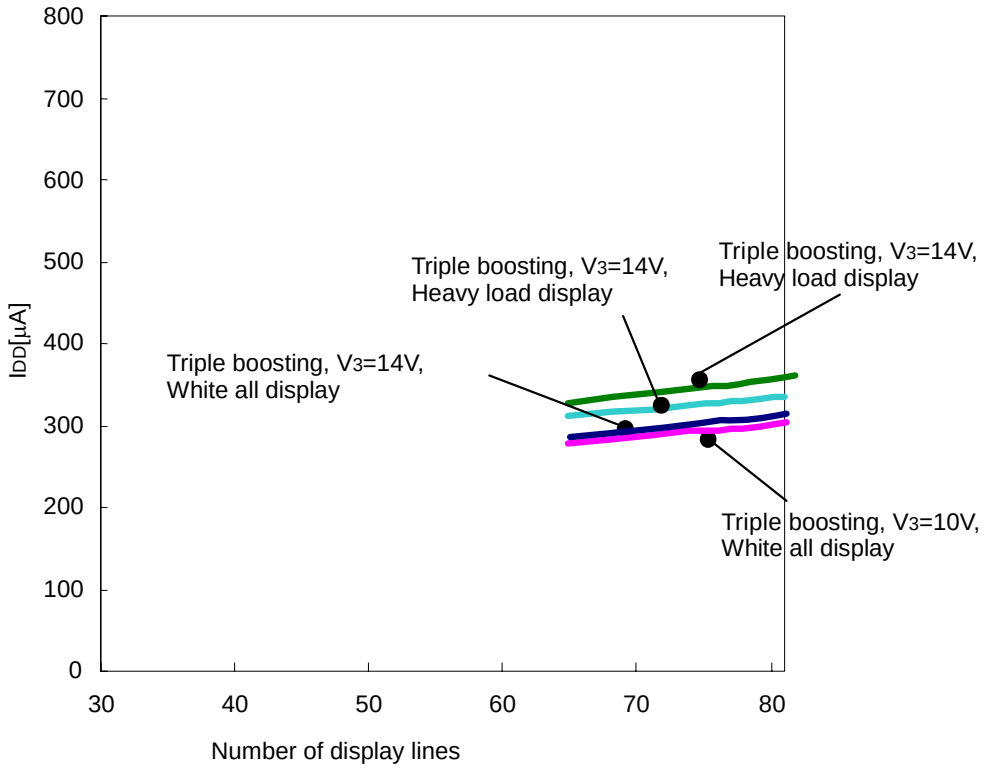


Fig.9.2

- Dynamic current consumption during access
  Indicates current consumption when the checker pattern pattern is written in f_{CYC}.

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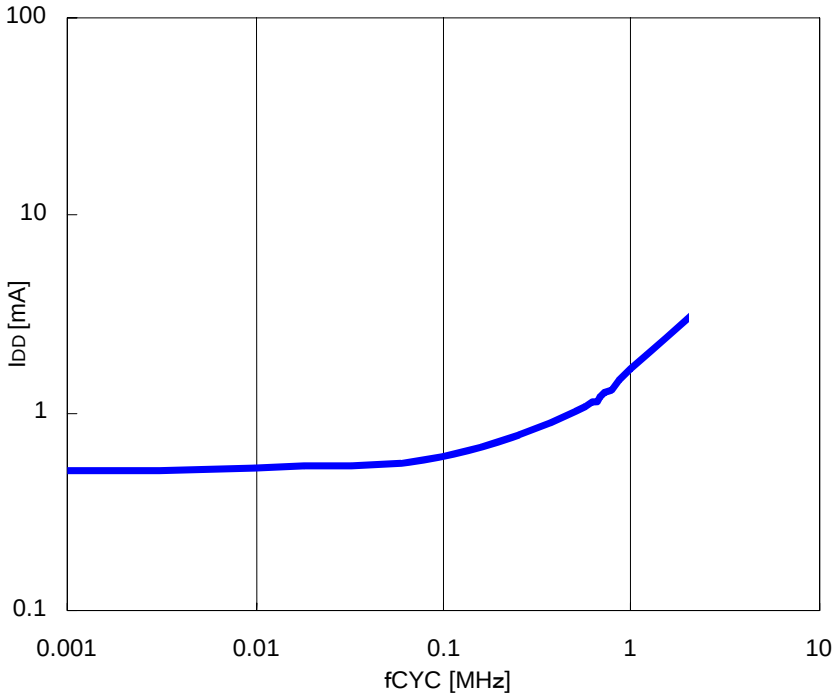

Conditions:
$V_{DD} = V_{DD2} = 5.0V$,
$V_3 = 14V$
When the external power supply is used

Fig.9.3

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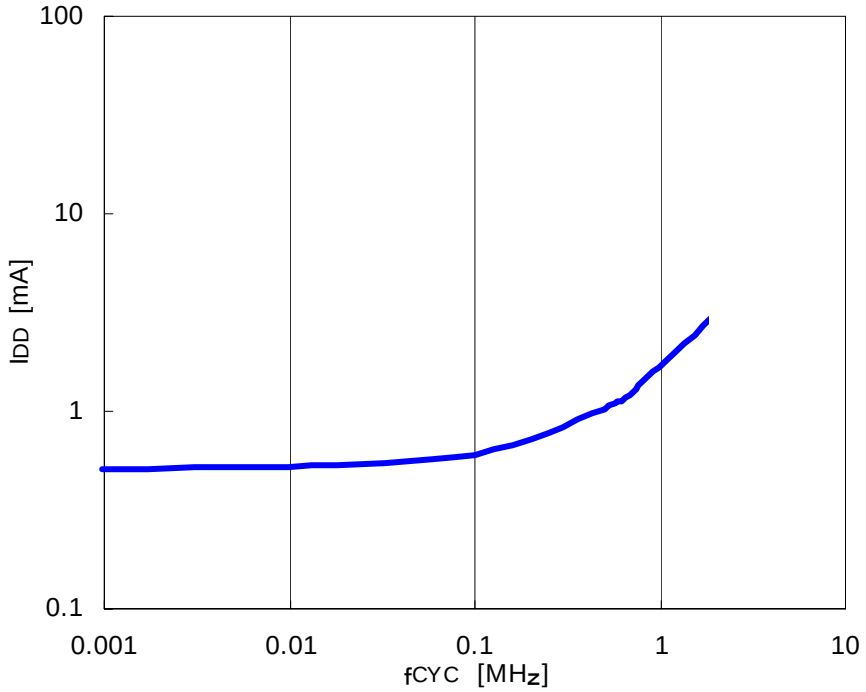

Conditions:
$V_{DD} = V_{DD2} = 5.0V$,
$V_3 = 14V$
When the external power supply is used

Fig.9.4

- Operating Voltage Rage of V_{DI} Series and V_3 Series

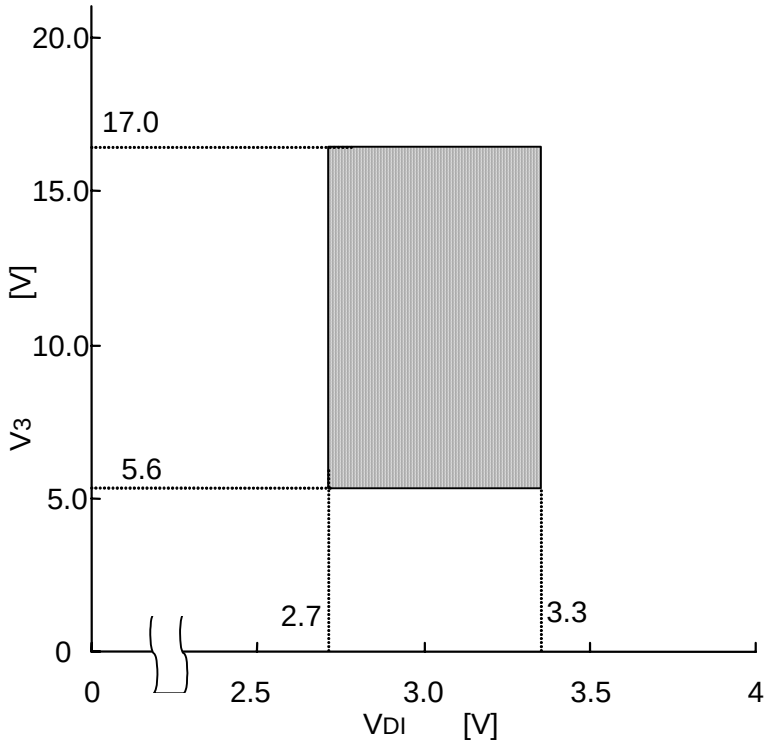

Fig.9.5

- Relationship between display line *I*, display clock frequency f_{CL} and liquid crystal frame f_{FR}

Table 9.9

Item	f_{CL}	f_{FR}
Built-in oscillator circuit used	See P.41	$\frac{f_{CL}}{(I+7)\times 24}$
External clock used	External input (f_{CL})	$\frac{f_{CL}}{(I+7)\times 24}$

9.2 Temperature sensor characteristics

Table 9.10

Item	Symbol	Condition	Standard value			Unit	Applicable pin
			Min.	Typ.	Max.		
Operating voltage range	V_{SV}		2.7		5.5	V	V_{DD}
Operating temperature range	Ta		-40		85	°C	
Temperature gradient	T_{ACCA}	-40～85°C	-5.0		5.0	°C	SV_{D2} *1, 2
Output voltage	V_{SVD2}	-40°C 25°C 85°C	1.472 1.176 0.887	1.496 1.200 0.911	1.520 1.224 0.935	V	SV_{D2} *1, 2
Output voltage temperature gradient	V_{GRA}	*2	—	-4.70	—	mV/°C	SV_{D2} *1, 2
Output voltage setup time	t_{SEN}		100	—	—	mS	SV_{D2} *1, 4
Operating current	I_{SEN}	25°C	—	10	30	μA	V_{DD}

[* Reference items]

*1 Please apply neither capacity nor the resistance load between V_{DD}, V_{DI}, V_{DD2} and terminal SV_{D2} of the output of an analog voltage of the sensor to obtain an accurate output voltage value.

*2 The typ. value of the sensor analog output voltage SVD2 when ambient temperature is Ta [°C] is approximated by the following expression.

It should be noted that (Expression 9-1) uses units of mV.

$$V_{SVD2}=-0.002\bullet Ta^2-4.590\bullet Ta+1316[mV] \qquad \text{(Expression 9-1)}$$

The sensor analog output voltage is output with accuracy of ±5°C of temperature conversion at -40 to 85°C.

*3 Approximate linear gradient of the V_{SVD2} output within the specified temperature range. Apply to all the operating temperature range.

Based on the temperature accuracy of ±5°C and temperature variation of the sensor analog voltage of -4.70mV/°C, the accuracy of the sensor analog output has variations of

$$\Delta V_{SVD2}=\pm\,(4.70\times 5)\cong\pm 24[mV]$$

when centering around the value determined by (Expression 9-1) at any ambient temperature Ta [°C]. The relationship between the accuracy of the sensor analog output and temperature is shown in Fig.9.6.

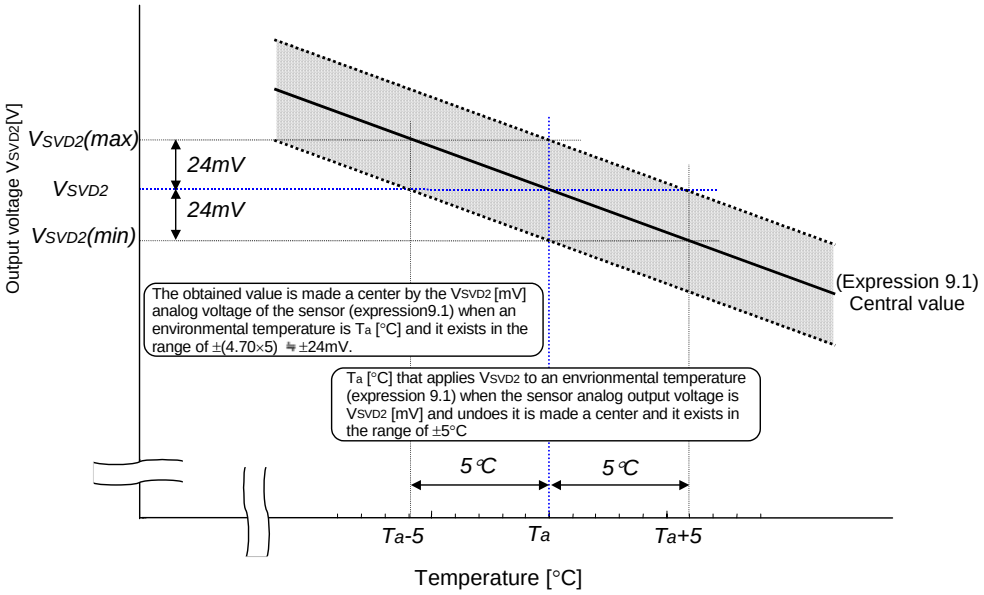

Fig.9.6

*4. The wait time after inputting the temperature sensor ON command until the output voltage can be monitored steadily. Apply when the capacity is not connected to the SVD2 pin. Be sure to sample the output voltage after a fixed wait time or longer.

10. TIMING CHARACTERICTICS

10.1 System bus read/write characteristics 1 (80 system MPU)

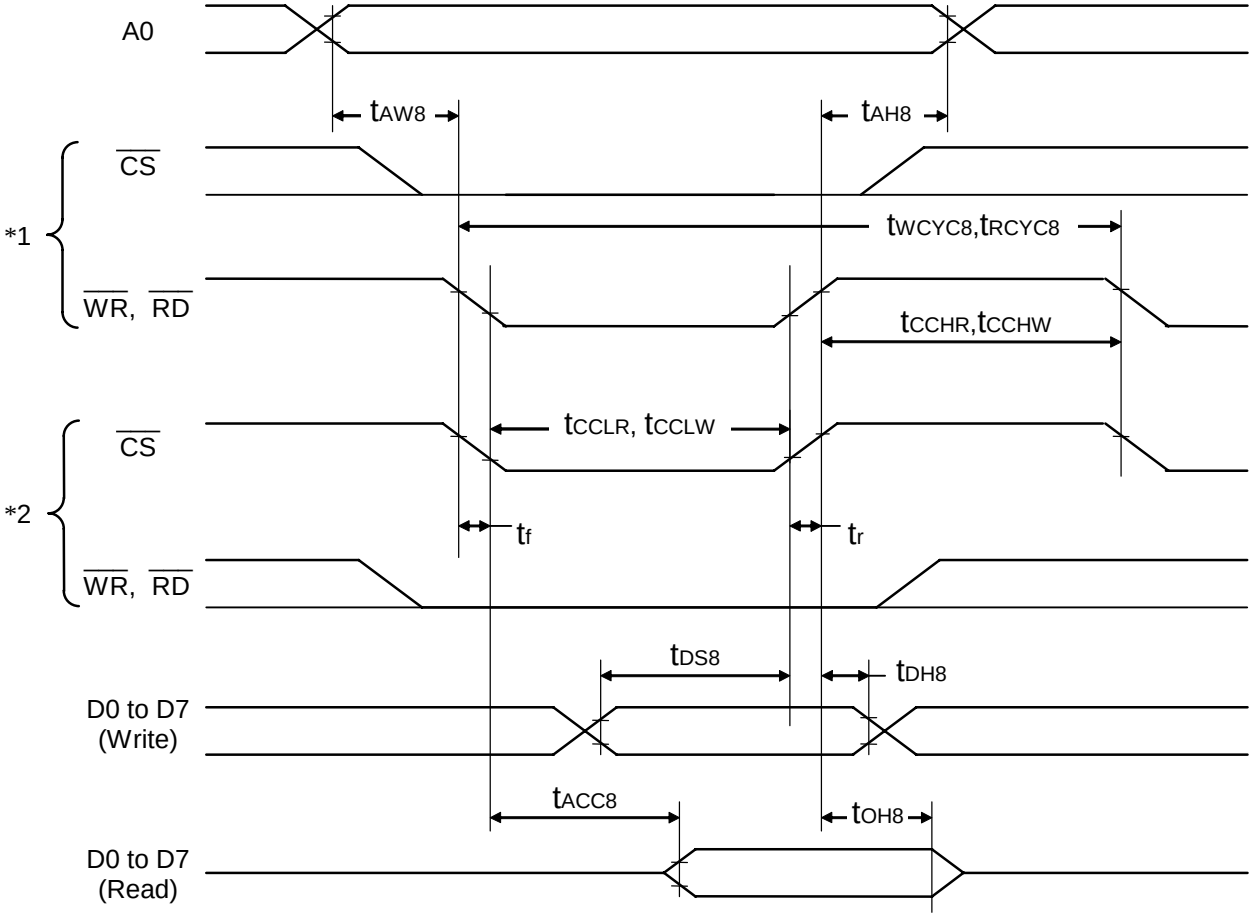

Fig.10.1

10. TIMING CHARACTERICTICS

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Table 10.1

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Item	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System write cycle time	$\overline{WR}$, $\overline{CS}$	t_{WCYC8}		500	—	
System read cycle time	$\overline{RD}$, $\overline{CS}$	t_{RCYC8}		3500	—	
Control Low-pulse width ($\overline{WR}$)	$\overline{WR}$, $\overline{CS}$	t_{CCLW}		200	—	
Control Low-pulse width ($\overline{RD}$)	$\overline{RD}$, $\overline{CS}$	t_{CCLR}		1500	—	
Control High-pulse width ($\overline{WR}$)	$\overline{WR}$, $\overline{CS}$	t_{CCHW}		200	—	
Control High-pulse width ($\overline{RD}$)	$\overline{RD}$, $\overline{CS}$	t_{CCHR}		200	—	
Data setup time	D0 to D7	t_{DS8}		200	—	
Data hold time ($\overline{WR}$)		t_{DH8}		15	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	1500	
Output disable time		t_{OH8}		5	200	

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Table 10.2

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Item	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		50	—	ns
Address setup time		t_{AW8}		0	—	
System write cycle time	$\overline{WR}$, $\overline{CS}$	t_{WCYC8}		1050	—	
System read cycle time	$\overline{RD}$, $\overline{CS}$	t_{RCYC8}		3700	—	
Control Low-pulse width ($\overline{WR}$)	$\overline{WR}$, $\overline{CS}$	t_{CCLW}		500	—	
Control Low-pulse width ($\overline{RD}$)	$\overline{RD}$, $\overline{CS}$	t_{CCLR}		2000	—	
Control High-pulse width ($\overline{WR}$)	$\overline{WR}$, $\overline{CS}$	t_{CCHW}		500	—	
Control High-pulse width ($\overline{RD}$)	$\overline{RD}$, $\overline{CS}$	t_{CCHR}		550	—	
Data setup time	D0 to D7	t_{DS8}		250	—	
Data hold time ($\overline{WR}$)		t_{DH8}		450	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	2000	
Output disable time		t_{OH8}		50	550	

*1. This is in case of making the access by $\overline{WR}$ and $\overline{RD}$, setting the $\overline{CS}$ = LOW.
*2. This is in case of making the access by $\overline{CS}$, setting the $\overline{WR}$, $\overline{RD}$ = LOW.
*3. Input signal rise and fall time (t_r, t_f) must not exceed 15ns. When the system cycle time is used at a high speed, it is specified by ($t_r + t_f$) ≤ ($t_{WCYC8} - t_{CCLW} - t_{CCHW}$) or ($t_r + t_f$) ≤ ($t_{RCYC8} - t_{CCLR} - t_{CCHR}$)
*4. Timing is entirely specified with reference to 20% or 80% of V_{DD}.
*5. t_{CCLW} and t_{CCLR} are specified in terms of the overlapped period when $\overline{CS}$ is at LOW level and $\overline{WR}$ and $\overline{RD}$ are at LOW level.

10.2 System bus read/write characteristics 2 (68 system MPU)

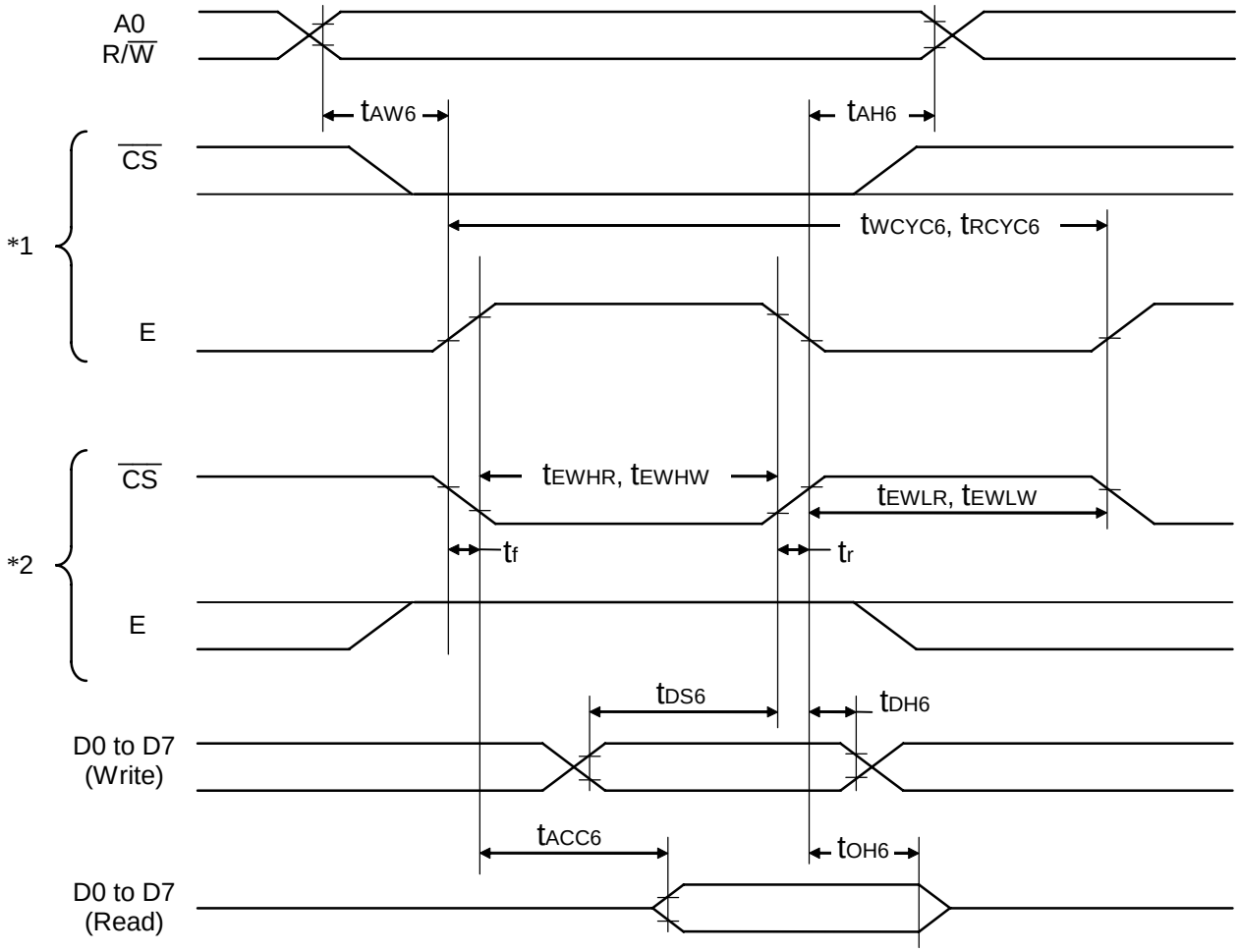

Fig.10.2

10. TIMING CHARACTERICTICS

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Table 10.3

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Item		Signal	Symbol	Condition	Specified value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System write cycle time		E, $\overline{CS}$	t_{WCYC6}		500	—	
System read cycle time		E, $\overline{CS}$	t_{RCYC6}		3500	—	
Data setup time		D0 to D7	t_{DS6}		200	—	
Data hold time (E)			t_{DH6}		30	—	
Access time			t_{ACC6}	C_L=100pF	—	1500	
Output disable time			t_{OH6}		5	200	
Enable HIGH-pulse width	Read	E, $\overline{CS}$	t_{EWHR}		1500	—	
	Write	E, $\overline{CS}$	t_{EWHW}		200	—	
Enable LOW-pulse width	Read	E, $\overline{CS}$	t_{EWLR}		200	—	
	Write	E, $\overline{CS}$	t_{EWLW}		200	—	

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Table 10.4

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Item		Signal	Symbol	Condition	Specified value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		50	—	ns
Address setup time			t_{AW6}		0	—	
System write cycle time		E, $\overline{CS}$	t_{WCYC6}		1050	—	
System read cycle time		E, $\overline{CS}$	t_{RCYC6}		3700	—	
Data setup time		D0 to D7	t_{DS6}		250	—	
Data hold time (E)			t_{DH6}		450	—	
Access time			t_{ACC6}	C_L=100pF	—	1500	
Output disable time			t_{OH6}		50	500	
Enable HIGH-pulse width	Read	E, $\overline{CS}$	t_{EWHR}		2000	—	
	Write	E, $\overline{CS}$	t_{EWHW}		500	—	
Enable LOW-pulse width	Read	E, $\overline{CS}$	t_{EWLR}		550	—	
	Write	E, $\overline{CS}$	t_{EWLW}		500	—	

*1. This is in case of making the access by E, setting the $\overline{CS}$ = LOW.
*2. This is in case of making the access by $\overline{CS}$, setting the E = HIGH.
*3. The rise time and the fall time (t_r & t_f) of the input signals should be set to 15ns or less. When it is necessary to use the system cycle time at high speed, the rise time and the fall time should be so set to conform to $(t_r + t_f) \leq (t_{WCYC6} - t_{EWLW} - t_{EWHW})$ or $(t_r + t_f) \leq (t_{RCYC6} - t_{EWLR} - t_{EWHR})$
*4. All the timing should basically be set to 20% or 80% of the V_{DD}.
*5. t_{EWLW}, t_{EWLR} should be set to the overlapping zone where the $\overline{CS}$ is on the LOW level and where the E is on the HIGH level.

10.3 Serial Interface

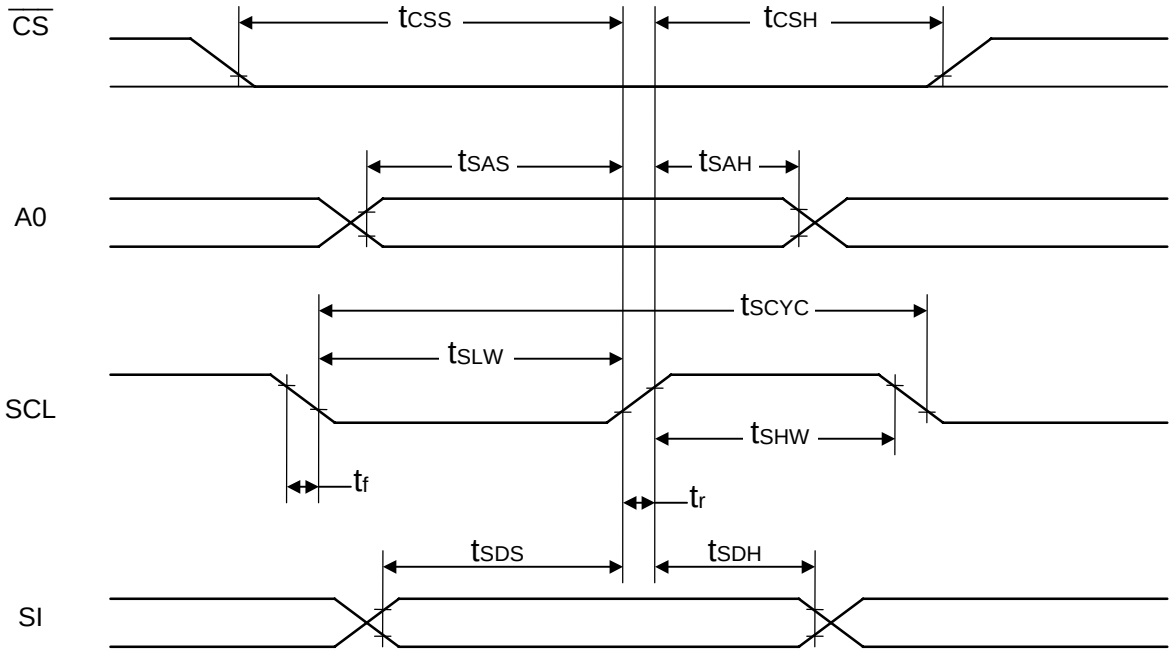

Fig.10.3

10. TIMING CHARACTERICTICS

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Table 10.5

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified		Unit
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}		250	—	ns
SCL HIGH pulse width		t_{SHW}		100	—	
SCL LOW pulse width		t_{SLW}		100	—	
Address setup time	A0	t_{SAS}		150	—	
Address hold time		t_{SAH}		150	—	
Data setup time	SI	t_{SDS}		100	—	
Data hold time		t_{SDH}		100	—	
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}		150	—	
		t_{CSH}		150	—	

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Table 10.6

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified		Unit
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}		750	—	ns
SCL HIGH pulse width		t_{SHW}		350	—	
SCL LOW pulse width		t_{SLW}		350	—	
Address setup time	A0	t_{SAS}		200	—	
Address hold time		t_{SAH}		200	—	
Data setup time	SI	t_{SDS}		200	—	
Data hold time		t_{SDH}		200	—	
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}		200	—	
		t_{CSH}		200	—	

*1. Input signal rise and fall time (t_r, t_f) must not exceed 15ns.
*2. Timing is entirely specified with reference to 20% or 80% of V_{DD}.

10.4 Display Control Input and Output Timing

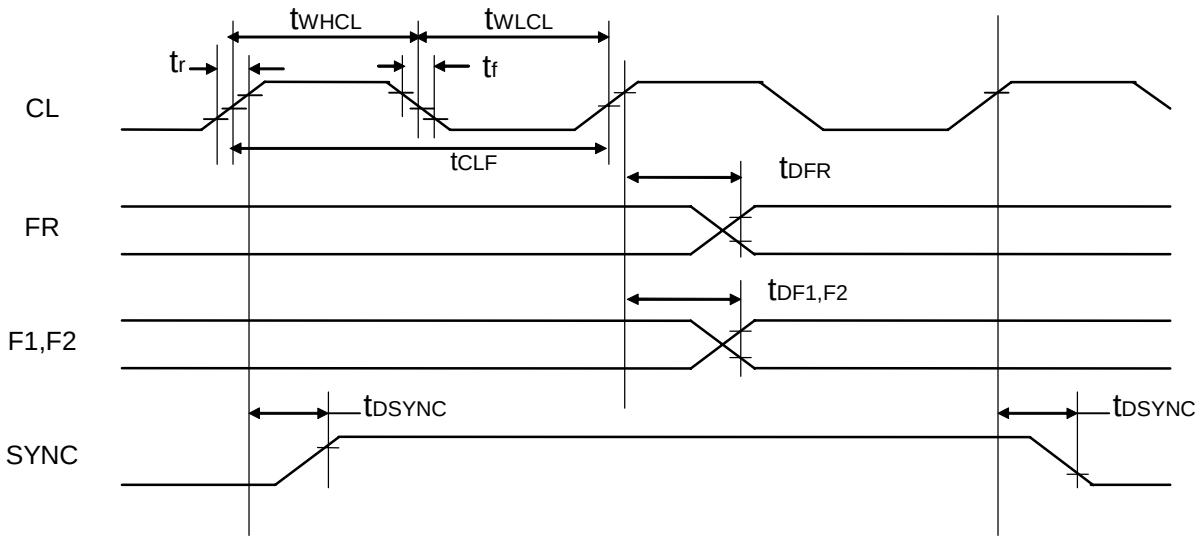

Fig.10.4

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Table 10.7 Output Timing (When built-in oscillator is used)

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	-0.5	—	0.5	ns
F1,F2 delay time	F1,F2	t_{DF1}, t_{F2}		-0.5	—	0.5	ns
SYNC delay time	SYNC	t_{DSYNC}		-0.5	—	0.5	ns

Table 10.8 Output Timing (When external clock is used)

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	-0.5	—	0.5	ns
F1,F2 delay time	F1,F2	t_{DF1}, t_{F2}		-0.5	—	0.5	ns
SYNC delay time	SYNC	t_{DSYNC}		-0.5	—	0.5	ns

Table 10.9 Input Timing

[V_{DD}=2.7V to 5.5V, T_a= -40 to 85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}		-1.0	—	1.0	µs
F1 and F2 delay time	F1,F2	$t_{DF1,F2}$		-1.0	—	1.0	µs
SYNC delay time	SYNC	t_{DSYNC}		-1.0	—	1.0	µs
Input clock duty ratio *3	CL	t_{CLD}		20	—	80	%
Input clock rise time (20% to 80%) *4		tr		—	—	15	ns
Input clock fall time (20% to 80%) *4		tf		—	—	15	Ns
Input clock cycle (1)		t_{CLF}	When single chip driving	2	—	—	µs
Low-level pulse width (1)		t_{WLCL}		0.4	—	—	µs
High-level pulse width (1)		t_{WHCL}		0.4	—	—	µs
Input clock cycle (2)		t_{CLF}	When master/slave configulation	—	—	—	µs
Low-level pulse width (2)		t_{WLCL}		0.4	—	—	µs
High-level pulse width (2)		t_{WHCL}		0.4	—	—	µs

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Table 10.10 Output Timing (When built-in oscillator is used)

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	-0.7	—	0.1	ns
F1,F2 delay time	F1,F2	t_{DF1}, t_{F2}		-0.7	—	0.1	ns
SYNC delay time	SYNC	t_{DSYNC}		-0.7	—	0.1	ns

Table 10.11 Output Timing (When external clock is used)

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	-0.1	—	0.7	ns
F1,F2 delay time	F1,F2	t_{DF1}, t_{F2}		-0.1	—	0.7	ns
SYNC delay time	SYNC	t_{DSYNC}		-0.1	—	0.7	ns

Table 10.12 Input Timing

[V_{DD}=2.7V to 5.5V, T_a= -40 to 95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}		-1.0	—	1.0	µs
F1 and F2 delay time	F1,F2	$t_{DF1,F2}$		-1.0	—	1.0	µs
SYNC delay time	SYNC	t_{DSYNC}		-1.0	—	1.0	µs
Input clock duty ratio *3	CL	t_{CLD}		20	—	80	%
Input clock rise time (20% to 80%) *4		tr		—	—	15	ns
Input clock fall time (20% to 80%) *4		tf		—	—	15	ns
Input clock cycle (1)		t_{CLF}	When single chip driving	2	—	—	µs
Low-level pulse width (1)		t_{WLCL}		0.4	—	—	µs
High-level pulse width (1)		t_{WHCL}		0.4	—	—	µs
Input clock cycle (2)		t_{CLF}	When master/slave configulation	2.8	—	—	µs
Low-level pulse width (2)		t_{WLCL}		1.4	—	—	µs
High-level pulse width (2)		t_{WHCL}		1.4	—	—	µs

*1. t_{CLF}, t_{WLCL}, t_{WHCL} are specified with reference to 50% of V_{DD}.

*2. Timing is entirely specified with reference to 20% or 80% of V_{DD}. Input and output voltage of CL is between V_{DD} and V_{SS} and then of F1, F2 and SYNC are between V_{DI} and V_{SS}, except t_{CLF}, t_{WLCL}, t_{WHCL}.

*3. CL duty ratio is defined as $t_{CLD} = \frac{t_{WHCL}}{t_{CLF}} \times 100[\%]$ or $t_{CLD} = \frac{t_{WLCL}}{t_{CLF}} \times 100[\%]$.

*4. If the timing is not specified, it is required to keep t_{CLF}, t_{WLCL}, t_{WHCL}.

10.5 Reset Input timing

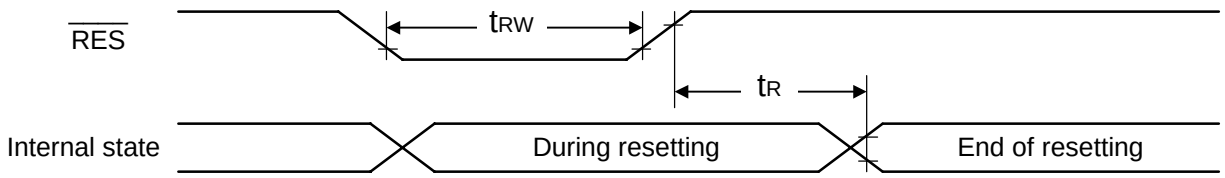

Fig.10.5

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Table 10.13

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
Reset time	—	t_R	—	—	—	1	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1	—	—	

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Table 10.14

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
Reset time	—	t_R	—	—	—	1	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1	—	—	

*1. Timing is entirely specified with reference to 20% and 80% of V_{DD}.

10.6 Temperature Sensor Measuring Timing

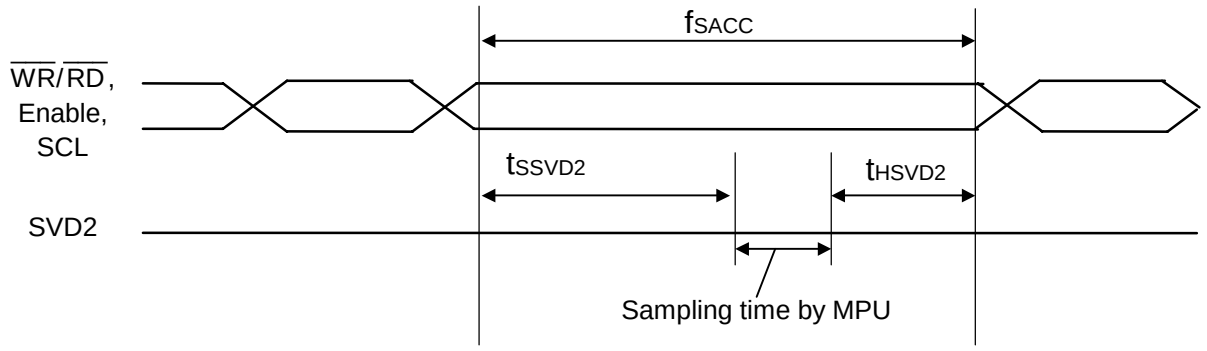

Table 10.15

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
MPU access cycle	$\overline{WR}$/$\overline{RD}$ (80 series MPU) Enable (68 series MPU) SCL (Serial Interface)	f_{SACC}	—	—	—	0	Hz
Sampling setup time	SV_{D2}	t_{SSVD2}		1	—	—	ms
Sampling hold time	SV_{D2}	t_{HSVD2}		0	—	—	ms

*1. While detecting outputs from SV_{D2}, stop access from the MPU (input from the $\overline{WR}$ or $\overline{RD}$ pin when the 80 series MPU is used, input from Enable pin when the 68 series MPU is used, input from SCL pin when the serial interface is used).

*2. Waiting time after stopping access from MPU and until SV_{D2} comes to be sampled.. This applies when the temperature sensor circuit has been turned on. When turning on the temperature sensor circuit after stopping access from MPU, secure the specified output voltage setup time.

*3. Waiting time after finish of SV_{D2} sampling by MPU and until MPU access can start.

11. MPU INTERFACE (Reference Example)

The S1D15721 Series can be connected to the 80 series MPU and 68 series MPU. Use of a serial interface allows operation with a smaller number of signal lines.

You can expand the display area using the S1D15721 Series as a multi-chip. In this case, the IC to be accesses can be selected individually by the chip select signal. After initialization by the $\overline{RES}$ pin, each input terminal of the S1D15721 Series must be placed under normal control.

(1) 80 series MPU

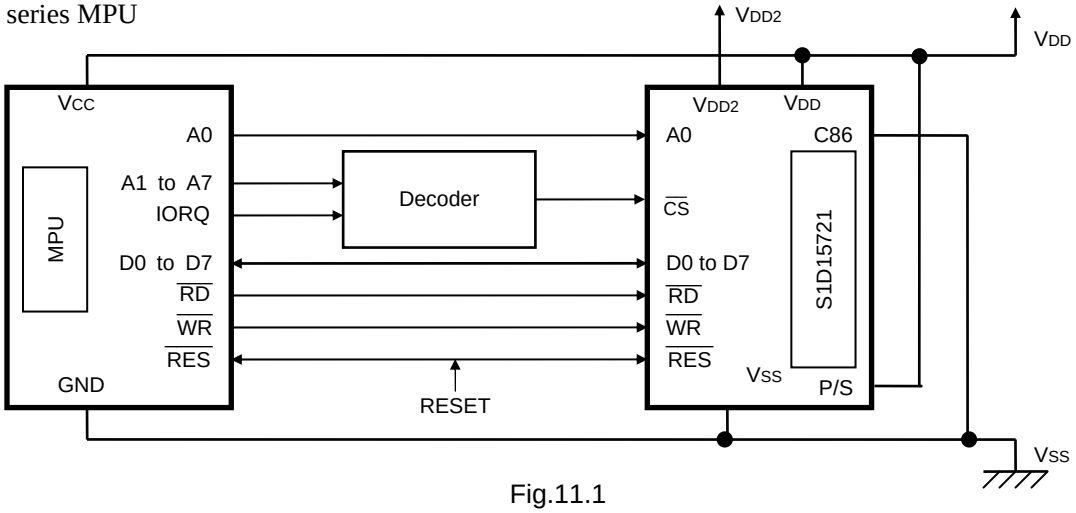

Fig.11.1

(2) 68 series MPU

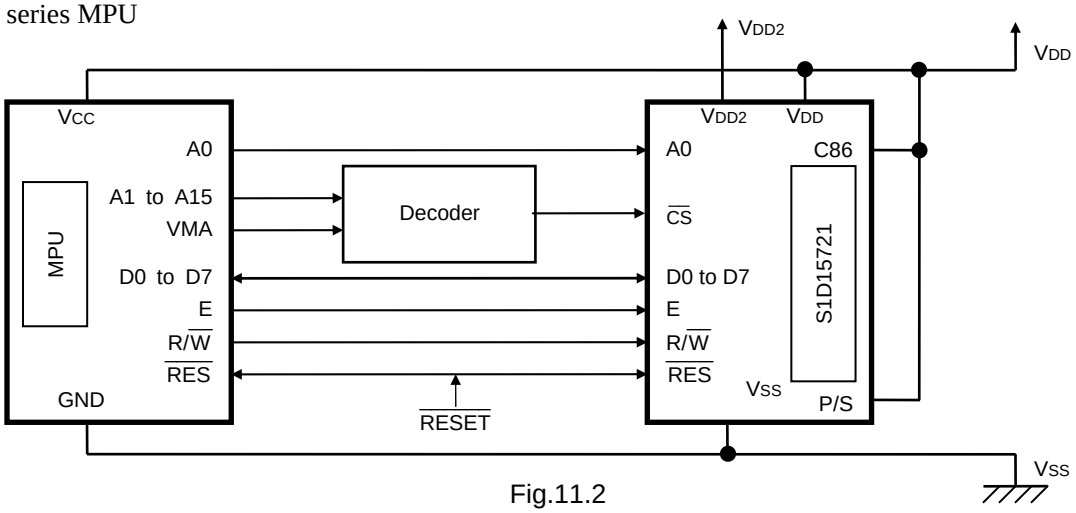

Fig.11.2

(3) Serial interface

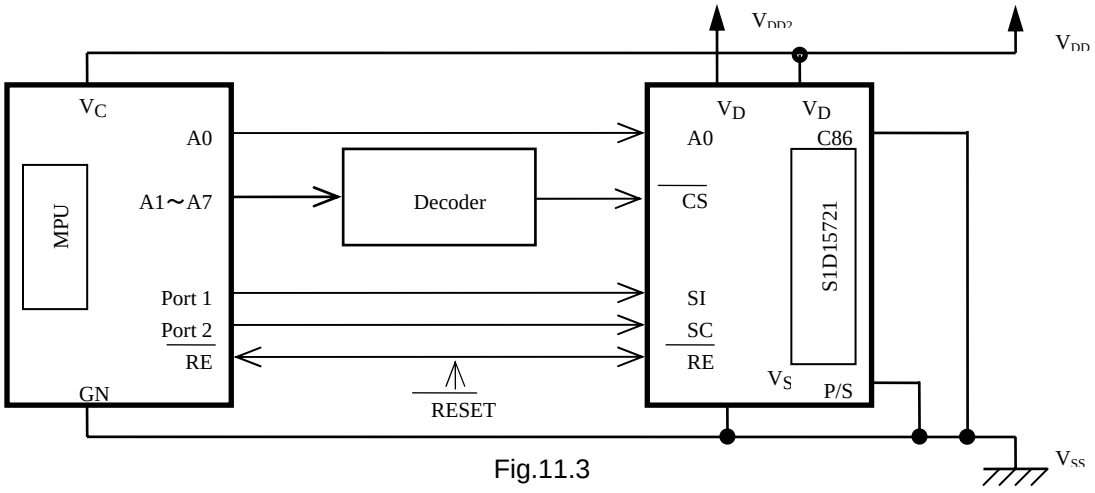

Fig.11.3

12. CONNECTION BETWEEN LCD DRIVERS (Reference Example)

You can easily expand the liquid crystal display area using the S1D15721 Series as a multi-chip. In this case, use the same model (S1D15721/S1D15721) as the master and slave systems.

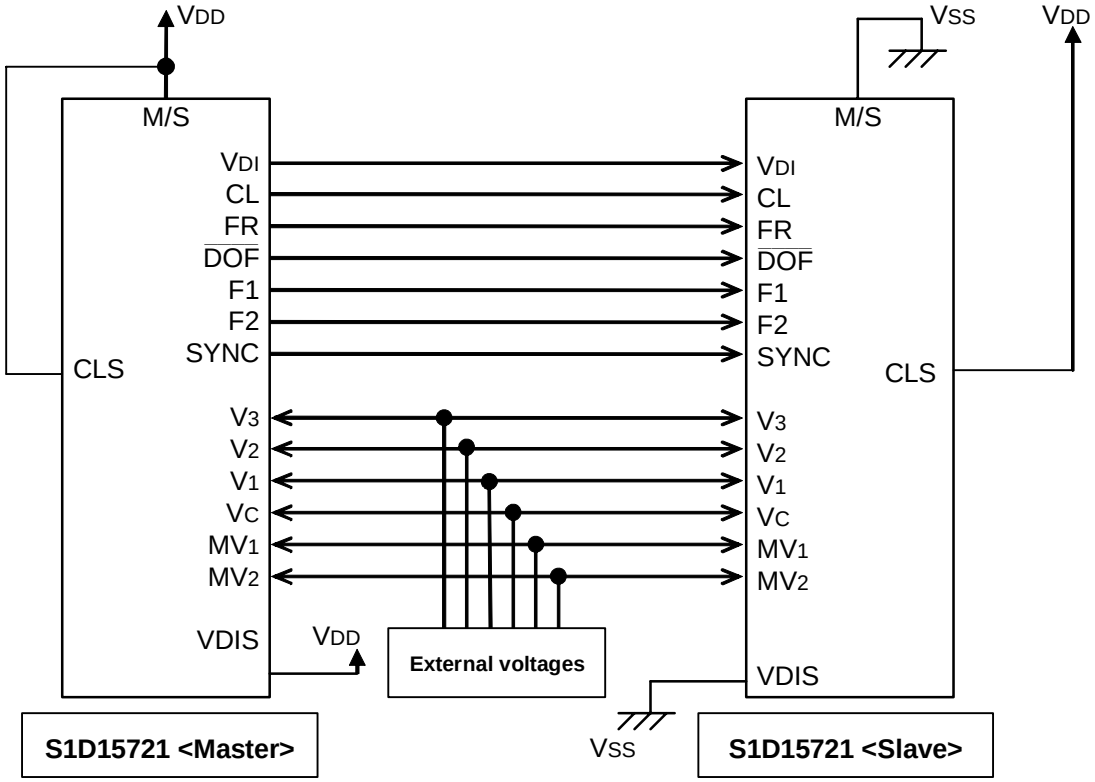

Fig.12.1 Master/slave connection example (Built-in oscillator Is used)

12. CONNECTION BETWEEN LCD DRIVERS (Reference Example)

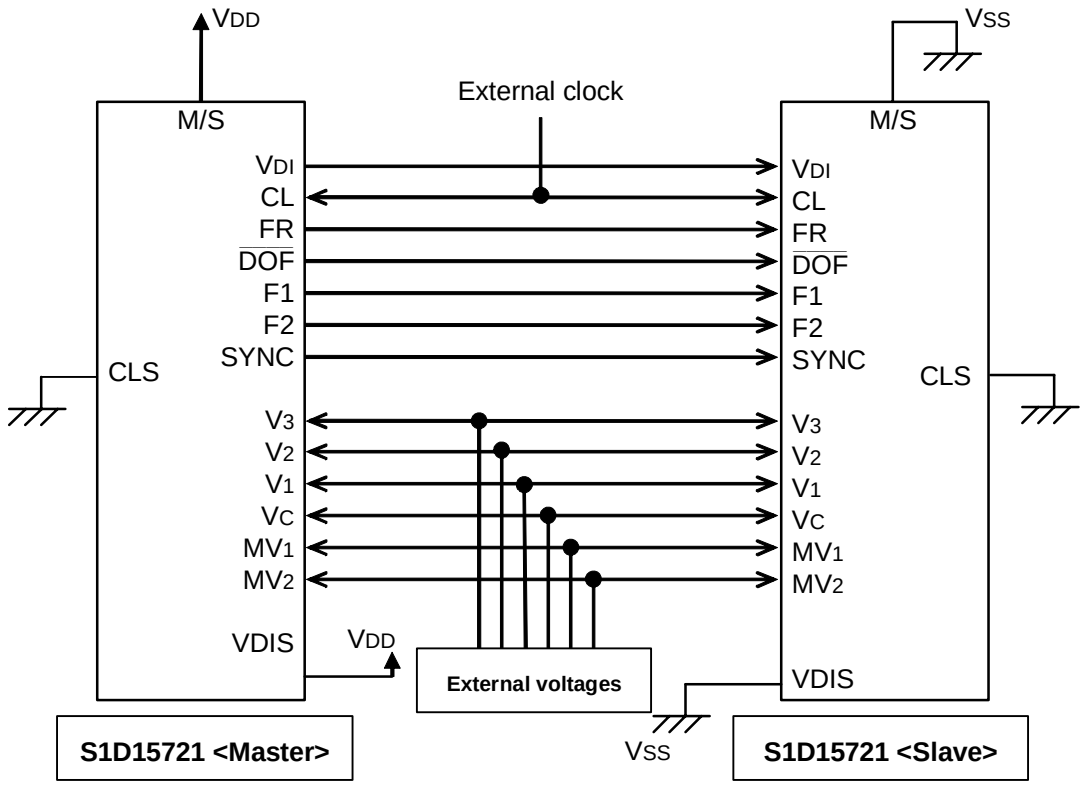

Fig.12.2 Master/slave connection example (External clock is used)

・When Built-in VDI generating circuit is not used.
In this case, VDIS of both master and slave are set to LOW, and common VDI voltage is supplied externally.

Another way is that both VDIs connect together with VDIS of both chips set to HIGH. It is recommended in case to be concerned power line swinging by big panel load, high wiring resistance, high speed MPU accessing etc.

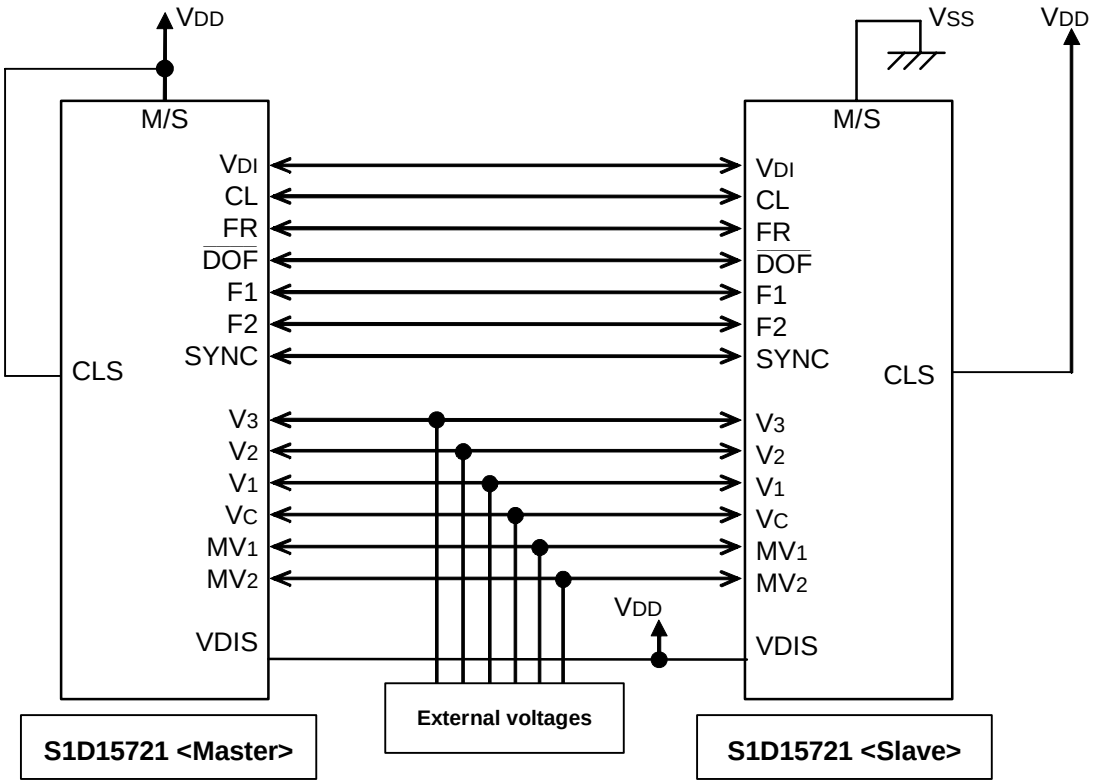

Fig.12.3 Master/slave connection example 3 (Built-in oscillator is used)

・When Master/slave configuration is used.

It is recommend to supply LCD Bias voltages externally. To supply LCD bias voltages of Master chip to slave chip is also possible. In this case built-in power circuit of slave side should be OFF.

There are following concerns in the case;

- Contrast difference between master side display and slave side display due to voltage drop of V3 to MV2 from wiring resistance.
- Slave side power consumpsion add to master side power consumption, therefore synchronizing signals may have noise and timing error may occur.

So that it is recommend to evaluate well and carefully in case with built-in power circuit in master/slave configuration

13. LCD PANEL WIRING (Reference Example)

You can easily expand the liquid crystal display area using the S1D15721 Series as a multi-chip. In the case of multi-chip configuration, use the same models.

(1) Single chip configuration example

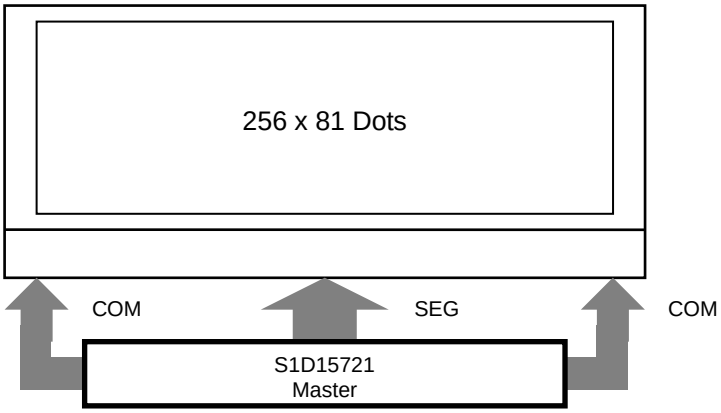

Fig.13.1 Single chip configuration example

(2) Double chip configuration example

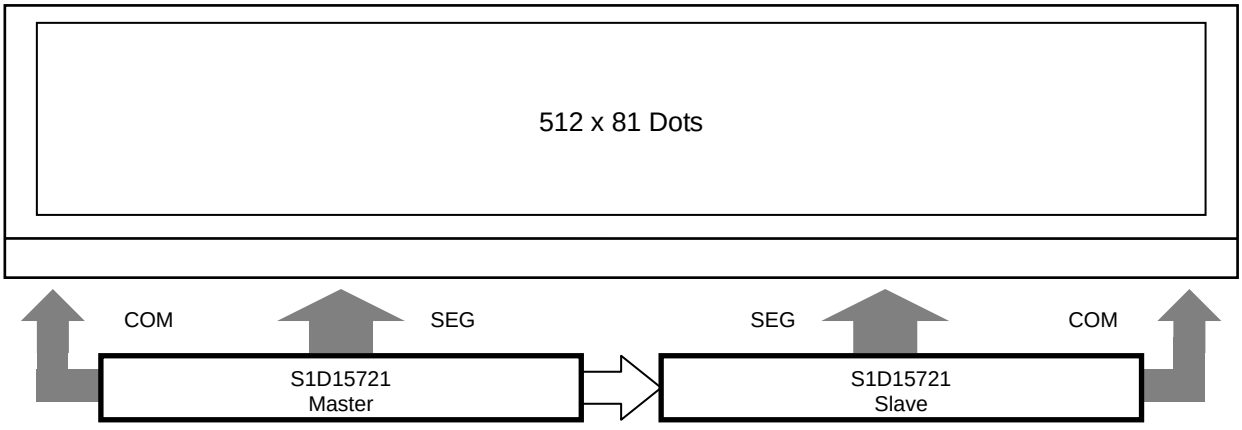

Fig.13.2 Double chip configuration example

14. CAUTIONS

Cautions must be exercised on the following points when using this Development Specification:

1. This Development Specification is subject to change for engineering improvement.
2. This development specification does not grant or guarantee you to exercise and/or use patents and/or other intellectual property rights held by a third party or SEIKO EPSON.
   The applications in this development specification are given in order to provide an understanding of our products. It should be noted that we are not liable for any circuit problems that may occur when using them.
   "Large" or "Small" in the characteristics table in this development specification refers to the relationship on a numbered line.
3. Reproduction or copy of any part or whole of this Development Specification without permission of our company, or use thereof for other business purposes is strictly prohibited.

For the use of the semi-conductor, cautions must be exercised on the following points:

[Cautions against Light]

The semiconductor will be subject to changes in characteristics when light is applied. If this IC is exposed to light, operation error may occur. To protect the IC against light, the following points should be noted regarding the substrate or product where this IC is mounted:

(1) Designing and mounting must be provided to get a structure which ensures a sufficient resistance of the IC to light in practical use.
(2) In the inspection process, environmental configuration must be provided to ensure a sufficient resistance of the IC to light.
(3) Means must be taken to ensure resistance to light on all the surfaces, backs and sides of the IC.

REVISION HISTORY

Rev.1.0

Page	Type	Description
ALL	New	New enactment

Rev.2.0

Page	Type	Description
P2	Add	In 2. features, add new model S1D15721D01B000
P4	Add	In 4.1 Chip assignment, add new model S1D15721D01B000 and die numbers.
P9	Add	In 5.1 Power pin, add descdription in V_{DI} pin when using master / slave configulation.
P12	Add	In 5.3 System Bus Connection Pin, add description of CL pin in case of external clock is used.
P21	Add	In 6.3 Oscillator circuit, add description of CL pin in case of external clock is used.
P23	Add	In 6.6 power circuit, add description during slave operation.
P30	Add	In 6.7 Examples of the peripheral circuits of the power circuit, add description “Non-polarity capacitances can be applicable.
P33	Correct	In 6.9.2 Precautions, correct number of figure (fig.6-15 to fig. 6-14)
P34	Correct	In 6.10 Reset circuit, correct “25 power save ON” to “25 power save OFF”.
P42	Add	In (16) Display Line Nubmer Set, in start point(block) register set parameter, add description in case of “common output status select” = Reverse)
P45	Add	In (21) Power control set, add description in case to stop built-in oscillaotor.
P48	Add	In (26) Power saving, add description in case of using external clock.
P49	Add	In (27) Temperature Gradient Set and (28) Status Read, add “for reference” at the values.
P54	Correct	In 7.3.1 initial setup, correct followings. - Command number of V3 adjust voltage from (23) to (22) - Add (29) Temperature sensor ON/OFF
P56	Add	In 7.3.3 Power OFF, - Add sequence of external clock is stopped - Add Note *13) in case of using external clock.
P57,58	Add Change	In 7.3.4 Change the Number of Line. -Add sequence in case of external clock and external LCD voltages. -Change Number of Note.
P58	Add	In 7.3.5 Refresh, add 3 commands.
P59	Add	In 8. Absolute Maximum Ratings, add new model S1D15721D01B000, and add description in Notes 2.
P60	Add	In 9.1 DC Characteristics, add new model S1D15721D01B. And devide description of interface voltages to V_{DD} system and V_{DI} system.
P62	Expand	In table 9-2, expand input voltages.
P62 P63	Correct	In 9.1.1 Dynamic current consumption value, correct values. (Typo) (Value of VDD=5V, Triple boosting, V3=14V <-> VDD=3V, Quintuple, 14V) (Value of VDD=5V, Triple boosting, V3=10V <-> VDD=3V, Quadruple, 10V)
P65	Correct	In 9.1.4 Reference Data, correct following descriptions. (Typo) - Upper side of Fig.9.2, “Triple boosting, V3=10V, Heavy load display” correct to “Quadruple boosting, V3=10V, Heavy load display”, and “Triple boosting, V3=10V, White all display” correct to “Quadruple boosting, V3=10V, White all display”. - Lower side of Fig.9.2, “Quintruple boosting, V3=14V, White all display” correct to “Triple boosting, V3=14V, White all display”
P67	Add	In Dynamic current consumption during access, add fig of new model S1D15721D01B.

Page	Type	Description
P69	Correct	In 9.2 Temperature sensor characteristics, change number of note in tSEN from “*1,3” to “*1,4”. Correct number of figure, from “Fig 9.7” to “Fig. 9.6”.
P71 to 81	Add	In 10 Timing characteristics, add characteristics of new model S1D15721D01B000. Correct “t_{CYC8}” to“t_{WCYC8}”, “t_{RCYC8}” and correct “t_{CYC6}” to“t_{WCYC6}”, “t_{RCYC6}”.
P77	Change	In 10-4 Display Control Input and Outpit Timing, change definition of timings in timing chart (Fig. 10.4)
P79	Add	In Table 10.12 devide timing characteristics to single chip usage and master/slave configulation usage. Add note *1) and *4). Add description in note *2)
P83 to 84	Add	In 12 Connection between LCD Drivers (Reference Example), add Figure(Fig 12.2) in case of external clock is used. Add descriptions in case of “Built-in VDI generating circuit is not used” and “When master slave configulation is used.”

Rev.2.1

Page	Type	Description
P.2 P.59 P.60	Expand	Expand boosting power supply VDD2 range. In 2. Features, change boosting power supply VDD2-VSS from “VDD to 5.5V” to “VDI to 5.5V”. In 8. Absolute maximum rating, change power voltage (2) VDD2 from “VDD to +6.0” to “VDI to +6.0”. In 9.1 DC Characteristics, change operating voltage (2) VDD2 from “VDD” to “VDI”.
P.9	Delete and Add	5.1 Power Pin, in VDI description, delete comment"To use this IC on master/slave, use each VDI power independently." And add comment of "Another way is that both VDIs connect together with VDIS of both chips set to HIGH. It is recommended in case to be concerned power line swinging by big panel load, high wiring resistance, high speed MPU accessing etc."
P55	Add	In 7.3.2 Data display, at note, add comment <All area which is set by "(5) Display start line set" and"(16) Display Line Number Set" command, and Page20 (correspond to COMS)>
P83 to 85	Change, Add	In 12. CONNECTION BETWEEN LCD DRIVERS, change figures with external voltages to V3 to MV2, and add fig.12.3. Add caution in case with built-in power circuit in master/slave configuration.

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