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S1D13506 LCD/CRT/TV Controller

S5U13506P00C100 PCI Evaluation Board User Manual

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1 Introduction

This manual describes the setup and operation of the S5U13505P00C100 PCI Evaluation Board. The S5U13506P00C100 is designed as an evaluation platform for the S1D13506 Color LCD/CRT/TV Controller chip.

This document is updated as appropriate. Please check the Epson Research and Development website at http://www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Features

The S5U13506P00C100 features the following:

- S1D13506 Color LCD/CRT/TV controller chip
- PCI bus operation using on-board PCI bridge
- Headers for connecting to a 3.3V host bus interface (5V host bus interface also possible with modifications to the board)
- 1Mx16 EDO DRAM
- Configuration options
- Headers for S1D13506 current consumption measurements
- 4/8-bit 3.3V or 5V monochrome passive LCD panel support
- 4/8/16-bit 3.3V or 5V color passive LCD panel support
- 9/12/18-bit 3.3V or 5V TFT/D-TFD LCD panel support
- Embedded RAMDAC for CRT and TV support
- Software initiated Power Save Mode

3 Installation and Configuration

The S5U13506P00C100 is designed to support as many platforms as possible. The board incorporates a DIP switch and several jumpers which allow both evaluation board and S1D13506 LCD controller settings to be configured for a specified evaluation platform.

3.1 Configuration DIP Switches

The S1D13506 LCD controller has 16 configuration inputs (MD[15:0]) which are read on the rising edge of RESET#. Where appropriate, the S5U13506P00C100 hard-wires some of these configuration inputs, but in order to configure the S1D13505 for multiple host bus interfaces an eight-position DIP switch is required. The following figure shows the location of DIP switch S1 on the S5U13506P00C100 board.

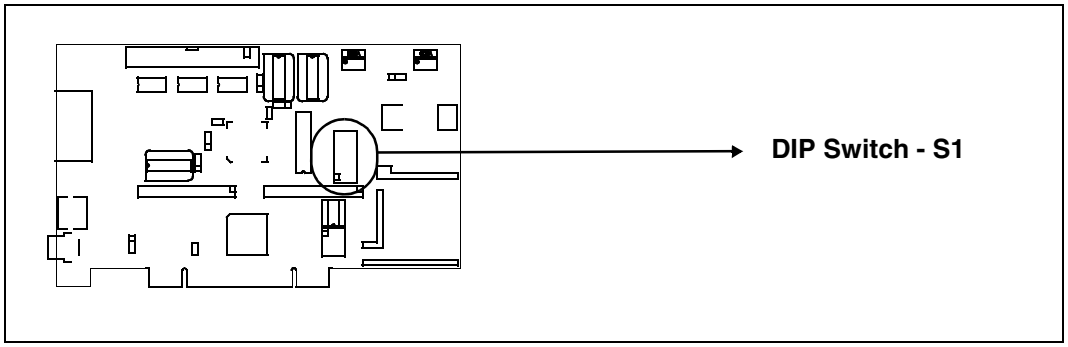

Figure 3-1: Configuration DIP Switch (S1) Location

The following DIP switch settings configure the S1D13506.

Table 3-1: Configuration DIP Switch Settings

Switch	Signal	Value of this pin at rising edge of RESET# is used to configure:	
		Closed/On=1	**Open/Off=0**
S1-1	MD15	WAIT# is always driven.	WAIT# is tristated when S1D13506 is not selected
S1-2	MD1	See Table 3-2:, “Host Bus Interface Selection” on page 8	
S1-3	MD2		
S1-4	MD3		
S1-5	MD4	Little Endian	Big Endian
S1-6	MD5	WAIT# is active high	WAIT# is active low
S1-7	MD11	See Table 3-2:, “Host Bus Interface Selection” on page 8	
S1-8	MD12	BUSCLK input divided by 2	BUSCLK input not divided

= Required configuration when used in a PCI environment

The following table shows the Host Bus Interface options available. The host bus interface is selected according to the evaluation platform to be used.

Table 3-2: Host Bus Interface Selection

MD11	MD3	MD2	MD1	Host Bus Interface
0	0	0	0	SH-4/SH-3
0	0	0	1	MC68K Bus 1
0	0	1	0	MC68K Bus 2
0	0	1	1	Generic
0	1	0	0	Reserved
0	1	0	1	MIPS/ISA
0	1	1	0	PowerPC
0	1	1	1	PC Card
1	1	1	1	Philips PR31500/PR31700 / Toshiba TX3912

= Required configuration when used in a PCI environment

3.2 Configuration Jumpers

The S5U13505B00C has seven jumper blocks which configure various board settings. The jumper positions for each function are shown below.

Table 3-3: Jumper Settings

Jumper	Function	Position 1-2	Position 2-3	Jumper Off
JP1	BUSCLK Selection	BUSCLK from U2 oscillator	BUSCLK from H2 header	n/a
JP2	CLKI Selection	CLKI from U3 oscillator	CLKI is the same as BUSCLK	n/a
JP3	VDD current	Normal operation	n/a	Current measurement for VDD
JP4	DACVDD current	Normal operation	n/a	Current measurement for DACVDD
JP5	LCD Panel Voltage	+5V LCDVCC	+3.3V LCDVCC	n/a
JP6	Panel Enable Polarity	LCDPWR active high	LCDPWR active low	n/a
JP7	PCI FPGA enable	Disable FPGA for non-PCI host	n/a	Enable FPGA for PCI host
JP8	IREF for CRT/TV DAC	4.6mA for CRT	9.2mA for TV	n/a

= Default configuration

JP1 - BUSCLK Selection

JP1 selects the source for BUSCLK.
When the jumper is at position 1-2, the BUSCLK source is provided by the oscillator at U2 (default setting).
When the jumper is at position 2-3, the BUSCLK source is provided by the non-PCI host system.

Note
When used in a PCI environment, JP1 must be set to the 1-2 position.

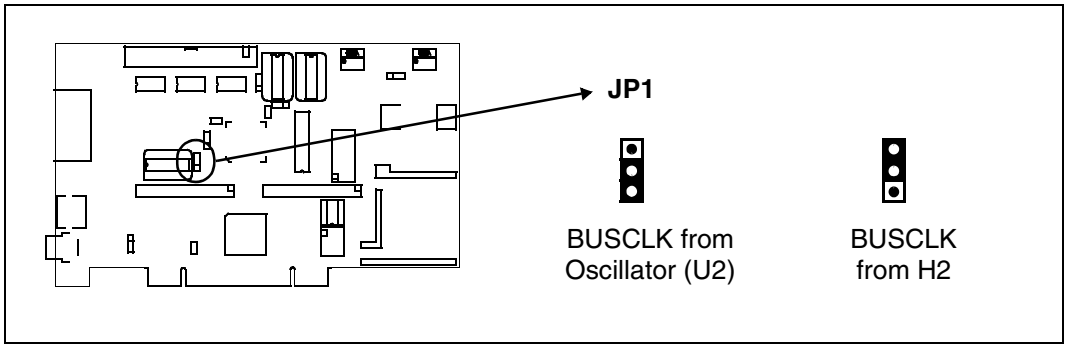

Figure 3-2: Configuration Jumper (JP1) Location

JP2 - CLKI Selection

JP2 selects the source for CLKI.
When the jumper is at position 1-2, the CLKI source is provided by the oscillator at U3 (default setting).
When the jumper is at position 2-3, the CLKI source is the same as BUSCLK (provided by the non-PCI host system).

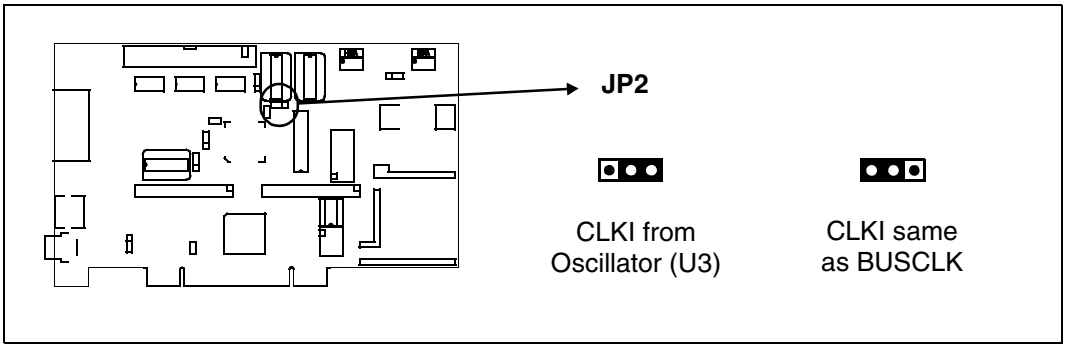

Figure 3-3: Configuration Jumper (JP2) Location

JP3 - VDD current

JP3 allows the measurement of S1D13505 VDD current consumption.
When the jumper is at position 1-2, the evaluation board is operating normally (default setting).
When no jumper is installed, VDD current consumption can be measured by connecting an ammeter to JP3.

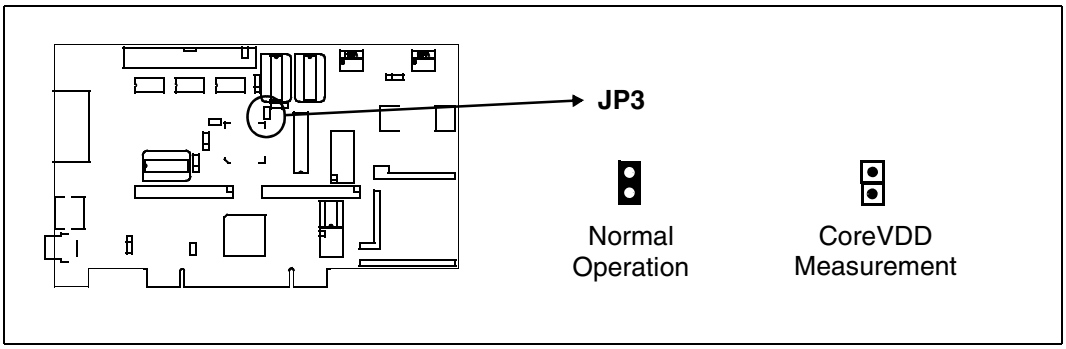

Figure 3-4: Configuration Jumper (JP3) Location

JP4 - DACVDD current

JP4 allows the measurement of S1D13505 DACVDD current consumption.
When the jumper is at position 1-2, the evaluation board is operating normally (default setting).
When no jumper is installed, DACVDD current consumption can be measured by connecting an ammeter to JP4.

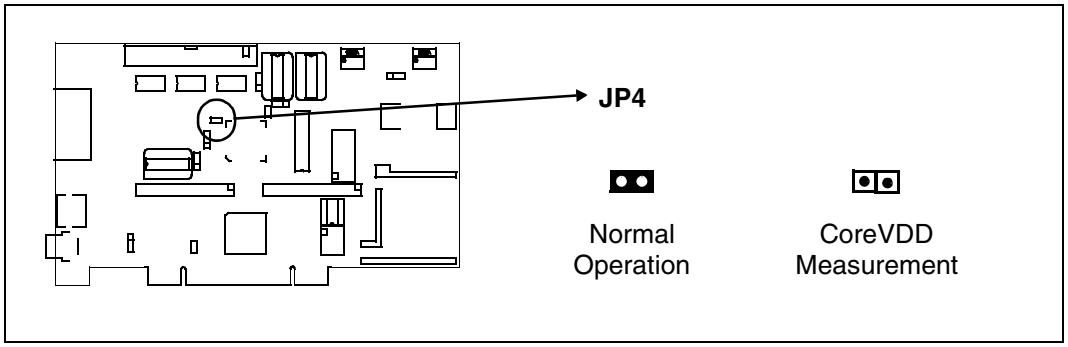

Figure 3-5: Configuration Jumper (JP4) Location

JP5 - LCD panel voltage

JP5 selects the voltage level to the LCD panel.
When the jumper is at position 1-2, the LCD panel voltage level is configured for 5.0V.
When the jumper is at position 2-3, the LCD panel voltage level is configured for 3.3V (default setting).

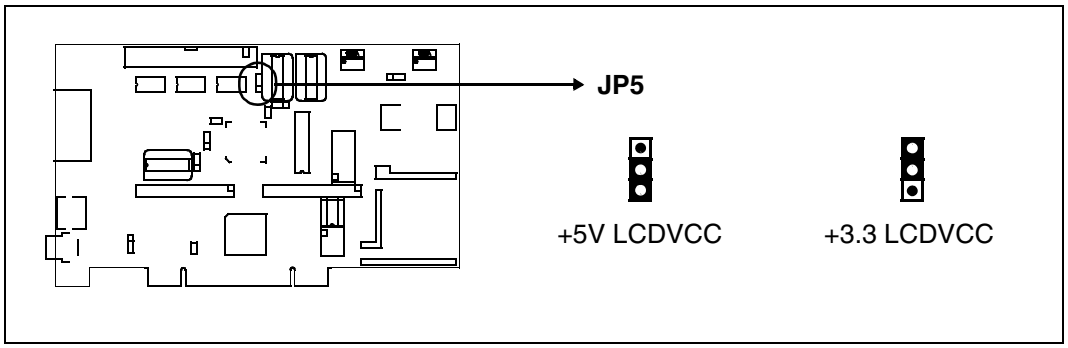

Figure 3-6: Configuration Jumper (JP5) Location

JP6 - Panel Enable Polarity

JP6 selects the polarity of the LCDPWR panel enable signal.
When the jumper is at position 1-2, the LCDPWR signal is active high (default setting).
When the jumper is at position 2-3, the LCDPWR signal is active low.

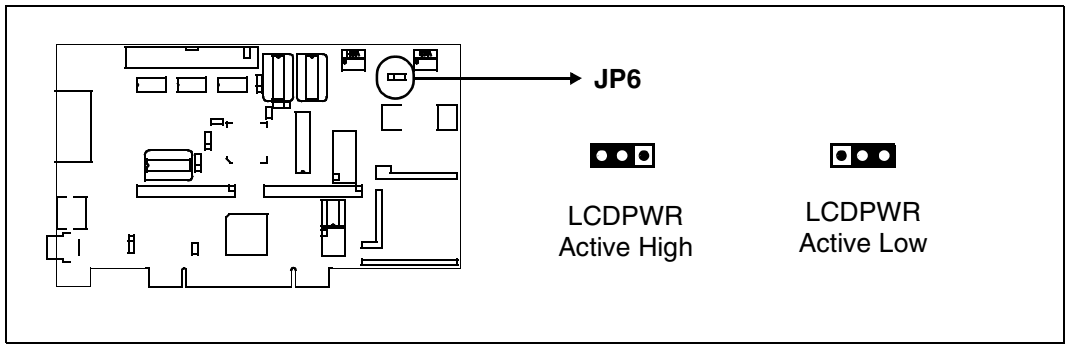

Figure 3-7: Configuration Jumper (JP6) Location

JP7 - PCI FPGA Enable

JP7 controls the PCI FPGA.
When no jumper is installed, the PCI FPGA is enabled and the evaluation board may be used in a PCI environment (default setting).
When the jumper is in position 1-2, the PCI FPGA is disabled and the evaluation board may be used with a non-PCI host system.

Note
Non-PCI host system must be connected to headers H1 and H2.

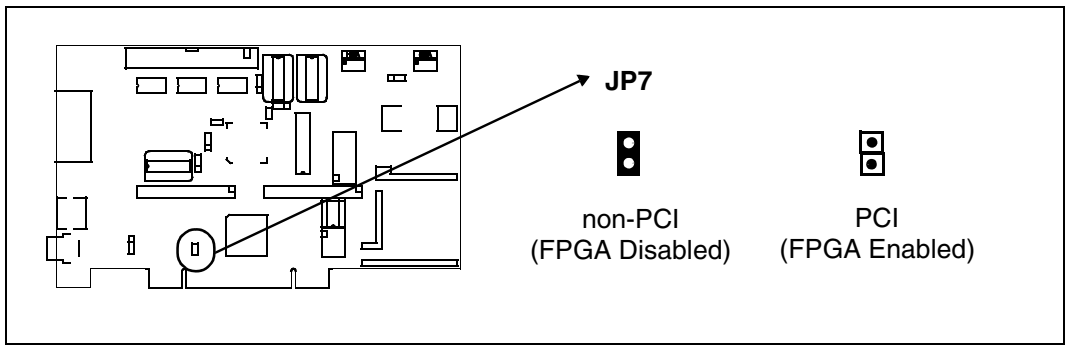

Figure 3-8: Configuration Jumper (JP7) Location

JP8 - IREF for CRT/TV DAC

JP8 selects the magnitude of the IREF current used by the embedded RAMDAC.
When the jumper is at position 1-2, the IREF current is 4.6mA. This setting is used for CRT display.
When the jumper is at position 2-3, the IREF current is 9.2mA. This setting is used for TV display, but it may be used by CRT display as well.

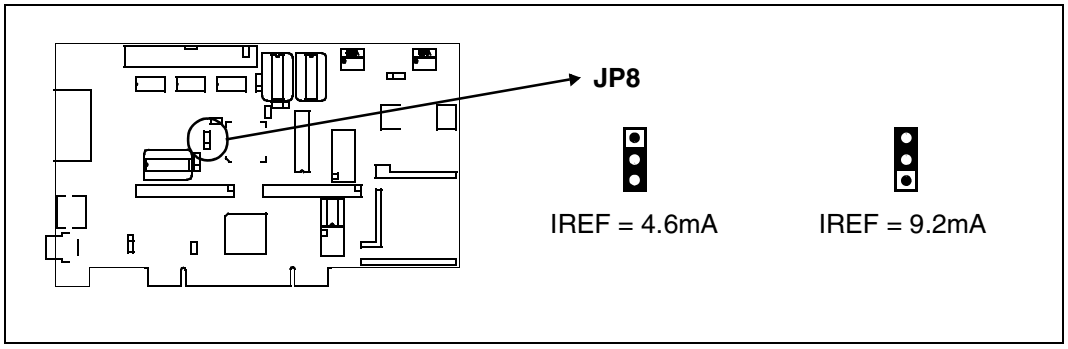

Figure 3-9: Configuration Jumper (JP8) Location

4 Technical Description

The S5U13506P00C100 operates with both PCI and non-PCI evaluation platforms. It supports passive LCD panels (4/6/16-bit), TFT/D-TFD panels (9/12/18-bit), CRT displays (analog RGB output) and TV (NTSC and PAL).

4.1 PCI Bus Support

The S5U13506P00C100 does not have on-chip PCI bus interface support. The S5U13506P00C100 uses the PCI FPGA to support the PCI bus.

4.2 Non-PCI Host Interface Support

The S5U13506P00C100 is specifically designed to support a standard PCI bus environment (using the PCI Bridge Adapter FPGA). However, the S5U13506P00C100 can directly support many other Host Bus Interfaces. When the FPGA is disabled (using jumper JP7), headers H1 and H2 provide the necessary IO pins to interface to the Host Bus Interfaces listed in Table 4-4:, “CPU Interface Pin Mapping”.

Note

The S5U13506P00C100 is designed to work only with 3.3V systems. To use it with a 5V system, some modifications must be done to the board as follows:

1. Replace the 3.3V DRAM (U6) on the board with a 5V DRAM.
2. Cut the trace between JP9-2 and JP9-3 on the solder side of the board.
3. Connect JP9-1 and JP9-2. This will set IOVDD to 5V.

4.2.1 CPU Interface Pin Mapping

The functions of the S1D13506 host interface pins are mapped to each host bus interface according to the following table.

Table 4-4: CPU Interface Pin Mapping

S1D13505 Pin Names	Generic	Hitachi SH-4/SH-3	MIPS/ISA	Motorola MC68K Bus 1	Motorola MC68K Bus 2	Motorola PowerPC	PC Card	Philips PR31500 /PR31700	Toshiba TX3912
AB20	A20	A20	LatchA20	A20	A20	A11	A20	ALE	ALE
AB19	A19	A19	SA19	A19	A19	A12	A19	/CARDREG	CARDREG*
AB18	A18	A18	SA18	A18	A18	A13	A18	/CARDIORD	CARDIORD*
AB17	A17	A17	SA17	A17	A17	A14	A17	/CARDIOWR	CARDIOWR*
AB[16:13]	A[16:13]	A[16:13]	SA[16:13]	A[16:13]	A[16:13]	A[15:18]	A[16:13]	Connected to V_{DD}	
AB[12:1]	A[12:1]	A[12:1]	SA[12:1]	A[12:1]	A[12:1]	A[19:30]	A[12:1]	A[12:1]	A[12:1]
AB0	A0[1]	A0[1]	SA0	LDS#	A0	A31	A0[1]	A0	A0
DB[15:8]	D[15:0]	D[15:8]	SD[15:0]	D[15:8]	D[31:24]	D[0:7]	D[15:0]	D[23:16]	D[23:16]
DB[7:0]	D[7:0]	D[7:0]	SD[7:0]	D[7:0]	D[23:16]	D[8:15]	D[7:0]	D[31:24]	D[31:24]
WE1#	WE1#	WE1#	SBHE#	UDS#	DS#	$\overline{BI}$	-CE2	/CARDxCSH	CARDxCSH*
M/R#	External Decode							Connected to V_{DD}	
CS#	External Decode							Connected to V_{DD}	
BUSCLK	BCLK	CKIO	CLK	CLK	CLK	CLKOUT	CLK	DCLKOUT	DCLKOUT
BS#	Connected to V_{DD}	BS#	Connected to V_{DD}	AS#	AS#	$\overline{TS}$	Connected to V_{DD}	Connected to V_{DD}	
RD/WR#	RD1#	RD/WR#	Connected to V_{DD}	R/W#	R/W#	$\overline{RD/WR}$	-CE1	/CARDxCSL	CARDxCSL*
RD#	RD0#	RD#	MEMR#	Connected to V_{DD}	SIZ1	TSIZ0	-OE	/RD	RD*
WE0#	WE0#	WE0#	MEMW#	Connected to V_{DD}	SIZ0	TSIZ1	-WE	/WE	WE*
WAIT#	WAIT#	RDY# /WAIT#	IOCHRDY	DTACK#	DSACK1#	$\overline{TA}$	-WAIT	/CARDxWAIT	CARDxWAIT*
RESET#	RESET#	RESET#	inverted RESET	RESET#	RESET#	RESET#	inverted RESET	RESET#	PON*

Note
[1] A0 for these busses is not used internally by the S1D13506.

4.2.2 CPU Bus Connector Pin Mapping

The pinouts for Connector H1 are listed in the following table.

Table 4-5: CPU/BUS Connector (H1) Pinout

Pin No.	Function
1	Connected to DB0 of the S1D13506
2	Connected to DB1 of the S1D13506
3	Connected to DB2 of the S1D13506
4	Connected to DB3 of the S1D13506
5	Ground
6	Ground
7	Connected to DB4 of the S1D13506
8	Connected to DB5 of the S1D13506
9	Connected to DB6 of the S1D13506
10	Connected to DB7 of the S1D13506
11	Ground
12	Ground
13	Connected to DB8 of the S1D13506
14	Connected to DB9 of the S1D13506
15	Connected to DB10 of the S1D13506
16	Connected to DB11 of the S1D13506
17	Ground
18	Ground
19	Connected to DB12 of the S1D13506
20	Connected to DB13 of the S1D13506
21	Connected to DB14 of the S1D13506
22	Connected to DB15 of the S1D13506
23	Connected to RESET# of the S1D13506
24	Ground
25	Ground
26	Ground
27	+12 volt supply, required in non-PCI applications
28	+12 volt supply, required in non-PCI applications
29	Connected to WE0# of the S1D13506
30	Connected to WAIT# of the S1D13506
31	Connected to CS# of the S1D13506
32	Connected to MR# of the S1D13506
33	Connected to WE1# of the S1D135065
34	S1D13506 supply, provided by the S5U13506P00C100

The pinouts for Connector H2 are listed in the following table.

Table 4-6: CPU/BUS Connector (H2) Pinout

Pin No.	Function
1	Connected to AB0 of the S1D13506
2	Connected to AB1 of the S1D13506
3	Connected to AB2 of the S1D13506
4	Connected to AB3 of the S1D13506
5	Connected to AB4 of the S1D13506
6	Connected to AB5 of the S1D13506
7	Connected to AB6 of the S1D13506
8	Connected to AB7 of the S1D13506
9	Ground
10	Ground
11	Connected to AB8 of the S1D13506
12	Connected to AB9 of the S1D13506
13	Connected to AB10 of the S1D13506
14	Connected to AB11 of the S1D13506
15	Connected to AB12 of the S1D13506
16	Connected to AB13 of the S1D13506
17	Ground
18	Ground
19	Connected to AB14 of the S1D13506
20	Connected to AB15 of the S1D13506
21	Connected to AB16 of the S1D13506
22	Connected to AB17 of the S1D13506
23	Connected to AB18 of the S1D13506
24	Connected to AB19 of the S1D13506
25	Ground
26	Ground
27	+5 volt supply, required in non-PCI applications
28	+5 volt supply, required in non-PCI applications
29	Connected to RD/WR# of the S1D13506
30	Connected to BS# of the S1D13506
31	Connected to S1D13506 BUSCLK if JP1 is in position 2-3
32	Connected to RD# of the S1D13506
33	Connected to AB20 of the S1D13506
34	Not connected

4.3 LCD Support

The S1D13506 supports 4/8-bit dual and single passive monochrome panels, 4/8/16-bit dual and single passive color panels, and 9/12/18-bit active matrix color TFT/D-TFD panels. All necessary signals are provided on the 40-pin LCD connector (J1). The interface signals are alternated with grounds on the cable to reduce cross-talk and noise. When supporting an 18-bit TFT/D-TFD panel, the S1D13505 can display 64K of a possible 256K colors because only 16 of the18 bits of LCD data are available from the S1D13505. For details, refer to the *S1D13506 Hardware Functional Specification*, document number X25B-A-001-xx.

For S1D13506 FPDAT[15:0] pin mapping for various types of panel see Table 4-7:, “LCD Signal Connector (J4)” on page 19.

4.3.1 LCD Interface Pin Mapping

Table 4-7: LCD Signal Connector (J4)

S1D13505 Pin Names	Connector Pin No.	Monochrome Passive Panels			Color Passive Panels						Color TFT/D-TFD Panels		
		Single		Dual	Single	Single Format 1	Single Format 2	Single	Dual				
		4-bit	8-bit	8-bit	4-bit	8-bit	8-bit	16-Bit	8-bit	16-bit	9-bit	12-bit	18-bit
FPDAT0	1 and 6		D0	LD0		D0	D0	D0	LD0	LD0	R2	R3	R5
FPDAT1	3		D1	LD1		D1	D1	D1	LD1	LD1	R1	R2	R4
FPDAT2	5		D2	LD2		D2	D2	D2	LD2	LD2	R0	R1	R3
FPDAT3	7		D3	LD3		D3	D3	D3	LD3	LD3	G2	G3	G5
FPDAT4	9	D0	D4	UD0	D0	D4	D4	D8	UD0	UD0	G1	G2	G4
FPDAT5	11	D1	D5	UD1	D1	D5	D5	D9	UD1	UD1	G0	G1	G3
FPDAT6	13 and 4	D2	D6	UD2	D2	D6	D6	D10	UD2	UD2	B2	B3	B5
FPDAT7	15	D3	D7	UD3	D3	D7	D7	D11	UD3	UD3	B1	B2	B4
FPDAT8	17							D4		LD4	B0	B1	B3
FPDAT9	19							D5		LD5		R0	R2
FPDAT10	21							D6		LD6			R1
FPDAT11	23							D7		LD7		G0	G2
FPDAT12	25							D12		UD4			G1
FPDAT13	27							D13		UD5			G0
FPDAT14	29							D14		UD6		B0	B2
FPDAT15	31							D15		UD7			B1
FPSHIFT	33	FPSHIFT											
DRDY	35 and 38	MOD				FPSHIFT2	MOD				DRDY		
FPLINE	37	FPLINE											
FPFRAME	39	FPFRAME											
GND	2 and 8-26 (Even Pins)	GND											
N/C	28	N/C											
N/C	30	N/C											
LCDVCC	32	+5V or +3.3V according to JP5											
+12V	34	+12V											
N/C	36	N/C											
NC (pin 75)[2]	40	Panel Enable, active low (LCDPWR)[2]											

= Driven low

Note

[1] For FPDATxx to LCD interface hardware connections refer to the Display Interface AC Timing section of the *S1D13506 Hardware Functional Specification*, document number X25B-A-001-xx.

[2] The S5U13506B00C was designed using S1D13506 pin 75 (LCDPWR) to control the LCD bias power. This design is **no longer supported**. Applications should use one of the available GPIO pins to control the LCD bias power allowing for software control of power sequencing delays. For further information on LCD power sequencing, see the *S1D13506 Programming Notes and Examples*, document number X25B-G-003-xx.

4.3.2 Buffered LCD Connector

J4 provides the same LCD panel signals as those directly from S1D13505, but with voltage-adapting buffers which can be set to 3.3V or 5V. Pin 32 on this connector provides power for the LCD panel logic at the same voltage as the buffer power supply.

4.4 CRT/TV Support

4.4.1 CRT/TV Interface Pin Mapping

CRT/TV signals are supplied on a standard CRT connector (J2), Composite Video connector (J1), and S-Video connector (J3):

Table 4-8: CRT/TV Interface Pin Mapping

S1D13506 Pin Name	CRT	Composite Video	S-Video
HRTC	Horizontal retrace	N/A	N/A
VRTC	Vertical retrace	N/A	N/A
RED	Red	N/A	Luminance
GREEN	Green	Composite	N/A
BLUE	Blue	N/A	Chrominance

4.4.2 CRT Support

CRT support is provided on connector J2 via the S1D13506 embedded RAMDAC. An external current reference is implemented to provide the necessary RAMDAC output gain. The reference current (IREF) should be set to 4.6mA using jumper JP8.

Note
When IREF is set to 4.6mA, the DAC Output Select bit (REG[05Bh] bit 3) must be set to 1.

CRT output is not available when TV output is enabled.

4.4.3 TV Support

The S1D13506 supports PAL or NTSC TV output. Composite Video is available on connector J1 and S-Video is available on connector J3. An external current reference is implemented to provide the necessary RAMDAC output gain. The reference current should be set to 9.2mA using jumper JP8.

TV output is not available when CRT output is enabled. PAL and NTSC modes cannot be enabled at the same time.

4.5 Current consumption measurement

The evaluation board has 2 headers, JP3 and JP4, which allow the independent measurement of S1D13506 VDD and DACVDD current consumption. To measure the current, remove the appropriate jumper and connect an ammeter to the corresponding header pins.

5 References

5.1 Documents

- Epson Research and Development, Inc., *S1D13506 Hardware Functional Specification*, Document Number X25B-A-001-xx.
- Epson Research and Development, Inc., *S1D13506 Programming Notes and Examples*, Document Number X25B-G-003-xx.

5.2 Document Sources

- Epson Research and Development Website: http://www.erd.epson.com.

6 Parts List

Item	Quantity	Reference	Part	Footprint	Comments
1	38	C1,C2,C3,C4,C5,C6, C7,C8,C9,C10,C11, C12,C13,C16,C17, C18,C19,C20,C22, C23,C24,C27,C29, C30,C31,C40,C41, C42,C43,C44,C45, C46,C47,C48,C49, C50,C51,C52	0.1uF	C0805	Kemet C0805C104K4RACTU generic
2	6	C14,C15,C21,C36, C37,C38	68uF/10V/10%	—	Kemet T491D686K010AS or equivalent
3	2	C35,C39	33uF/20V/10%	—	Kemet T491D336K020AS or equivalent
4	3	D1,D2,D3	BAV99	SOT23	Fairchild Semiconductor BAV99
5	2	H1,H2	HEADER 17X2	HDR2X17	Thomas&Betts 609-3407 altern. Samtec TSW-117-05-G-D or equiv.
6	5	JP1,JP2,JP5,JP6,JP8	Header 3x1, 0.1" pitch, unshrouded	SIP3	—
7	3	JP3,JP4,JP7	Header 2x1, 0.1" pitch, unshrouded	SIP2	—
8	1	J1	C-VIDEO	—	CUI RCJ-014
9	1	J2	VGA CONNECTOR	DB15/PS2CON	NorComp 181-015-213R561 or equivalent
105	1	J3	S-VIDEO	—	Kycon KMDGX-4S-BS-99 or equivalent Mini DIN 4 pin
11	1	J4	CON40A	HDR2X20A	Samtec TST-120-01-G-D or equivalent
12	5	L1,L2,L3,L4,L5	Ferrite Bead	INDUCTOR1	Steward 28F0181-ISR-10
13	1	Q1	MMBT2222A	SOT23	Fairchild Semiconductor MMBT2222A or equivalent
14	3	R1,R2,R36	100K,5%	R0805	—
15	3	R4,R5,R6	150R,1%	R0805	generic
16	1	R7	0R	R0805	—
17	16	R9,R10,R11,R12,R13, R14,R15,R16,R17, R18,R20,R39,R40, R41,R42,R44	15K,5%	R0805	—
18	1	R19	1.5K,1%	R0805	generic
19	4	R21,R37,R38,R43	1K,1%	R0805	—
20	1	R23	69.8R,1%	R0805	—
21	1	R24	140R,1%	R0805	generic
22	1	S1	SW DIP-8	DIPSW8	Grayhill 76SB08S
23	1	U1	S1D13506F00A	TQFP128	Epson S1D13506F00A
24	1	U2	40MHz	DIP14	Epson SG8002DB, 40MHz socketed
25	1	U3	25.175MHz	DIP14	Epson SG8002DB, 25MHz socketed

Item	Quantity	Reference	Part	Footprint	Comments
26	1	U4	14.31818MHz	DIP14	Epson SG8002DB, 14.31818MHz socketed
27	1	U5	LT1117CM-3.3	DDPAK-2	Linear Technologies LT1117CM-3.3
28	1	U6	DRAM 1Mx16-SOJ, Lead free	SOJ42	ISSI IS41LV16100B-50KL
29	1	U7	LT1117CST-3.3	—	Linear Technologies LT1117CST-3.3
30	1	U8	INVERTER SINGLE NC7S04	SC70-5	Fairchild Semiconductor NC7S04P5
31	3	U9,U10,U11	74AHC244	SO20W	TI 74AHC244
32	1	U14	EPF6016TC144-2	TQFP144	Altera EPF6016TC144-2
33	1	U15	EPC1PI8N	DIP8	Altera EPC1PI8N programmed, socketed

7 Schematic Diagrams

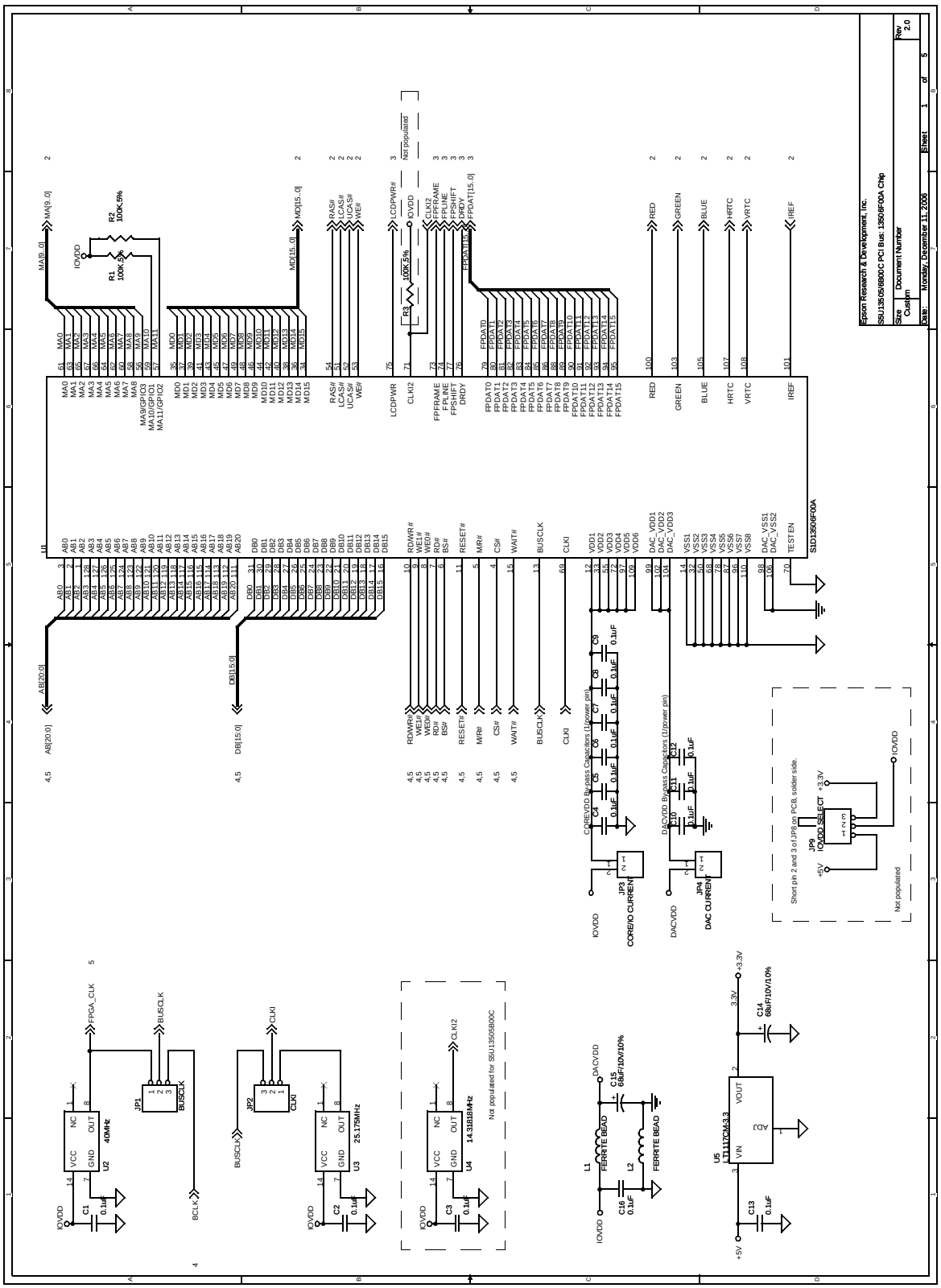

Figure 7-1: S5U13506P00C100 Evaluation Board Schematics (1 of 5)

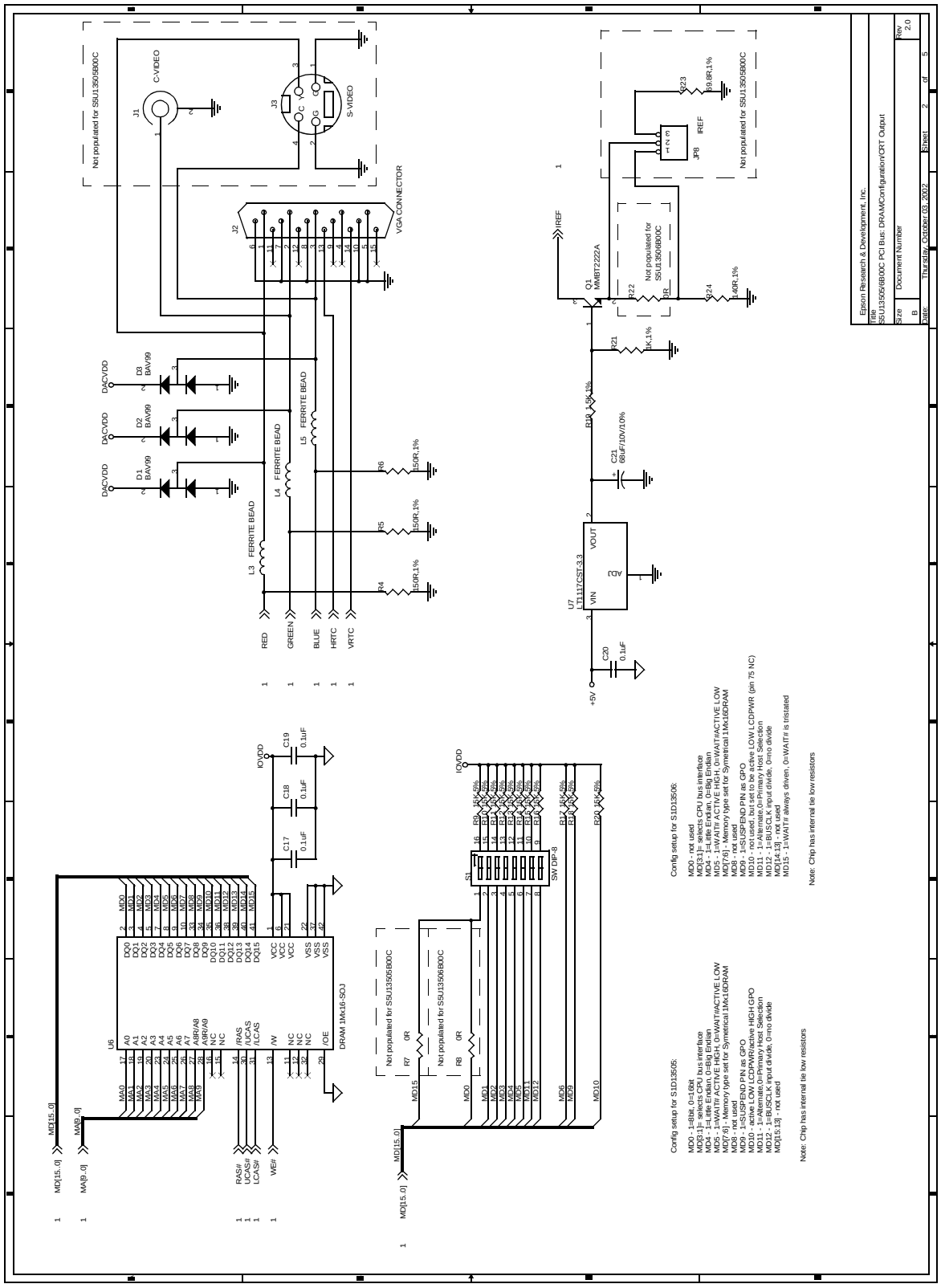

Figure 7-2: S5U13506P00C100 Evaluation Board Schematics (2 of 5)

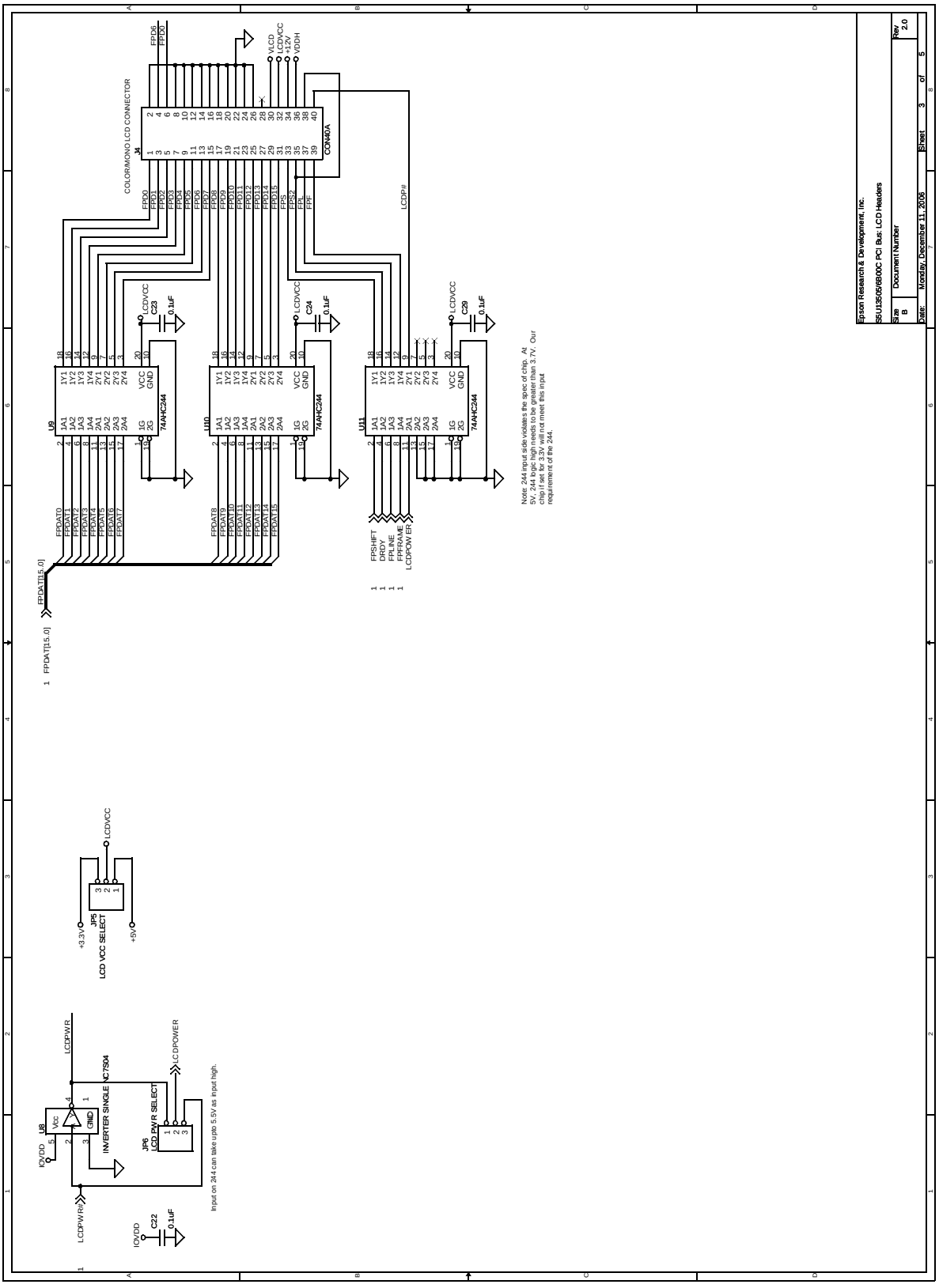

Figure 7-3: S5U13506P00C100 Evaluation Board Schematics (3 of 5)

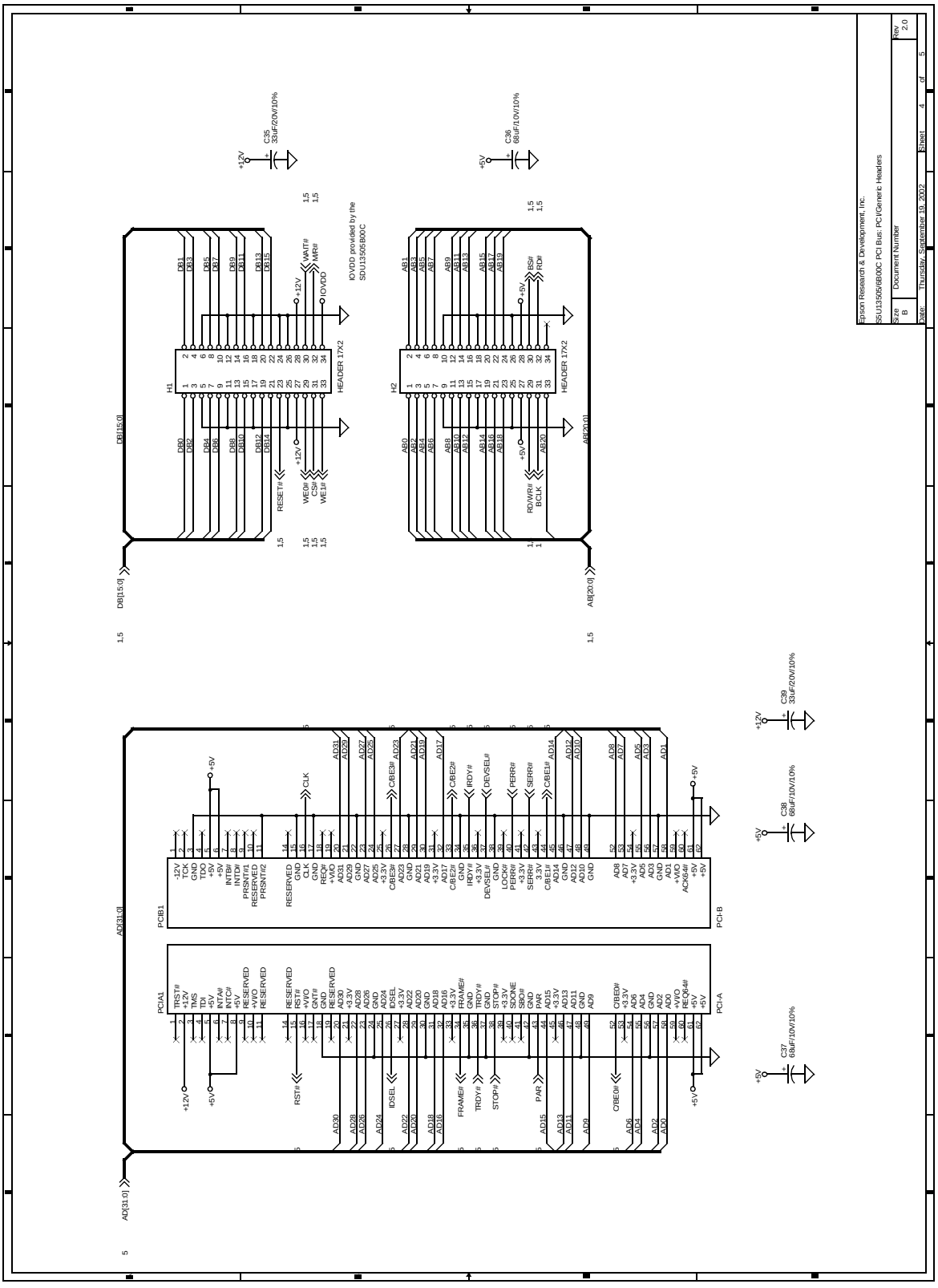

Figure 7-4: S5U13506P00C100 Evaluation Board Schematics (4 of 5)

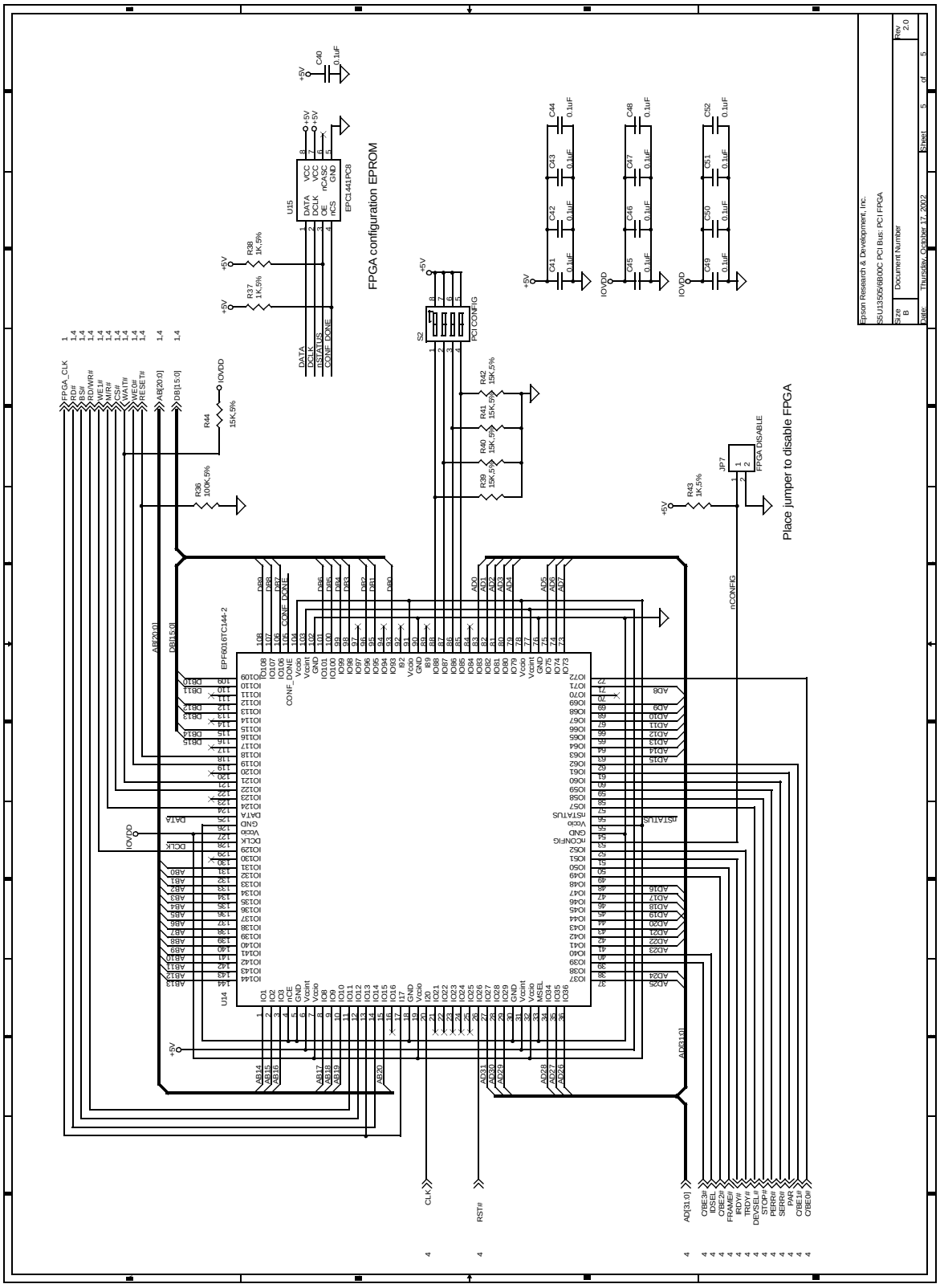

Figure 7-5: S5U13506P00C100 Evaluation Board Schematics (5 of 5)

8 Board Layout

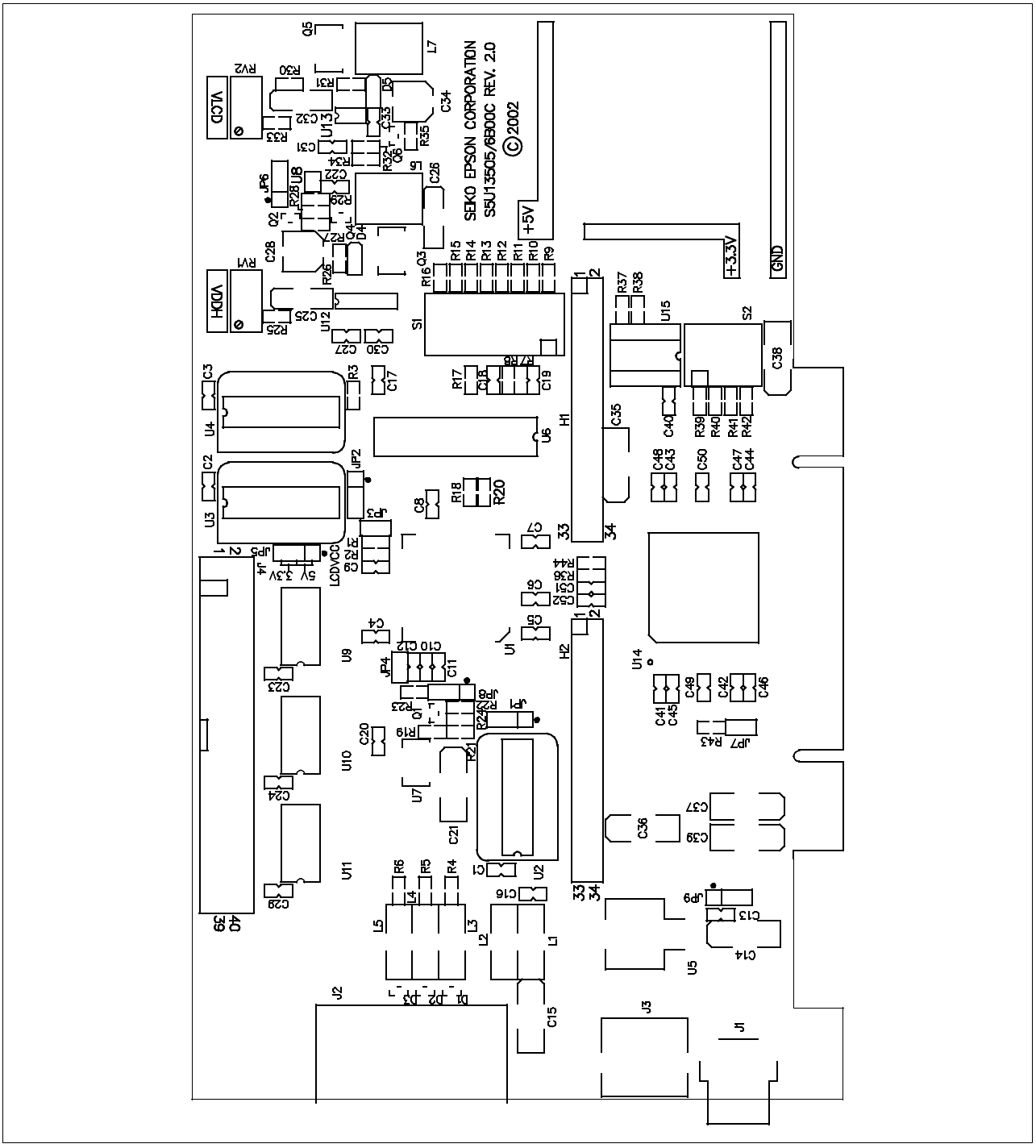

Figure 8-1: S5U13506P00C100 Evaluation Board Layout

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X23A-G-014-02 Revision 2.0

- update sales offices

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- initial release

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