

## S1D/S2D13515 LCD Controller

April 2009

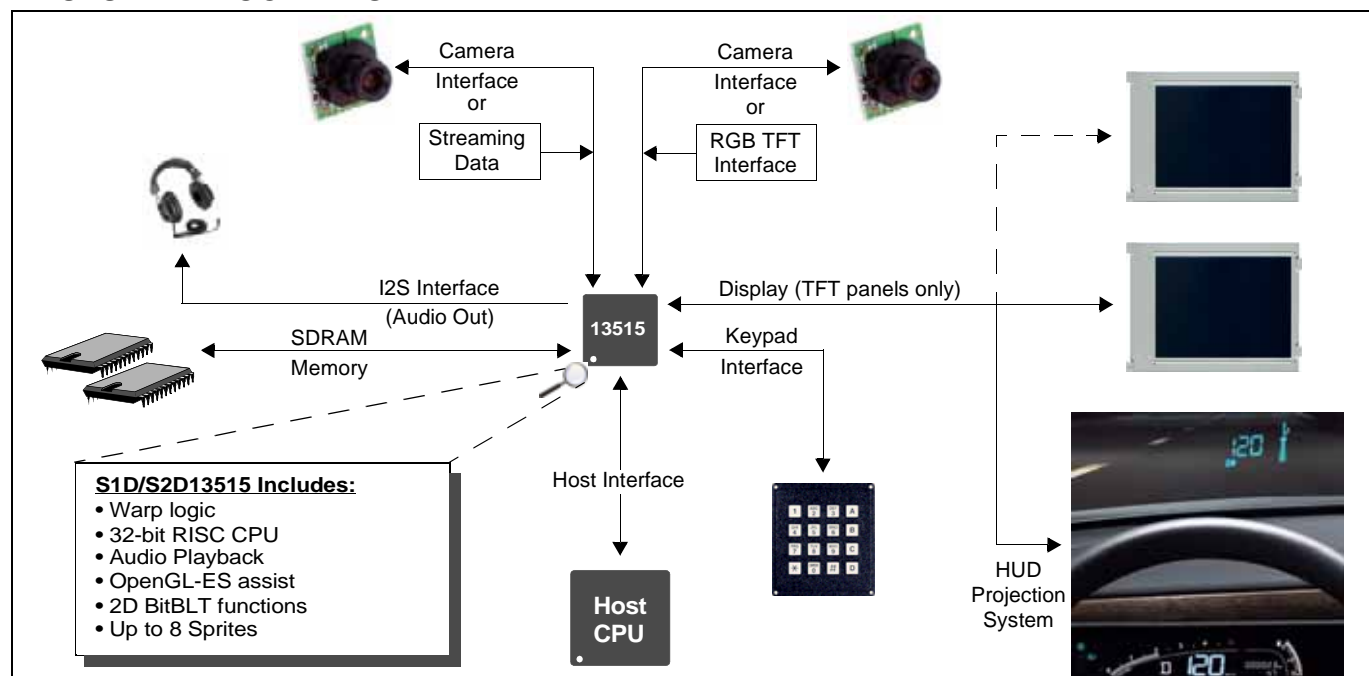
The S1D/S2D13515 is a highly integrated LCD Controller targeted at the embedded and automotive markets. It advances on the successes of other Epson LCD controllers by embedding a proprietary 32-bit RISC CPU and associated accelerator blocks to achieve an increase in flexibility and functionality over previous designs. Routines are provided allowing for audio playback, 2D BitBLT operations, warp and filtering operations, and the ability to offer OpenGL-ES 1.1 support. In particular, the Warp Logic functions make this an ideal solution for the automotive Heads-Up Display (HUD) market, or pseudo 3D navigation displays.

The S1D/S2D13515 is an affordable, low power device which uses a flexible external SDRAM memory interface to provide its frame buffer. It supports a wide variety of CPU interfaces and LCD panel outputs, including Double Display panels, which makes it an excellent choice for instrumentation or center cluster applications.

### ■ FEATURES

- Indirect and Direct CPU interfaces
- SPI or I2C Host interface
- External SDRAM Memory interface
- Can display 2 RGB panels simultaneously (some restrictions apply)
- Support for Double Display panels
- Programmable resolutions and color depths up to 32 bpp
- Video Input / Camera Port supporting flexible configurations of 8-bit Cameras and RGB input streams
- Sprite Engine with up to 8 sprites
- Multiple windows supporting Alpha Blending, Double Buffering, and Horizontal Flip
- Warp logic for HUD projection correction or other distortion compensation
- 32-bit embedded RISC processor with accelerator blocks
  - Audio playback ( WAV, Ogg Vorbis, etc.)
  - OpenGL-ES 1.1 compliant
  - 2D BitBLT Acceleration with API
  - Programmable startup sequence without Host
- 2 channel PWM
- I2S and I2C outputs
- SPI Flash Memory Interface
- Keypad interface (5x5 matrix support)
- Temperature range:
  - S1D13515: -40 to +85 °C
  - S2D13515: -40 to +105 °C
- Package: QFP22-256 and PBGA1U-256

### ■ SYSTEM BLOCK DIAGRAM



## S1D/S2D13515

### DESCRIPTION

#### External Display Buffer

- Uses external SDRAM as display buffer
- Supports x32 SDRAM interface (Size: 16/32/64M byte)
- SDRAM clock: 100MHz
- External memory is accessible by the internal and Host CPUs
- Provides configurable linear access to memory in 4M byte paging windows

#### CPU Interface

- Direct/indirect interface support for most popular CPU interfaces
- SPI or I2C Host Interface
- Supports 25MHz Host bus clock

#### Display Support

- Single or Dual panel implementations (Dual can have independent images)
- Color TFT Panel with optional serial command interface
- EID and Sharp Double Display Panels
- NTSC/PAL TV Output can be realized by using an external video encoder such as the Epson S1D13746
- Color Depths: 8/16/24 bpp
- Target resolutions / Color Depths:  
800x480 + 320x240 simultaneous @ 24 bpp, 60Hz  
1024x768, 24 bpp, 60Hz

#### Display Features

- Warp logic corrects projection anomalies on HUD
- Multiple Windows (Layers) support:
  - Horizontal Flip
  - Double Buffering
  - Alpha Blending
- Sprite Engine supports up to 8 sprite layers with Alpha blending and transparency
- Interrupts available
  - Supports maskable non-display (Vsync) interrupt
  - Supports delayed version of Vsync Interrupt

#### Embedded CPU

- Embedded CPU Speed: 50MHz (typical)
- 32-bit RISC CPU can be used for:
  - Audio decode (Supported Codecs: MP3, AAC, WAV, ADPCM, Ogg Vorbis)
  - 2D BitBLT Acceleration with API
  - OpenGL-ES assist (OpenGL-ES v1.1 compliant)
  - OEM defined functions

#### Digital Video

- Video Input / Camera port supporting either 1x 8-bit camera, 2x 8-bit cameras, 1x RGB data stream, 2x RGB data streams, simultaneous 1x 8-bit and 1x RGB data stream input (when second camera input is used only single panel is available)
  - Supports ITU-R BT.656 YUV format
  - Supports down-scaling of the video input stream
  - Captures YUV data into SDRAM as RGB format

#### Miscellaneous

- Internal System Speed: 50MHz typical
- 2 channel PWM for backlight control
- I2C Interface (typically used for Camera)
- I2S Interface (typically used for audio output)
- SPI Flash Memory Interface
- Keypad Interface with 5 x 5 matrix support
- General Purpose IO pins available
- Flexible Clock Structure:
  - Two embedded PLLs
  - Built-in crystal input
  - Digital clock input
  - Clocks dynamically turned off for power saving
- Operating Temperature Range:
  - S1D13515: -40 to +85 °C
  - S2D13515: -40 to +105 °C
- CORE<sub>VDD</sub> 1.8 volts and IO<sub>VDD</sub> 3.3 volts
- Package: QFP22-256 and PBGA1U-256
- S1D13515 also available (non-automotive specification)

### CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- Technical Documentation
- CPU Independent Software Utilities
- Evaluation Boards
- Royalty Free source level driver code

#### Japan

Seiko Epson Corporation  
IC International Sales Group  
421-8, Hino, Hino-shi  
Tokyo 191-8501, Japan  
Tel: +81-42-587-5814  
Fax: +81-42-587-5117

#### North America

Epson Electronics America, Inc.  
2580 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: +1-800-228-3964  
Fax: +1-408-922-0238

#### China

Epson (China) Co., Ltd.  
7F, Jinbao Bldg.  
No. 89 Jinbao St.  
Dongcheng District  
Beijing 100005, China  
Tel: +86-10-6410-6555  
Fax: +86-10-6410-7320

#### Taiwan

Epson Taiwan Technology & Trading Ltd.  
14F, No. 7  
Song Ren Road  
Taipei 110, Taiwan  
Tel: +886-2-8786-6688  
Fax: +886-2-8786-6660

#### Hong Kong

Epson Hong Kong Ltd.  
20/F, Harbour Centre  
25 Harbour Road  
Wanchai, Hong Kong  
Tel: +852-2585-4600  
Fax: +852-2827-4346

#### Europe

Epson Europe Electronics GmbH  
Riesstrasse 15  
80992 Munich, Germany  
Tel: +49-89-14005-0  
Fax: +49-89-14005-110

#### Singapore

Epson Singapore Pte., Ltd.  
1 HarbourFront Place  
#03-02 HarbourFront Tower One  
Singapore 098633  
Tel: +65-6586-5500  
Fax: +65-6271-3182

#### Korea

Seiko Epson Corp.  
Korea Office  
50F, LK1 63 Bldg.  
60 Yoido-dong, Youngdeungpo-Ku,  
Seoul, 150-763, Korea  
Tel: +82-2-784-6027  
Fax: +82-2-767-3677

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