Revision History

AS7C351232-10BIN 90ball TFBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Issue	Jan. 2017

FEATURES

- Fast access time : 10ns
- **Low power consumption:**
  Operating current : 125mA (TYP.)
  Standby current : 4mA (TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : B0# (DQ0 ~ DQ7)
  B1# (DQ8 ~ DQ15)
  B2# (DQ16~DQ23)
  B3# (DQ24~DQ31)
- Data retention voltage : 1.5V (MIN.)
- **ROHS Compliant/Pb & Halogen free**
- Package : 90-ball 8mm x 13mm TFBGA

GENERAL DESCRIPTION

The AS7C351232-10BIN is a 16M-bit high speed CMOS static random access memory organized as 512K words by 32 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C351232-10BIN operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

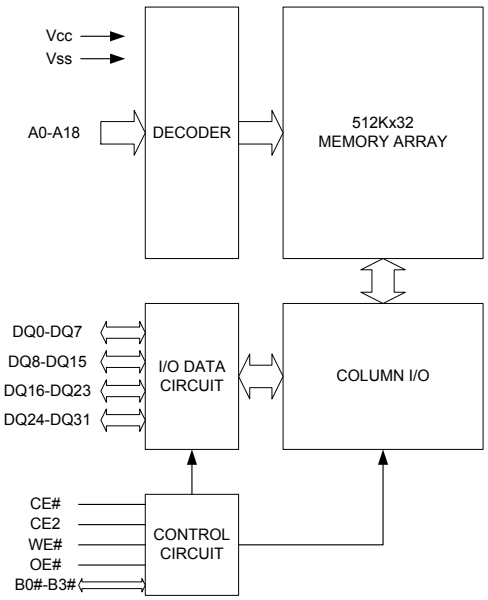
PRODUCT FAMILY

Product Family	Operating Temperature	V_{CC} Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{CC},TYP.)
AS7C351232-10BIN	-40 ~ 85℃	2.7 ~ 3.6V	10ns	4mA	125mA

ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Temperature Range(℃)	Packing Type	Alliance Part Number
90-ball (8mm x 13mm) TFBGA	10	-40℃~85℃	Tray	AS7C351232-10BIN
			Tape Reel	AS7C351232-10BINTR

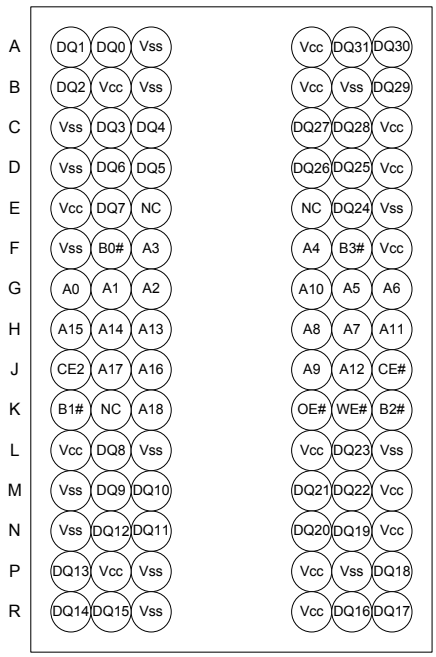
FUNCTIONAL BLOCK DIAGRAM



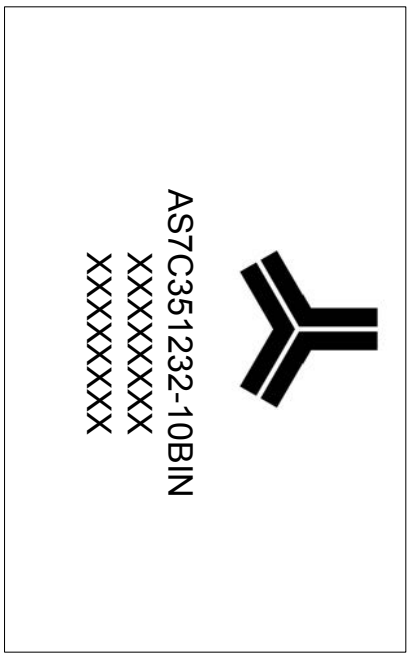
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - DQ31	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
B0# - B3#	Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION



TFBGA(See through with Top View)



TFBGA (Top View)

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	-40 to 85(I grade)	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	B0#	B1#	B0#	B1#	I/O OPERATION				SUPPLY CURRENT
									DQ0-7	DQ8-15	DQ16-23	DQ24-31	
Standby	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	I_{SB1}
	X	L	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	
Output Disable	L	H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	I_{CC}
	L	H	X	X	H	H	H	H	High-Z	High-Z	High-Z	High-Z	
Read	L	H	L	H	L	H	H	H	D_{OUT}	High-Z	High-Z	High-Z	I_{CC}
	L	H	L	H	H	L	H	H	High-Z	D_{OUT}	High-Z	High-Z	
	L	H	L	H	H	H	L	H	High-Z	High-Z	D_{OUT}	High-Z	
	L	H	L	H	H	H	H	L	High-Z	High-Z	High-Z	D_{OUT}	
	L	H	L	H	L	L	L	L	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	
Write	L	H	X	L	L	H	H	H	D_{IN}	High-Z	High-Z	High-Z	I_{CC}
	L	H	X	L	H	L	H	H	High-Z	D_{IN}	High-Z	High-Z	
	L	H	X	L	H	H	L	H	High-Z	High-Z	D_{IN}	High-Z	
	L	H	X	L	H	H	H	L	High-Z	High-Z	High-Z	D_{IN}	
	L	H	X	L	L	L	L	L	D_{IN}	D_{IN}	D_{IN}	D_{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM.	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.3	3.6	V
Input High Voltage	V_{IH}*1			2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}*2			- 0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -4mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	CE# $\leqq$ 0.2V and CE2 $\geqq$ V_{CC}-0.2V, other pins at 0.2V or V_{CC}-0.2V, $I_{I/O}$ = 0mA; f=max.	-10	-	125	180	mA
Standby Power Supply Current	I_{SB1}	CE# $\geqq$ V_{CC} - 0.2V; other pins at 0.2V or V_{CC}-0.2V.		-	4	40	mA

Notes:
1. $V_{IH(MAX.)} = V_{CC}$ + 2.0V for pulse width less than 6ns.
2. $V_{IL(MIN.)} = V_{SS}$ - 2.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at $V_{CC} = V_{CC(TYP.)}$ and T_A = 25℃

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Speed	10 ns
Input Pulse Levels	0.2V to V_{CC}-0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	V_{CC}/2
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -4mA/8mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C351232-10BIN		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	ns
Address Access Time	t_{AA}	-	10	ns
Chip Enable Access Time	t_{ACE}	-	10	ns
Output Enable Access Time	t_{OE}	-	4.5	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	2	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	4	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	4	ns
Output Hold from Address Change	t_{OH}	2	-	ns
Byte Control Access Time	t_{BA}	-	4.5	ns
Byte Control to High-Z Output	t_{BHZ}*	-	4	ns
Byte Control to Low-Z Output	t_{BLZ}*	0	-	ns

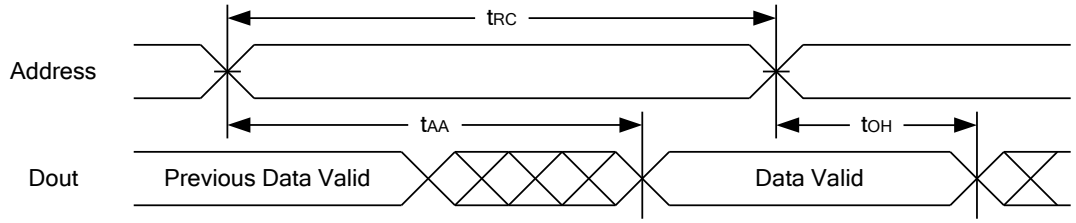
(2) WRITE CYCLE

PARAMETER	SYM.	AS7C351232-10BIN		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	ns
Address Valid to End of Write	t_{AW}	8	-	ns
Chip Enable to End of Write	t_{CW}	8	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	8	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}*	2	-	ns
Write to Output in High-Z	t_{WHZ}*	-	4	ns
Byte Control Valid to End of Write	t_{BW}	8	-	ns

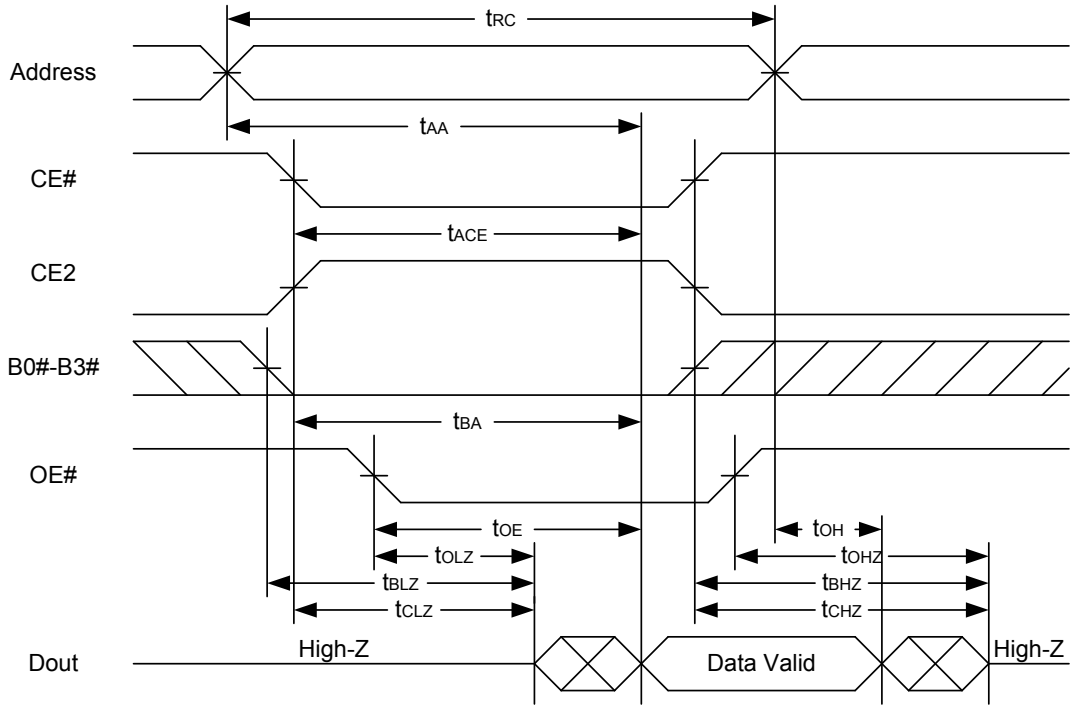
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

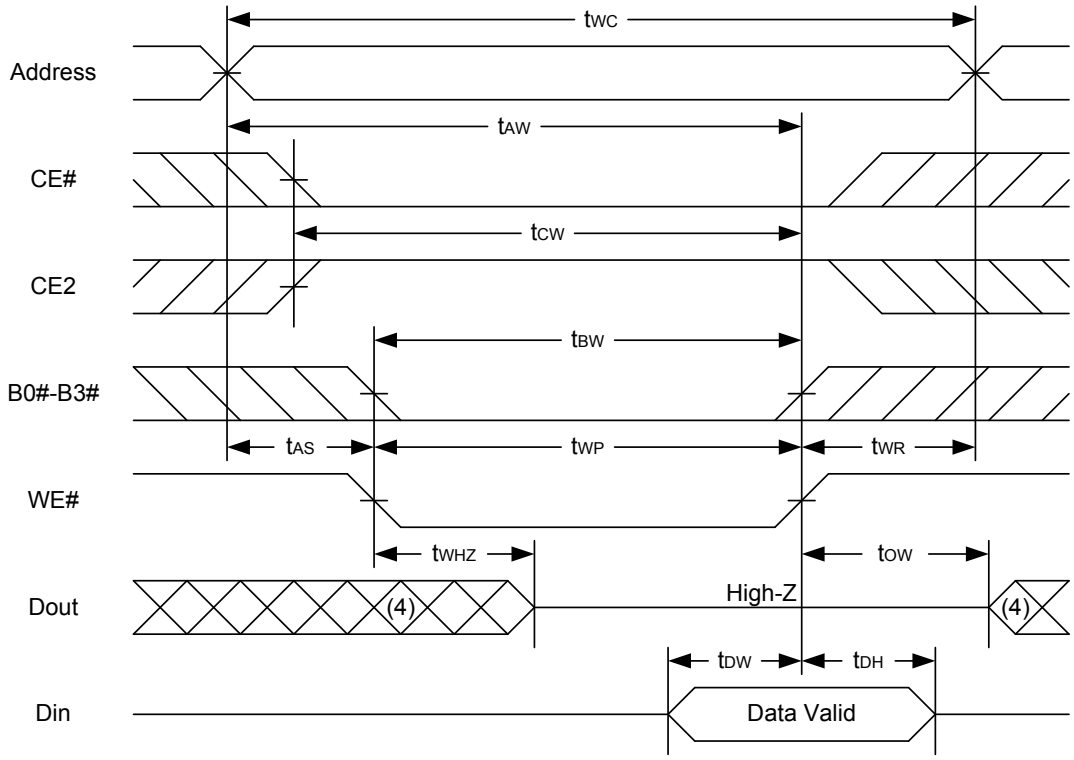


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

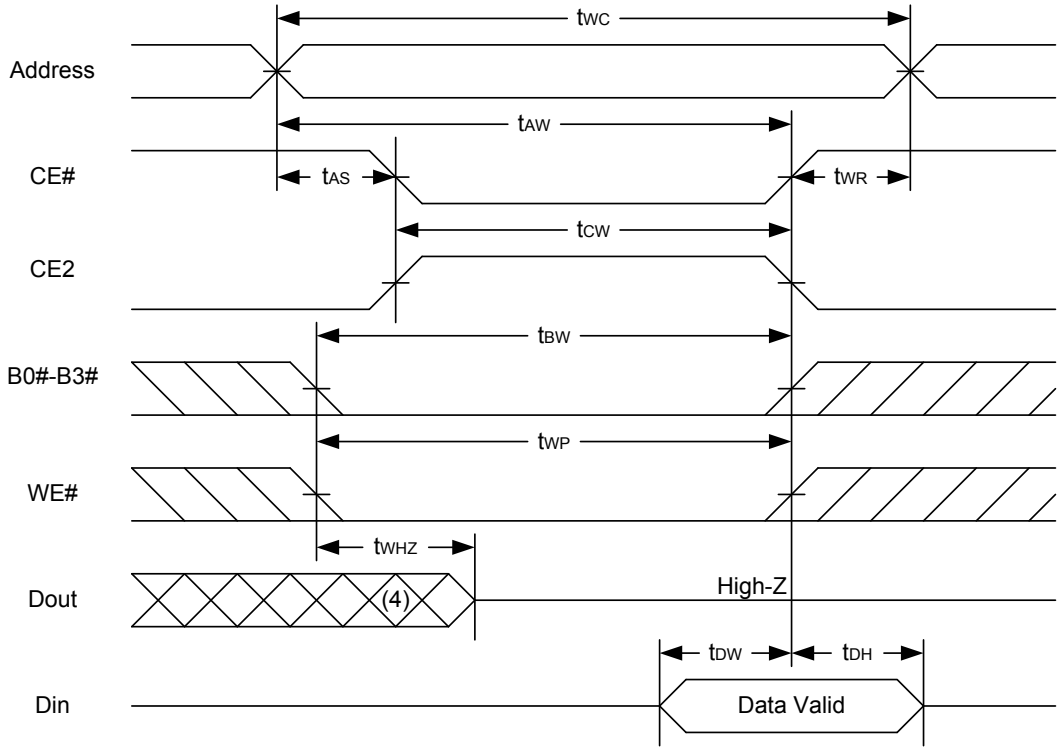


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low, CE2 = high, and B0#, B1#, B2# or B3# = low.
3.Address must be valid prior to or coincident with CE# = low, CE2 = high, and B0#, B1#, B2# or B3# = low transition; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

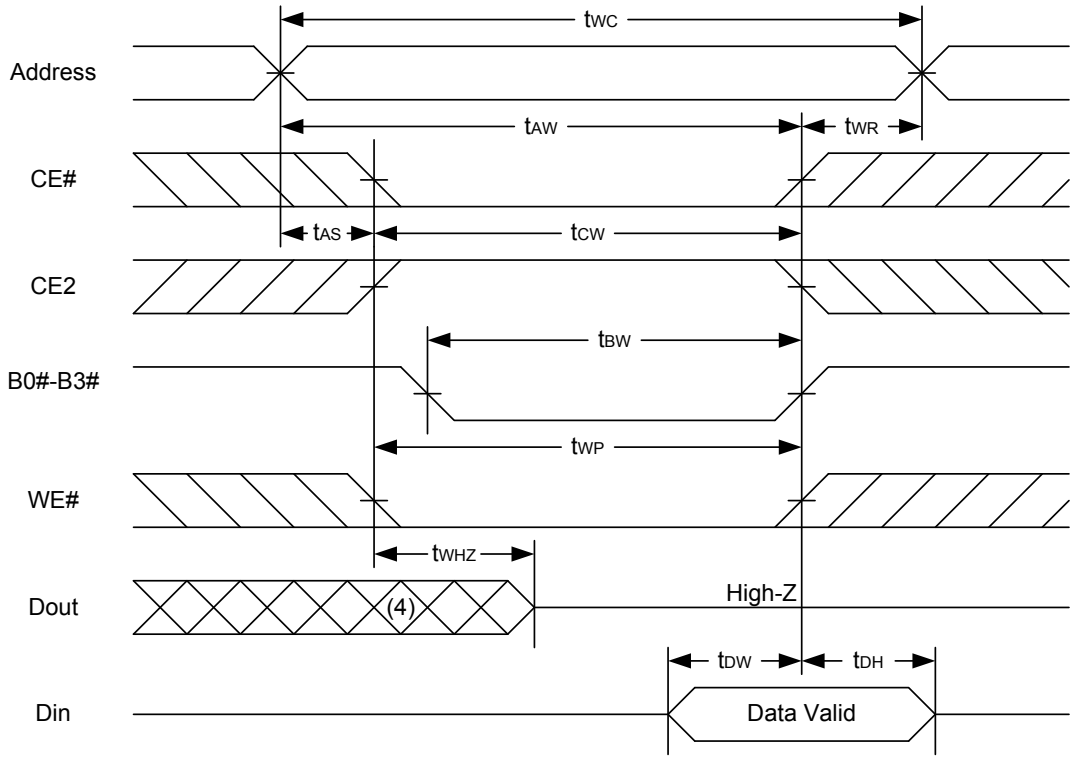
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



WRITE CYCLE 3 (B0# ~ B3# Controlled) (1,4,5)



Notes :
1. A write occurs during the overlap of a low CE#, high CE2, low WE#, and B0#, B1#, B2# or B3# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, B0# ~ B3# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

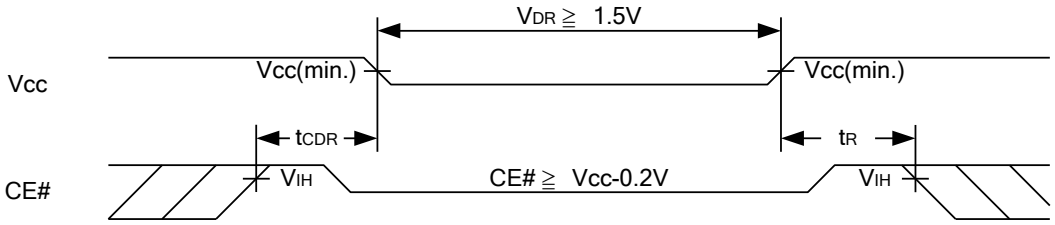
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V	1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V Other pins at 0.2V or V_{CC}-0.2V	-	4	40	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC*}	-	-	ns

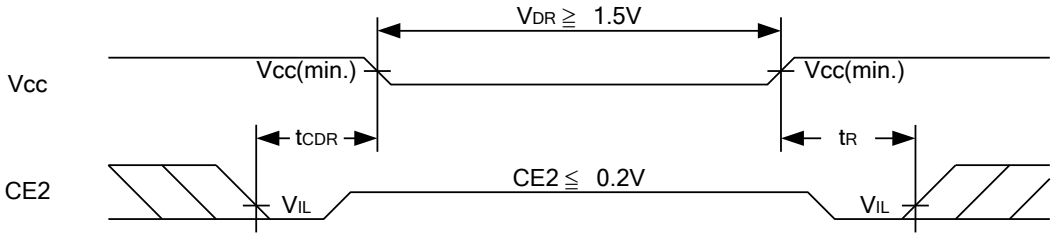
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)

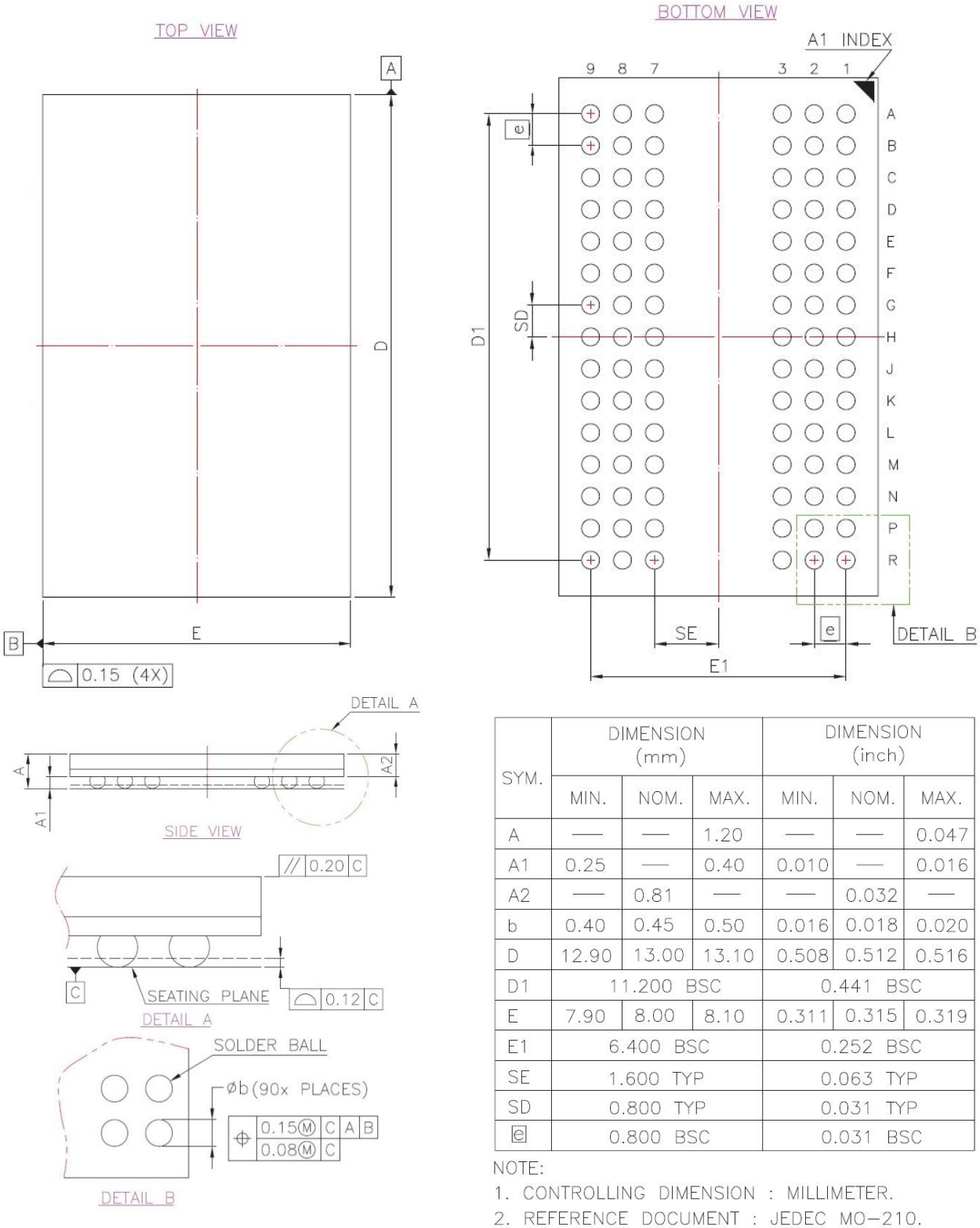


Low V_{CC} Data Retention Waveform (2) (CE2 controlled)



PACKAGE OUTLINE DIMENSION

90-ball 8mm × 13mm TFBGA Package Outline Dimension



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.25	—	0.40	0.010	—	0.016
A2	—	0.81	—	—	0.032	—
b	0.40	0.45	0.50	0.016	0.018	0.020
D	12.90	13.00	13.10	0.508	0.512	0.516
D1	11.200 BSC			0.441 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.400 BSC			0.252 BSC		
SE	1.600 TYP			0.063 TYP		
SD	0.800 TYP			0.031 TYP		
e	0.800 BSC			0.031 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-210.

PART NUMBERING SYSTEM

AS7C	351232	10	B	I	N
SRAM	3=3.3v 51232=512K x 32	10=10 ns	B = TFBGA	I=Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free

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