

512K X 32 BIT HIGH SPEED CMOS SRAM

# Revision History AS7C351232-10BIN 90ball TFBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Issue	Jan. 2017

Alliance Memory Inc. 511 Taylor Way, San Carlos, CA 94070 TEL: (650) 610-6800 FAX: (650) 620-9211 Alliance Memory Inc. reserves the right to change products or specification without notice

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#### 512K X 32 BIT HIGH SPEED CMOS SRAM

#### **FEATURES**

Fast access time: 10ns
 Low power consumption:
 Operating current: 125mA (TYP.)
 Standby current: 4mA (TYP.)

■ Single 3.3V power supply

■ All inputs and outputs TTL compatible

■ Fully static operation

■ Tri-state output

■ Data byte control : B0# (DQ0 ~ DQ7)

B1# (DQ8 ~ DQ15) B2# (DQ16~DQ23) B3# (DQ24~DQ31)

■ Data retention voltage : 1.5V (MIN.)

ROHS Compliant/Pb & Halogen free

■ Package: 90-ball 8mm x 13mm TFBGA

#### **GENERAL DESCRIPTION**

The AS7C351232-10BIN is a 16M-bit high speed CMOS static random access memory organized as 512K words by 32 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C351232-10BIN operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

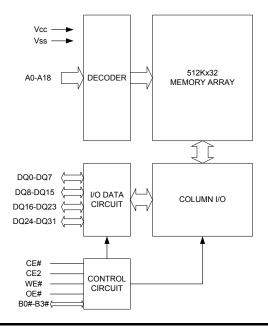
#### PRODUCT FAMILY

Product	Operating	V <sub>CC</sub> Range	Speed	Power Dissipation		
Family			Speed	Standby(I <sub>SB1</sub> ,TYP.)	Operating(Icc,TYP.)	
AS7C351232-10BIN	-40 ~ 85°C	2.7 ~ 3.6V	10ns	4mA	125mA	

#### **ORDERING INFORMATION**

Package Type	Access Time (Speed/ns)	Temperature Range(°C)	Packing Type	Alliance Part Number
90-ball (8mm x 13mm)	10 -40°C~85°C		Tray	AS7C351232-10BIN
TFBGA	.0		Tape Reel	AS7C351232-10BINTR

#### **FUNCTIONAL BLOCK DIAGRAM**

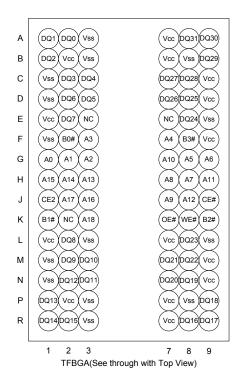


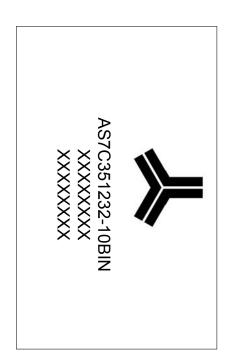
#### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - DQ31	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
B0# - B3#	Byte Control
Vcc	Power Supply
Vss	Ground
NC	No Connection



### **PIN CONFIGURATION**





TFBGA (Top View)

#### **ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V <sub>CC</sub> relative to V <sub>SS</sub>	V <sub>T1</sub>	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V <sub>T2</sub>	-0.5 to Vcc+0.5	V
Operating Temperature	T <sub>A</sub>	-40 to 85(I grade)	$^{\circ}$
Storage Temperature	T <sub>STG</sub>	-65 to 150	$^{\circ}$
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	Іоит	50	mA

<sup>\*</sup>Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

#### **TRUTH TABLE**

MODE	CE#	CE2	OE#	OE# WE# B0#		B1# B0#		B1#		I/O OPE	RATION		SUPPLY
WIODL	CL#	CLZ	OL#	VV L#	DU#	D1#	D0#	D1#	DQ0-7	DQ8-15	DQ16-23	DQ24-31	CURRENT
Standby	Н	Х	Х	Χ	Χ	Χ	Χ	Χ	High-Z	High-Z	High-Z	High-Z	I <sub>SB1</sub>
Stariuby	Х	L	Х	Х	Χ	Х	Х	Х	High-Z	High-Z	High-Z	High-Z	ISB1
Output Disable	L	Н	Н	Н	Χ	Χ	Χ	Χ	High-Z	High-Z	High-Z	High-Z	Icc
Output Disable	L	Н	Х	Х	Ι	Н	Η	Н	High-Z	High-Z	High-Z	High-Z	ICC
	L	Н	L	Н	L	Н	Н	Н	Dout	High-Z	High-Z	High-Z	
	L	Н	L	Н	Н	L	Н	Н	High-Z	Dout	High-Z	High-Z	
Read	L	Н	L	Н	Н	Н	L	Н	High-Z	High-Z	Dout	High-Z	Icc
	L	Н	L	Н	Н	Н	Н	L	High-Z	High-Z	High-Z	Dout	
	L	Н	L	Н	L	L	L	L	Dout	Dout	D <sub>оит</sub>	Dout	
	L	Н	Х	L	L	Н	Н	Н	Din	High-Z	High-Z	High-Z	
	L	Н	Χ	L	Η	L	Н	Н	High-Z	DIN	High-Z	High-Z	
Write	L	Н	Χ	L	Н	Н	L	Н	High-Z	High-Z	Din	High-Z	Icc
	L	Н	Х	L	Η	Н	Н	L	High-Z	High-Z	High-Z	Din	
	L	Н	Χ	L	┙	L	L	L	D <sub>IN</sub>	Din	Din	D <sub>IN</sub>	

Note:  $H = V_{IH}$ ,  $L = V_{IL}$ , X = Don't care.

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#### **DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYM.	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	Vcc			2.7	3.3	3.6	V
Input High Voltage	V <sub>IH</sub> *1			2.2	-	Vcc+0.3	V
Input Low Voltage	V <sub>IL</sub> *2			- 0.3	-	0.8	V
Input Leakage Current	ILI	$V_{CC} \ge V_{IN} \ge V_{SS}$		- 1	-	1	μA
Output Leakage Current	ILO	Vcc ≧ Vouт ≧ Vss, Output Disabled		- 1	-	1	μΑ
Output High Voltage	Vон	I <sub>OH</sub> = -4mA		2.4	-	-	V
Output Low Voltage	Vol	I <sub>OL</sub> = 8mA		-	-	0.4	V
Average Operating Power supply Current	Icc	CE# $\leq$ 0.2V and CE2 $\geq$ Vcc-0.2V, other pins at 0.2V or Vcc-0.2V, $I_{I/O}$ = 0mA; f=max.	-10	-	125	180	mA
Standby Power Supply Current	I <sub>SB1</sub>	CE# $\geq$ V <sub>CC</sub> - 0.2V; other pins at 0.2V or V <sub>CC</sub> -0.2V.	•	-	4	40	mA

- 1.  $V_{IH}(MAX.) = V_{CC} + 2.0V$  for pulse width less than 6ns. 2.  $V_{IL}(MIN.) = V_{SS} 2.0V$  for pulse width less than 6ns.
- 3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- 4. Typical values are included for reference only and are not guaranteed or tested. Typical valued are measured at  $V_{CC}$  =  $V_{CC}$ (TYP.) and  $T_A$  = 25 $^{\circ}$ C

#### **CAPACITANCE** $(T_A = 25^{\circ}C, f = 1.0MHz)$

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	Cin	-	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	10	pF

Note: These parameters are guaranteed by device characterization, but not production tested.

#### **AC TEST CONDITIONS**

Speed	10 ns
Input Pulse Levels	0.2V to V <sub>CC</sub> -0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	Vcc/2
Output Load	$C_L = 30pF + 1TTL$ , $I_{OH}/I_{OL} = -4mA/8mA$

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# 512K X 32 BIT HIGH SPEED CMOS SRAM

# **AC ELECTRICAL CHARACTERISTICS**

#### (1) READ CYCLE

PARAMETER	SYM.	AS7C351	UNIT	
PARAMETER	STIVI.	MIN.	MAX.	UNII
Read Cycle Time	t <sub>RC</sub>	10	-	ns
Address Access Time	taa	-	10	ns
Chip Enable Access Time	tace	-	10	ns
Output Enable Access Time	toe	-	4.5	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	2	-	ns
Output Enable to Output in Low-Z	toLz*	0	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	4	ns
Output Disable to Output in High-Z	tonz*	-	4	ns
Output Hold from Address Change	tон	2	-	ns
Byte Control Access Time	t <sub>BA</sub>	-	4.5	ns
Byte Control to High-Z Output	t <sub>BHZ</sub> *	-	4	ns
Byte Control to Low-Z Output	t <sub>BLZ</sub> *	0	-	ns

#### (2) WRITE CYCLE

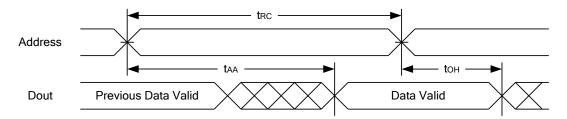
PARAMETER	SYM.	AS7C351	LINIT	
PARAIVIETER	STIVI.	MIN.	MAX.	UNIT
Write Cycle Time	twc	10	-	ns
Address Valid to End of Write	taw	8	-	ns
Chip Enable to End of Write	tcw	8	-	ns
Address Set-up Time	tas	0	-	ns
Write Pulse Width	twp	8	-	ns
Write Recovery Time	twR	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	6	-	ns
Data Hold from End of Write Time	tон	0	-	ns
Output Active from End of Write	tow*	2	-	ns
Write to Output in High-Z	twHz*	-	4	ns
Byte Control Valid to End of Write	t <sub>BW</sub>	8	-	ns

<sup>\*</sup>These parameters are guaranteed by device characterization, but not production tested.

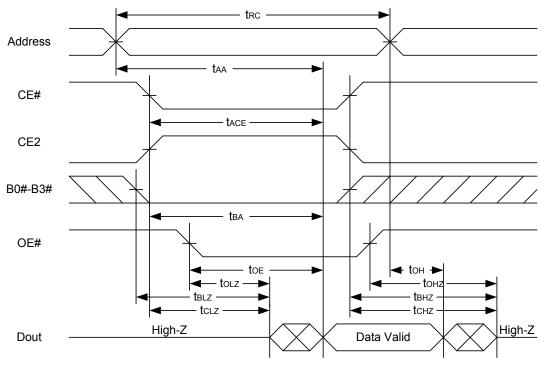
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#### **TIMING WAVEFORMS**

#### **READ CYCLE 1** (Address Controlled) (1,2)



#### READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



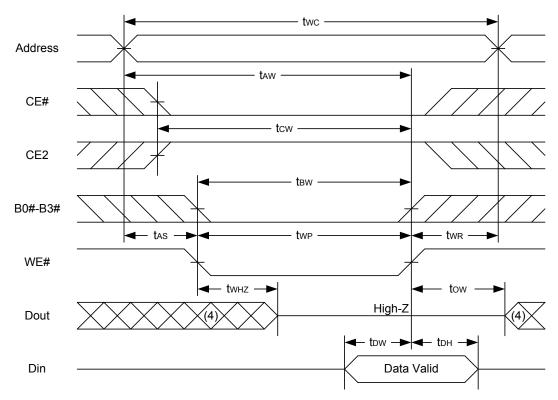
#### Notes:

- 1.WE# is high for read cycle.
- 2.Device is continuously selected OE# = low, CE# = low, CE2 = high, and B0#, B1#, B2# or B3# = low.
- 3.Address must be valid prior to or coincident with CE# = low, CE2 = high, and B0#, B1#, B2# or B3# = low transition; otherwise t<sub>AA</sub> is the limiting parameter.
- $4.t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are specified with  $C_L$  = 5pF. Transition is measured  $\pm 500$ mV from steady state.
- 5.At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{CLZ}$ .

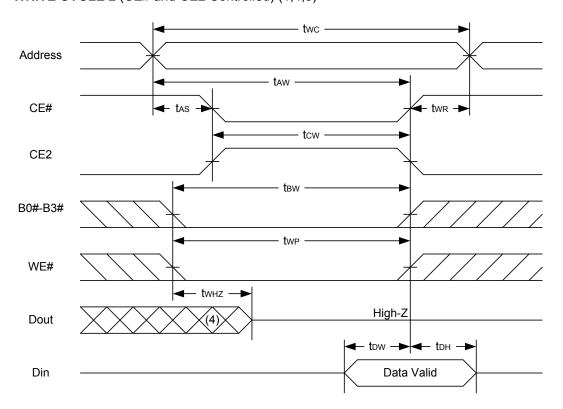
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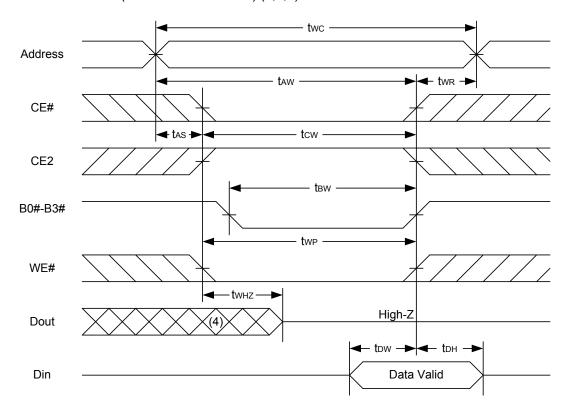
#### WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



#### WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



#### WRITE CYCLE 3 (B0# ~ B3# Controlled) (1,4,5)



- 1.A write occurs during the overlap of a low CE#, high CE2, low WE#, and B0#, B1#, B2# or B3# = low.
- 2. During a WE# controlled write cycle with OE# low, twp must be greater than twHZ + tow to allow the drivers to turn off and data to be placed on the bus.
- 3. During this period, I/O pins are in the output state, and input signals must not be applied.
  4. If the CE#, B0# ~ B3# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
- $5.t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L$  = 5pF. Transition is measured  $\pm 500$ mV from steady state.

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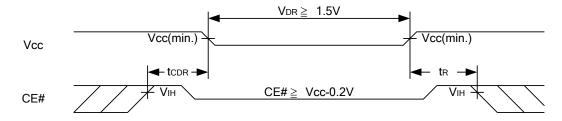
#### **DATA RETENTION CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	$V_{DR}$	$CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$	1.5	-	3.6	V
Data Retention Current	$I_{DR}$	$V_{CC}$ = 1.5V $CE\# \geq V_{CC}$ - 0.2V or $CE2 \leq 0.2V$ Other pins at 0.2V or $V_{CC}$ -0.2V	1	4	40	mA
Chip Disable to Data Retention Time	tcdr	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	<b>t</b> R		t <sub>RC*</sub>	-	-	ns

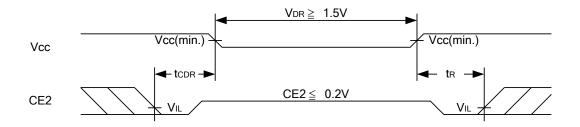
t<sub>RC\*</sub> = Read Cycle Time

### **DATA RETENTION WAVEFORM**

Low Vcc Data Retention Waveform (1) (CE# controlled)



#### Low Vcc Data Retention Waveform (2) (CE2 controlled)

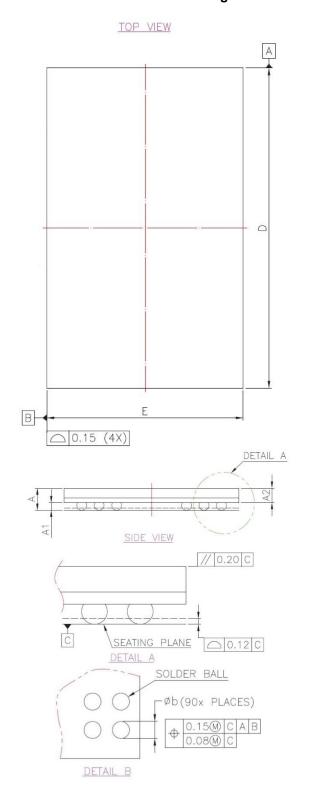


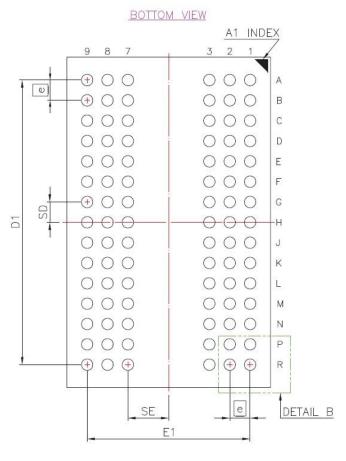
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#### PACKAGE OUTLINE DIMENSION

#### 90-ball 8mm × 13mm TFBGA Package Outline Dimension





CVII	DIMENSION (mm)			DIMENSION (inch)			
SYM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А			1.20	s <del></del> -		0.047	
A1	0.25		0.40	0.010		0.016	
A2	-	0.81	2 <del></del> 27		0.032		
b	0.40	0.45	0.50	0.016	0.018	0.020	
D	12.90	13.00	13.10	0.508	0.512	0.516	
D1	1	1.200 E	BSC	0.441 BSC			
E	7.90	8.00	8.10	0.311	0.315	0.319	
E1	6.400 BSC			0.252 BSC			
SE	1.600 TYP			0.063 TYP			
SD	0	.800 TY	'P	0.031 TYP			
е	0.800 BSC			0.031 BSC			

#### NOTE:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. REFERENCE DOCUMENT : JEDEC MO-210.

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#### PART NUMBERING SYSTEM

AS7C	351232	10	В	_	N
SRAM	3=3.3v 51232=512K x 32	10=10 ns	B = TFBGA	I=Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free



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