

**RevisionHistory**

512 Kb x16 Pseudo Static RAM

**48ball-FPBGA**

| Revision | Details               | Date      |
|----------|-----------------------|-----------|
| Rev 1.0  | Preliminary datasheet | Aug. 2018 |

## GENERAL DESCRIPTION

The AS1C512K16P-70BIN is 8,388,608 bits of Pseudo SRAM which uses DRAM type memory cells, but this device has refresh-free operation and extreme low power consumption technology. Furthermore the interface is compatible to a low power Asynchronous type SRAM. The AS1C512K16P-70BIN is organized as 524,288 Words x 16 bit.

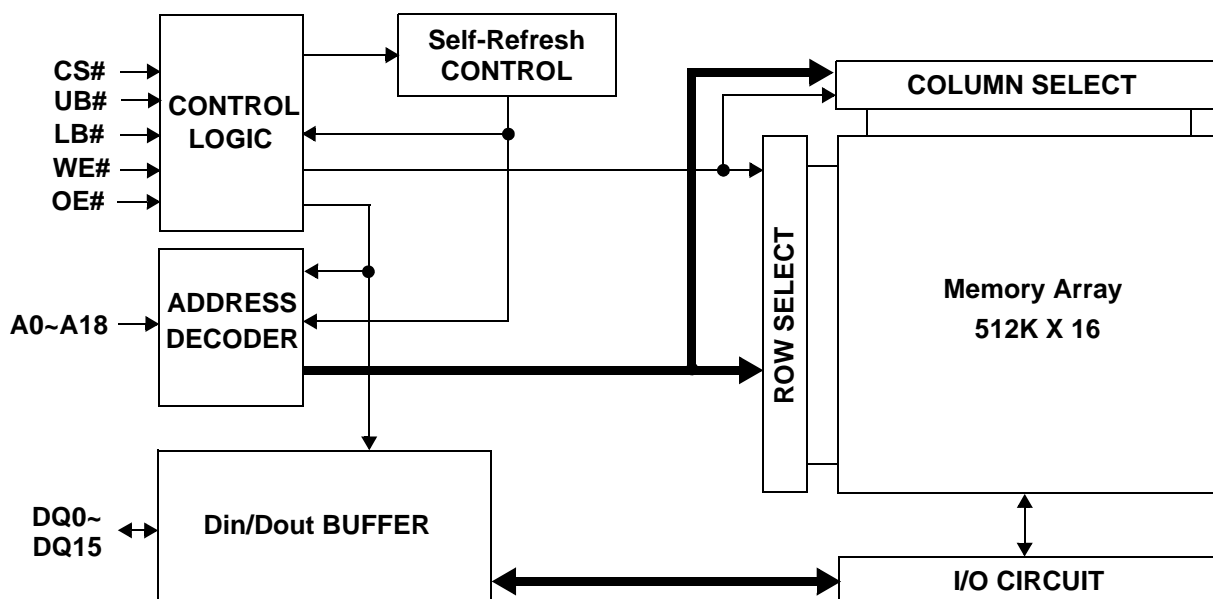
## FEATURES

- Organization :512K x16
- Address access speed 70ns
- Power Supply Voltage : 2.6 ~ 3.3V
- Separated I/O power(VccQ) & Core power(Vcc)
- Three state outputs
- Byte read/write control by UB# / LB#
- Auto-TCSR for power saving
- Package type : 48-FPBGA 6.0x7.0
- Operating Temperature
  - . Industrial : -40 °C ~ 85 °C

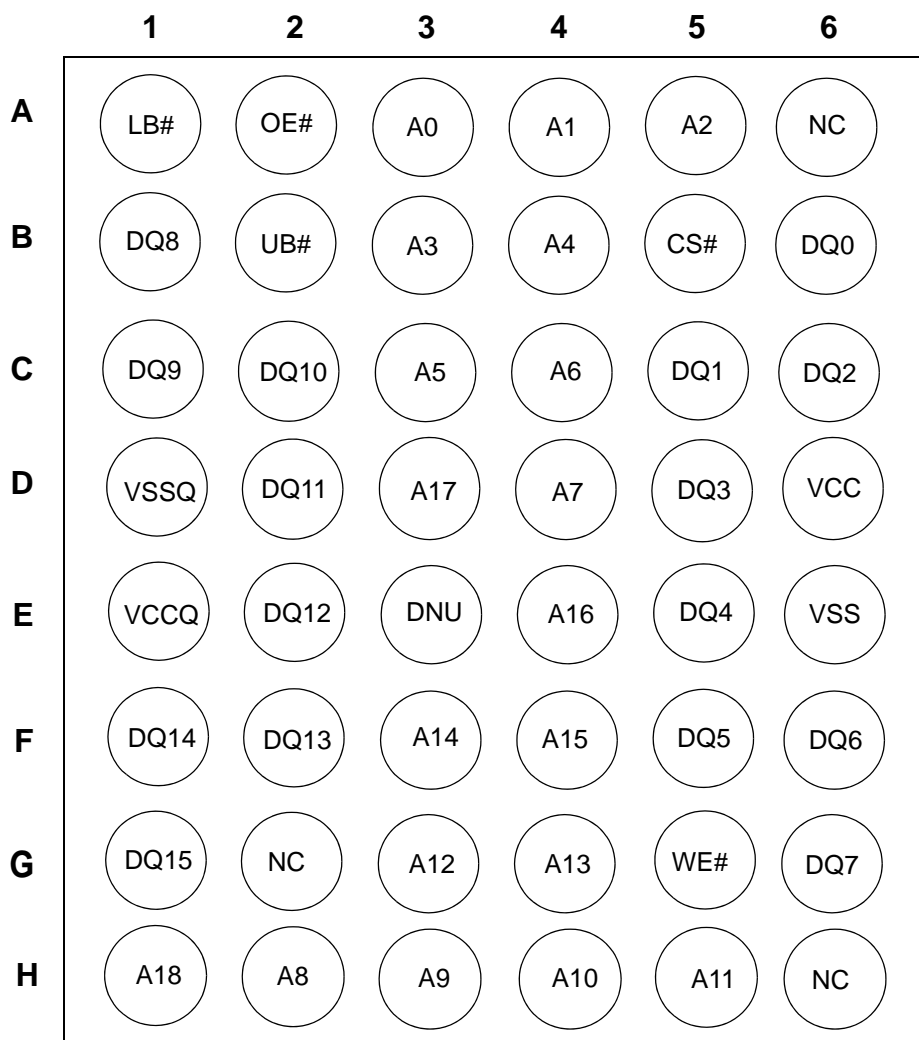
## PRODUCT FAMILY

| Part Number       | Operating Temp. | Power Supply | Speed (t <sub>RC</sub> ) | Power Dissipation                |                                   |   |
|-------------------|-----------------|--------------|--------------------------|----------------------------------|-----------------------------------|---|
|                   |                 |              |                          | Standby (I <sub>SB</sub> , Max.) | Operating I <sub>CC</sub> ( Max.) |   |
|                   |                 |              |                          |                                  | I <sub>CC1</sub> ( f = 1MHz)      | I <sub>CC2</sub> ( f = f <sub>max</sub> ) |
| AS1C512K16P-70BIN | -40 °C to 85 °C | 2.6V to 3.3V | 70ns                     | 120uA                            | 5mA                               | 25mA                                      |

## FUNCTION BLOCK DIAGRAM



## PIN DESCRIPTION ( 48-FPBGA-6.00x7.00 )



**TOP VIEW (Ball Down)**

| Name               | Function            | Name   | Function                         |
|--------------------|---------------------|--------|----------------------------------|
| CS#                | Chip select input   | LB#    | Lower byte (DQ <sub>0-7</sub> )  |
| OE#                | Output enable input | UB#    | Upper byte (DQ <sub>8-15</sub> ) |
| WE#                | Write enable input  | VCC    | Power supply                     |
| DQ <sub>0-15</sub> | Data in-out         | VCCQ   | I/O power supply                 |
| A <sub>0-18</sub>  | Address inputs      | VSS(Q) | Ground                           |
| DNU                | Do not use          | NC     | No connection                    |

## ABSOLUTE MAXIMUM RATINGS <sup>1)</sup>

| Parameter                             |            | Symbol                             | Ratings                                      | Unit |
|---------------------------------------|------------|------------------------------------|--|------|
| Voltage on Any Pin Relative to Vss    |            | V <sub>IN</sub> , V <sub>OUT</sub> | -0.2 to V <sub>CCQ</sub> +0.3                | V    |
| Voltage on Vcc supply relative to Vss |            | V <sub>CC</sub> , V <sub>CCQ</sub> | -0.2 <sup>2)</sup> to V <sub>CCQ</sub> +0.3V | V    |
| Power Dissipation                     |            | P <sub>D</sub>                     | 1.0  | W    |
| Storage Temperature                   |            | T <sub>STG</sub>                   | -65 to 150                                   | °C   |
| Operating Temperature                 | Industrial | T <sub>A</sub>                     | -40 to 85                                    | °C   |

- Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device.  
Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Undershoot at power-off : -1.0V in case of pulse width ≤ 20ns

## FUNCTIONAL DESCRIPTION

| CS# | OE# | WE# | LB# | UB# | DQ <sub>0~7</sub> | DQ <sub>8~15</sub> | Mode             | Power    |
|-----|-----|-----|-----|-----|-------------------|--------------------|------------------|----------|
| H   | X   | X   | X   | X   | High-Z            | High-Z             | Deselected       | Stand by |
| L   | H   | H   | L   | X   | High-Z            | High-Z             | Output Disabled  | Active   |
| L   | H   | H   | X   | L   | High-Z            | High-Z             | Output Disabled  | Active   |
| L   | L   | H   | L   | H   | Data Out          | High-Z             | Lower Byte Read  | Active   |
| L   | L   | H   | H   | L   | High-Z            | Data Out           | Upper Byte Read  | Active   |
| L   | L   | H   | L   | L   | Data Out          | Data Out           | Word Read        | Active   |
| L   | X   | L   | L   | H   | Data In           | High-Z             | Lower Byte Write | Active   |
| L   | X   | L   | H   | L   | High-Z            | Data In            | Upper Byte Write | Active   |
| L   | X   | L   | L   | L   | Data In           | Data In            | Word Write       | Active   |

Note:

- X means don't care. (Must be low or high state)

## RECOMMENDED DC OPERATING CONDITIONS

| Parameter          | Symbol            | Min             | Typ | Max                  | Unit |
|--------------------|-------------------|-----------------|-----|----------------------|------|
| Supply voltage     | $V_{CC}$          | 2.6             | 3.0 | 3.3                  | V    |
|                    | $V_{CCQ}$         | 2.6             | 3.0 | 3.3                  | V    |
| Ground             | $V_{SS}, V_{SSQ}$ | 0               | 0   | 0                    | V    |
| Input high voltage | $V_{IH}$          | $0.8 * V_{CCQ}$ | -   | $V_{CCQ} + 0.2^{1)}$ | V    |
| Input low voltage  | $V_{IL}$          | $-0.2^{2)}$     | -   | $0.2 * V_{CCQ}$      | V    |

1. Overshoot:  $V_{CC} + 1.0$  V in case of pulse width  $\leq 20$ ns
2. Undershoot:  $-1.0$  V in case of pulse width  $\leq 20$ ns
3. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> ( $f=1$ MHz, $T_A=25^{\circ}\text{C}$ )

| Item                     | Symbol   | Test Condition | Min | Max | Unit |
|--------------------------|----------|----------------|-----|-----|------|
| Input capacitance        | $C_{IN}$ | $V_{IN}=0$ V   | -   | 8   | pF   |
| Input/Output capacitance | $C_{IO}$ | $V_{IO}=0$ V   | -   | 8   | pF   |

1. Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

| Parameter                 | Symbol    | Test Conditions   | Min             | Typ | Max             | Unit          |
|---------------------------|-----------|---|-----------------|-----|-----------------|---------------|
| Input leakage current     | $I_{LI}$  | $V_{IN}=V_{SS}$ to $V_{CCQ}$ , $V_{CC}=V_{CCmax}$   | -1              | -   | 1               | $\mu\text{A}$ |
| Output leakage current    | $I_{LO}$  | $CS\# = V_{IH}$ , $OE\# = V_{IH}$ or $WE\# = V_{IL}$ ,<br>$V_{IO}=V_{SS}$ to $V_{CCQ}$ , $V_{CC}=V_{CCmax}$   | -1              | -   | 1               | $\mu\text{A}$ |
| Average operating current | $I_{CC1}$ | Cycle time = 1 $\mu\text{s}$ , $I_{IO}=0$ mA, 100% duty,<br>$CS\# \leq 0.2$ V,<br>$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CCQ} - 0.2$ V  | -               | -   | 5               | mA            |
|                           | $I_{CC2}$ | Cycle time = Min, $I_{IO}=0$ mA, 100% duty,<br>$CS\# = V_{IL}$ , $V_{IN}=V_{IL}$ or $V_{IH}$  | -               | -   | 25              | mA            |
| Output low voltage        | $V_{OL}$  | $I_{OL} = 0.5$ mA, $V_{CC}=V_{CCmin}$   | -               | -   | $0.2 * V_{CCQ}$ | V             |
| Output high voltage       | $V_{OH}$  | $I_{OH} = -0.5$ mA, $V_{CC}=V_{CCmin}$  | $0.8 * V_{CCQ}$ | -   | -               | V             |
| Standby current (CMOS)    | $I_{SB}$  | $CS\# \geq V_{CCQ} - 0.2$ V, Other inputs = 0 ~ $V_{CCQ}$<br>(Typ. condition : $V_{CC}=3.0$ V @ $25^{\circ}\text{C}$ )<br>(Max. condition : $V_{CC}=3.3$ V @ $85^{\circ}\text{C}$ ) | -               | -   | 120             | $\mu\text{A}$ |

1. Maximum  $I_{CC}$  specifications are tested with  $V_{CC} = V_{CCmax}$ .

## AC OPERATING CONDITIONS

**Test Conditions** (Test Load and Test Input/Output Reference)

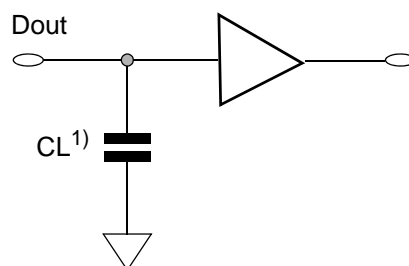
Input Pulse Level : 0.2V to  $V_{CCQ}-0.2V$

Input Rise and Fall Time : 5ns

Input and Output reference Voltage :  $V_{CCQ}/2$

Output Load (See right) :  $CL^{(1)} = 30pF$

1. Including scope and Jig capacitance

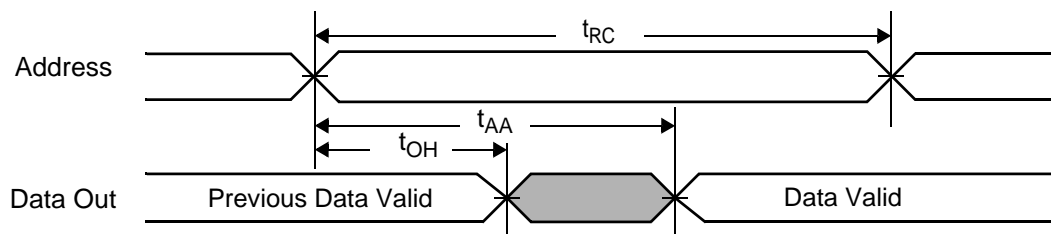


## AC CHARACTERISTICS

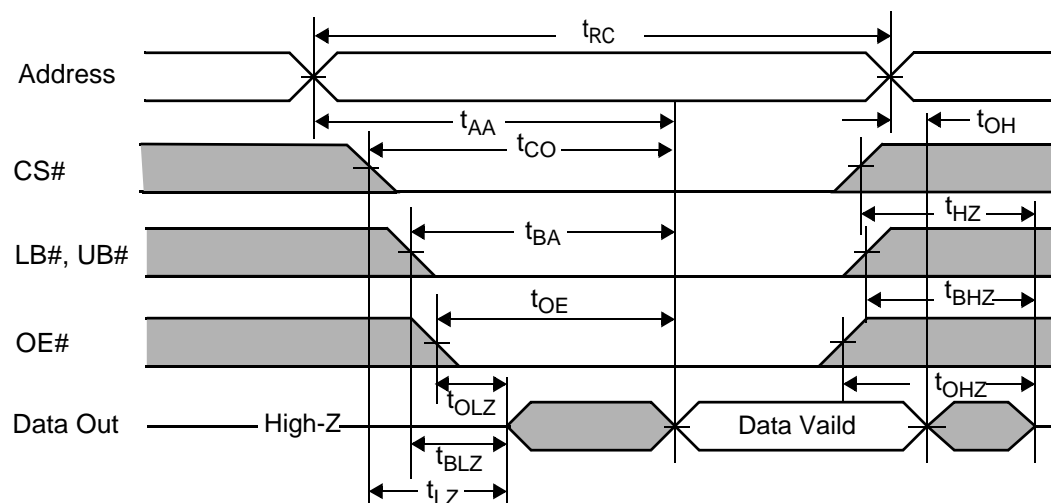
| Parameter List |                                   | Symbol    | Speed |     | Unit |
|----------------|-----------------------------------|-----------|-------|-----|------|
|                |                                   |           | Min   | Max |      |
| Read           | Read Cycle Time                   | $t_{RC}$  | 70    | 10k | ns   |
|                | Address access time               | $t_{AA}$  | -     | 70  | ns   |
|                | Chip enable to data output        | $t_{CO}$  | -     | 70  | ns   |
|                | Output enable to valid output     | $t_{OE}$  | -     | 25  | ns   |
|                | UB#, LB# enable to data output    | $t_{BA}$  | -     | 25  | ns   |
|                | Chip enable to low-Z output       | $t_{LZ}$  | 10    | -   | ns   |
|                | UB#, LB# enable to low-Z output   | $t_{BLZ}$ | 0     | -   | ns   |
|                | Output enable to low-Z output     | $t_{OLZ}$ | 0     | -   | ns   |
|                | Chip disable to high-Z output     | $t_{HZ}$  | 0     | 20  | ns   |
|                | UB#, LB# disable to high-Z output | $t_{BHZ}$ | 0     | 20  | ns   |
|                | Output disable to high-Z output   | $t_{OHZ}$ | 0     | 20  | ns   |
|                | Output hold from Address change   | $t_{OH}$  | 5     | -   | ns   |
| Write          | Write Cycle Time                  | $t_{WC}$  | 70    | 10k | ns   |
|                | Chip enable to end of write       | $t_{CW}$  | 60    | -   | ns   |
|                | Address setup time                | $t_{AS}$  | 0     | -   | ns   |
|                | Address valid to end of write     | $t_{AW}$  | 60    | -   | ns   |
|                | UB#, LB# valid to end of write    | $t_{BW}$  | 60    | -   | ns   |
|                | Write pulse width                 | $t_{WP}$  | 50    | -   | ns   |
|                | Write recovery time               | $t_{WR}$  | 0     | -   | ns   |
|                | Write to output high-Z            | $t_{WHZ}$ | 0     | 20  | ns   |
|                | Data to write time overlap        | $t_{DW}$  | 20    | -   | ns   |
|                | Data hold from write time         | $t_{DH}$  | 0     | -   | ns   |
|                | End write to output low-Z         | $t_{OW}$  | 5     | -   | ns   |

## TIMING DIAGRAMS

**READ CYCLE (1)** (Address controlled, CS#=OE#=V<sub>IL</sub>, WE#=V<sub>IH</sub>, UB# or/and LB#=V<sub>IL</sub>)



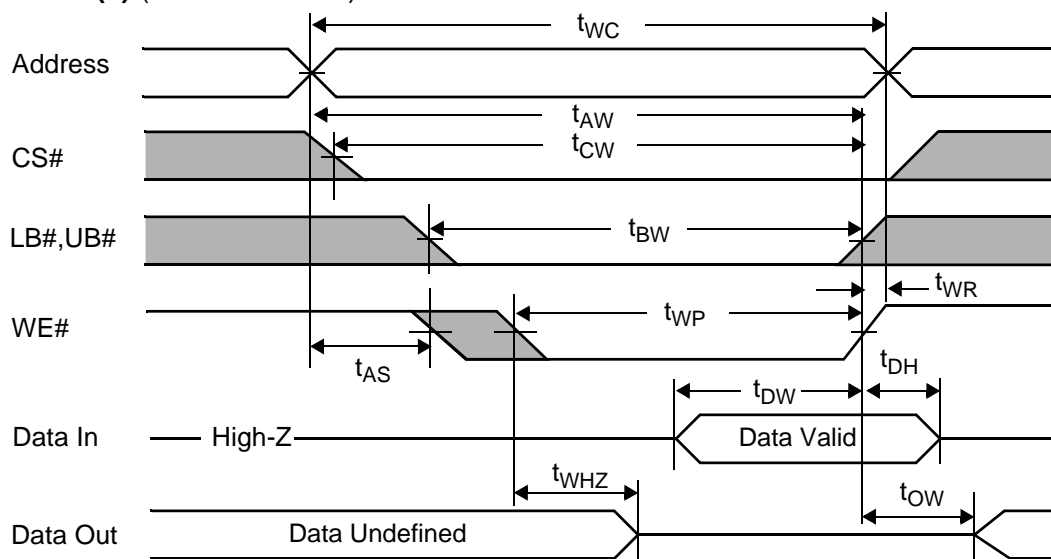
**READ CYCLE (2)** (WE#=V<sub>IH</sub>)



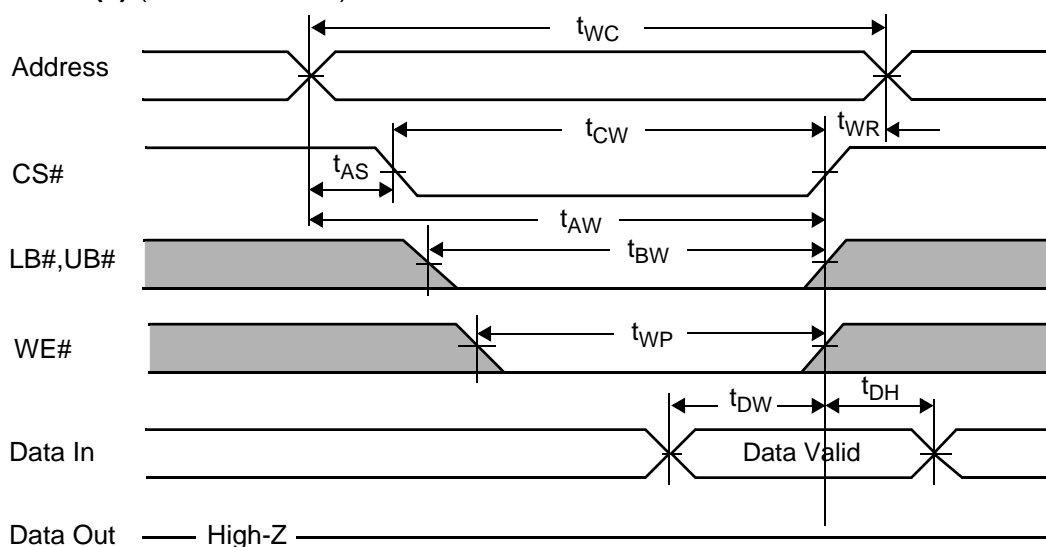
### NOTES (READ CYCLE)

1.  $t_{HZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than  $t_{RC}$  for continuous periods > 10us.

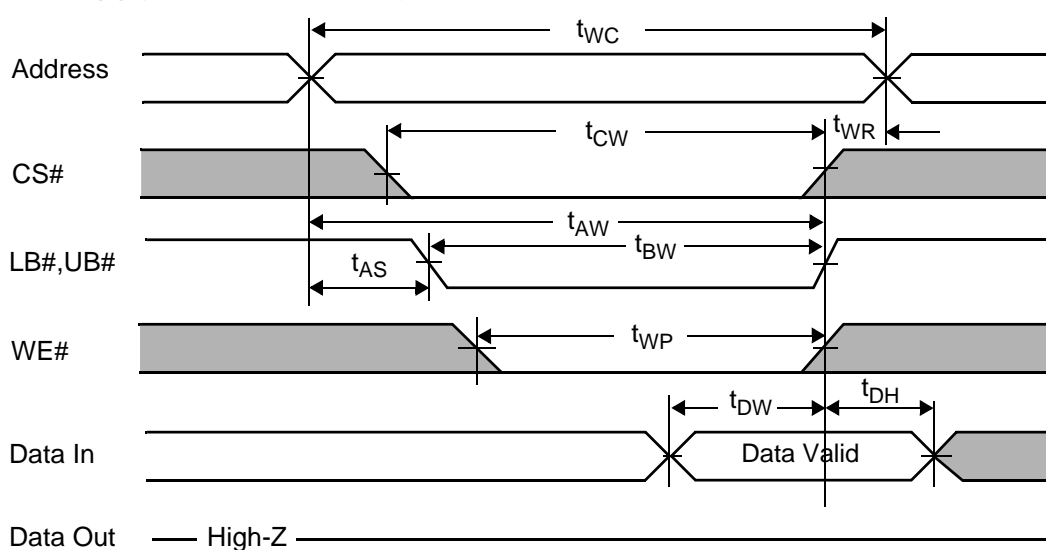
## WRITE CYCLE (1) (WE# controlled)



## WRITE CYCLE (2) (CS# controlled)



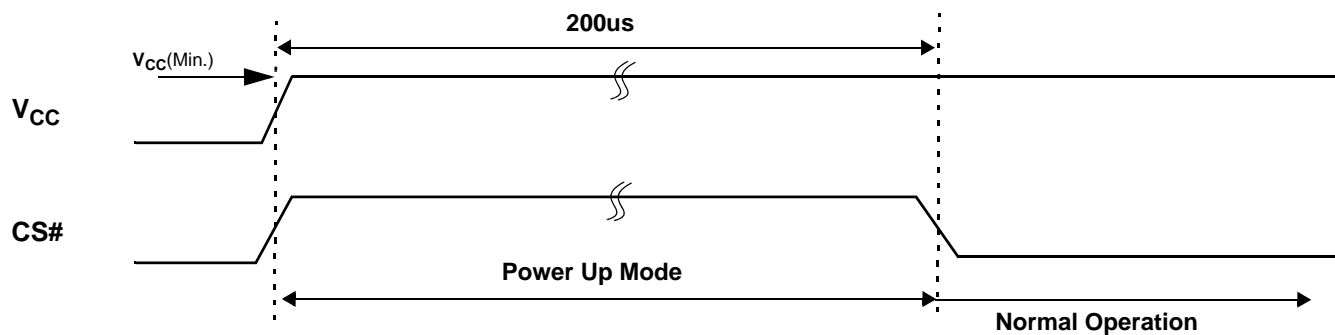
## WRITE CYCLE (3) (UB#/LB# controlled)



**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap( $t_{WP}$ ) of low CS#, low WE# and low UB# or LB#. A write begins at the last transition among low CS# and low WE# with asserting UB# or LB# low for single byte operation or simultaneously asserting UB# and LB# low for word operation. A write ends at the earliest transition among high CS# and high WE#. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from CS# going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as CS# or WE# going high.
5. Do not access device with cycle timing shorter than  $t_{WC}$  for continuous periods > 10us.

## TIMING WAVEFORM OF POWER UP



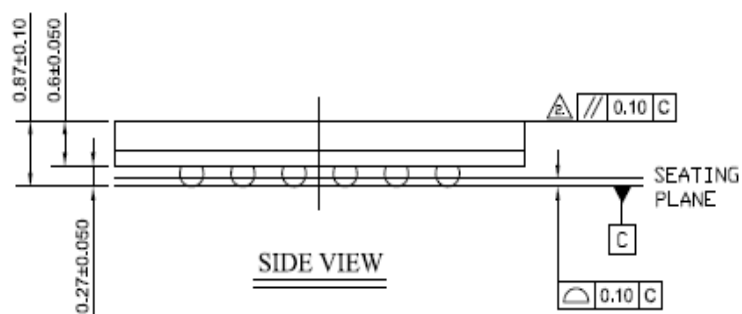
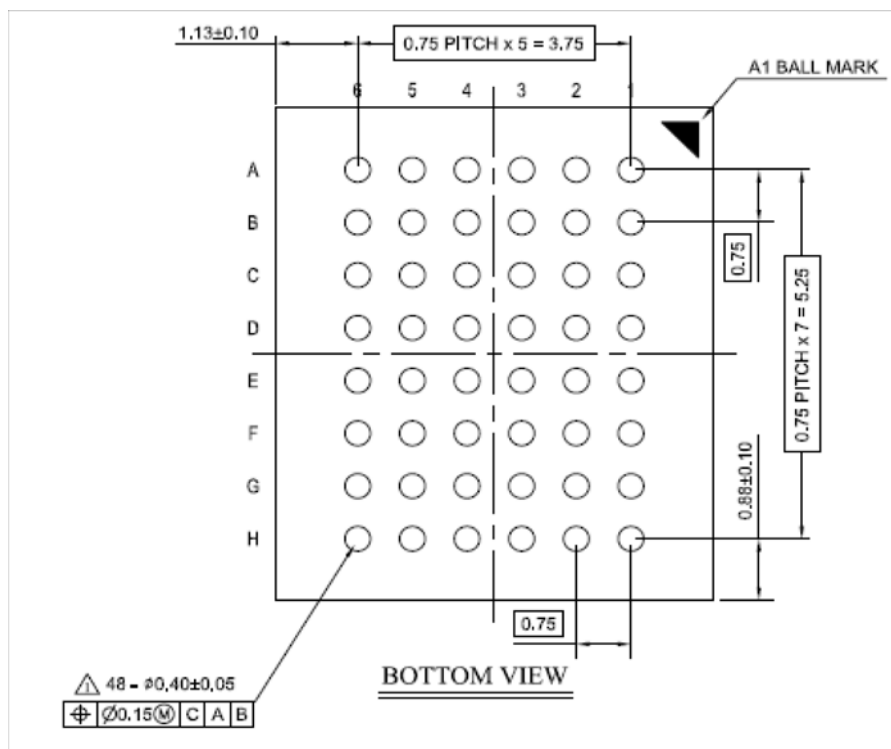
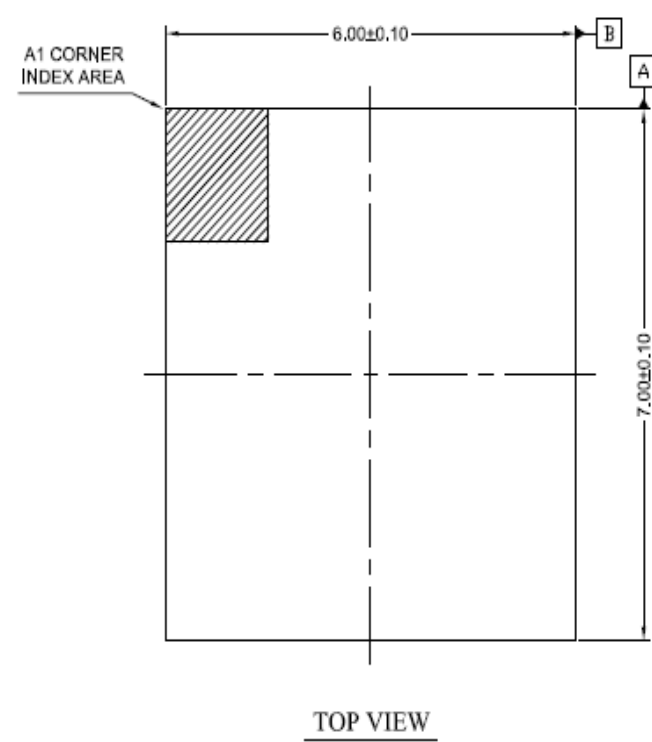
### NOTE ( POWER UP )

1. After  $V_{CC}$  reaches  $V_{CC}(\text{Min.})$  , wait  $200\mu\text{s}$  with  $CS\#$  high. Then you get into the normal operation.



Unit: millimeters

## PACKAGE DIMENSION

48 Ball Fine Pitch BGA (0.75mm ball pitch)



NOTE :

1. ALL DIMENSION ARE IN MILLIMETERS.
2.  POST REFLOW SOLDER BALL DIAMETER.  
(Pre Reflow Diameter :  $0.35 \pm 0.02$ )
3.  TOLERANCE INCLUDES WARPAGE.

## PART NUMBERING SYSTEM

| AS1C        | 512K16P                             | -70  | B        | I                               | N                                | XX                                   |
|-------------|-------------------------------------|------|----------|---------------------------------|----------------------------------|--------------------------------------|
| PSEUDO SRAM | 512K16=512kb x 16<br>P= PSEUDO SRAM | 70ns | B = FBGA | I=Industrial<br>(-40° C~+85° C) | Indicates Pb and<br>Halogen Free | Packing Type<br>None:Tray<br>TR:Reel |



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