Revision History
1024K x 8 BIT SUPER LOW POWER CMOS SRAM

Revision	Details	Date
Rev 1.0	Initial Release	Nov 2020
Rev 1.1	Introduce AS6C8008B-45BIN part (48ball TFBGA 6x8mm)	April 2023

FEATURES

- Fast access time: 45/55ns
- Low power consumption:
  Operating current: 12/11mA (Typ.)
  Standby current: 2.5µA (Typ.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage: 1.5V (Min.)
- Package:
  44-pin 400 mil TSOP II
  48-ball 6x8mm TFBGA

GENERAL DESCRIPTION

The AS6C8008B is an 8,388,608-bit low power CMOS static random access memory organized as 1,048,576 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

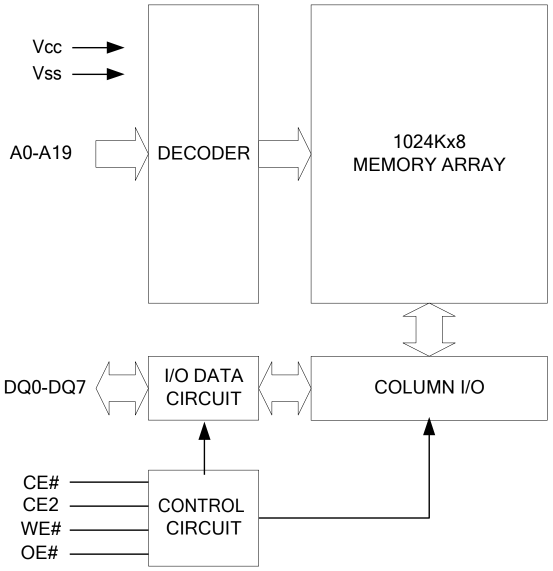
The AS6C8008B is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C8008B operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V_{CC} Range	Speed	Power Dissipation	
				Standby (I_{SB1},Typ.)	Operating (I_{CC},Typ.)
AS6C8008B	-40 ~ 85℃	2.7 ~ 3.6V	45ns	2.5µA	12mA
AS6C8008B	-40 ~ 85℃	2.7 ~ 3.6V	55ns	2.5µA	11mA

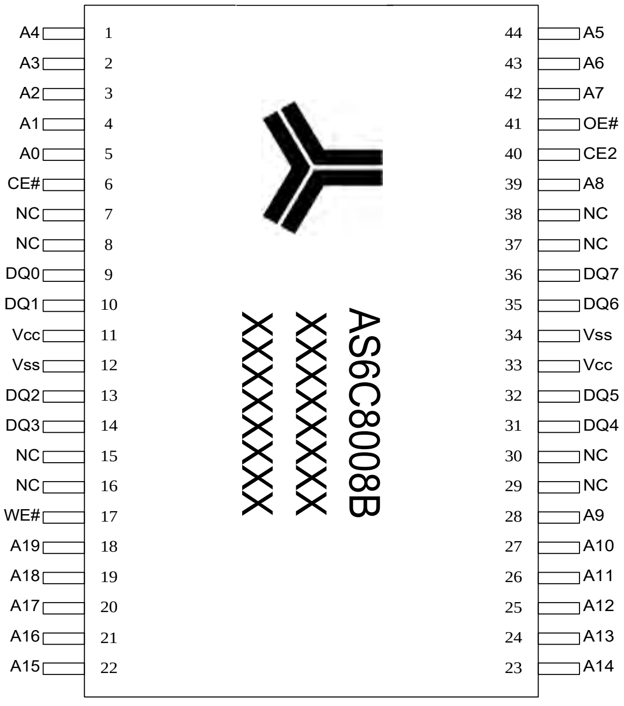
FUNCTIONAL BLOCK DIAGRAM



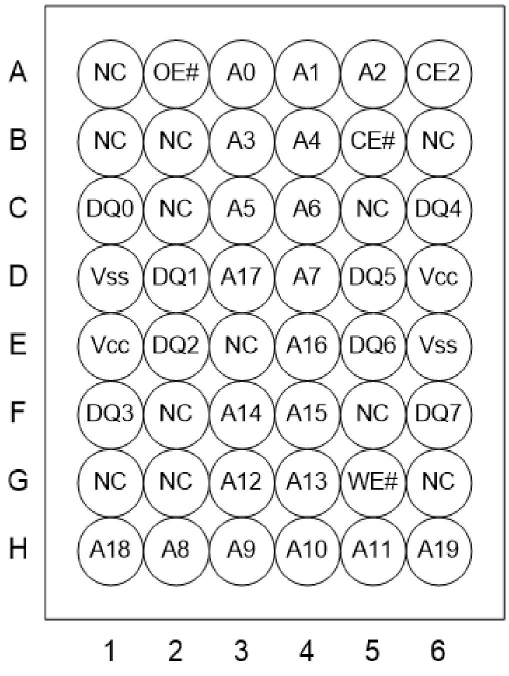
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION



TSOP II



	1	2	3	4	5	6
A	NC	OE#	A0	A1	A2	CE2
B	NC	NC	A3	A4	CE#	NC
C	DQ0	NC	A5	A6	NC	DQ4
D	Vss	DQ1	A17	A7	DQ5	Vcc
E	Vcc	DQ2	NC	A16	DQ6	Vss
F	DQ3	NC	A14	A15	NC	DQ7
G	NC	NC	A12	A13	WE#	NC
H	A18	A8	A9	A10	A11	A19

TFBGA(See through with Top View)

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	-40 to 85	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I_{SB1}
	X	L	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	H	High-Z	I_{CC},I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC},I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC},I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.[*4]	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.0	3.6	V
Input High Voltage	V_{IH}[*1]			2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}[*2]			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$ Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.2	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE#≦0.2V and CE2≧V_{CC}-0.2V $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V	- 45	-	12	20	mA
			- 55	-	11	18	mA
	I_{CC1}	Cycle time = 1µs CE#≦0.2V and CE2≧V_{CC}-0.2V $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V		-	3	5	mA
Standby Power Supply Current	I_{SB1}	CE# ≧V_{CC} -0.2V or CE2≦0.2V Other pins at 0.2V or V_{CC} -0.2V	40℃	-	2.5	5	µA[*5]
				-	2.5	20	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 6ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃
5. This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS6C8008B-45		AS6C8008B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	45	-	55	-	ns
Address Access Time	t_{AA}	-	45	-	55	ns
Chip Enable Access Time	t_{ACE}	-	45	-	55	ns
Output Enable Access Time	t_{OE}	-	25	-	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	15	-	20	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	15	-	20	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	ns

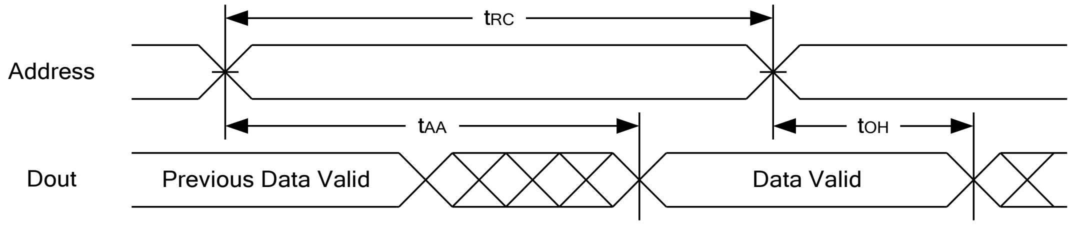
(2) WRITE CYCLE

PARAMETER	SYM.	AS6C8008B-45		AS6C8008B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	45	-	55	-	ns
Address Valid to End of Write	t_{AW}	40	-	50	-	ns
Chip Enable to End of Write	t_{CW}	40	-	50	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	45	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	20	ns

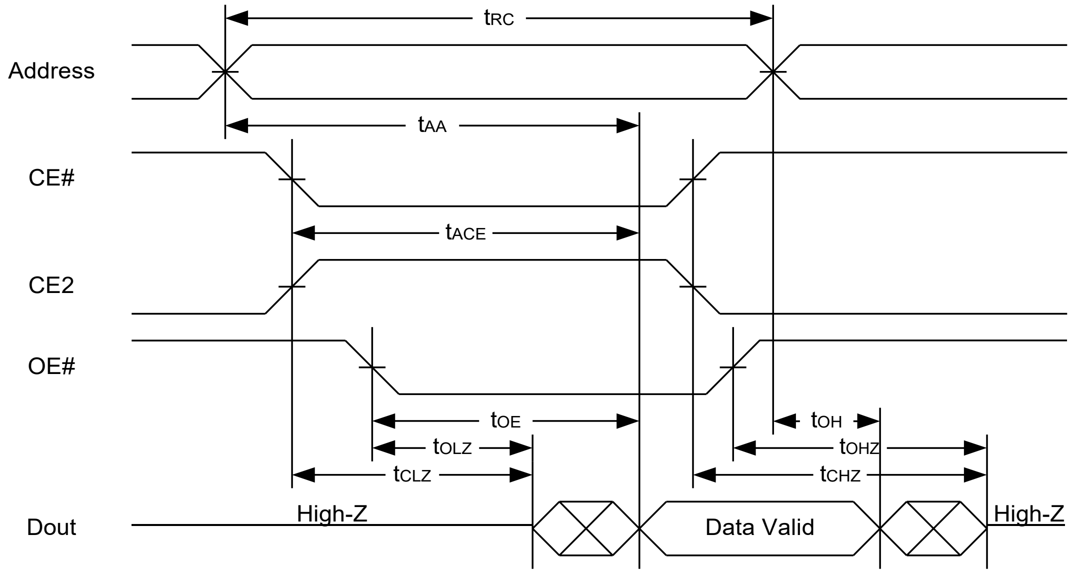
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

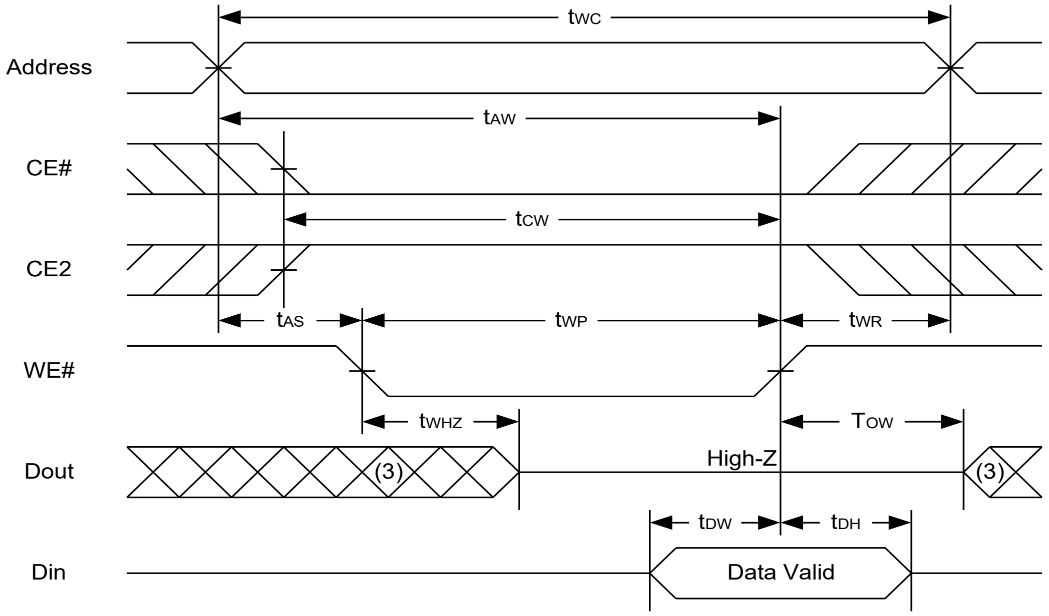


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

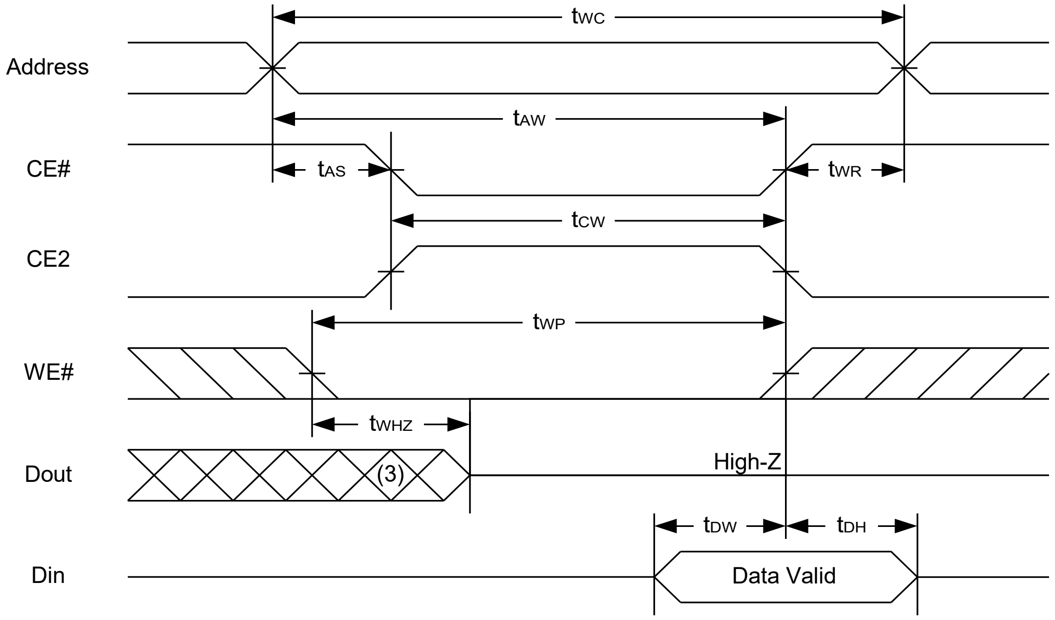


Notes :
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



Notes :

1.A write occurs during the overlap of a low CE#, high CE2, low WE#.

2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.

3. During this period, I/O pins are in the output state, and input signals must not be applied.

4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.

5. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

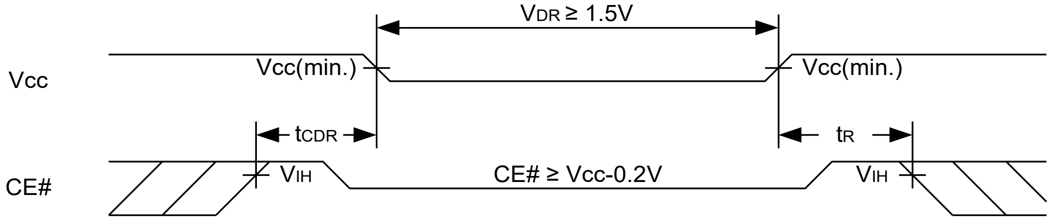
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V or CE2≦0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧V_{CC} -0.2V or CE2≦0.2V Other pins at 0.2V or V_{CC} -0.2V	40℃	-	2	5	μA
				-	2	20	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

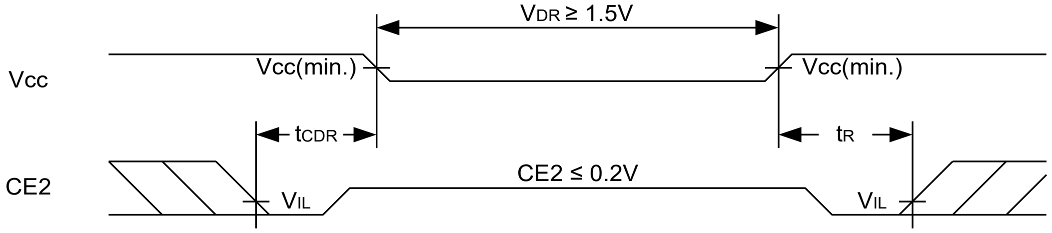
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)

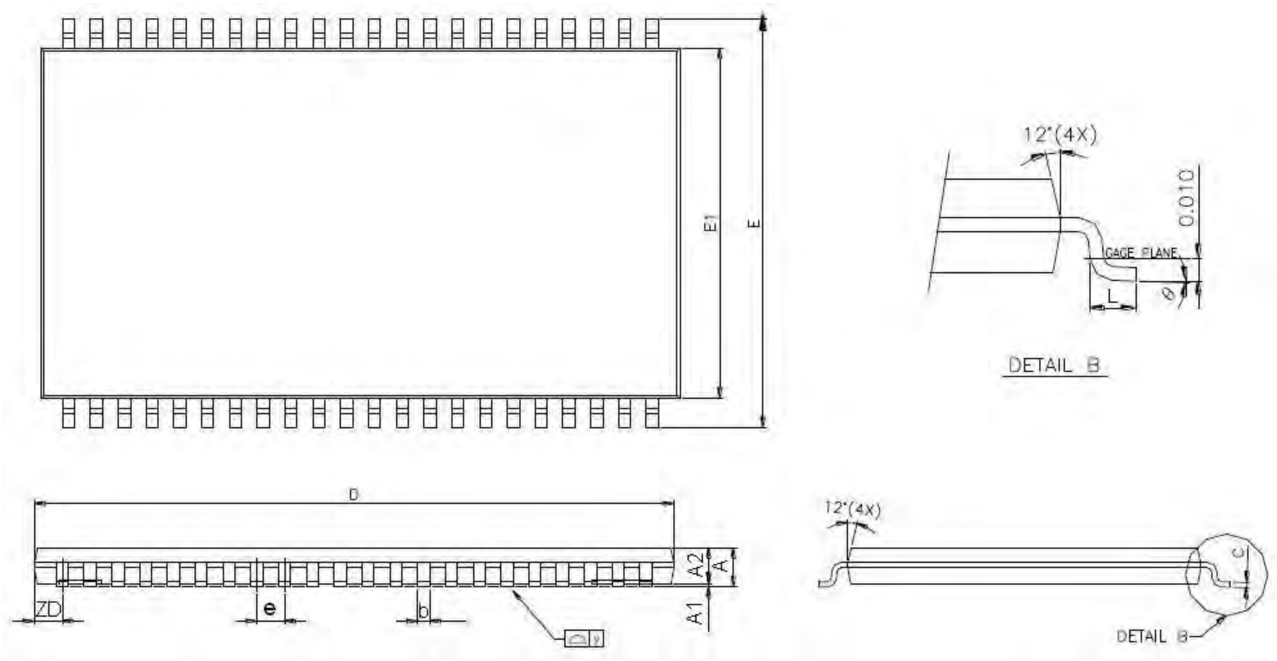


Low Vcc Data Retention Waveform (2) (CE2 controlled)



PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP II Package Outline Dimension

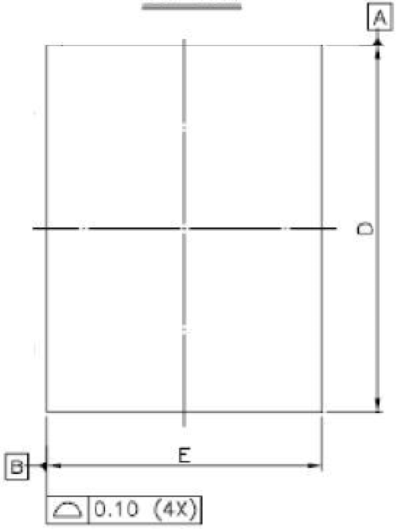


SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
Θ	0°	3°	6°	0°	3°	6°

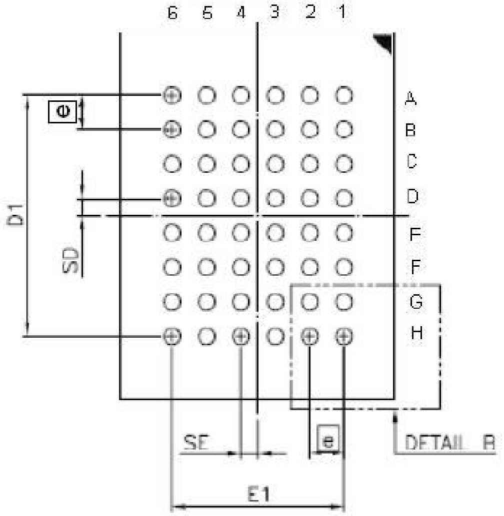
PACKAGE OUTLINE DIMENSION

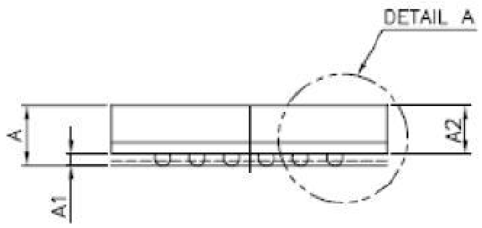
48-ball 6x8mm TFBGA

TOP VIEW

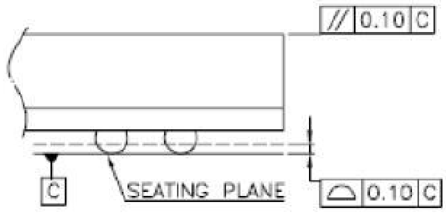


BOTTOM VIEW

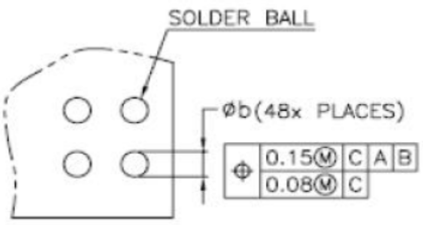




SIDE VIEW



DETAIL A



DETAIL B

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

ORDERING INFORMATION

Alliance Part Number	Organization	VCC Range	Package	Operating Temp	Speed (ns)
AS6C8008B-45ZIN	1024K x 8	2.7 ~ 3.6V	44-pin 400 mil TSOP II	Industrial -40°C ~ 85°C	45
AS6C8008B-55ZIN	1024K x 8	2.7 ~ 3.6V	44-pin 400 mil TSOP II	Industrial -40°C ~ 85°C	55
AS6C8008B-45BIN	1024K x 8	2.7 ~ 3.6V	48-ball 6x8mm TFBGA	Industrial -40°C ~ 85°C	45

PART NUMBERING SYSTEM

AS6C	8008B	-45/55	Z	I	N	XX
AS6C = Low Power SRAM	Device Number **80** = 8Meg **08** = x8 bit **B** = B die version	Access Time **45** = 45ns **55** = 55ns	**Z**=TSOPII **B**=TFBGA	**I** = Industrial Temp -40°C~ 85°C	**N =** Pb and Halogen Free	Packing Type **None** : Tray **TR** : Reel

Alliance Memory, Inc.
12815 NE 124th Street Suite D
Kirkland, WA 98034
Tel: 425-898-4456
Fax: 425-896-8628
www.alliancememory.com

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