Revision History
8Mb - 512k x 16bit SUPER LOW POWER CMOS SRAM

Revision	Details	Date
Rev 1.0	Initial Release	Nov 2020

FEATURES

- Fast access time : 45/55ns
- Low power consumption:
  Operating current : 12mA /10mA(TYP.)
  Standby current : 2.5μA (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
  UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- Package : 48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The AS6C8016B is a 8,388,608-bit low power CMOS static random access memory organized as 524,288 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

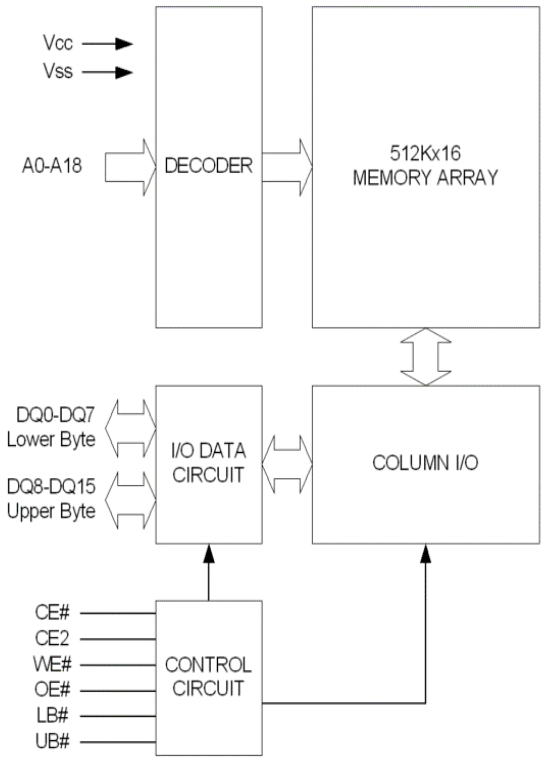
The AS6C8016B is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C8016B operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V_{CC} Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{CC},TYP.)
AS6C8016B-45BIN	-40 ~ 85℃	2.7 ~ 3.6V	45ns	2.5μA	12mA
AS6C8016B-55BIN	-40 ~ 85℃	2.7 ~ 3.6V	55ns	2.5μA	10mA

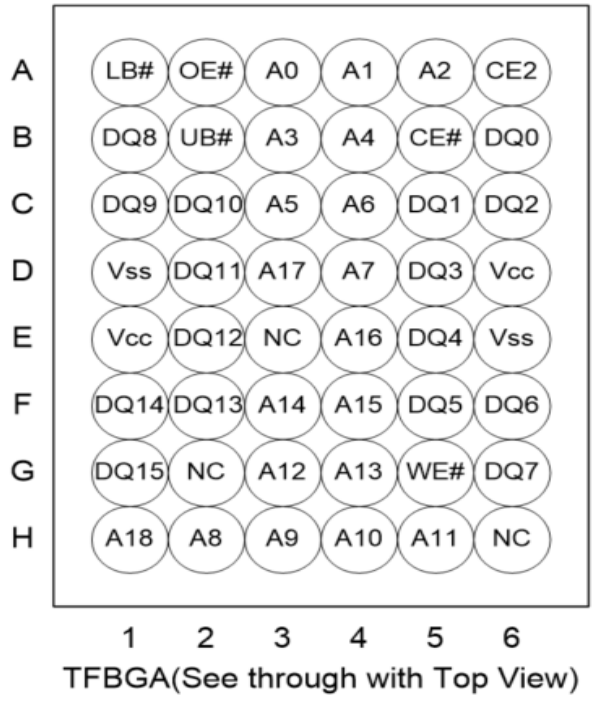
FUNCTIONAL BLOCK DIAGRAM



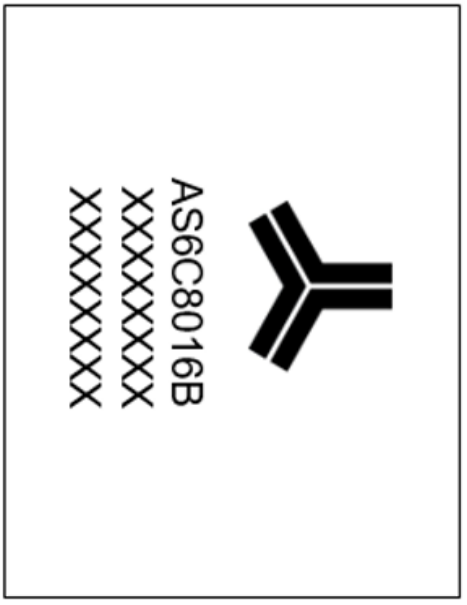
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION



TFBGA(See through with Top View)



TFBGA (Top View)

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	-40 to 85	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High – Z	High – Z	I_{SB1}
	X	L	X	X	X	X	High – Z	High – Z	
	X	X	X	X	H	H	High – Z	High – Z	
Output Disable	L	H	H	H	L	X	High – Z	High – Z	I_{CC},I_{CC1}
	L	H	H	H	X	L	High – Z	High – Z	
Read	L	H	L	H	L	H	D_{OUT}	High – Z	I_{CC},I_{CC1}
	L	H	L	H	H	L	High – Z	D_{OUT}	
	L	H	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	H	X	L	L	H	D_{IN}	High – Z	I_{CC},I_{CC1}
	L	H	X	L	H	L	High – Z	D_{IN}	
	L	H	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.0	3.6	V
Input High Voltage	V_{IH}*1			2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}*2			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.4	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE#≦0.2V and CE2≧V_{CC}-0.2V $I_{I/O}$ = 0mA Others at 0.2V or V_{CC}-0.2V	-45	-	12	20	mA
			-55	-	10	18	mA
	I_{CC1}	Cycle time = 1µs CE#≦0.2V and CE2≧V_{CC}-0.2V $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V		-	3	5	mA
Standby Power Supply Current	I_{SB1}	CE# ≧V_{CC}-0.2V or CE2≦0.2V Other pins at 0.2V or V_{CC}-0.2V	40℃	-	2.5	5	µA
				-	2.5	20	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 6ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 6ns.
3. Over/Undershootspecifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS6C8016B-45		AS6C8016B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	45	-	55	-	ns
Address Access Time	t_{AA}	-	45	-	55	ns
Chip Enable Access Time	t_{ACE}	-	45	-	55	ns
Output Enable Access Time	t_{OE}	-	25	-	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	15	-	20	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	15	-	20	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	ns
LB#, UB# Access Time	t_{BA}	-	45	-	55	ns
LB#, UB# to High-Z Output	t_{BHZ}*	-	20	-	25	ns
LB#, UB# to Low-Z Output	t_{BLZ}*	10	-	10	-	ns

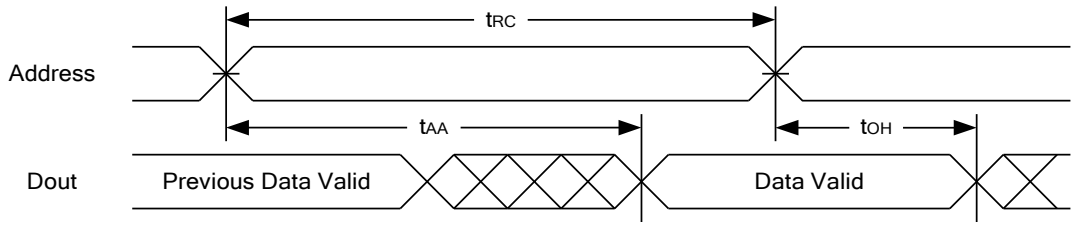
(2) WRITE CYCLE

PARAMETER	SYM.	AS6C8016B-45		AS6C8016B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	45	-	55	-	ns
Address Valid to End of Write	t_{AW}	40	-	50	-	ns
Chip Enable to End of Write	t_{CW}	40	-	50	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	45	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	20	ns
LB#, UB# Valid to End of Write	t_{BW}	35	-	45	-	ns

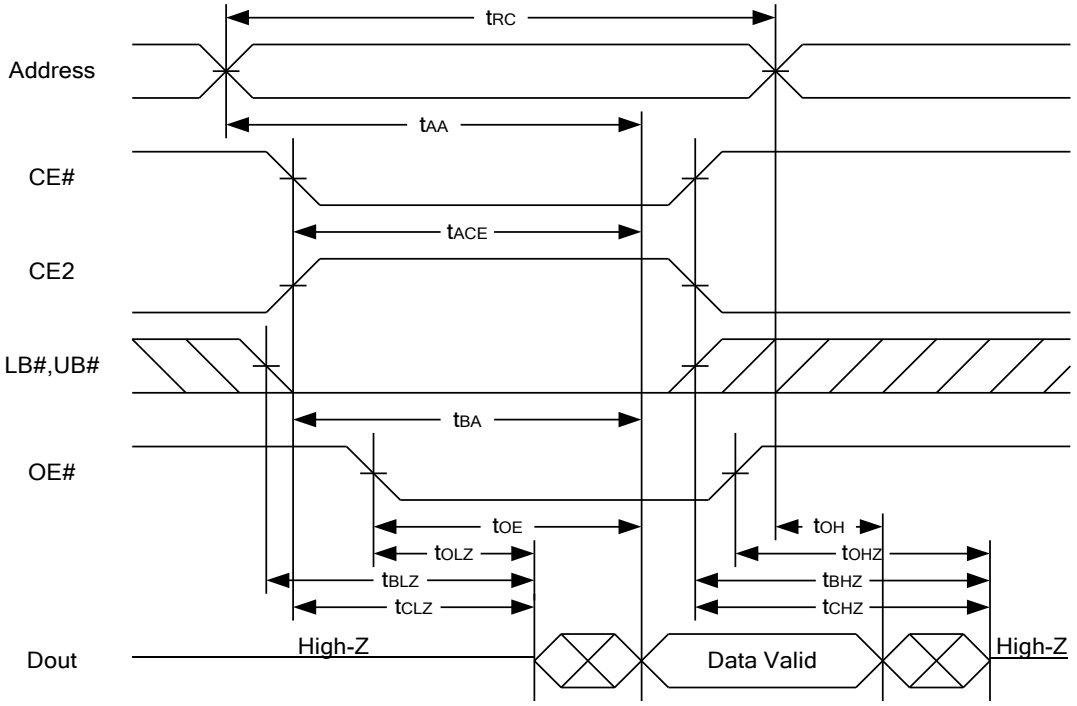
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

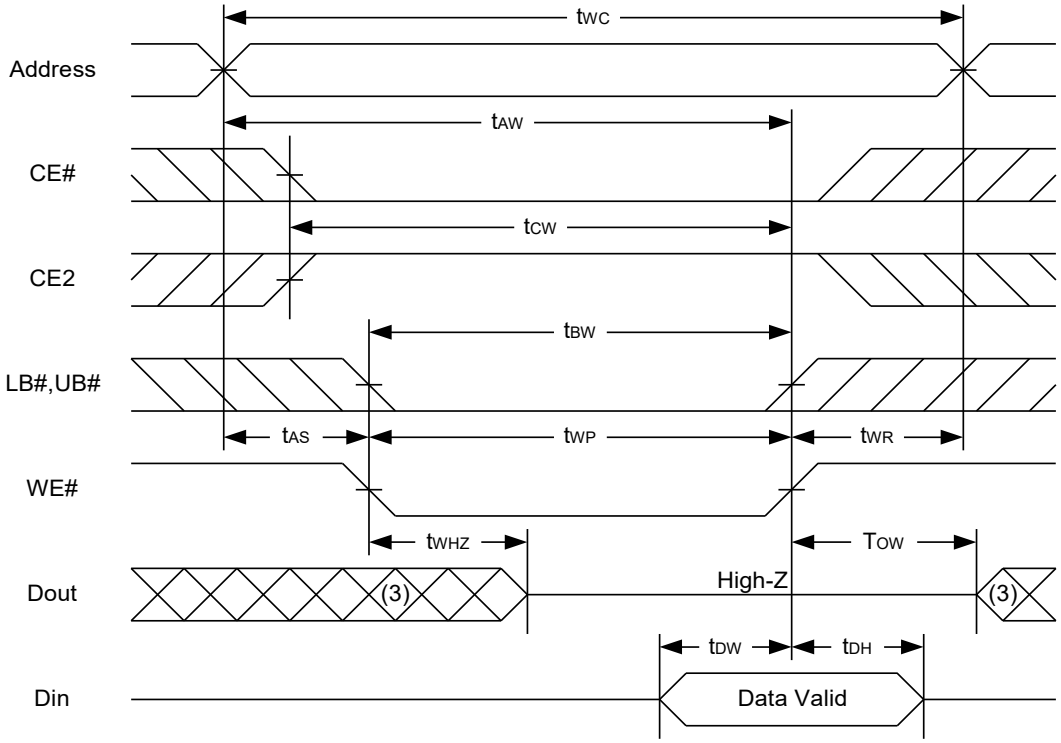


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

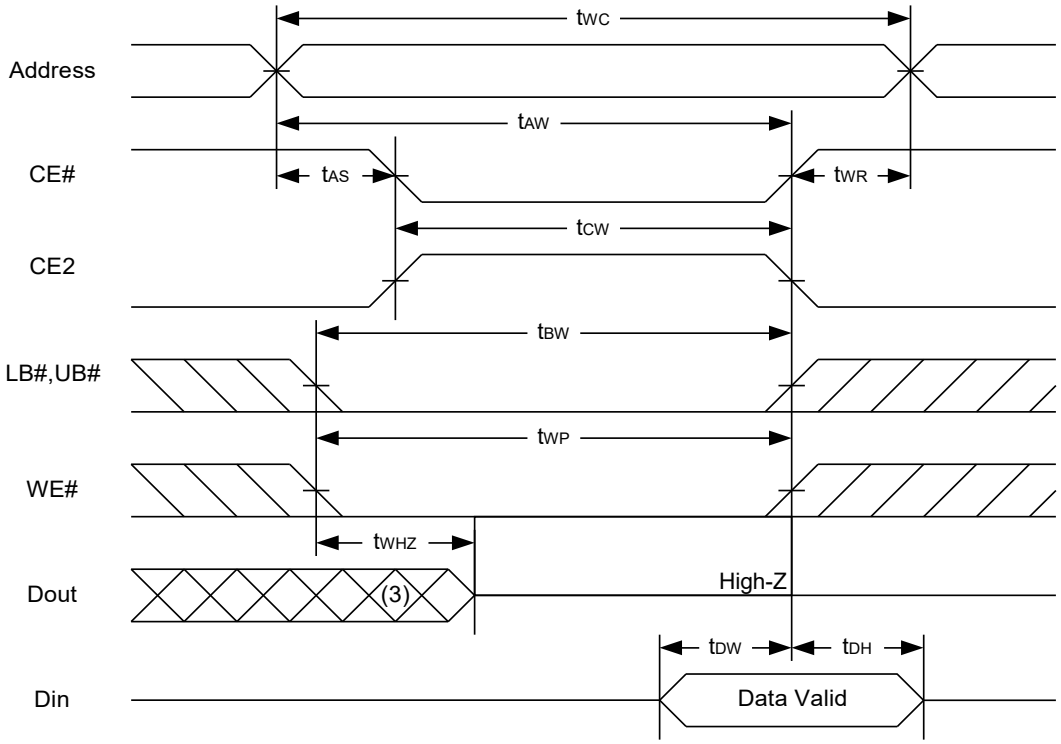


Notes :
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

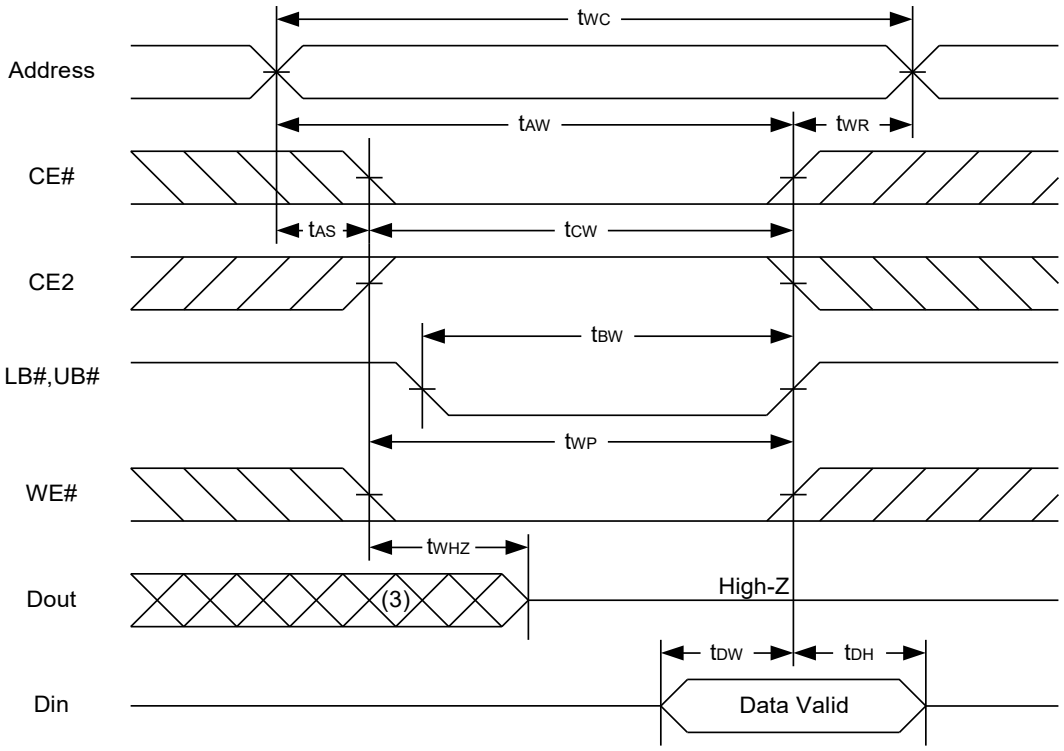
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :
1. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

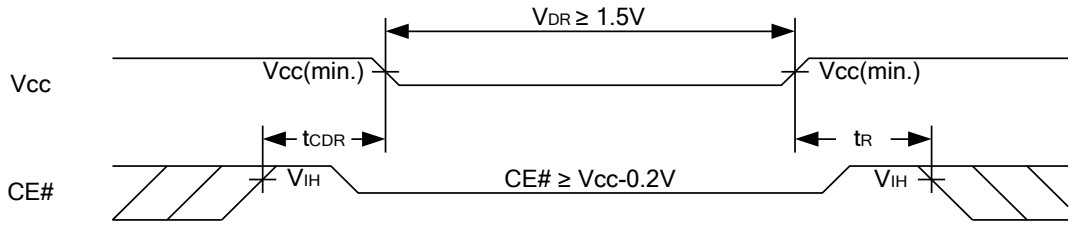
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V or CE2≦0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧V_{CC}-0.2V or CE2≦0.2V Other pins at 0.2V or V_{CC}-0.2V	40℃	-	2	5	µA
				-	2	20	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

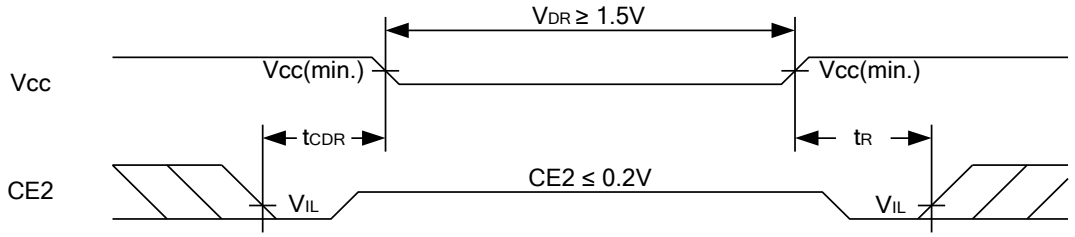
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

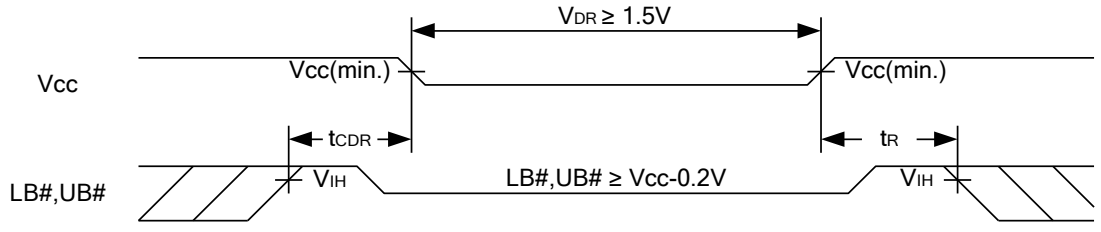
Low Vcc Data Retention Waveform (1) (CE# controlled)



Low Vcc Data Retention Waveform (2) (CE2 controlled)

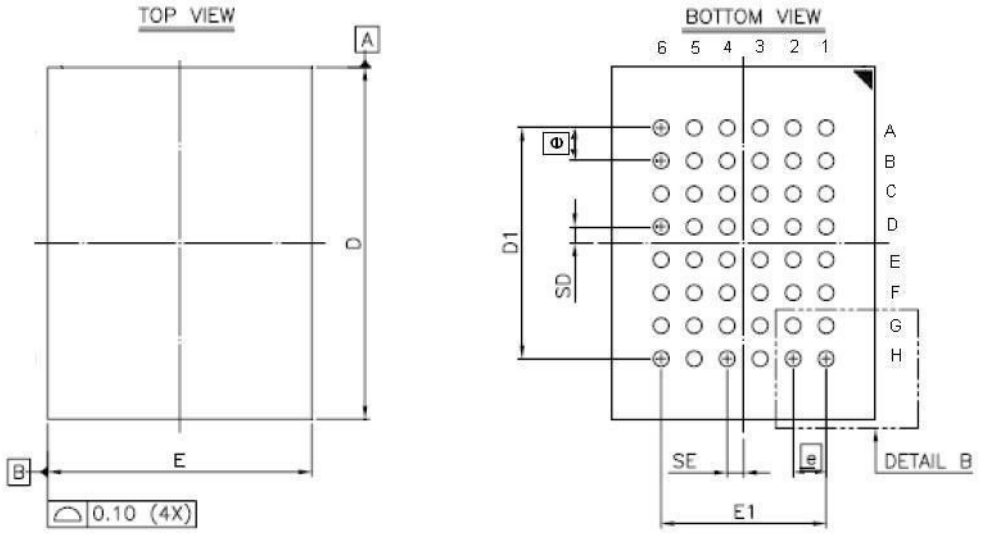


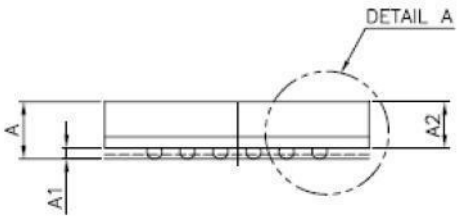
Low Vcc Data Retention Waveform (3) (LB#, UB# controlled)



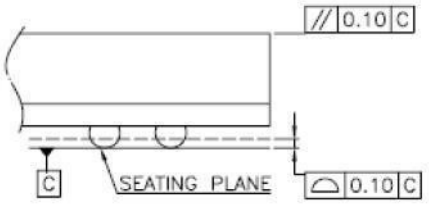
PACKAGE OUTLINE DIMENSION

48-ball 6mm × 8mm TFBGA Package Outline Dimension

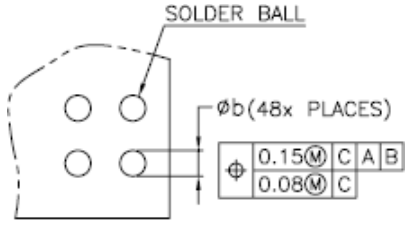




SIDE VIEW



DETAIL A



DETAIL B

A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

ORDERING INFORMATION

Part Number	Organization	VCC Range	Package	Operating Temp	Speed (ns)
AS6C8016B-45BIN	512K x 16	2.7 ~ 3.6V	48ball 6mmx8mm FBGA	Industrial -40°C ~ 85°C	45
AS6C8016B-55BIN	512K x 16	2.7 ~ 3.6V	48ball 6mmx8mm FBGA	Industrial -40°C ~ 85°C	55

PART NUMBERING SYSTEM

AS6C	8016B	-45/55	B	I	N	XX
Low Power SRAM	Device Number 80 = x8Mb 16 = x16Mb B = B die version	Access Time	B=FBGA	I=Industrial temp -40°C~ 85°C	Indicates Pb and Halogen Free	Packing Type None:Tray TR: Reel

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