# 256K X 36, 512K X 18
# 3.3V Synchronous SRAMs
# 3.3V I/O, Burst Counter
# Pipelined Outputs, Single Cycle Deselect

**AS8C803600**
**AS8C801800**

## Features

- **256K x 36, 512K x 18 memory configurations**
- **Supports high system speed:**
  - *150MHz 3.8ns clock access time*
- **$\overline{LBO}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)**
- **3.3V core power supply**
- **Power down controlled by ZZ input**
- **3.3V I/O supply ($V_{DDQ}$)**
- **Packaged in a JEDEC Standard 100-pin thin plastic quad flatpack (TQFP)**

## Description

The AS8C803600/801800 are high-speed SRAMs organized as 256K x 36 / 512K x 18. The SRAMs contain write, data, address and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the AS8C803600/801800 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the $\overline{LBO}$ input pin.

The AS8C803600/801800 SRAMs utilize the latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP),

## Pin Description Summary

| | | | |
|---|---|---|---|
| $A_0$-$A_{18}$ | Address Inputs | Input | Synchronous |
| $\overline{CE}$ | Chip Enable | Input | Synchronous |
| $CS_0$, $\overline{CS_1}$ | Chip Selects | Input | Synchronous |
| $\overline{OE}$ | Output Enable | Input | Asynchronous |
| $\overline{GW}$ | Global Write Enable | Input | Synchronous |
| $\overline{BWE}$ | Byte Write Enable | Input | Synchronous |
| $\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$(1) | Individual Byte Write Selects | Input | Synchronous |
| CLK | Clock | Input | N/A |
| $\overline{ADV}$ | Burst Address Advance | Input | Synchronous |
| $\overline{ADSC}$ | Address Status (Cache Controller) | Input | Synchronous |
| $\overline{ADSP}$ | Address Status (Processor) | Input | Synchronous |
| $\overline{LBO}$ | Linear / Interleaved Burst Order | Input | DC |
| ZZ | Sleep Mode | Input | Asynchronous |
| $I/O_0$-$I/O_{31}$, $I/O_{P1}$-$I/O_{P4}$ | Data Input / Output | I/O | Synchronous |
| $V_{DD}$, $V_{DDQ}$ | Core Power, I/O Power | Supply | N/A |
| $V_{SS}$ | Ground | Supply | N/A |

**NOTE:**

1. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for other devices

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**September 2010**

## Pin Definitions(1)

| Symbol | Pin Function | I/O | Active | Description |
|---|---|---|---|---|
| $A_0$-$A_{18}$ | Address Inputs | I | N/A | Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low. |
| $\overline{ADSC}$ | Address Status (Cache Controller) | I | LOW | Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses. |
| $\overline{ADSP}$ | Address Status (Processor) | I | LOW | Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$. |
| $\overline{ADV}$ | Burst Address Advance | I | LOW | Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance. |
| $\overline{BWE}$ | Byte Write Enable | I | LOW | Synchronous byte write enable gates the byte write inputs $\overline{BW_1}$-$\overline{BW_4}$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW}$x inputs are passed to the next stage in the circuit. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle. |
| $\overline{BW_1}$-$\overline{BW_4}$ | Individual Byte Write Enables | I | LOW | Synchronous byte write enables. $\overline{BW_1}$ controls $I/O_{0-7}$, $I/O_{P1}$, $\overline{BW_2}$ controls $I/O_{8-15}$, $I/O_{P2}$, etc. Any active byte write causes all outputs to be disabled. |
| $\overline{CE}$ | Chip Enable | I | LOW | Synchronous chip enable. $\overline{CE}$ is used with $CS_0$ and $\overline{CS_1}$ to enable the IDT71V67603/7803. $\overline{CE}$ also gates $\overline{ADSP}$. |
| CLK | Clock | I | N/A | This is the clock input. All timing references for the device are made with respect to this input. |
| $CS_0$ | Chip Select 0 | I | HIGH | Synchronous active HIGH chip select. $CS_0$ is used with $\overline{CE}$ and $\overline{CS_1}$ to enable the chip. |
| $\overline{CS_1}$ | Chip Select 1 | I | LOW | Synchronous active LOW chip select. $\overline{CS_1}$ is used with $\overline{CE}$ and $CS_0$ to enable the chip. |
| $\overline{GW}$ | Global Write Enable | I | LOW | Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ supersedes individual byte write enables. |
| $I/O_0$-$I/O_{31}$ $I/O_{P1}$-$I/O_{P4}$ | Data Input/Output | I/O | N/A | Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK. |
| $\overline{LBO}$ | Linear Burst Order | I | LOW | Asynchronous burst order selection input. When $\overline{LBO}$ is HIGH, the interleaved burst sequence is selected. When $\overline{LBO}$ is LOW the Linear burst sequence is selected. $\overline{LBO}$ is a static input and must not change state while the device is operating. |
| $\overline{OE}$ | Output Enable | I | LOW | Asynchronous output enable. When $\overline{OE}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state. |
| $V_{DD}$ | Power Supply | N/A | N/A | 3.3V core power supply. |
| $V_{DDQ}$ | Power Supply | N/A | N/A | 3.3V I/O Supply. |
| $V_{SS}$ | Ground | N/A | N/A | Ground. |
| NC | No Connect | N/A | N/A | NC pins are not electrically connected to the device. |
| ZZ | Sleep Mode | I | HIGH | Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the AS8C803600/1800 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. |

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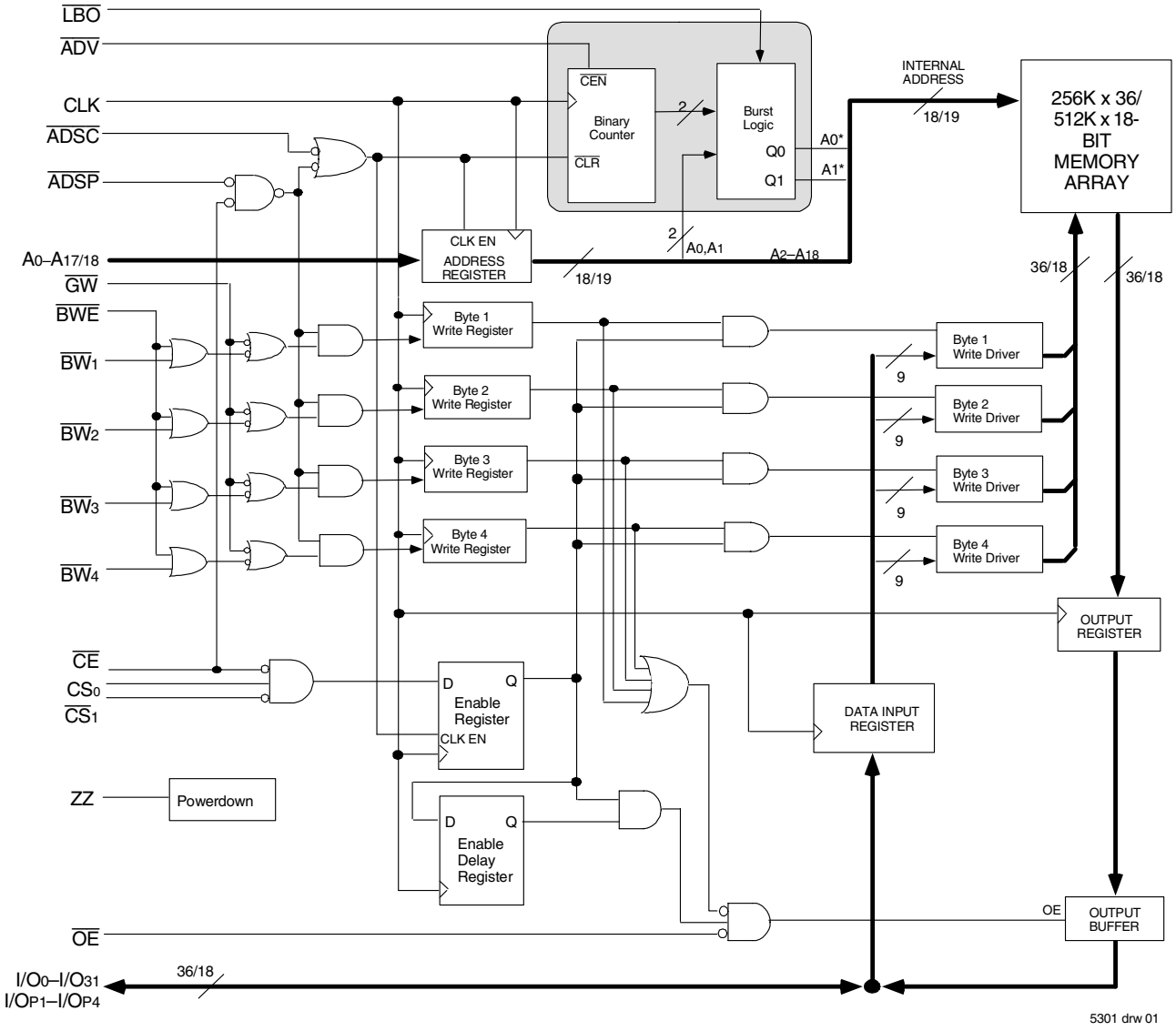
**NOTE:**
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

# Functional Block Diagram



## Absolute Maximum Ratings(1)

| Symbol | Rating | Commercial | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| $V_{TERM}$(3,6) | Terminal Voltage with Respect to GND | -0.5 to $V_{DD}$ | V |
| $V_{TERM}$(4,6) | Terminal Voltage with Respect to GND | -0.5 to $V_{DD}$ +0.5 | V |
| $V_{TERM}$(5,6) | Terminal Voltage with Respect to GND | -0.5 to $V_{DDQ}$ +0.5 | V |
| $T_A$(7) | Operating Temperature | -0 to +70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +125 | °C |
| $P_T$ | Power Dissipation | 2.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{DD}$ terminals only.
3. $V_{DDQ}$ terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed $V_{DDQ}$ during power supply ramp up.
7. $T_A$ is the "instant on" case temperature.

## Recommended Operating Temperature and Supply Voltage

| Grade | Temperature(1) | Vss | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 3.3V±5% | 3.3V±5% |
| Industrial | -40°C to +85°C | 0V | 3.3V±5% | 3.3V±5% |

5310 tbl 04

**NOTE:**
1. $T_A$ is the "instant on" case temperature.

## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| $V_{DDQ}$ | I/O Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| $V_{SS}$ | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage - Inputs | 2.0 | — | $V_{DD}$ +0.3 | V |
| $V_{IH}$ | Input High Voltage - I/O | 2.0 | — | $V_{DDQ}$ +0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.3(1) | — | 0.8 | V |

5310 tbl 05

**NOTE:**
1. $V_{IL}$ (min) = -1.0V for pulse width less than $t_{CYC/2}$, once per cycle.

## 100 Pin TQFP Capacitance
**($T_A$ = +25°C, f = 1.0MHz)**

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 5 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 7 | pF |

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## 119 BGA Capacitance
**($T_A$ = +25°C, f = 1.0MHz)**

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 7 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 7 | pF |

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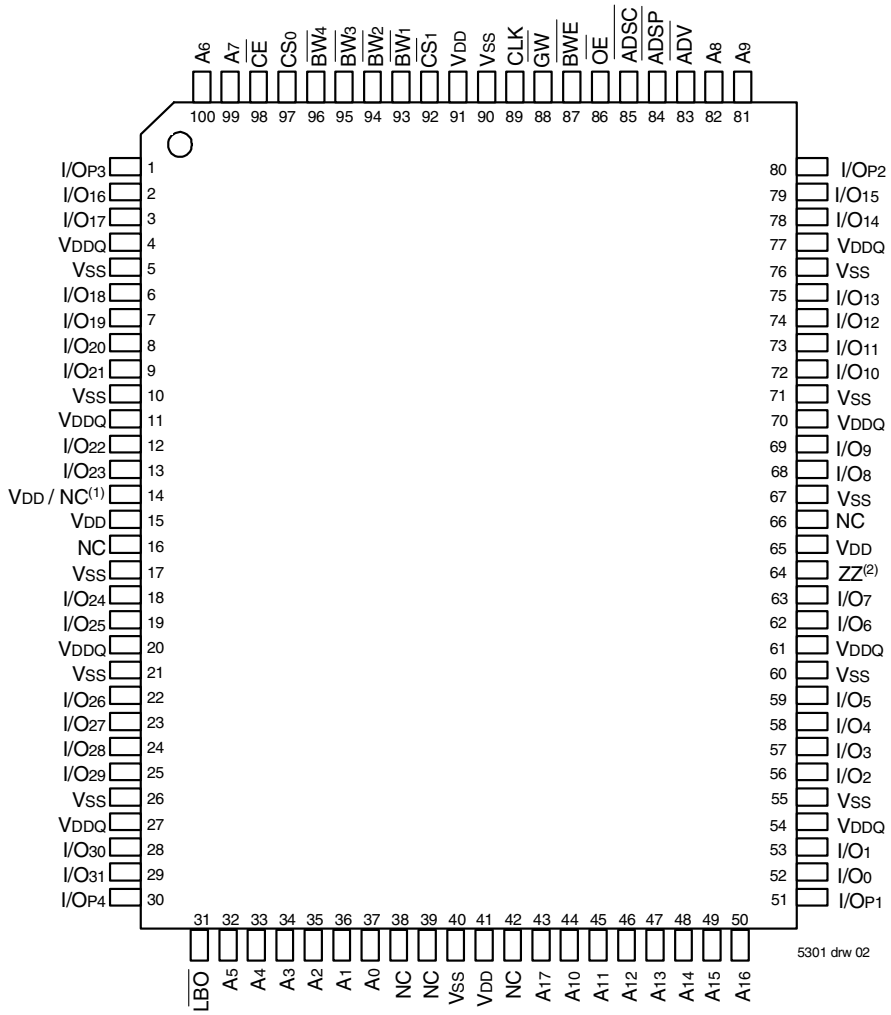
**NOTE:**
1. This parameter is guaranteed by device characterization, but not production tested.

## 165 fBGA Capacitance
**($T_A$ = +25°C, f = 1.0MHz)**

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 7 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 7 | pF |

5310 tbl 07b

## Pin Configuration – 256K x 36, 100-Pin TQFP

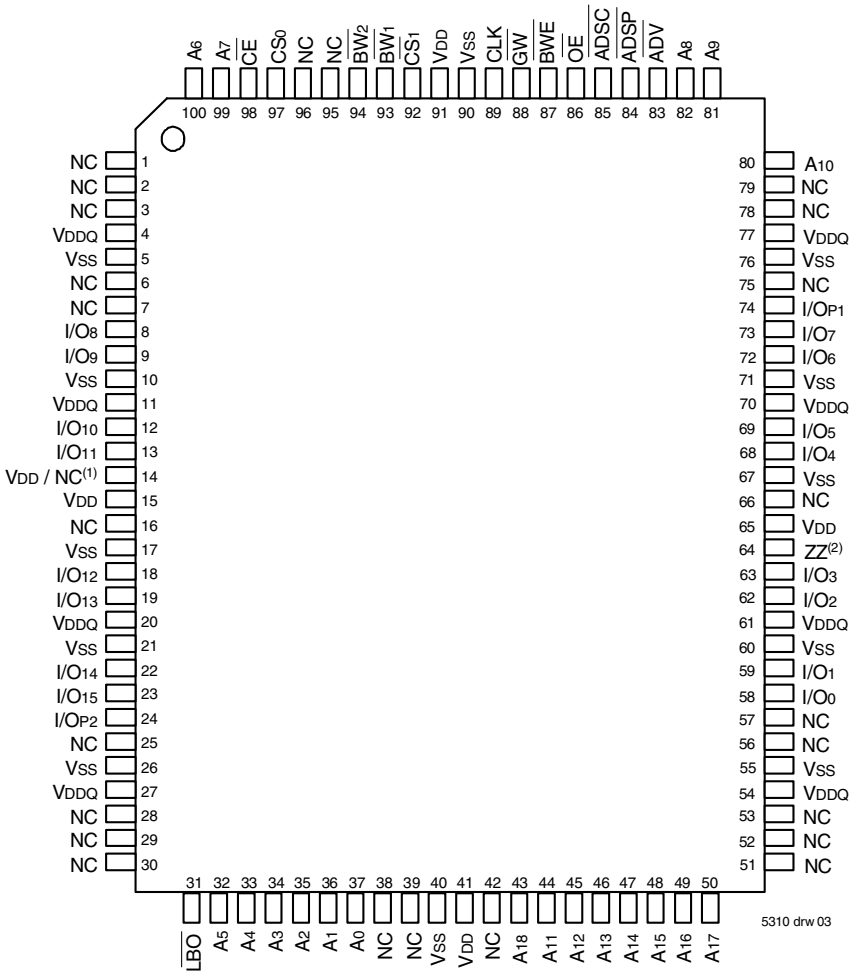



**Top View**

**NOTES:**

1. Pin 14 can either be directly connected to $V_{DD}$, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

## Pin Configuration – 512K x 18, 100-Pin TQFP




**Top View**

**NOTES:**

1. Pin 14 can either be directly connected to $V_{DD}$, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD}$ = 3.3V ± 5%)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 5 | µA |
| $\|I_{LZZ}\|$ | ZZ and $\overline{LBO}$ Input Leakage Current(1) | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 30 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{DDQ}$, Device Deselected | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = +8mA, $V_{DD}$ = Min. | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -8mA, $V_{DD}$ = Min. | 2.4 | — | V |

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**NOTE:**
1. The $\overline{LBO}$ pin will be internally pulled to $V_{DD}$ if it is not actively driven in the application and the ZZ pin will be internally pulled to $V_{SS}$ if not actively driven.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

| Symbol | Parameter | Test Conditions | 166MHz | 150MHz | | 133MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Com'l only | Com'l | Ind | Com'l | Ind | |
| $I_{DD}$ | Operating Power Supply Current | Device Selected, Outputs Open, $V_{DD}$ = Max., $V_{DDQ}$ = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = $f_{MAX}$(2) | 340 | 305 | 325 | 260 | 280 | mA |
| $I_{SB1}$ | CMOS Standby Power Supply Current | Device Deselected, Outputs Open, $V_{DD}$ = Max., $V_{DDQ}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2,3) | 50 | 50 | 70 | 50 | 70 | mA |
| $I_{SB2}$ | Clock Running Power Supply Current | Device Deselected, Outputs Open, $V_{DD}$ = Max., $V_{DDQ}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = $f_{MAX}$(2,3) | 160 | 155 | 175 | 150 | 170 | mA |
| $I_{ZZ}$ | Full Sleep Mode Supply Current | ZZ $\geq V_{HD}$, $V_{DD}$ = Max. | 50 | 50 | 70 | 50 | 70 | mA |

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**NOTES:**
1. All values are maximum guaranteed values.
2. At f = $f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of 1/$t_{CYC}$ while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. For I/Os $V_{HD}$ = $V_{DDQ}$ - 0.2V, $V_{LD}$ = 0.2V. For other inputs $V_{HD}$ = $V_{DD}$ - 0.2V, $V_{LD}$ = 0.2V.

## AC Test Conditions ($V_{DDQ}$ = 3.3V)

| | |
|---|---|
| Input Pulse Levels | 0 to 3V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| AC Test Load | See Figure 1 |

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## AC Test Load

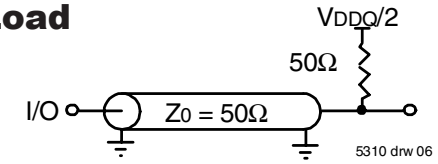


**Figure 1. AC Test Load**

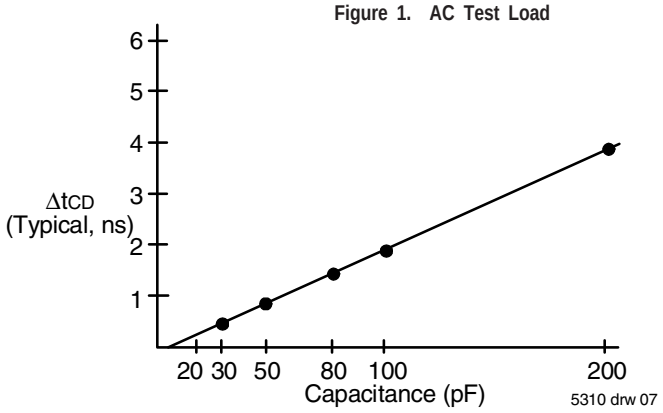


**Figure 2. Lumped Capacitive Load, Typical Derating**

## Synchronous Truth Table[1,3]

| Operation | Address Used | $\overline{CE}$ | $CS_0$ | $\overline{CS_1}$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW}x$ | $\overline{OE}$ (2) | CLK | I/O |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselected Cycle, Power Down | None | H | X | X | X | L | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | X | H | L | X | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | L | X | L | X | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | X | H | X | L | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | L | X | X | L | X | X | X | X | X | - | HI-Z |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | L | - | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | H | - | HI-Z |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | H | X | L | - | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | L | - | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | H | - | HI-Z |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | L | X | - | DIN |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | L | X | X | X | - | DIN |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | L | - | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | H | - | HI-Z |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | L | - | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | H | - | HI-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | X | L | - | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | X | H | - | HI-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | L | - | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | H | - | HI-Z |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | H | L | L | X | - | DIN |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | L | X | X | X | - | DIN |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | H | L | L | X | - | DIN |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | L | X | X | X | - | DIN |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | H | - | HI-Z |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | H | - | HI-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | H | - | HI-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | H | - | HI-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | L | L | X | - | DIN |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | L | X | X | X | - | DIN |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | L | L | X | - | DIN |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | L | X | X | X | - | DIN |

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**NOTES:**
1. L = $V_{IL}$, H = $V_{IH}$, X = Don't Care.
2. $\overline{OE}$ is an asynchronous input.
3. ZZ = low for this table.

## Synchronous Write Function Truth Table(1, 2)

| Operation | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW_1}$ | $\overline{BW_2}$ | $\overline{BW_3}$ | $\overline{BW_4}$ |
|---|---|---|---|---|---|---|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write all Bytes | L | X | X | X | X | X |
| Write all Bytes | H | L | L | L | L | L |
| Write Byte 1(3) | H | L | L | H | H | H |
| Write Byte 2(3) | H | L | H | L | H | H |
| Write Byte 3(3) | H | L | H | H | L | H |
| Write Byte 4(3) | H | L | H | H | H | L |

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**NOTES:**
1. L = $V_{IL}$, H = $V_{IH}$, X = Don't Care.
2. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable other devices
3. Multiple bytes may be selected during the same cycle.

## Asynchronous Truth Table(1)

| Operation(2) | $\overline{OE}$ | ZZ | I/O Status | Power |
|---|---|---|---|---|
| Read | L | L | Data Out | Active |
| Read | H | L | High-Z | Active |
| Write | X | L | High-Z – Data In | Active |
| Deselected | X | L | High-Z | Standby |
| Sleep Mode | X | H | High-Z | Sleep |

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**NOTES:**
1. L = $V_{IL}$, H = $V_{IH}$, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

## Interleaved Burst SequenceTable ($\overline{LBO}$=$V_{DD}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|---|---|---|---|---|---|---|---|---|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address(1) | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

5310 tbl 14

**NOTE:**
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

## Linear Burst Sequence Table ($\overline{LBO}$=Vss)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|---|---|---|---|---|---|---|---|---|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address(1) | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

5310 tbl 15

**NOTE:**
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

# AC Electrical Characteristics

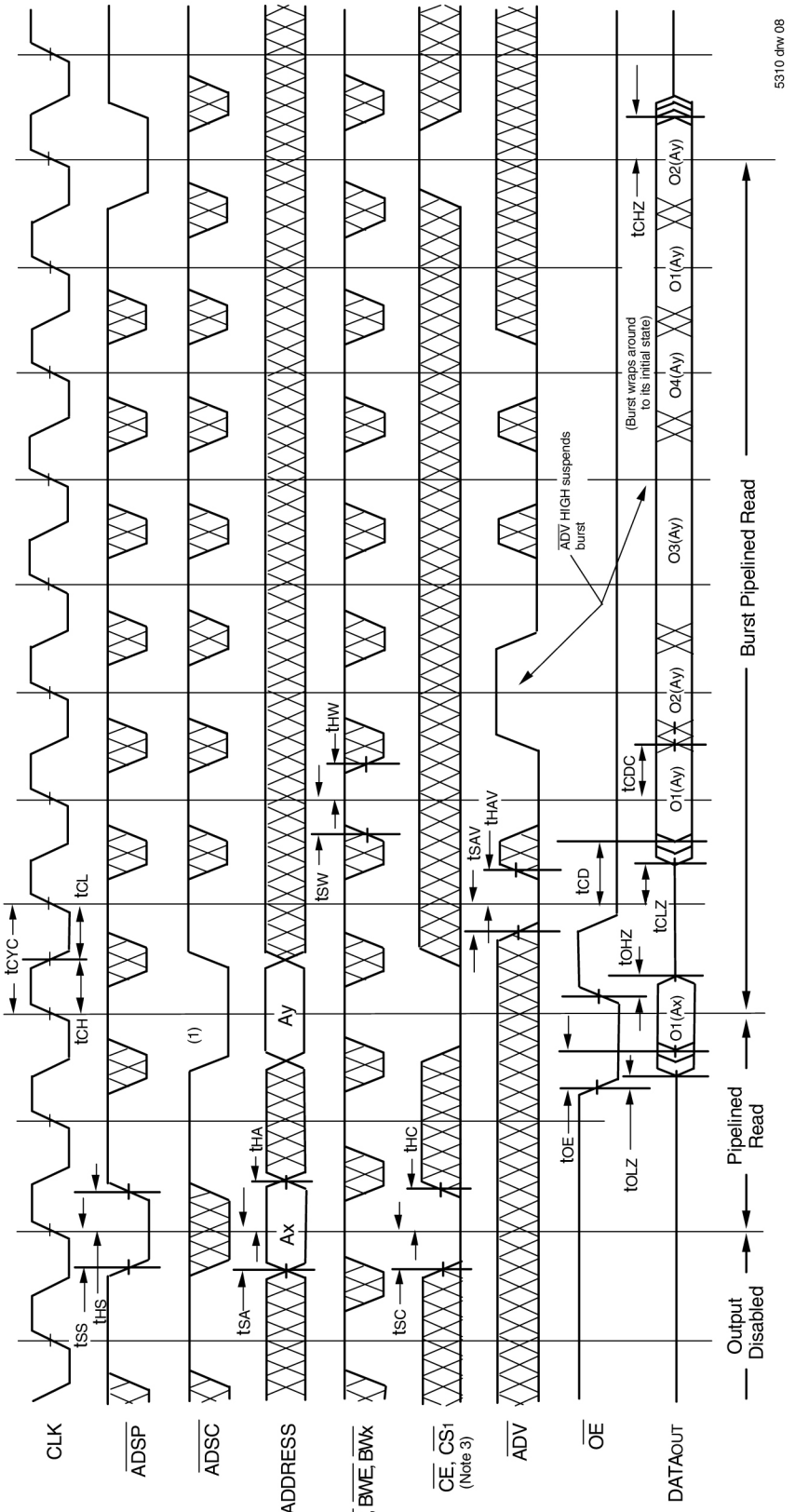
## ($V_{DD}$ = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

| Symbol | Parameter | 166MHz | | 150MHz | | 133MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| | | | | | | | | |
| $t_{CYC}$ | Clock Cycle Time | 6 | — | 6.7 | — | 7.5 | — | ns |
| $t_{CH}$(1) | Clock High Pulse Width | 2.4 | — | 2.6 | — | 3 | — | ns |
| $t_{CL}$(1) | Clock Low Pulse Width | 2.4 | — | 2.6 | — | 3 | — | ns |
| **Output Parameters** | | | | | | | | |
| $t_{CD}$ | Clock High to Valid Data | — | 3.5 | — | 3.8 | — | 4.2 | ns |
| $t_{CDC}$ | Clock High to Data Change | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_{CLZ}$(2) | Clock High to Output Active | 0 | — | 0 | — | 0 | — | ns |
| $t_{CHZ}$(2) | Clock High to Data High-Z | 1.5 | 3.5 | 1.5 | 3.8 | 1.5 | 4.2 | ns |
| $t_{OE}$ | Output Enable Access Time | — | 3.5 | — | 3.8 | — | 4.2 | ns |
| $t_{OLZ}$(2) | Output Enable Low to Output Active | 0 | — | 0 | — | 0 | — | ns |
| $t_{OHZ}$(2) | Output Enable High to Output High-Z | — | 3.5 | — | 3.8 | — | 4.2 | ns |
| **Set Up Times** | | | | | | | | |
| $t_{SA}$ | Address Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_{SS}$ | Address Status Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_{SD}$ | Data In Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_{SW}$ | Write Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_{SAV}$ | Address Advance Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_{SC}$ | Chip Enable/Select Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| **Hold Times** | | | | | | | | |
| $t_{HA}$ | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HS}$ | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HD}$ | Data In Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HW}$ | Write Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HAV}$ | Address Advance Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HC}$ | Chip Enable/Select Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| **Sleep Mode and Configuration Parameters** | | | | | | | | |
| $t_{ZZPW}$ | ZZ Pulse Width | 100 | — | 100 | — | 100 | — | ns |
| $t_{ZZR}$(3) | ZZ Recovery Time | 100 | — | 100 | — | 100 | — | ns |
| $t_{CFG}$(4) | Configuration Set-up Time | 24 | — | 27 | — | 30 | — | ns |

5310 tbl 16

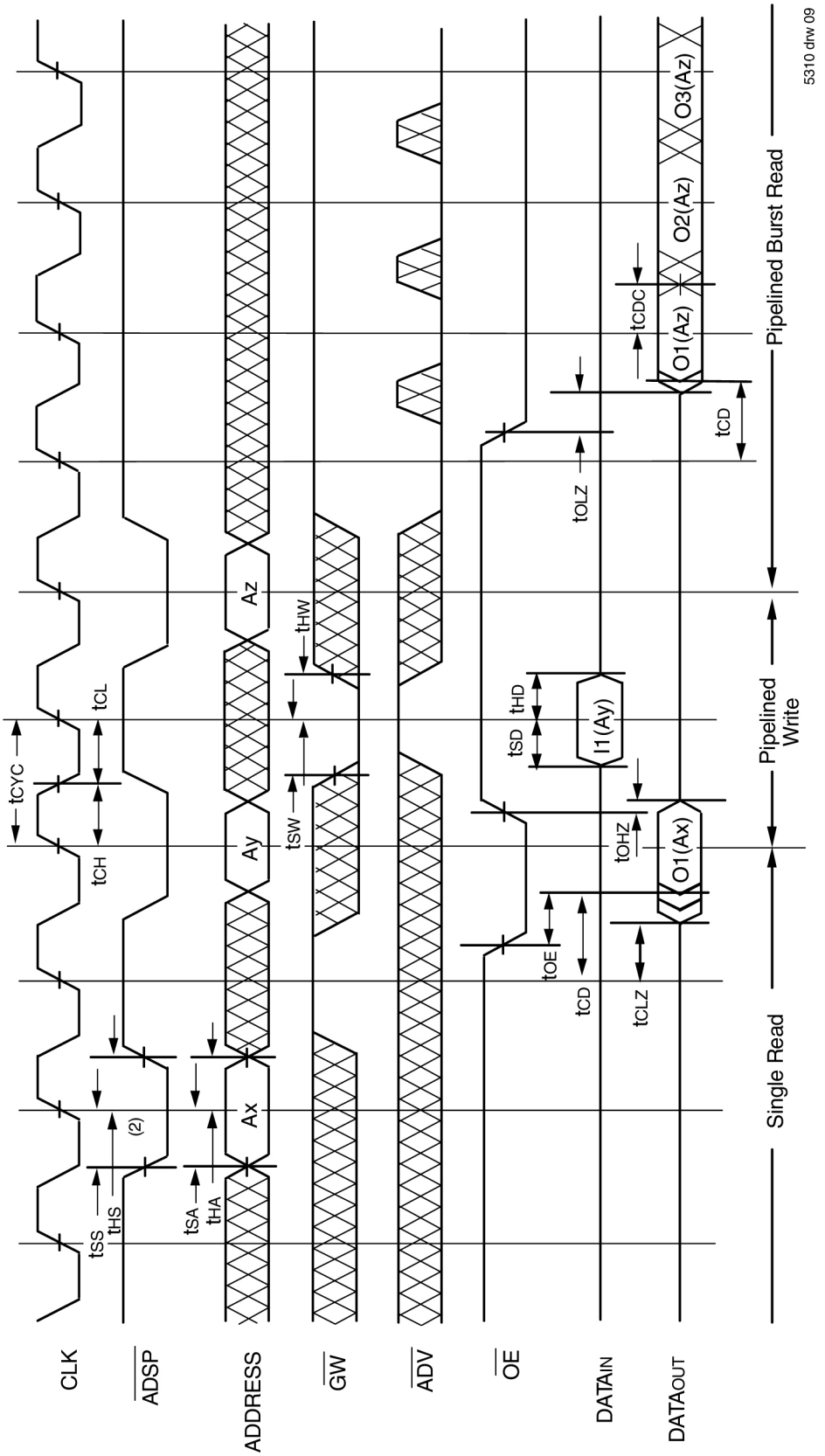
**NOTES:**
1. Measured as HIGH above $V_{IH}$ and LOW below $V_{IL}$.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. $t_{CFG}$ is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.

# Timing Waveform of Pipelined Read Cycle(1,2)



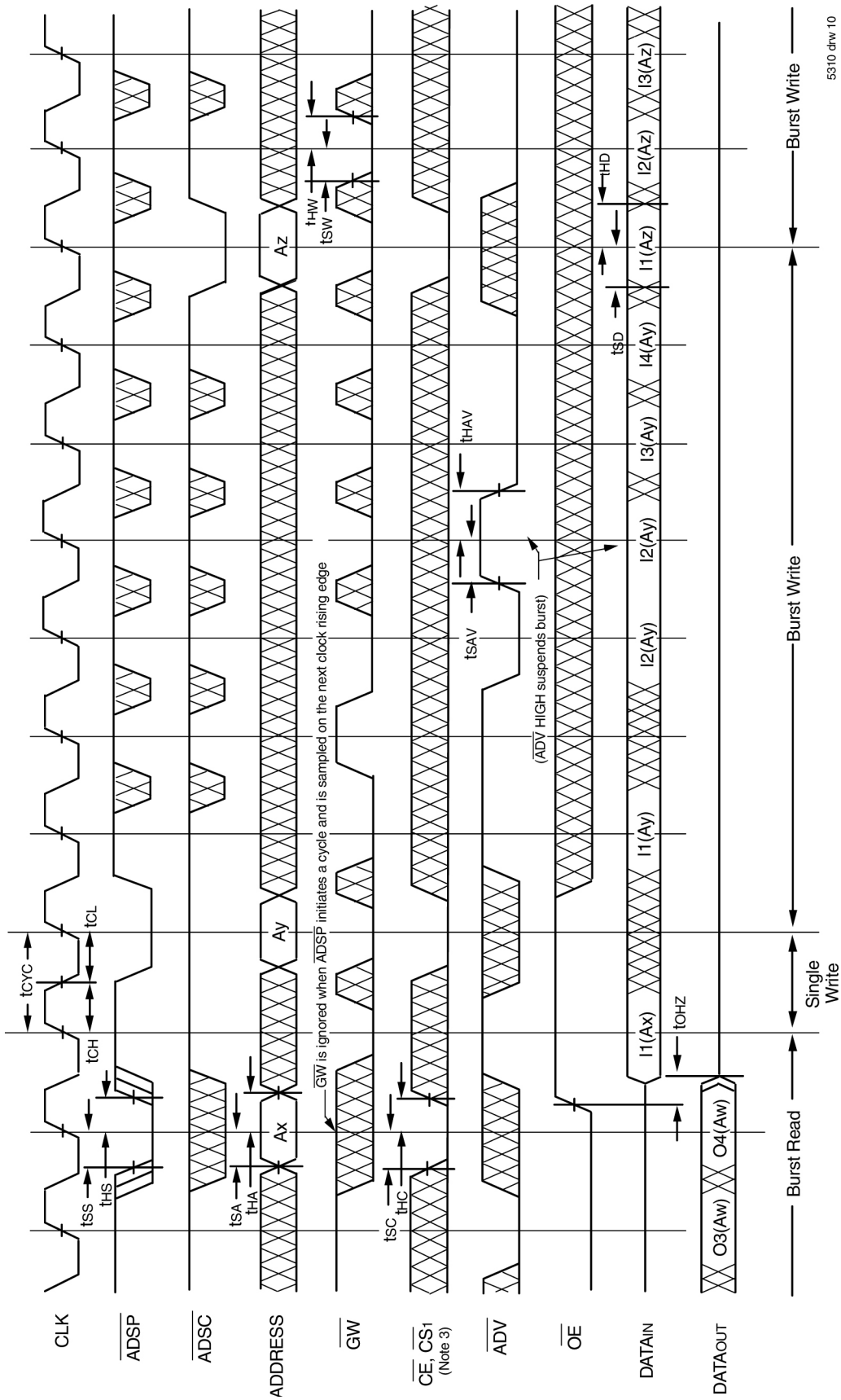

**NOTES:**
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. $CS_0$ timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, $CS_0$ is HIGH.

# Timing Waveform of Combined Pipelined Read and Write Cycles(1,2,3)



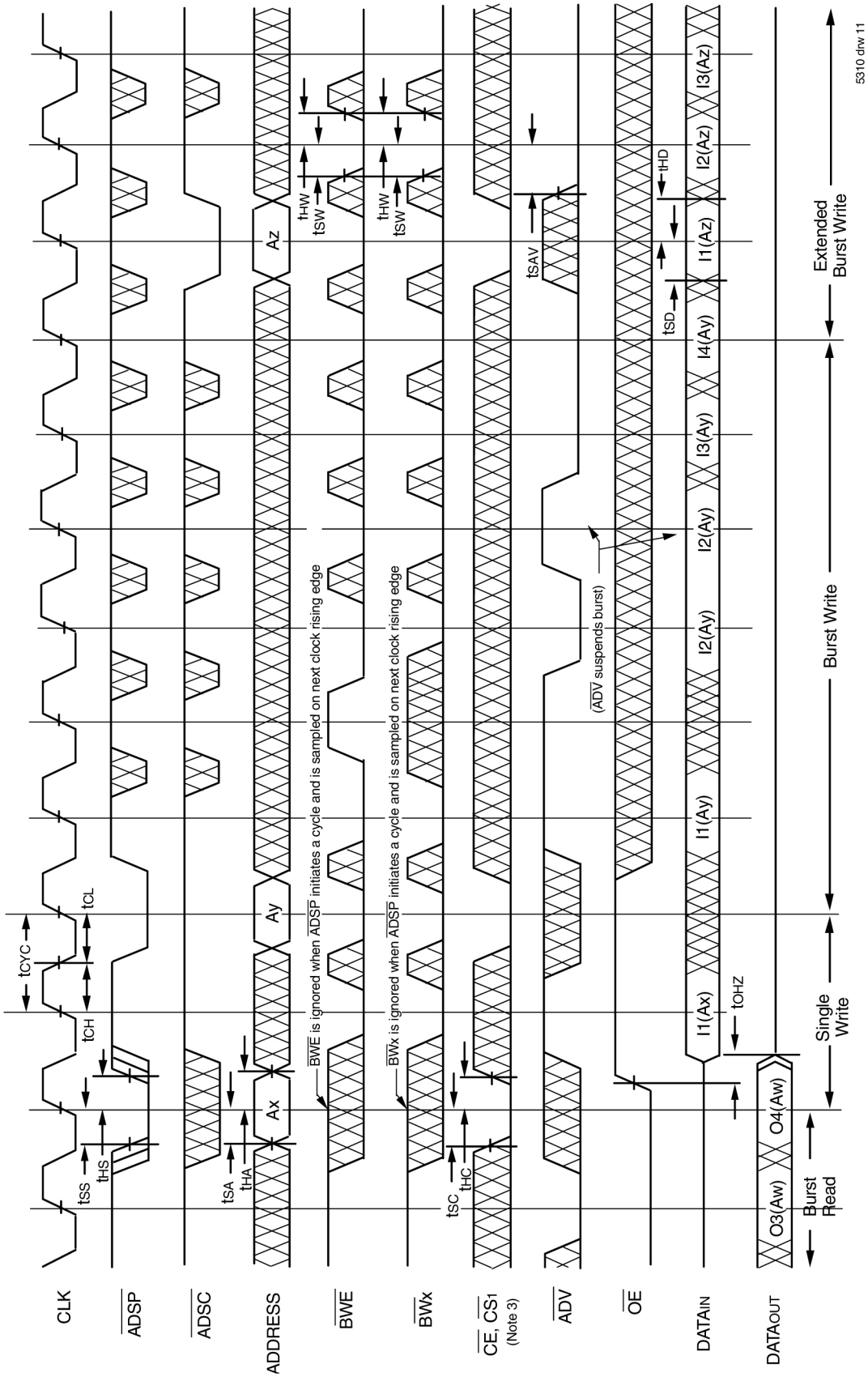

**NOTES:**
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS_1}$ are LOW, $CS_0$ is HIGH.
2. $\overline{ZZ}$ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay; O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

# Timing Waveform of Write Cycle No. 1 — $\overline{GW}$ Controlled(1,2,3)



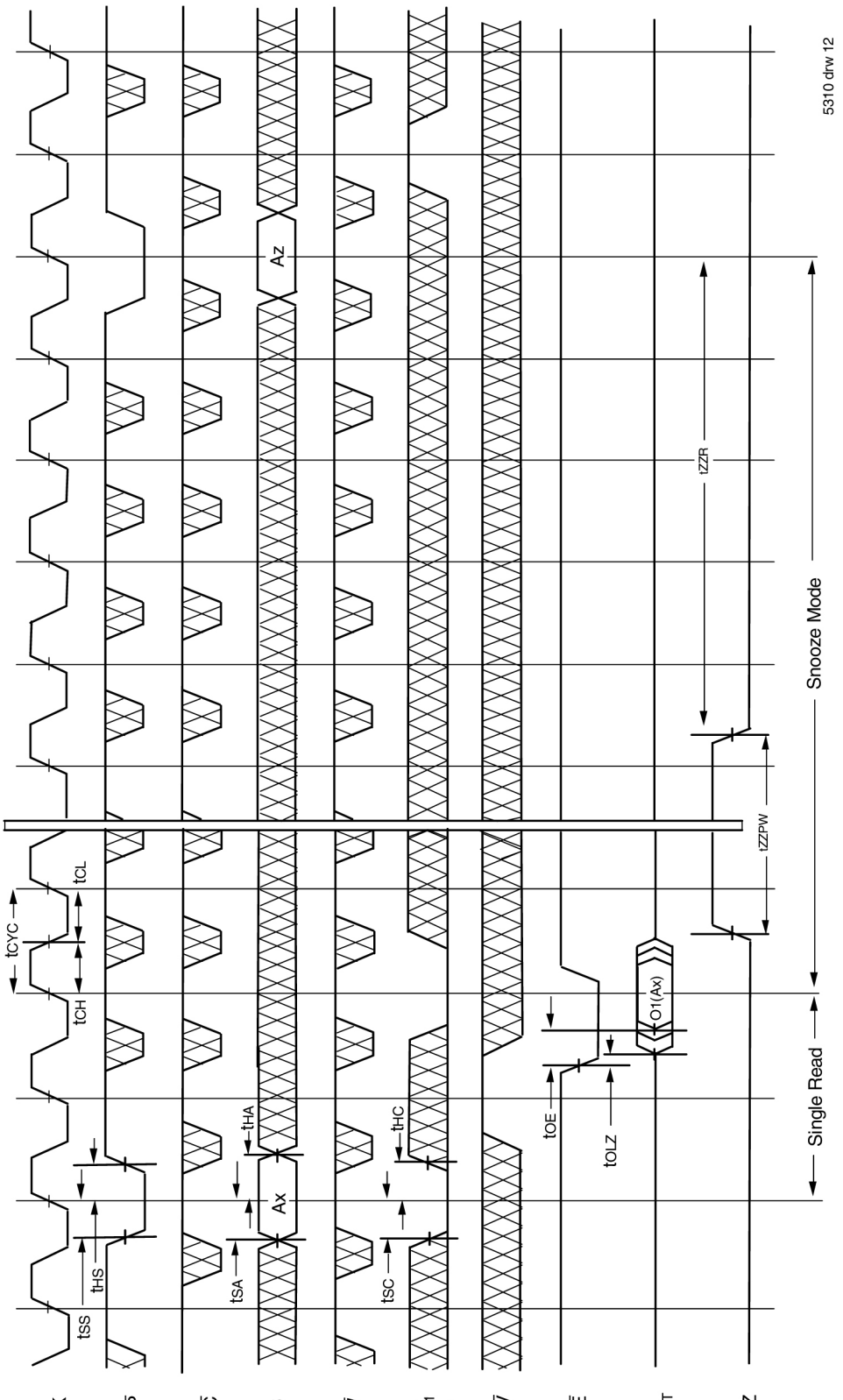

**NOTES:**
1. ZZ input is LOW, $\overline{BWE}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}$1 signals. For example, when $\overline{CE}$ and $\overline{CS}$1 are LOW on this waveform, CS0 is HIGH.

# Timing Waveform of Write Cycle No. 2 — Byte Controlled(1,2,3)



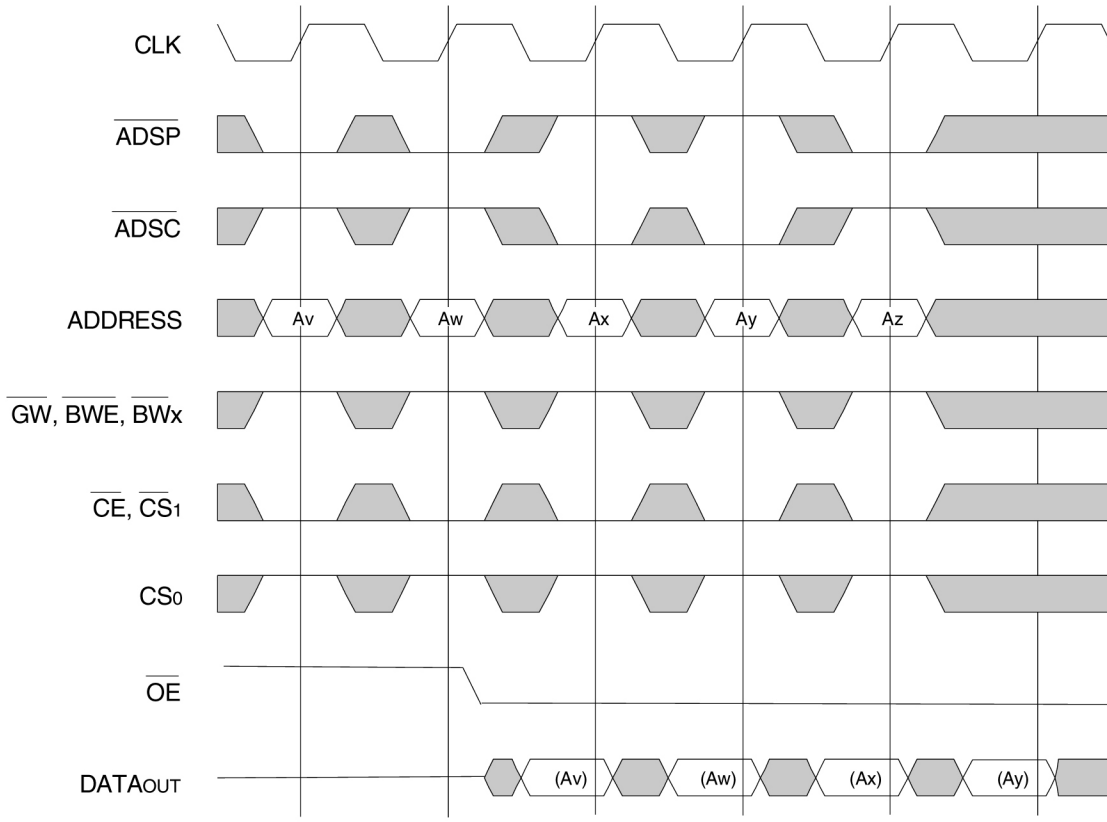

**NOTES:**
1. ZZ input is LOW, $\overline{GW}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

# Timing Waveform of Sleep (ZZ) and Power-Down Modes(1,2,3)




**NOTES:**
1. Device must power up in deselected Mode
2. $\overline{LBO}$ is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. $CS_0$ timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when CE and CS1 are LOW on this waveform, $CS_0$ is HIGH.

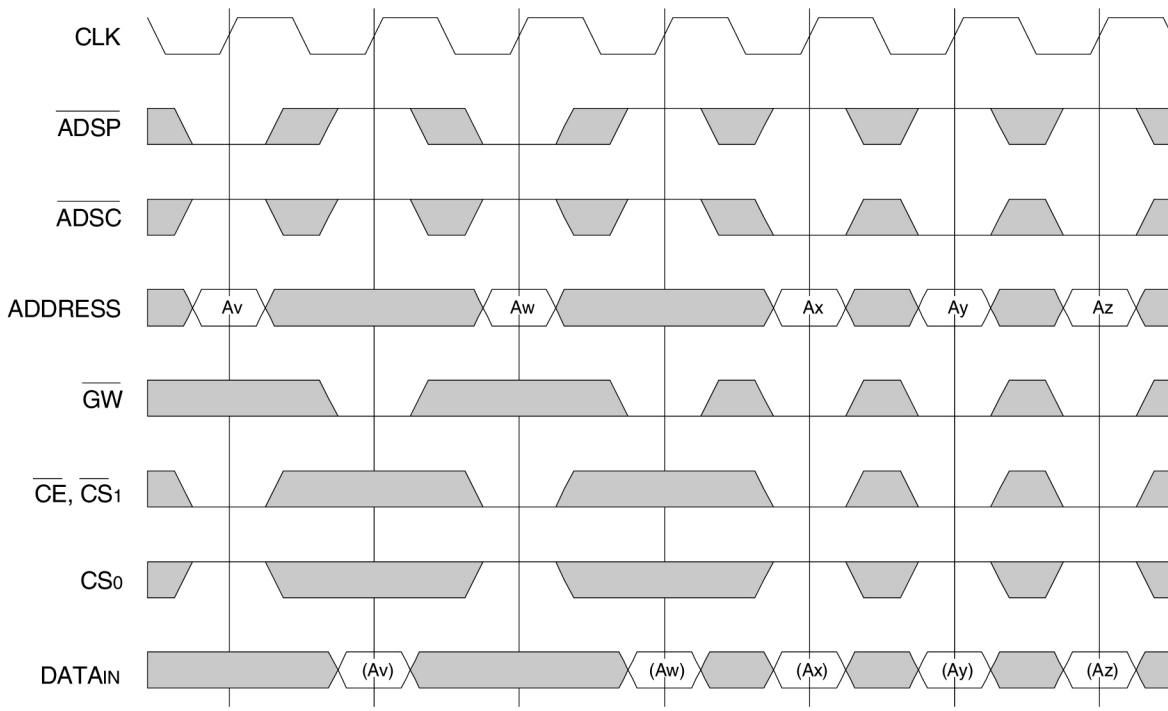
# Non-Burst Read Cycle Timing Waveform




5310 drw 14

**NOTES:**
1. ZZ input is LOW, ADV is HIGH and LBO is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, ADSP and ADSC function identically and are therefore interchangable.

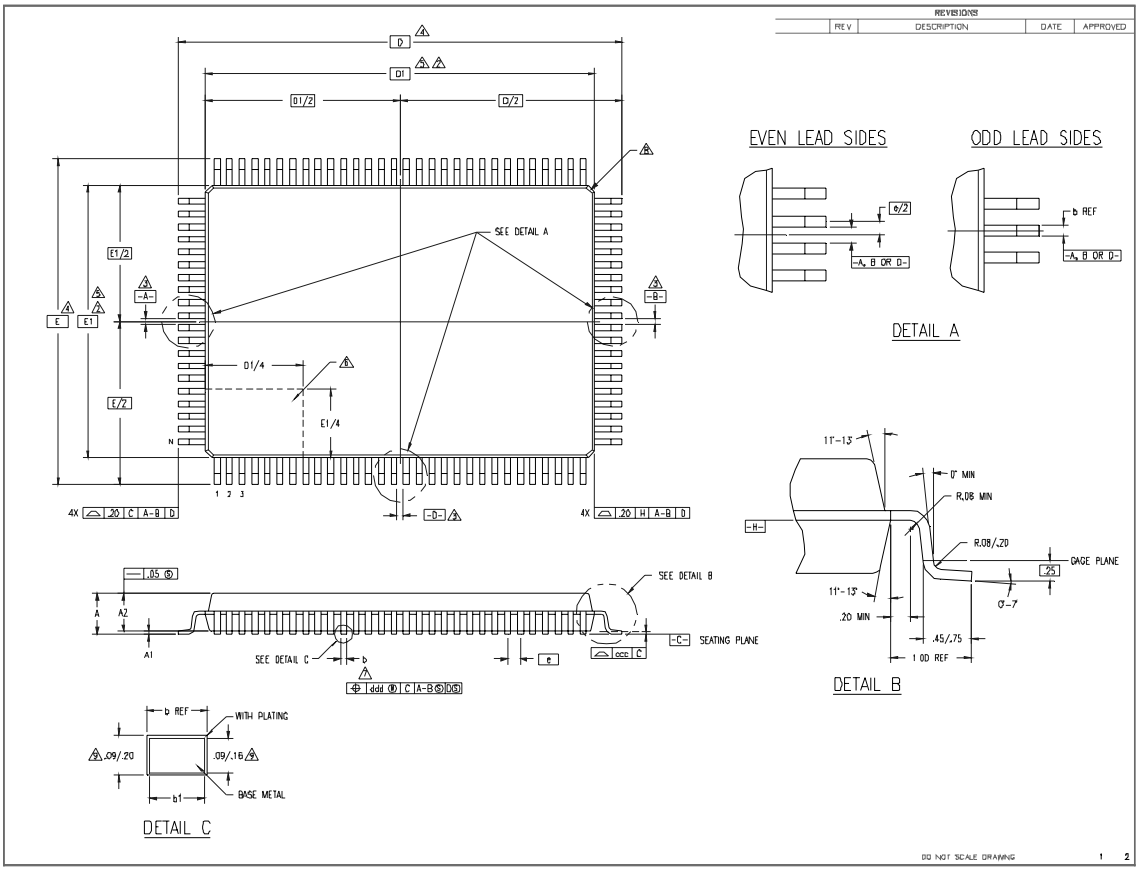
# Non-Burst Write Cycle Timing Waveform

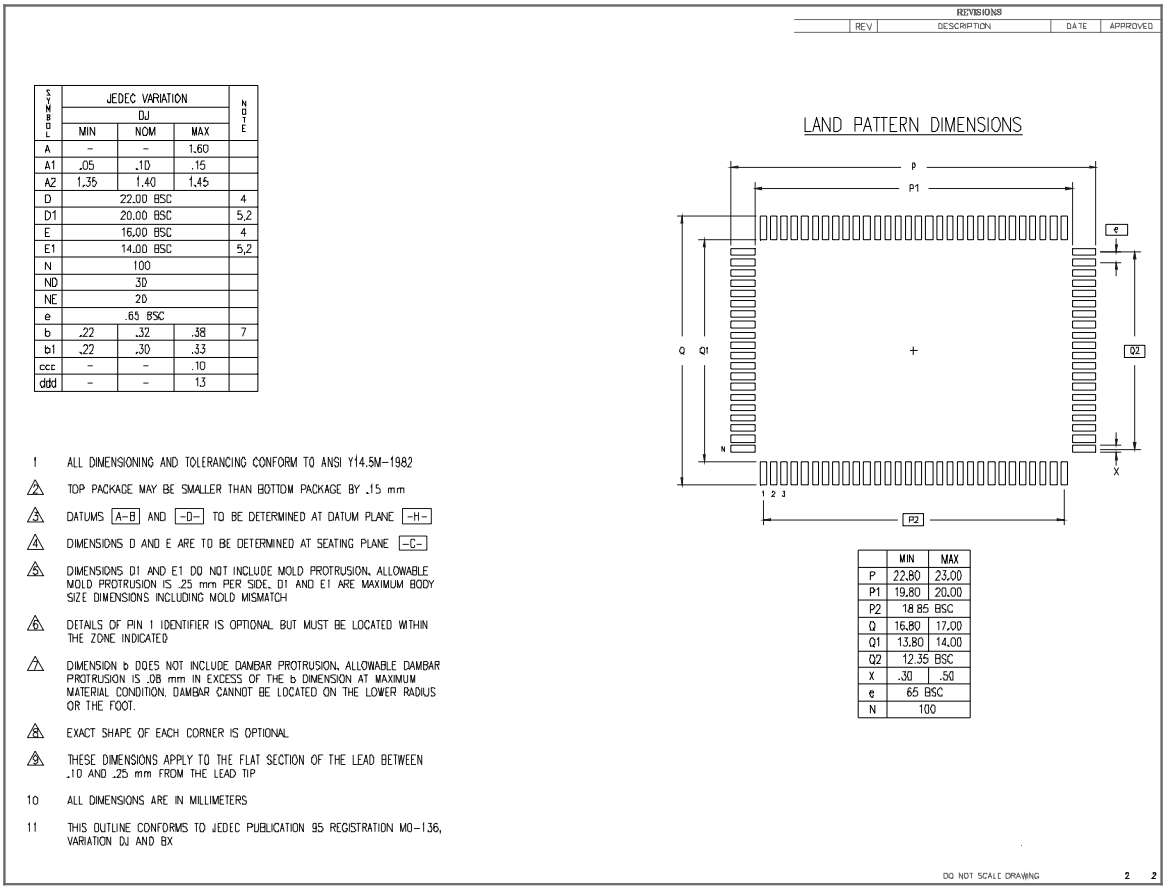



5310 drw 15

**NOTES:**
1. ZZ input is LOW, ADV and OE are HIGH, and LBO is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only GW writes are shown, the functionality of BWE and BWx together is the same as GW.
4. For write cycles, ADSP and ADSC have different limitations.

# 100-Pin Plastic Thin Quad Flatpack (TQFP) Package Diagram Outline




| SYMBOL | JEDEC VARIATION DJ | | | NOTE |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| A | – | – | 1.60 | |
| A1 | .05 | .10 | .15 | |
| A2 | 1.35 | 1.40 | 1.45 | |
| D | 22.00 BSC | | | 4 |
| D1 | 20.00 BSC | | | 5,2 |
| E | 16.00 BSC | | | 4 |
| E1 | 14.00 BSC | | | 5,2 |
| N | 100 | | | |
| ND | 30 | | | |
| NE | 20 | | | |
| e | .65 BSC | | | |
| b | .22 | .32 | .38 | 7 |
| b1 | .22 | .30 | .33 | |
| ccc | – | – | .10 | |
| ddd | – | – | .13 | |

LAND PATTERN DIMENSIONS




| | MIN | MAX |
|---|---|---|
| P | 22.80 | 23.00 |
| P1 | 19.80 | 20.00 |
| P2 | 18.85 BSC | |
| Q | 16.80 | 17.00 |
| Q1 | 13.80 | 14.00 |
| Q2 | 12.35 BSC | |
| X | .30 | .50 |
| e | 65 BSC | |
| N | 100 | |

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION DJ AND BX

DO NOT SCALE DRAWING 2 2

## ORDERING INFORMATION

| Alliance | Organization | VCC Range | Package | Operating Temp | Speed Mhz |
|---|---|---|---|---|---|
| AS8C803600-QC150N | 256K x 36 | 3.1 - 3.4V | 100 pin TQFP | Comercial: 0 - 70C | 150 |
| AS8C801800-QC150N | 512K x 18 | 3.1 - 3.4V | 100 pin TQFP | Comercial: 0 - 70C | 150 |

## PART NUMBERING SYSTEM

| AS8C | Device | Conf. | Mode | Package | Operating Temp | Speed | N |
|---|---|---|---|---|---|---|---|
| Sync. SRAM prefix | 80 = 8M | 18= x18<br>36 = x36 | 01= ZBT<br>00 = Pipelined<br>25 = Flow- Thru | Q = 100 Pin TQFP | 0 ~ 70C | 150MHz | N= Leadfree |

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Part Number: AS8C803600/801800
Document Version: v. 1.0

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