Radiation Hardened 5-channel Level Translator

with **cold sparing** and **3-state outputs**

1 GENERAL DESCRIPTION

The **AP54RHC504** is a radiation-hardened by design **5-channel level translator with 3-state outputs** that is ideally suited for space, medical imaging and other applications demanding radiation tolerance and high reliability. It is fabricated in a 180 nm CMOS process utilizing proprietary radiation-hardening techniques, delivering high resiliency to single-event effects (SEE) and to a total ionizing dose (TID) up to 30 krad (Si).

This device is a member of the Apogee Semiconductor AP54RHC logic family. All members of this family operate across a full **1.65 V to 5.5 V** range providing the system designer flexibility in logic-level interfaces. The AP54RHC504 can operate across this range on both of its supply voltage inputs, V_{CC}A and V_{CC}Y.

An output enable control pin allows the outputs to be placed in a high impedance (high-Z) state, simplifying usage in applications with shared busses or mixed power domains.

Zero-power penalty™ cold-sparing is supported, along with Class 2 ESD protection on all inputs and outputs. A proprietary output stage and robust power-on reset (POR) circuit allow the AP54RHC504 to be cold-spared in any redundant configuration with no static power loss on any pad of the device. The redundant output stage also features a high drive capability with low static power loss.

In addition, the AP54RHC504 features a triple-redundant design throughout its entire circuitry, which allows it to be immune to single-event transients (SET) without requiring additional redundant devices.

Ordering information may be found in Table 9 on Page 13.

1.1 FEATURES

- **1.65 VDC to 5.5 VDC** operation
- Inputs tolerant up to 5.5 VDC at any V_{CC}A or V_{CC}Y
- Extended operating temperature range (-55 °C to +125 °C)
- Proprietary **cold-sparing capability** with **zero** static power penalty
- **Built-in triple redundancy** for enhanced reliability
- Tri-state output drivers
- Class 2 ESD protection (4000 V HBM, 500 V CDM)
- TID resilience of **30 krad (Si)**
- SEL resilient up to LET of **80 MeV-cm²/mg**

1.2 LOGIC DIAGRAM

The AP54RHC504 logic function is shown below:

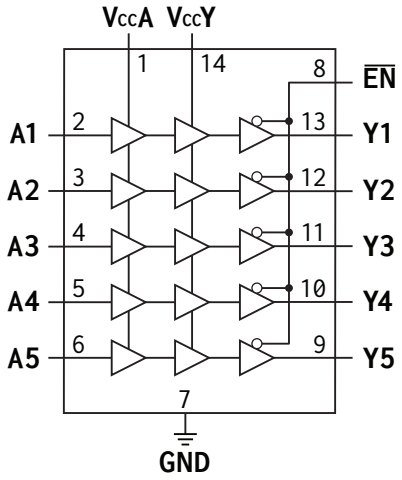

Figure 1: AP54RHC504 logic diagram

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2 ACRONYMS AND ABBREVIATIONS

ESD	Electrostatic Discharge
POR	Power On Reset
RHA	Radiation Hardness Assurance
SEE	Single Event Effects
SEL	Single Event Latchup
SET	Single Event Transient
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
CDM	Charged-device Model
HBM	Human-body Model

3 LOGIC DATA

The AP54RHC504 truth table is found in Table 1. **H** indicates HIGH logic level, **L** indicates LOW logic level, **X** indicates DON'T CARE and **Z** indicates HIGH-Z (TRI-STATE). Subscript **n** reflects one of the five buffers in the device (1 to 5). $V_{CC}A$ is unpowered when disconnected or shorted to GND.

Table 1: AP54RHC504 device truth table

Supply	Inputs		Output
$V_{CC}A$	$\overline{EN}$	A_n	Y_n
Unpowered	X	X	Z
Powered	H	X	Z
Powered	L	L	L
Powered	L	H	H

4 PIN CONFIGURATION

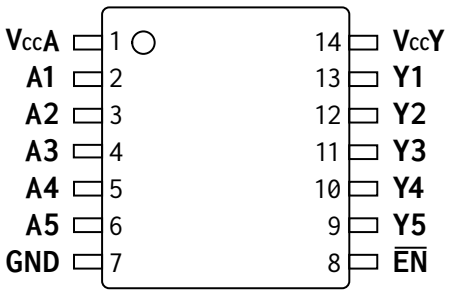


Figure 2: AP54RHC504 device pinout overview

Table 2: AP54RHC504 device pinout description

PIN NAME(S)	PIN NUMBER(S)	DESCRIPTION
A1 A2 A3 A4 A5	2 3 4 5 6	Inputs
Y1 Y2 Y3 Y4 Y5	13 12 11 10 9	3-State Outputs
$\overline{EN}$	8	Output Enable (active-low) referenced to $V_{CC}A$
$V_{CC}A$	1	Positive Voltage Supply (A Side)
$V_{CC}Y$	14	Positive Voltage Supply (Y Side)
GND	7	Ground

5 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

5.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 3 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (Table 4) is not guaranteed.

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 3: Absolute Maximum Ratings

SYMBOL	PARAMETER		VALUE	UNITS
$V_{CC}A$, $V_{CC}Y$	Supply Voltage		-0.5 to +5.5	V
V_I	Input voltage range		-0.5 to +5.5	V
V_O	Output voltage range		-0.5 to V_{CC} + 0.5 (1)	V
I_{IK} (V_I < 0)	Input clamp current		100	mA
I_O	Continuous output current (per pin)		100	mA
I_{CC}	Maximum supply current		100	mA
V_{ESD}	ESD Voltage	HBM	4000	V
		CDM	500	V
T_J	Operating junction temperature range		-55 to +150	°C
T_{STG}	Storage temperature range		-65 to +150	°C

(1) V_O must remain below absolute maximum rating of $V_{CC}A$, $V_{CC}Y$

5.2 RECOMMENDED OPERATING CONDITIONS

All recommended parameters below are specified across the entire operating temperature range unless otherwise specified.

Table 4: Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	MAX	UNITS
$V_{CC}A$, $V_{CC}Y$	Supply voltage		1.65	5.5	V
V_I	Input voltage range		0	5.5	V
V_O	Output voltage range		0	$V_{CC}Y$	V
V_{IH}	HIGH-level input voltage	$V_{CC}A$ = 1.65 to 1.95 V	1.4	-	V
		$V_{CC}A$ = 2.3 to 2.7 V	1.9	-	
		$V_{CC}A$ = 3.0 to 3.6 V	2.5	-	
		$V_{CC}A$ = 4.5 to 5.5 V	3.8	-	
V_{IL}	LOW-level input voltage	$V_{CC}A$ = 1.65 to 1.95 V	-	0.4	V
		$V_{CC}A$ = 2.3 to 2.7 V	-	0.6	
		$V_{CC}A$ = 3.0 to 3.6 V	-	0.9	
		$V_{CC}A$ = 4.5 to 5.5 V	-	1.35	
I_{OH}	HIGH-level output current	$V_{CC}Y$ = 1.65 to 1.95 V	-	-4	mA
		$V_{CC}Y$ = 2.3 to 2.7 V	-	-8	
		$V_{CC}Y$ = 3.0 to 3.6 V	-	-16	
		$V_{CC}Y$ = 4.5 to 5.5 V	-	-24	
I_{OL}	LOW-level output current	$V_{CC}Y$ = 1.65 to 1.95 V	-	4	mA
		$V_{CC}Y$ = 2.3 to 2.7 V	-	8	
		$V_{CC}Y$ = 3.0 to 3.6 V	-	16	
		$V_{CC}Y$ = 4.5 to 5.5 V	-	24	
t_r, t_f	Input rise or fall time (10% - 90%)	$V_{CC}A$ = 1.65 to 1.95 V	-	1000	ns
		$V_{CC}A$ = 2.3 to 2.7 V	-	600	
		$V_{CC}A$ = 3.0 to 3.6 V	-	500	
		$V_{CC}A$ = 4.5 to 5.5 V	-	400	

Table 5: Thermal Information

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_J	Operating junction temperature	-55	-	+125	°C
$R_{\theta JA}$	Junction to ambient thermal resistance	-	100	-	°C/W

5.3 STATIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 6: DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	$V_{CC}Y$	MIN	TYP	MAX	UNITS
V_{OL}	LOW-level output voltage[1]	I_O = 100 µA	1.65 to 5.5 V	-	0.02	0.05	V
		I_O = 1 mA	1.65 to 5.5 V	-	0.05	0.1	V
		I_O = 4 mA	2.3 V	-	0.3	0.6	V
			3.0 V	-	0.2	0.4	V
			4.5 V	-	0.2	0.4	V
		I_O = 8 mA	2.3 V	-	0.6	1.0	V
			3.0 V	-	0.4	0.8	V
			4.5 V	-	0.3	0.6	V
		I_O = 16 mA	3.0 V	-	1.0	1.4	V
			4.5 V	-	1.1	1.5	V
		I_O = 24 mA	4.5 V	-	1.1	1.5	V
V_{OH}	HIGH-level output voltage[1]	I_O = -100 µA	1.65 to 5.5 V	$V_{CC}Y$ - 0.1	$V_{CC}Y$ - 0.02	-	V
		I_O = -1 mA	1.65 to 5.5 V	$V_{CC}Y$ - 0.15	$V_{CC}Y$ - 0.08	-	V
		I_O = -4 mA	2.3 V	1.8	2.0	-	V
			3.0 V	2.6	2.8	-	V
			4.5 V	4.2	4.4	-	V
		I_O = -8 mA	2.3 V	1.4	1.7	-	V
			3.0 V	2.2	2.5	-	V
			4.5 V	3.9	4.1	-	V
		I_O = -16 mA	3.0 V	1.5	2.0	-	V
			4.5 V	3.3	3.8	-	V
		I_O = -24 mA	4.5 V	3.0	3.5	-	V
$I_{CC}Y$	Quiescent supply current	V_I = GND, $\overline{EN}$ = "0" I_O = 0 mA	5.5 V	-	100	150	µA
SYMBOL	**PARAMETER**	**CONDITIONS**	**$V_{CC}A$**	**MIN**	**TYP**	**MAX**	**UNITS**
I_I	Input current	V_I = V_{CC} or GND	1.65 to 5.5 V	-	-	±1	µA
I_{OZ}	Output leakage current[2]	V_I = V_{CC} or GND $\overline{EN}$ = "1"	1.65 to 5.5 V	-	-	±2.5	µA
I_{OFF}	Powerdown leakage current[2, 3]	V_I = V_{CC} or GND	0 to 5.5 V	-	-	5	µA
$I_{CC}A$	Quiescent supply current	V_I = V_{CC} or GND I_O = 0 mA	5.5 V	-	13	18	µA

(1) $V_{CC}A$ = 1.65 to 5.5 V for these conditions
(2) $V_{CC}Y$ = 0 to 5.5 V for these conditions
(3) V_{CC} is disconnected or at GND potential

5.4 DYNAMIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 7: AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	V_{CC} Y	MIN	TYP	MAX	UNITS
t_{pd} (1)	Propagation Delay (Input **A** to Output **Y**)	C_L = 50 pF	4.5 to 5.5 V	-	7.6	11	ns
			3.0 to 3.6 V	-	9	13	ns
			2.3 to 2.7 V	-	11	15	ns
			1.65 to 1.95 V	-	17	25	ns
t_{en} (2)	Output Enable Time (Input $\overline{\textbf{EN}}$ to Output **Y**)	C_L = 50 pF	4.5 to 5.5 V	-	15	25	ns
			3.0 to 3.6 V	-	22	35	ns
			2.3 to 2.7 V	-	29	41	ns
			1.65 to 1.95 V	-	43	53	ns
t_{dis} (3)	Output Disable Time (Input $\overline{\textbf{EN}}$ to Output **Y**)	C_L = 50 pF	4.5 to 5.5 V	-	16	25	ns
			3.0 to 3.6 V	-	22	35	ns
			2.3 to 2.7 V	-	28	40	ns
			1.65 to 1.95 V	-	42	51	ns
t_{sk}	Channel-to-channel skew	C_L = 50 pF	1.65 to 5.5 V	-	-	1	ns
C_{IN}	Input Capacitance(4)	V_I = V_{CC} or GND	1.65 to 5.5 V	-	2	4	pF
C_{PD}	Power dissipation capacitance(4)	I_O = 0 mA, f = 1 MHz	5.5 V	-	40	-	pF

(1) equivalent to t_{PLH}, t_{PHL}
(2) equivalent to t_{PZL}, t_{PZH}
(3) equivalent to t_{PLZ}, t_{PHZ}
(4) guaranteed by design

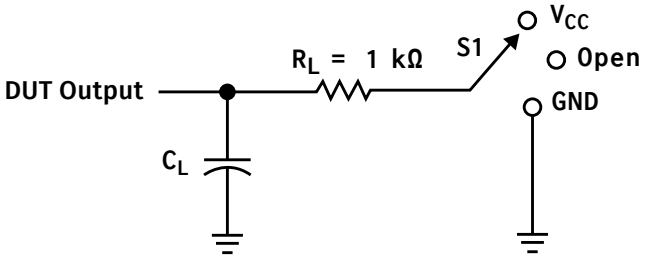
5.5 RADIATION RESILIENCE

For detailed radiation testing reports, please contact Apogee Semiconductor at sales@apogeesemi.com.

Table 8: Radiation Resilience Characteristics

PARAMETER	CONDITIONS	VALUE	UNITS
Total Ionizing Dose (TID)	Please contact Apogee Semiconductor for test report.	30	krad (Si)
SEE LET Threshold	Please contact Apogee Semiconductor for test report.	<80	MeV-cm^2/mg

5.6 CHARACTERISTICS MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}, t_{PZL}	V_{CC}
t_{PHZ}, t_{PZH}	GND

Figure 3: Load circuit for 3-state outputs

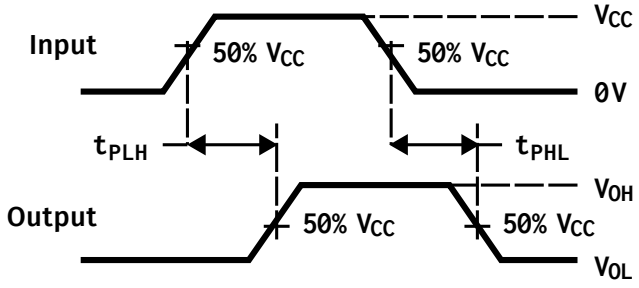


Figure 4: Propagation delay measurement

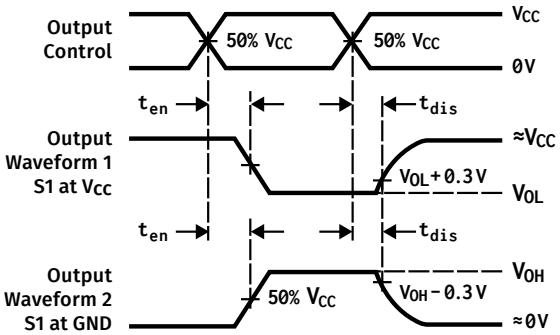


Figure 5: Enable and disable times, for low- and high-level enables

6 DETAILED DESCRIPTION

The AP54RHC504 is a 5-channel level translator with 3-state outputs designed to operate from a wide supply voltage of 1.65 to 5.5 V with fully redundant input and output stages, providing for superior radiation resilience.

The output and input stages are constructed with transient activated clamps (Figure 6, 7) that prevent inadvertent biasing of the V_{CC} power rail through parasitic diodes inherent to conventional input, output, and ESD circuits. To prevent the Y outputs that are referenced to $V_{CC}Y$ from powering up in an erroneous condition, the $V_{CC}A$ supply should power on before power is applied to $V_{CC}Y$. Powering $V_{CC}A$ on first ensures that the Y outputs will power on to the correct logic levels applied at the A inputs.

The AP54RHC family's I/O protection circuitry allows for cold sparing configurations as it avoids a leakage current penalty on inputs and outputs while in a power-down state. This can result in considerable power savings in systems where multiple-path redundancy is employed. The ESD clamp circuits for this logic family are designed to support Class 2 ESD levels of 4 kV HBM and 500 V CDM.

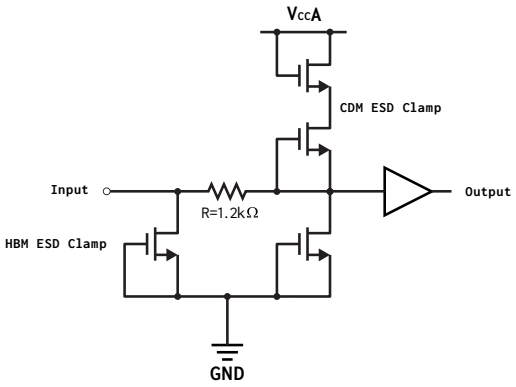


Figure 6: Details of input pin structure

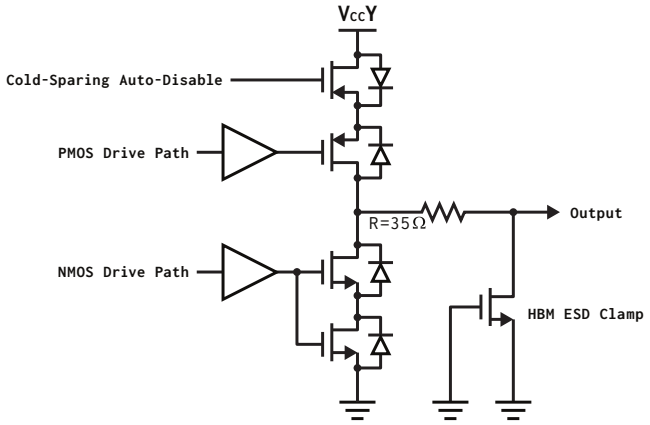


Figure 7: Details of output pin structure

7 APPLICATIONS INFORMATION

The AP54RHC504 provides a simple and robust means of interfacing digital logic between different voltage levels and domains. It can shift logic signals up from a lower voltage to a higher voltage or shift signals down from higher to lower voltages. The outputs may be tri-stated through assertion of the $\overline{EN}$ pin, which can be tied with power-supply enables or other control signals biased with reference to $V_{CC}A$.

Note

During tri-state, the application must ensure that the output pins are either held or switched to logic high or logic low levels i.e. close to $V_{CC}Y$ or **GND**, otherwise increased supply current can occur.

In an application utilizing a modern FPGA with 1.8 V I/O buffers that needs to interface to systems running at higher voltages (i.e. 5 V), the AP54RHC504 can be used to shift these signals to a range appropriate for the FPGA. The AP54RHC504 provides integrated triple modular redundancy (TMR), as well as SET resiliency on each buffer. In the event the 5 V supply is off, the AP54RHC504 will automaticaly tri-state the output buffers. The $\overline{EN}$ pin of the device can be tied to the FPGA power-enable logic such that $\overline{EN}$ is de-asserted when the 1.8 V I/O rail is not present.

7.1 APPLICATIONS EXAMPLE

As the AP54RHC family is radiation-hardened by design and includes internal TMR, it can be utilized in high-reliablity applications without additional supporting circuitry or devices. Nonetheless, some application requirements call for fully-redundant designs, where an “A” and a “B” device are required, often on separate power rails.

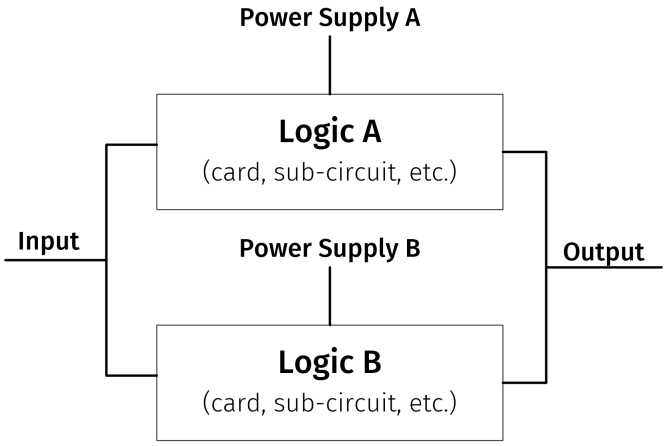


Figure 8: Cold sparing example.

With the cold-sparing capability of the AP54RHC family, fully redundant “A” and “B” functions may be placed in parallel (as seen in Figure 8) running off redundant power supplies. The inputs and outputs on each one of these functions are assumed to be based on the AP54RHC family, allowing for direct parallel connection without unwanted leakage current paths during cold sparing. In the event of a failure in power supply A or within function A, the system can simply shut power supply A off and switch on power supply B, without requiring additional input or output switching or configuration changes.

7.2 POWER SUPPLY RECOMMENDATIONS

This device can operate at any voltage within the range specified in Table 4 Recommended Operating Conditions.

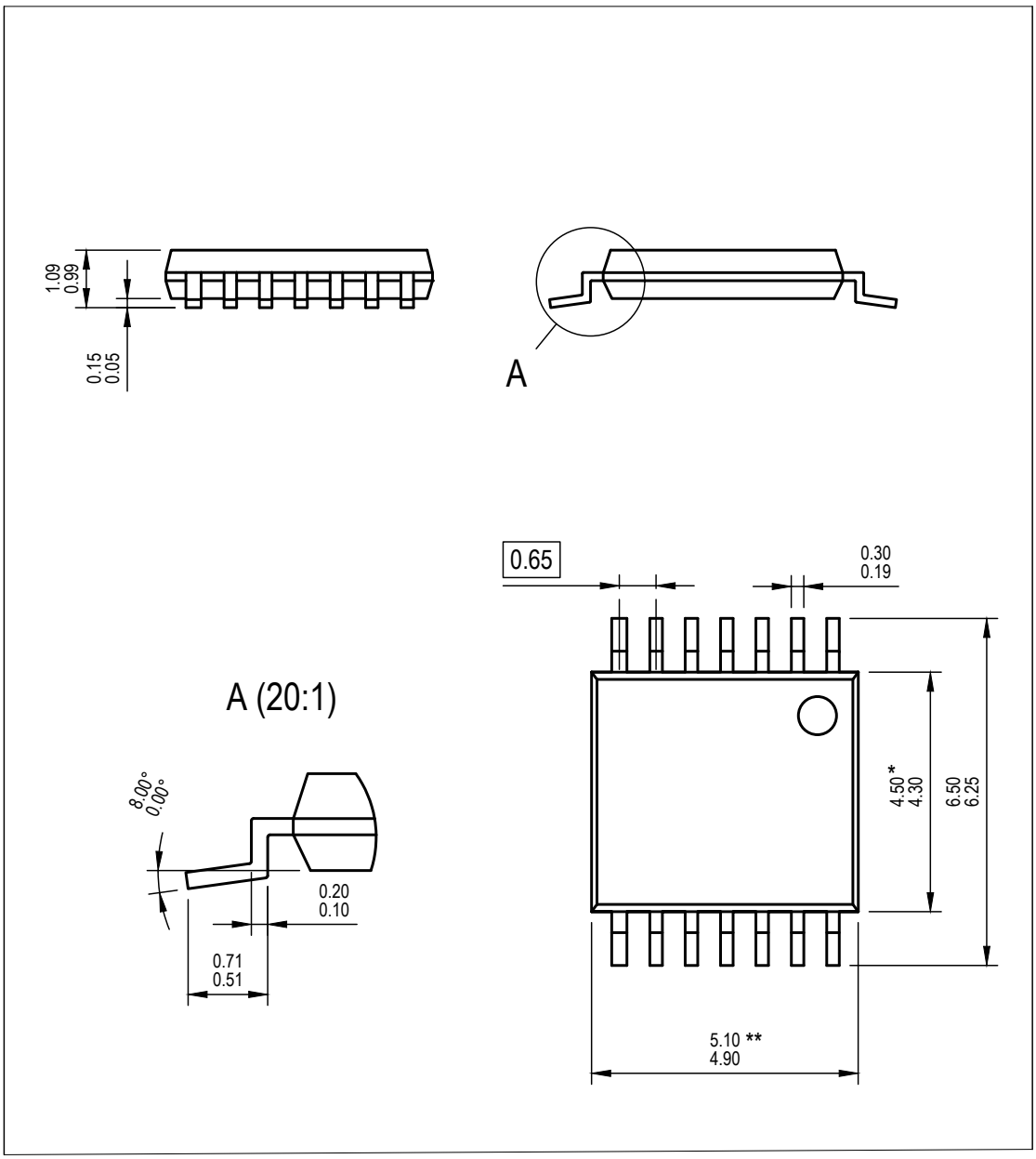
At a minimum, a 16 VDC (or higher), X7R-rated 0.1 µF ceramic decoupling capacitor should be placed near (within 1 cm) the V_{CC} pins of the device.

7.3 APPLICATION TIPS

Unused **inputs** must **not** be left floating. They may be connected to either a low (GND) or high (V_{CC}A) bias to provide a known state at the input of the device. Resistors may be used to tie off unused inputs. In the event of a design change, such resistors can be removed, thereby allowing use of the inputs without having to cut traces on the PCB.

An unused **output** may be left floating. It is suggested that it be routed to a test point or similar accessible structure in case the associated function needs to be utilized as part of a design revision.

8 PACKAGING INFORMATION



Notes:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

* Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25 mm each side.
** Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

Figure 9: Package Mechanical Detail

9 ORDERING INFORMATION

Example part numbers for the AP54RHC504 are listed in Table 9. The full list of options for this part can be found in Figure 10. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead time and purchasing on specific part numbers.

Table 9: AP54RHC504 Ordering Information

DEVICE	DESCRIPTION	PACKAGE
AP54RHC504ALT-W	Radiation Hardened 5-channel Level Translator (30 krad (Si))	Plastic TSSOP-14
AP54RHC504ELT-R	Radiation Hardened 5-channel Level Translator (for evaluation only)	Plastic TSSOP-14

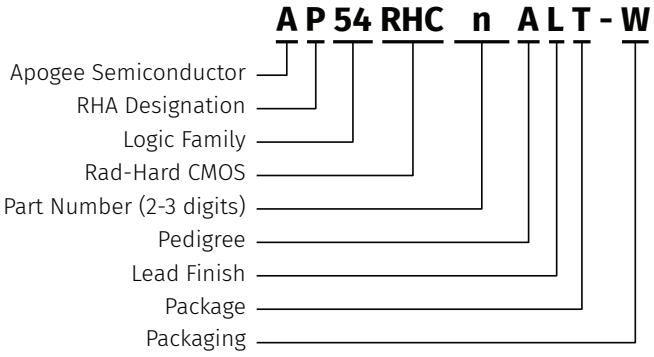


Figure 10: Part Number Decoder

1. RHA Designation
   - **P** 30 krad (Si)
2. Part Number
   - **_** 504 (5-channel level translator with 3-state outputs)
3. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
4. Lead Finish
   - **L** Tin-Lead (SnPb)
5. Package
   - **T** 14-pin Thin Shrink Small Outline Package (TSSOP)
6. Packaging
   - **W** Waffle Pack or ESD Foam Box
   - **R** Tape and Reel[1]

[1] Contact us for custom reel quantities. Orders less than full reel quantities may be shipped as cut tape.

10 REVISION HISTORY

REVISION	DESCRIPTION	DATE
A09	Updated detailed description with power-up sequence and $\overline{EN}$ biasing reference	2023-05-26
A08	Updated pin structure diagram, tri-state biasing in application information, and ordering information	2022-05-08
A07	Correct output pin structure diagram.	2021-12-06
A06	Updated ordering information.	2021-07-30
A05	Formatting updates.	2021-06-23
A04	Correct test conditions for 1.65 VDC at -4 mA.	2021-01-19
A03	Further updates to static and dynamic characteristics.	2020-12-16
A02	Update Static and Dynamic characteristics.	2020-10-23
A01	Initial public release.	2020-02-29
A00	Initial internal release.	2019-07-05

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11 LEGAL

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