

## DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

### Product Summary

$V_{(BR)DSS}$	$R_{DS(on) \max}$	$I_D$ $T_A = +25^\circ\text{C}$
-30V	65m $\Omega$ @ $V_{GS} = -10\text{V}$	-4.4A
	115m $\Omega$ @ $V_{GS} = -4.5\text{V}$	-3.2A

### Description

This new generation MOSFET has been designed to minimize the on-state resistance ( $R_{DS(ON)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.


### Applications

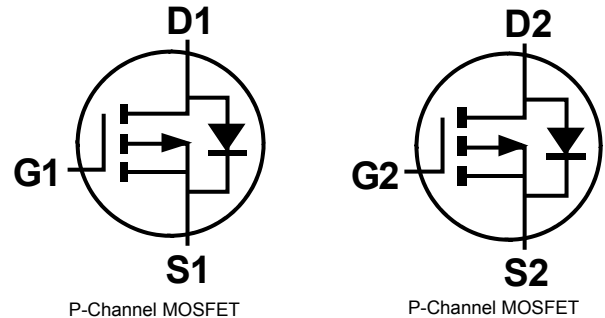
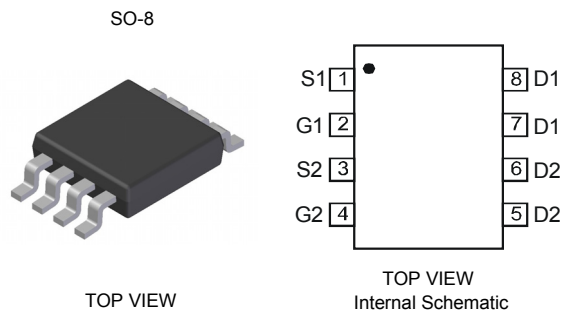
- Power Management Functions
- Analog Switch
- Load Switch
- Boost Switch

### Features

- Dual P-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q101 Standards for High Reliability**

### Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 
- Weight: 0.072g (approximate)

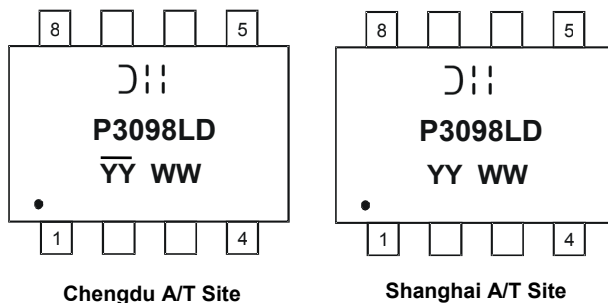



### Ordering Information (Note 4)

Part Number	Case	Packaging
DMP3098LSD-13	SO-8	2,500/Tape & Reel

- Notes:
- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  - See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  - For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

### Marking Information



 = Manufacturer's Marking  
 P3098LD = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY or YY = Year (ex: 14 = 2014)  
 WW = Week (01 - 53)  
 YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)  
 YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V <sub>DSS</sub>	-30	V
Gate-Source Voltage			V <sub>GSS</sub>	±20	V
Drain Current (Note 5)	Steady State	T <sub>A</sub> = +25°C	I <sub>D</sub>	-4.4	A
		T <sub>A</sub> = +70°C		-3.3	
Pulsed Drain Current (Note 6)			I <sub>DM</sub>	-15	A

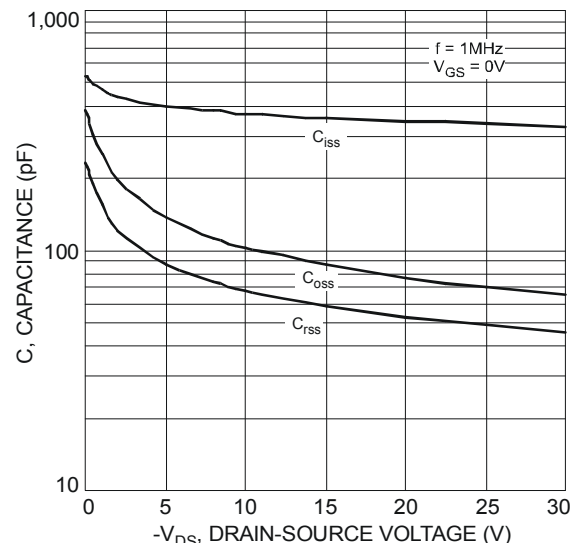
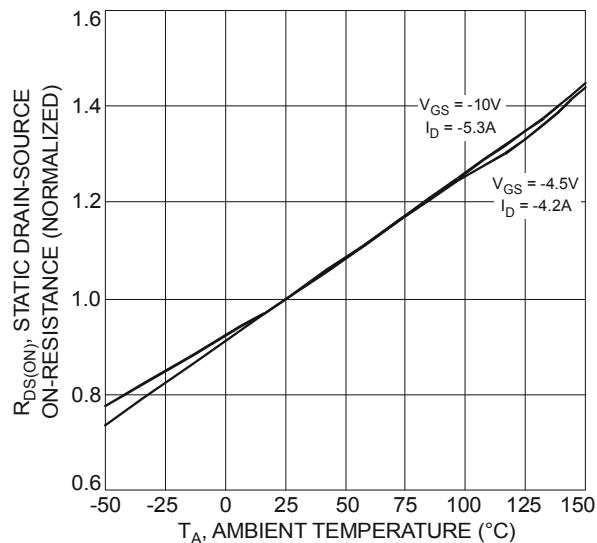
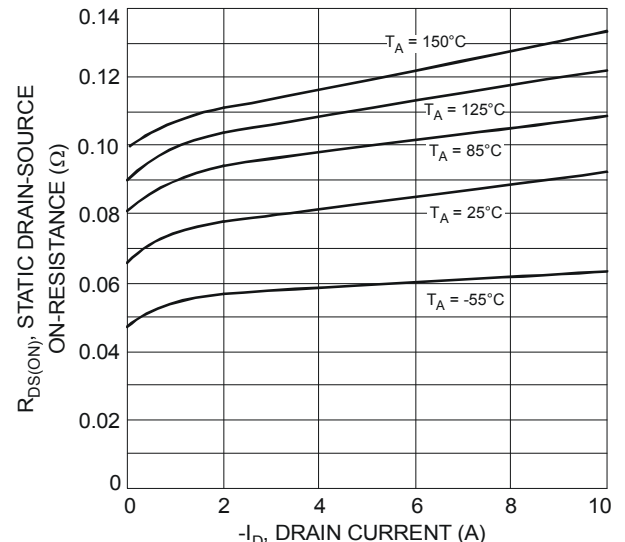
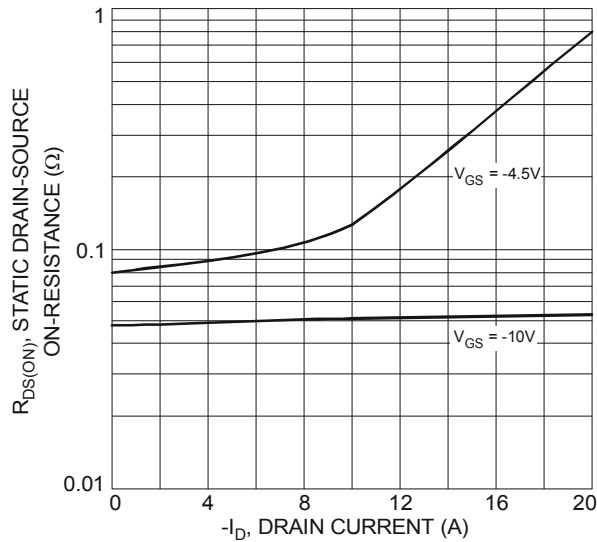
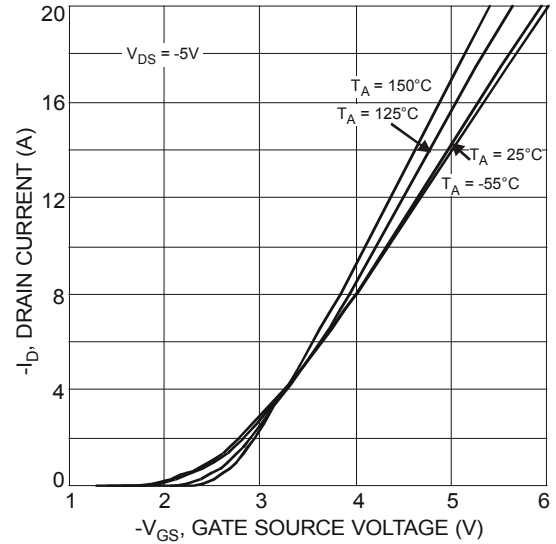
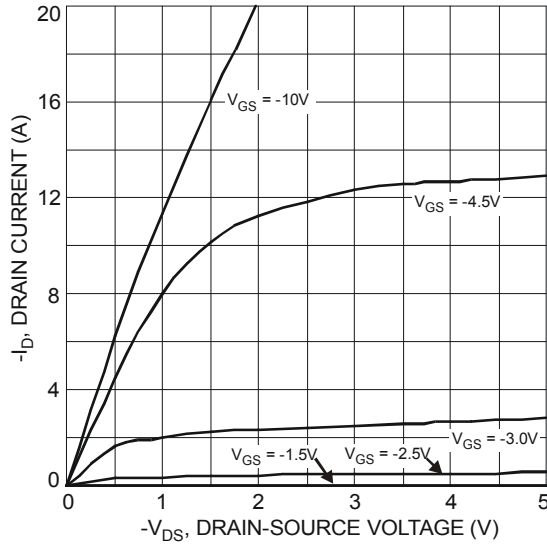
**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	1.8	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	70	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-1	μA	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1	1.7	-2.1	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	56	65	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -5.0A
		—	98	115		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.0A
Forward Transconductance	g <sub>fs</sub>	—	5.2	—	S	V <sub>DS</sub> = -10V, I <sub>D</sub> = -5.0A
Diode Forward Voltage (Note 7)	V <sub>SD</sub>	-0.5	—	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -2.6A
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	C <sub>iss</sub>	—	336	—	pF	V <sub>DS</sub> = -25V, V <sub>GS</sub> = 0V f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	70	—	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	49	—	pF	
Gate Resistance	R <sub>G</sub>	—	4.6	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
<b>SWITCHING CHARACTERISTICS</b>						
Total Gate Charge	Q <sub>g</sub>	—	4.0 7.8	—	nC	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5.0A V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -5.0A
Gate-Source Charge	Q <sub>gs</sub>	—	1.0	—		V <sub>DS</sub> = -15V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5.0A
Gate-Drain Charge	Q <sub>gd</sub>	—	2.5	—		V <sub>DS</sub> = -15V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5.0A
Turn-On Delay Time	t <sub>d(on)</sub>	—	6.0	—	ns	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -1A, R <sub>G</sub> = 6.0Ω
Rise Time	t <sub>r</sub>	—	5.0	—		
Turn-Off Delay Time	t <sub>d(off)</sub>	—	17.6	—		
Fall Time	t <sub>f</sub>	—	9.5	—		

Notes: 5. Device mounted on 2 oz. 1" x 1" Copper pads on 2" x 2" FR-4 PCB.  
6. Pulse width ≤10μS, Duty Cycle ≤1%.  
7. Short duration pulse test used to minimize self-heating effect.



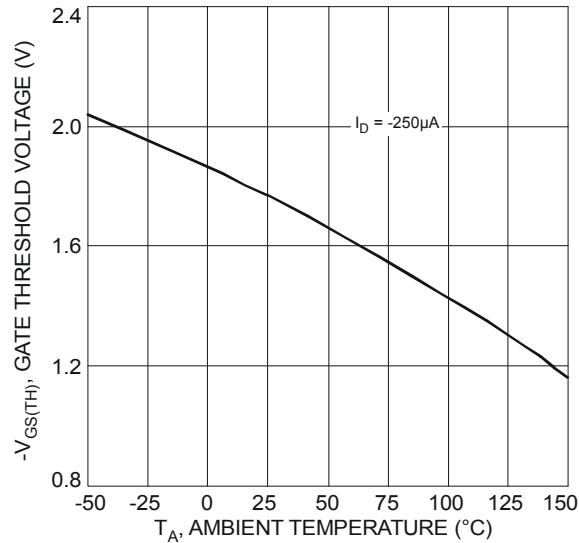


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

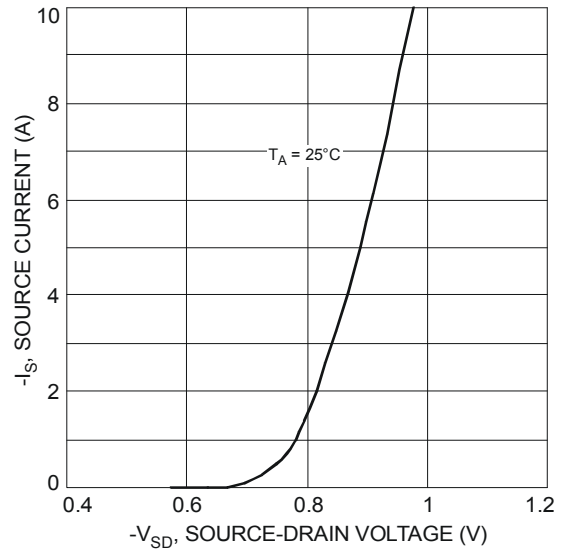
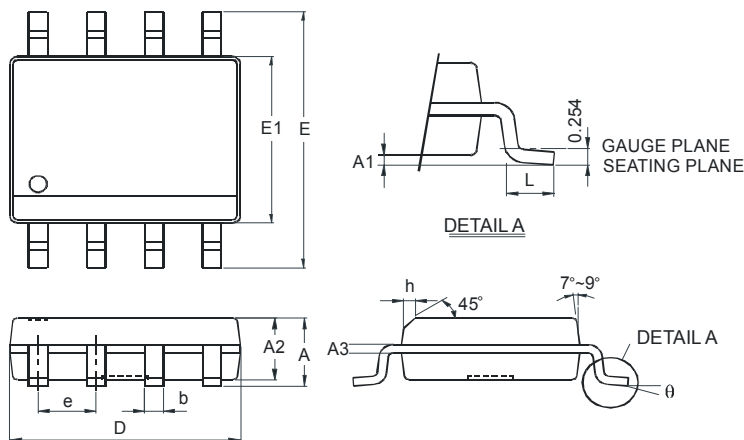


Fig. 8 Diode Forward Voltage vs. Current

## Package Outline Dimensions

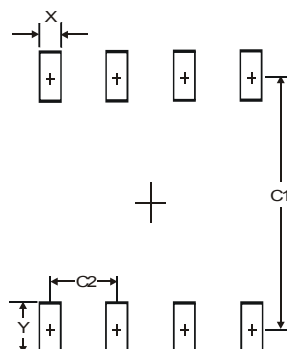
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

## Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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