A Product Line of
Diodes Incorporated

PI3WVR2646

2:1 MIPI 4-Data Lane Switch

Features

- SPDT (10x) Switch Type and Signal Type Support D-PHY and C-PHY
- Data Rate: D-PHY (2.5Gbps) 4-Data Lane and C-PHY (2.5Gsps) 3-Data Lane
- Supports 2:1 clock differential signal
- -3 dB Bandwidth: 4.1 GHz Typical
- Low Crosstalk: -30 dB@1.25 GHz
- Input Signals 0 to 1.3V
- R_{ON}: 6Ω Typical LP & HS MIPI
- ΔR_{ON}: 0.1Ω Typical LP & HS MIPI
- R_{ON_FLAT}: 0.3Ω Typical LP & HS MIPI
- I_{CCZ}: 0.5uA Typical
- I_{CC}: 32μA Max
- C_{ON}: 1.5pF Typical
- Skew of Opposite Transitions of the Same Output: 6ps Typical
- V_{DD} Operating Range: 1.5V to 3.6V
- ESD Tolerance: 2kV HBM
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 36-Ball, WLCSP (GH) 2.10x2.10

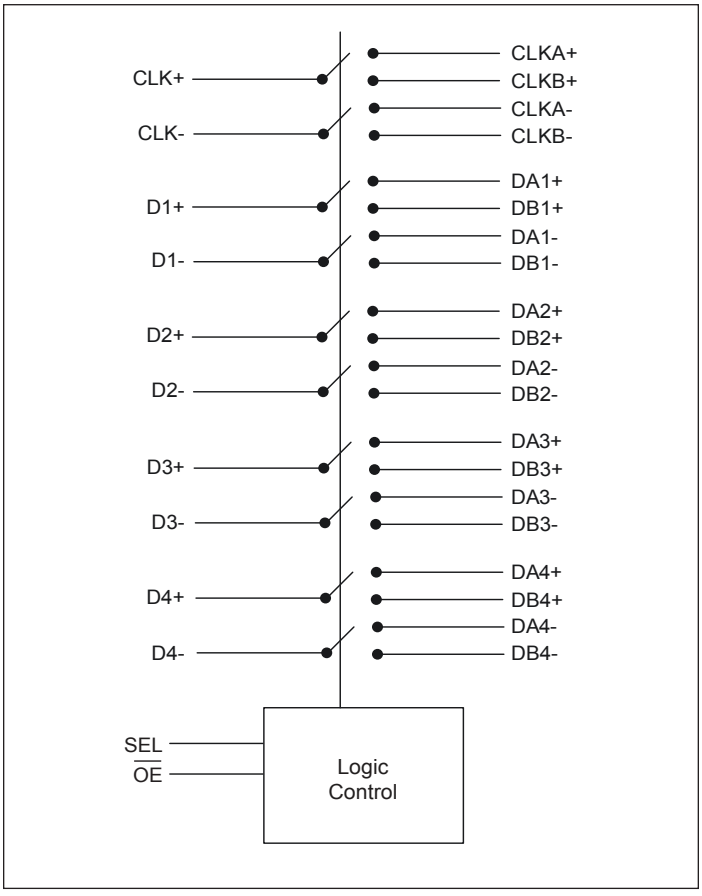
Application(s)

- Cellular Phones, Smart Phone
- Tablets
- Laptops
- Displays

Description

The DIODES™ PI3WVR2646 is a four-data-lane MIPI-D-PHY switch. This 10 channel single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed (HS) or low-power (LP) MIPI signal. The PI3WVR2646 is designed for the MIPI specification and allows connection to a CSI or DSI module.

Block Diagram



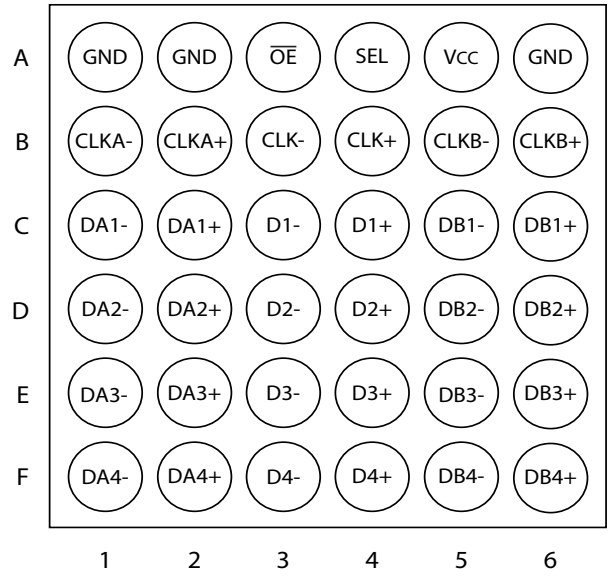
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Truth Table

SEL	$\overline{OE}$	Function
LOW	LOW	CLK+ = CLKA+, CLK- = CLKA-, Dn(+/-) = DAn(+/-)
HIGH	LOW	CLK+ = CLKB+, CLK- = CLKB-, Dn(+/-) = DBn(+/-)
X	HIGH	Clock and Data Ports High Impedance

Pin Configuration(Top View)



Pin Description

Pin#	Pin Name	Type	Description
A1	GND	Ground	Ground
A2	GND	Ground	Ground
A3	$\overline{OE}$	I	Output enable. if $\overline{OE}$ is low, IC is enabled. if $\overline{OE}$ is high, IC is power down and all I/Os are Hi-Z
A4	SEL	I	Switch logic control
A5	VCC	Power	1.5V to 3.6V power supply
A6	GND	Ground	Ground
B1	CLKA-	I/O	Clock negative differential signal for port A
B2	CLKA+	I/O	Clock positive differential signal for port A
B3	CLK-	I/O	Clock negative differential signal for COM port
B4	CLK+	I/O	Clock positive differential signal for COM port
B5	CLKB-	I/O	Clock negative differential signal for port B
B6	CLKB+	I/O	Clock positive differential signal for port B
C1	DA1-	I/O	Negative differential signal 1 for port A
C2	DA1+	I/O	Positive differential signal 1 for port A

Pin Description Cont.

Pin#	Pin Name	Type	Description
C3	D1-	I/O	Negative differential signal 1 for COM port
C4	D1+	I/O	Positive differential signal 1 for COM port
C5	DB1-	I/O	Negative differential signal 1 for port B
C6	DB1+	I/O	Positive differential signal 1 for port B
D1	DA2-	I/O	Negative differential signal 2 for port A
D2	DA2+	I/O	Positive differential signal 2 for port A
D3	D2-	I/O	Negative differential signal 2 for COM port
D4	D2+	I/O	Positive differential signal 2 for COM port
D5	DB2-	I/O	Negative differential signal 2 for port B
D6	DB2+	I/O	Positive differential signal 2 for port B
E1	DA3-	I/O	Negative differential signal 3 for port A
E2	DA3+	I/O	Positive differential signal 3 for port A
E3	D3-	I/O	Negative differential signal 3 for COM port
E4	D3+	I/O	Positive differential signal 3 for COM port
E5	DB3-	I/O	Negative differential signal 3 for port B
E6	DB3+	I/O	Positive differential signal 3 for port B
F1	DA4-	I/O	Negative differential signal 4 for port A
F2	DA4+	I/O	Positive differential signal 4 for port A
F3	D4-	I/O	Negative differential signal 4 for COM port
F4	D4+	I/O	Positive differential signal 4 for COM port
F5	DB4-	I/O	Negative differential signal 4 for port B
F6	DB4+	I/O	Positive differential signal 4 for port B

Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

V_{CC}, Supply Voltage, ... -0.5V to 4.5V
V_{CNTRL}, DC Input Voltage ($\overline{OE}$, SEL)(1) ..... -0.5V to V_{CC}
V_{SW}, DC Switch I/O Voltage(1,2) ..... -0.3V to 2.5V
I_{IK}, DC Input Diodes Current ..... -50mA
I_{OUT}, DC Output Current 25mA
T_{STG}, Storage Temperature ..... -65°C to +150°C
Tj, Junction Temperature ..... 125°C
ESD:
Human Body Model, JEDEC: JESD22-A114, All Pins 2.0kV
Charged Device Model, JEDEC: JESD22-C101 ..... 1.0kV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V_{SW} refers to analog data switch paths.

Recommended Operating Conditions

The Recommended operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Description	Test Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		1.5	3.6	V
V_{CNTRL}	Control Input Voltage (SEL, $\overline{OE}$)(1)		0	V_{CC}	V
V_{SW}	Switch I/O Voltage (CLK-, D-, CLKA-, CLKB-, DA-, DB-)	- HS Mode	0	0.5	V
		- LP Mode	0	1.3	V
T_A	Operating Temperature		-40	+85	°C

Note:

1. The control inputs must be held HIGH or LOW; they must not float.

DC and Transient Characteristics

All typical values are at T_A = 25°C unless otherwise specified.

Symbol	Description	Test Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage ($\overline{OE}$, SEL)	I_{IN} = -18mA	1.5	-1.2		-0.6	V
V_{IH}	Input Voltage High	SEL, $\overline{OE}$	1.5 to 3.3	1.0			V
V_{IL}	Input Voltage Low	SEL, $\overline{OE}$	1.5 to 3.3			0.5	V
I_{IN}	Control Input Leakage ($\overline{OE}$, SEL)	V_{CNTRL} = 0 to V_{CC}	3.3	-0.5		0.5	µA
$I_{NO(OFF)}$ $I_{NC(OFF)}$	Off Leakage Current of Port	V_{SW} = 0.0 ≤ DATA ≤ 1.3V	3.3	-0.5		0.5	µA
$I_{A(ON)}$	On Leakage Current of Common Ports	V_{SW} = 0.0 ≤ DATA ≤ 1.3V	3.3	-0.5		0.5	µA

DC and Transient Characteristics Cont.

Symbol	Description	Test Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW} = 0.0 or 1.3V	0	-0.5		0.5	µA
I_{OZ}	Off-State Leakage	V_{SW} = 0.0 ≤ DATA ≤ 1.3V, $\overline{OE}$ = High	3.6	-0.5		0.5	µA
$R_{ON\_MIPI\_HS}$	Switch On Resistance for HS MIPI	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, All I/O Switches = 0.2V	1.5		6		Ω
			2.5				
			3.3				
$R_{ON\_MIPI\_LP}$	Switch On Resistance for LP MIPI	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, All I/O Switches = 1.2V	1.5		6		Ω
			2.5				
			3.3				
$\Delta R_{ON\_MIPI\_HS}$	On Resistance Matching Between HS MIPI Channels(1)	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, All I/O Switches = 0.2V	1.5		0.1		Ω
			2.5				
			3.3				
$\Delta R_{ON\_MIPI\_LP}$	On Resistance Matching Between LP MIPI Channels(1)	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, All I/O Switches = 1.2V	1.5		0.1		Ω
			2.5				
			3.3				
$R_{ON\_FLAT\_MIPI\_HS}$	On Resistance Flatness for HS MIPI	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, All I/O Switches = 0 to 0.5V	1.5		0.3		Ω
			2.5				
			3.3				
$R_{ON\_FLAT\_MIPI\_LP}$	On Resistance Flatness for LP MIPI	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, All I/O Switches = 0 to 1.3V	1.5		0.3		Ω
			2.5				
			3.3				
I_{CC}	Quiescent Supply Current	V_{SEL} = 0 or V_{CC}, I_{OUT} = 0, $\overline{OE}$ = 0V	3.6		15	32	µA
I_{CCZ}	Quiescent Supply Current (High Impedance)	V_{SEL} = 0 or V_{CC}, I_{OUT} = 0, $\overline{OE}$ = High	3.6		0.5	1.0	µA
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	V_{SEL} = 0 or V_{CC}, $\overline{OE}$ = 1.5V	3.6		1		µA

AC Electrical Characteristics

All typical values are for V_{CC} = 3.3V and T_A = 25°C unless otherwise specified.

Symbol	Description	Test Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
t_{INIT}	Initialization Time V_{CC} to Output(1)	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 3.6		60		µs
t_{EN}	Enable Time $\overline{OE}$ to Output	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 3.6		60	150	µs
t_{DIS}	Disable Time $\overline{OE}$ to Output	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 3.6		35	250	ns
t_{ON}	Turn-On Time SEL to Output	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 3.6		350	1500	ns
t_{OFF}	Turn-Off Time SEL to Output	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 3.6		125	800	ns
t_{BBM}	Break-Before-Make Time	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 3.6			1000	ns
t_{PD}	Propagation Delay(1)	C_L = 0pF, R_L = 50Ω	1.5 to 3.6			0.25	ns
O_{IRR}	Differential Off Isolation for MIPI(1)	R_L = 50Ω, f = 1250MHz, $\overline{OE}$ = HIGH, V_{SW} = 0.5V	1.5 to 3.6		-26		dB
X_{TALK}	Differential Crosstalk for MIPI(1)	R_L = 50Ω, f = 1250MHz, SEL = HIGH, V_{SW} = 0.5V	1.5 to 3.6			-30	dB
I_{LOSS}	Differential Insertion Loss(1)	R_L = 50Ω, C_L = 0pF, f = 1250MHz, V_{SW} = 0.5V	1.5 to 3.6		-0.8		
BW	Differential -3db Bandwidth(1)	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.5V	1.5 to 3.6	3	4.1		GHz

Note:

1. Guaranteed by characterization.

High-Speed-Related AC Electrical Characteristics

Symbol	Description	Test Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
$t_{SK(P)}$	D-PHY HS Mode Skew of Opposite Transitions of the Same Output(1)	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.3V	1.5 to 3.6		4		ps
	C-PHY HS Mode Skew of 3 channels in same lane	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.5V	1.5 to 3.6		4		
	D-PHY HS Mode Skew of all group A or group B channels(1)	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.3V	1.5 to 3.6		8		

Note:
1. Guaranteed by characterization.

Capacitance

Symbol	Description	Test Conditions	T_A = -40°C to +85°C			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance(1)	V_{CC} = 0V, f = 1MHz		2.1		pF
C_{ON}	On Capacitance(1)	V_{CC} = 3.3V, $\overline{OE}$ = 0V, f = 1250MHz (In HS common value)		1.5		pF
C_{OFF}	Off Capacitance(1)	V_{CC} or $\overline{OE}$ = 3.3V, f = 1250MHz (Both sides in HS common value)		0.9		pF

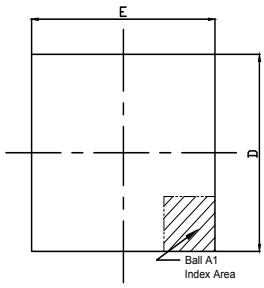
Note:
1. Guaranteed by characterization.

Part Marking

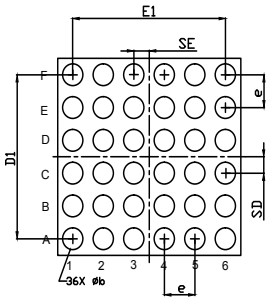
Z: Die Rev
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code

Packaging Mechanical

36-WLCSP (GH)

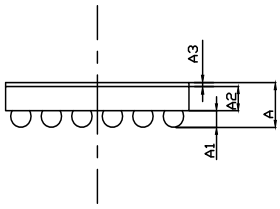


TOP VIEW

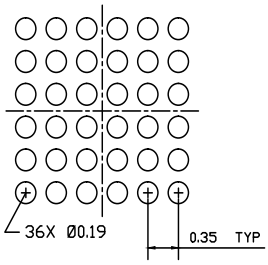


BOTTOM VIEW

PKG.	DIMENSIONS(MM)		
SYMBOL	Min.	Nom.	Max.
A	0.393	0.438	0.483
A1	0.135	0.155	0.175
A2	0.238	0.258	0.278
A3	0.020	0.025	0.030
D	2.070	2.100	2.130
E	2.070	2.100	2.130
D1	1.700	1.750	1.800
E1	1.700	1.750	1.800
b	0.190	0.210	0.230
e	0.350BSC		
SD	0.175 BSC		
SE	0.175 BSC		



SIDE VIEW



BOTTOMRECOMMEND LAND PATTERN VIEW

Note:

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

DIODES INCORPORATED PERICOM ENABLING SERIAL CONNECTIVITY

DATE: 02/10/20

DESCRIPTION: 36-Ball, WLCSP, 2.10x2.10 (X1-WLB2121-36)

PACKAGE CODE: GH (GH36)

DOCUMENT CONTROL #: PD-2252 **REVISION:A**

20-1127

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI3WVR2646GHEX	GH	36-Ball, 2.10x2.10, (WLCSP) X1-WLB2121-36

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
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3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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