PI3HDX414

HDMI 1.4b 1:4 Splitter for 3.4 Gbps Data Rate with Equalization & Pre-emphasis

General Features

- **Support up to 3.4Gbps TMDS Serial Link Compliant with HDMI 1.4b requirement**
- **HDMI1.4b 1-to-4 Active Splitter and Demux up to 340 MHz TMDS Clock Frequency**
- **AC and DC Coupled Differential Signaling Input**
- **Configurable TMDS Output Signal Conditioning Setting for Port Selection, Pre-emphasis, Voltage Swing, Slew Rate Controls**
- **Support Squelch Mode with Built-in Clock detector**
- **Highly Configurable 8-step Receiver Equalization Setting from 2.5 dB to 20 dB**
- **Support Receiver Squelch mode with clock channel detector for low power mode**
- **HPD Signal Detection for active output ports detection and management**
- **Control Status Register controlled by Pin-strapping or I2C mode programming**
- **ESD protection on I/O pins to connector: 8KV contact and 2KV HBM**
- **3.3V Single Power Supply**
- **Packaging (Pb-free & Green): 80-contact LQFP (FCE80)**

General Description

Pericom Semiconductor's PI3HDX414, active-drive switch solution is targeted for high-resolution video networks that are based on HDMI/DVI standards, and TMDS signal processing.

The PI3HDX414 is an active single TMDS channel to four TMDS channel Splitter and DeMux with Hi-Z outputs. The device drives differential signals to four video display units. It provides controllable output swing levels that can be controlled through pin control or I2C control, depending on the mode select pin. This solution also provides a unique advanced pre-emphasis technique to increase rise and fall times.

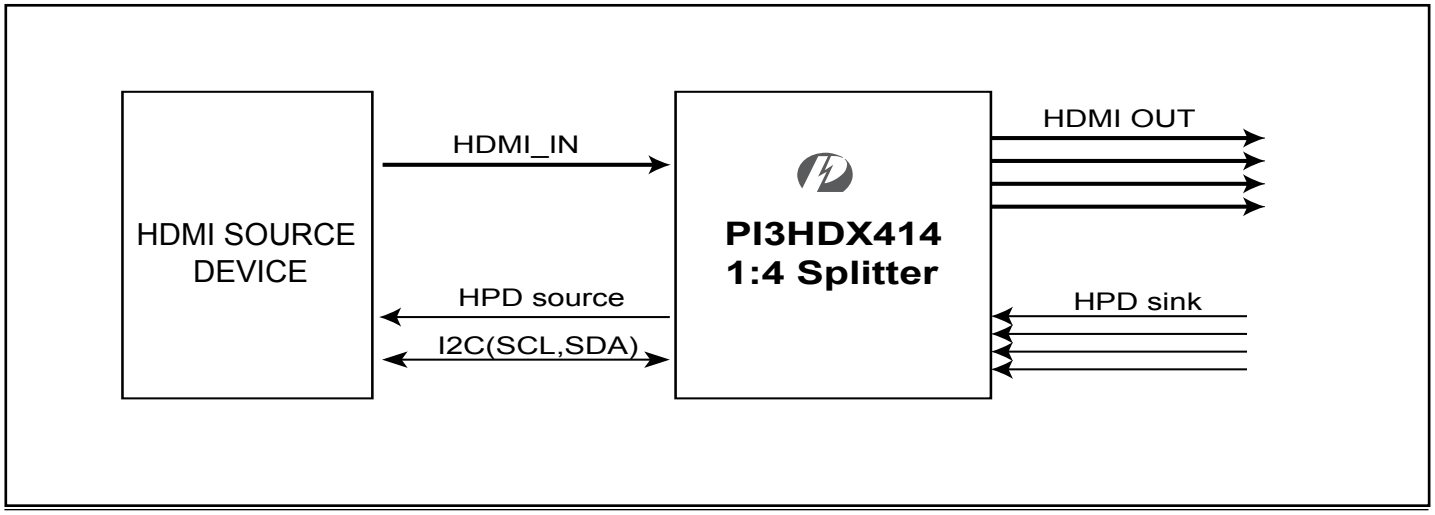
The maximum HDMI/DVI data rate of 3.4Gbps provides a 1920x1080 @60Hz resolution or 4K @30Hz required for 4K HDTV and PC graphics products. For PC graphics application, the device sits at the driver's side to switch between multiple display units, such as PC LCD monitor, projector, TV, etc.

PI3HDX414 ensures transmitting high bandwidth video streams from PC graphics source to end display units. It will also provide enhanced robust ESD/EOS protection, which is required by many consumer video networks today.

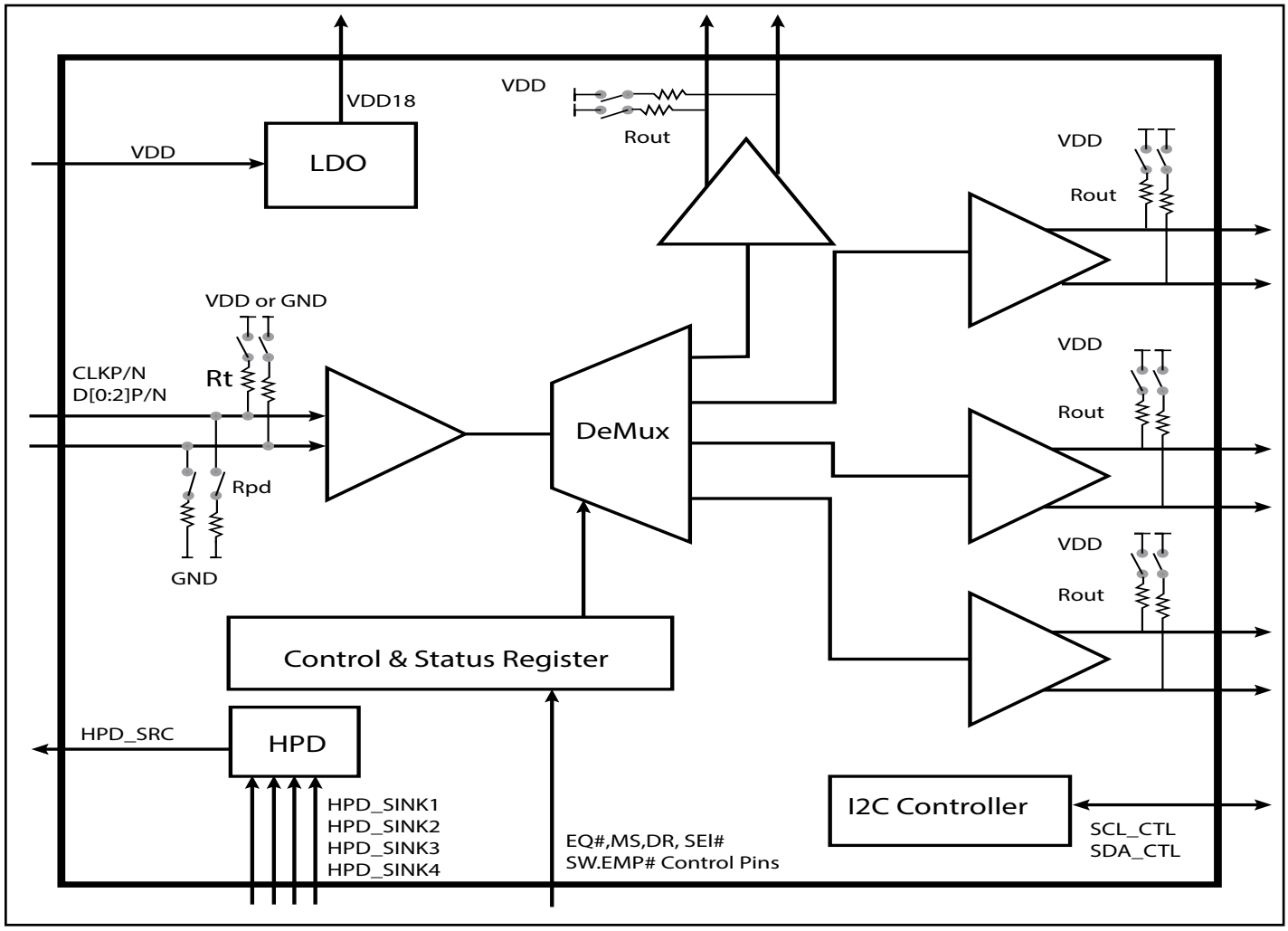
Application

- HDMI Peripherals
- Wall Multi Screen Display
- Notebook PC and Docking
- TV, Monitor and Set-Top-Box

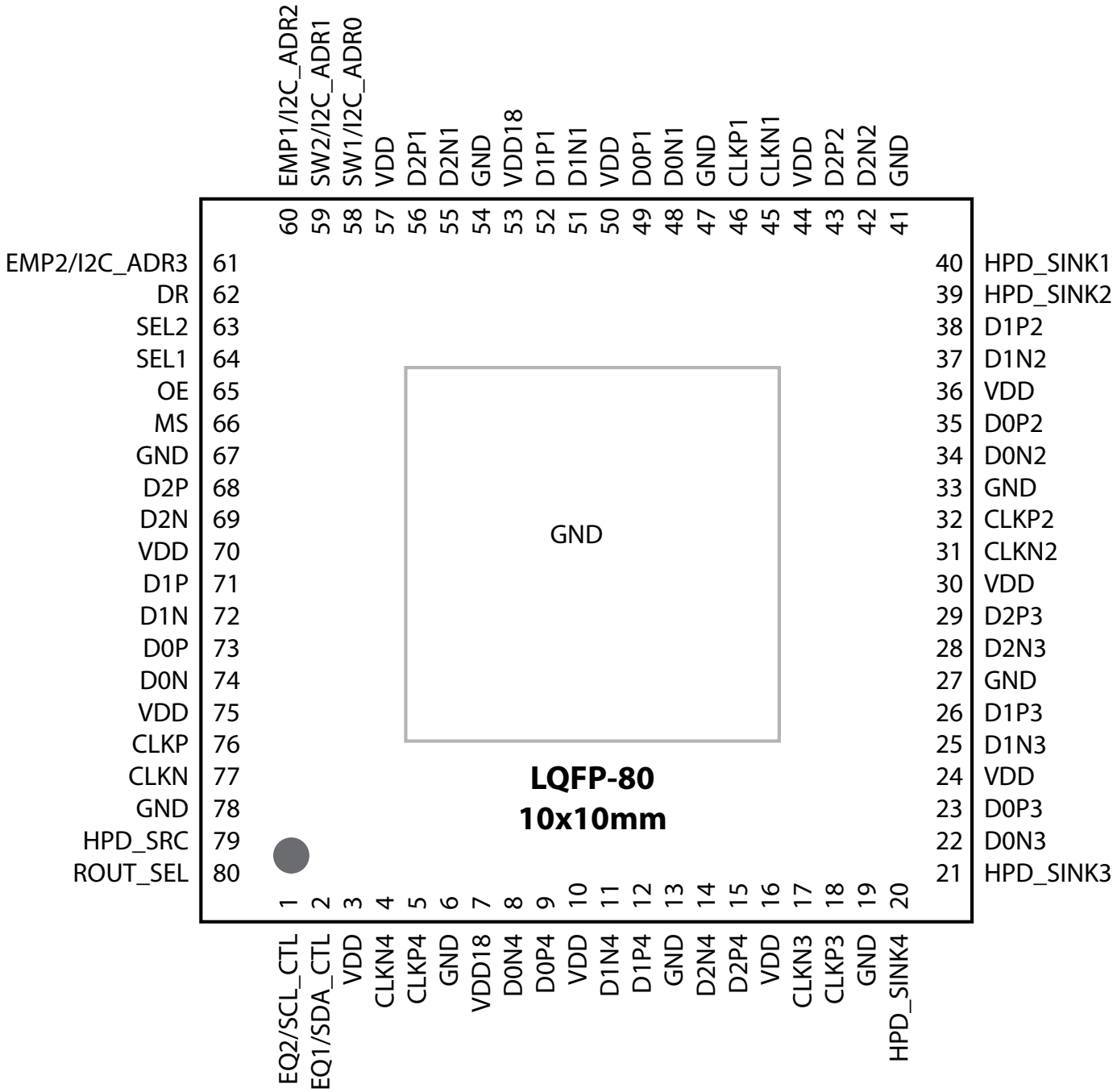
Typical Application



Block Diagram



Pin Configuration (Top-Side View)



Pin Description

Pin #	Pin Name	Type	Description
Data Signals			
77 76 74 73 72 71 69 68	CLKN CLKP D0N D0P D1N D1P D2N D2P	I	TMDS Clock and Data input pins. Rt = 50 Ohm; Rpd = 200 kOhm.
45 46 48 49 51 52 55 56	CLKN1 CLKP1 D0N1 D0P1 D1N1 D1P1 D2N1 D2P1	O	TMDS Outputs Port 1. ROUT_SEL pin enables Output Termination Resistor (Rout=50 Ohm).
31 32 34 35 37 38 42 43	CLKN2 CLKP2 D0N2 D0P2 D1N2 D1P2 D2N2 D2P2	O	TMDS Outputs Port 2. ROUT_SEL pin enables Output Termination Resistor (Rout=50 Ohm).
17 18 22 23 25 26 28 29	CLKN3 CLKP3 D0N3 D0P3 D1N3 D1P3 D2N3 D2P3	O	TMDS Outputs Port 3. ROUT_SEL pin enables Output Termination Resistor (Rout=50 Ohm).
4 5 8 9 11 12 14 15	CLKN4 CLKP4 D0N4 D0P4 D1N4 D1P4 D2N4 D2P4	O	TMDS Outputs Port 4. ROUT_SEL pin enables Output Termination Resistor (Rout=50 Ohm).

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Control Signals</td></tr>
<tr><td>1</td><td>EQ2/SCL_CTL</td><td>IO</td><td>Shared Pin decided by MS (Mode Selection) Pin status

Pin MS = "High" : assign as SCL_CTL pin. SCL_CTL: I^{2}C Clock, compatible with I^{2}C-Bus specification up to 400kb/s.
Pin MS = "Low" : assign as EQ2 pin

Internal Pull-up at 100 Kohm and Pull-Down at 100 Kohm. Pin Control EQ mode setting is below. "M" is Tri-state.

<table>
<tr><th>EQ2</th><th>EQ1</th><th>Equalization Setting (dB)</th></tr>
<tr><td>0</td><td>M</td><td>2.5</td></tr>
<tr><td>0</td><td>0</td><td>5</td></tr>
<tr><td>M</td><td>0</td><td>7.5</td></tr>
<tr><td>0</td><td>1</td><td>10</td></tr>
<tr><td>M</td><td>M</td><td>12.5</td></tr>
<tr><td>1</td><td>0</td><td>15</td></tr>
<tr><td>1</td><td>M</td><td>17.5</td></tr>
<tr><td>1</td><td>1</td><td>20</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>EQ1/SDA_CTL</td><td>IO</td><td>Shared Pin decided by MS (Mode Selection) Pin status. Internal Pull-Up at 100 Kohm and Pull-Down at 100 Kohm. Please refer to Pin# 1 Control EQ mode setting table.</td></tr>
<tr><td>58
59
60
61</td><td>SW1/I2C_ADR0
SW2/I2C_ADR1
EMP1/I2C_ADR2
EMP2/I2C_ADR3</td><td>I</td><td>Shared Pin.
Pin MS = "High" : assign as I^{2}C Address pins, I2C_ADR[3:0].
Pin MS = "Low" : assign as Pin control mode, SW[2:1] and EMP[2:1].

SW2 and SW1 pin configuration for voltage swing control. Internal Pull-Up at 100 Kohm.

<table>
<tr><th>SW2</th><th>SW1</th><th>Voltage Swing</th></tr>
<tr><td>0</td><td>0</td><td>500 mV</td></tr>
<tr><td>0</td><td>1</td><td>500mV -10 %</td></tr>
<tr><td>1</td><td>0</td><td>500mV +10 %</td></tr>
<tr><td>1</td><td>1</td><td>500mV +20 %</td></tr>
</table>

EMP2 and EMP1 pin configuration for pre-emphasis control. These pins are internally Pull-Up at 100 Kohm.

<table>
<tr><th>EMP2</th><th>EMP1</th><th>Pre-emphasis Setting (dB)</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1.5</td></tr>
<tr><td>1</td><td>0</td><td>2.5</td></tr>
<tr><td>1</td><td>1</td><td>3.5</td></tr>
</table>
</td></tr>
</table>

Pin #	Pin Name	Type	Description
66	MS	I	Mode Selection pin. Internal Pull-Up with 100 Kohm. "High" : I2C Control Mode "Low" : Pin Control Mode
80	Rout_SEL	I	Source Termination Rout Selection pin. Internal pull-up at 100 Kohm. "High" : Rout Source Termination Output "Low" : Open Drain Output
65	OE	I	Output Enable Control pin. Active high. Internal pull-up at 100 Kohm. "High" : Output Enable "Low" : Disable TMDS Receiver and Driver block. Rout and Rt is "OFF"
62	DR	I	Direction Control pin. "High" : all ports are Enable at same time. "Low" : Output ports are controlled by SEL[2:1] pins
64 63	SEL1 SEL2	I	Port Selection pins. Internal pull-up at 100 Kohm. SEL2 / SEL1 / Description 0 / 0 / Port 1 is Active 0 / 1 / Port 2 is Active 1 / 0 / Port 3 is Active 1 / 1 / Port 4 is Active
40 39 21 20	HPD_SINK1 HPD_SINK2 HPD_SINK3 HPD_SINK4	I	Sink-side Hot Plug Detect pins
79	HPD_SRC	O	Source-side Hot Plug Detect Pin
Power Pins			
3,10,16,24,30 36,44,50,57,70 75	VDD	PWR	3.3V Power Supply
7, 53	VDD18	PWR	LDO Output for internal core power supplier. Add external 4.7 uF Capacitor to GND
6,13,19,27,33, 41,47,54,67,78	GND	GND	Ground pins

Description of Operation

Squelch Mode:

Output Disable (Squelch) Mode uses TMDS Clock channel signal detection. When low voltage levels on the TMDS input clock signals are detected, Squelch state enables and TMDS output port signals shall disable; when the TMDS clock input signal levels are above a pre-determined threshold voltage, output ports shall return to the normal voltage swing levels.

When enable Squelch mode, input termination resistor will be enabled together. When Squelch is disabled through I2C register programming RX_SET[1]="1" and no TMDS input signal condition, TMDS D[0:2]P/N will be undetermined status. In Squelch state, TMDS output is high impedance state or TMDS output port shall 50 Ohm pull-up at source termination output.

Source Connection Detector Mode:

Default mode is "Enable Connector Detector". When I2C Register Offset 0x00 CONFIG[2] register set "0", the default mode can disable. When HDMI ports have no connector inserted in, HPD_SINKx (x:1,2,3,4) is "Low" status, and disable the unconnected port. When all of HDMI ports do not have connectors inserted, TMDS input 50 Ohm resister shall turn off. In stand-by mode, source-side TMDS connection detector mode is under operation waiting to normal mode recovery.

Function Control Table

OE	MS	DR	SEL2	SEL1	HDMI Outputs	HPD_SRC Function (with external 1 Kohm Pull-up resistor)
0	x	x	x	x	All Port Disable	0
Pin Cotrol Mode						
1	0	1	x	x	All Ports Active	(HPD1+HPD2+HPD3+HPD4)
1	0	0	0	0	Enable Port 1	HPD1
1	0	0	0	1	Enable Port 2	HPD2
1	0	0	1	0	Enable Port 3	HPD3
1	0	0	1	1	Enable Port 4	HPD4
I2C Control Mode						
1	1	x	x	x	I2C Programming Mode	(HPD1 * Port1 EN + HPD2 * Port2 EN + HPD3 * Port3 EN + HPD4 * Port4 EN)

HPD Control Mode

TMDS Selection (Input)	HPDx(Input)	Description	Notes
Port[x] Select	1	Port[x] is enabled	1) x=1, 2, 3, 4. x is consistent for one port. 2) HPD control function can be disable by 0x00[2] in I2C control mode.
Port[x] Select	0	Port[x] is Disabled	

I²C Register Control

I²C Register Control

Pin Name	I/O	Description
SCL_CTL	I	I²C Clock, compatible with I2C-bus specification, up to 400 kb/s
SDA_CTL	IO	I²C Data, compatible with I2C-bus specification, up to 400 kb/s
I2C_ADR[3:0]	I	I²C control address setting
Byte output : 0x00 - 0x07	O	I²C control registers output

I²C Address Byte

	b[7] MSB	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (R/W)
Address Byte	1	0	1	A3	A2	A1	A0	1/0*

* Read "1", Write "0"

I²C Control Register

Offset	Name	Description	Power Up Condition	Type
0x00	CONFIG[7:0]	[7] Enable TMDS Standby mode "0": Standby mode "1": Normal mode In standby mode, TMDS Equalizer and Output Driver shall power down. [6] Output Port 1 is selected "0" : Disable "1" : Active [5] Output Port 2 is selected "0" : Disable "1" : Active [4] Output Port 3 is selected "0" : Disable "1" : Active [3] Output Port 4 is selected "0" : Disable "1" : Active [2] Source Connection Detector control "0" : Disable source connection detector "1" : Enable connection detector (as default) When this port has no connector asserted as HPD_SINKx = "Low", the port will be no active status. When all four ports do not inserted any connectors, TMDS input 50 Ohm shall turn off [1:0] Reserved	0xFF	R/W

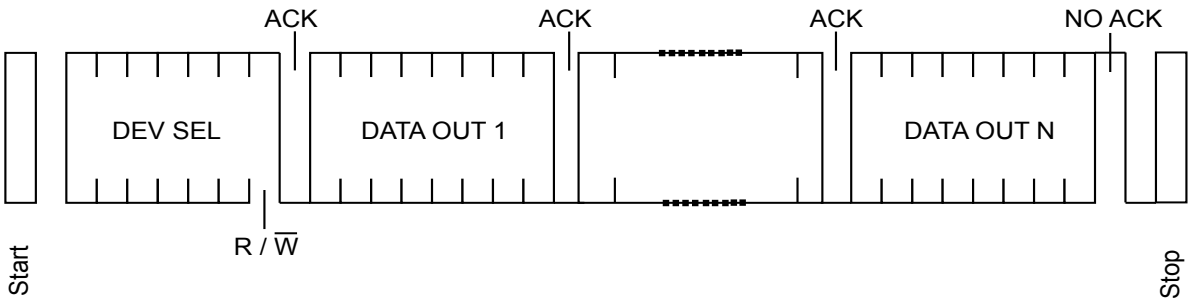
<table>
<tr><th>Offset</th><th>Name</th><th>Description</th><th>Power Up Condition</th><th>Type</th></tr>
<tr><td>0x01</td><td>RX_SET[7:0]</td><td>Receiver Port Equalization setting
[7] Disable port termination resistors
"0" = Rpd connected (default)
"1" = Rpd disconnected
[6] TMDS input termination V-bias selection
"0" : Connect to GND (default)
"1" : Connect to VDD
[5] V-bias register selection enable
"0" : b[6] control disable (as default, pin control only)
"1" : b[6] control enable
[4:2] EQ programmable setting
<table><tr><th>b[4:2]</th><th>EQ Setting (dB)</th></tr><tr><td>000</td><td>2.5</td></tr><tr><td>001</td><td>5</td></tr><tr><td>010</td><td>7.5</td></tr><tr><td>011</td><td>10</td></tr><tr><td>100</td><td>12.5</td></tr><tr><td>101</td><td>15</td></tr><tr><td>110</td><td>17.5</td></tr><tr><td>111</td><td>20</td></tr></table>[1] Squelch disable
"0" : Squelch enable (as default)
"1" : Squelch disable
[0] Reserved</td><td>0x00</td><td>R/W</td></tr>
<tr><td>0x02</td><td>TX_SET[7:0] for Port 1</td><td>TMDS Output Port 1 setting
[7] TMDS output control
"0" : Open drain mode
"1" : Double termination mode
[6:4] TMDS output Pre-emphasis control
"000" : 0 dB
"001" : 1.5 dB
"010" : 2.5 dB
"011" : 3.5 dB
"1xx" : 6 dB (750 mVpp swing)
[3:2] Reserved by test adjust
TMDS output swing setting
"00" : 500 mV as default setting
"01" : -10%
"10" : +10%
"11" : +20%
[1:0] Reserved by test adjust
TMDS output slew rate setting
"00" : Default setting
"01"/"10" : + 5%
"11" : +10%</td><td>0x00</td><td>R/W</td></tr>
</table>

Offset	Name	Description	Power Up Condition	Type
0x03	TX_SET[7:0] for Port 2	TMDS Output Port 2 Setting [7] TMDS output control "0" : Open drain mode "1" : Double termination mode [6:4] TMDS Output Pre-emphasis control "000" : 0 dB "001" : 1.5 dB "010" : 2.5 dB "011" : 3.5 dB "1xx" : 6 dB (750 mVpp swing) [3:2] Reserved by test only. TMDS Output Swing setting "00" : 500mV as default "01" : -10% "10" : +10% "11" : +20% [1:0] Reserved by testing adjust. TMDS output slew rate setting "00" : Default Setting "01"/"10" : + 5% "11" : +10%	0x00	R/W
0x04	TX_SET[7:0] for Port 3	TMDS Output Port 3 Setting [7] TMDS Output control "0" : Open drain mode "1" : Double termination mode [6:4] TMDS Output Pre-emphasis control "000" : 0 dB "001" : 1.5 dB "010" : 2.5 dB "011": 3.5 dB "1xx" : 6 dB (750 mVpp swing) [3:2] Reserved by test only. TMDS output swing setting "00" : 500mV as default "01" : -10% "10" : +10% "11" : +20% [1:0] Reserved by test adjust. TMDS output slew rate setting "00" : Default Setting "01" : +5% "10" : + 5% "11" : +10%	0x00	R/W

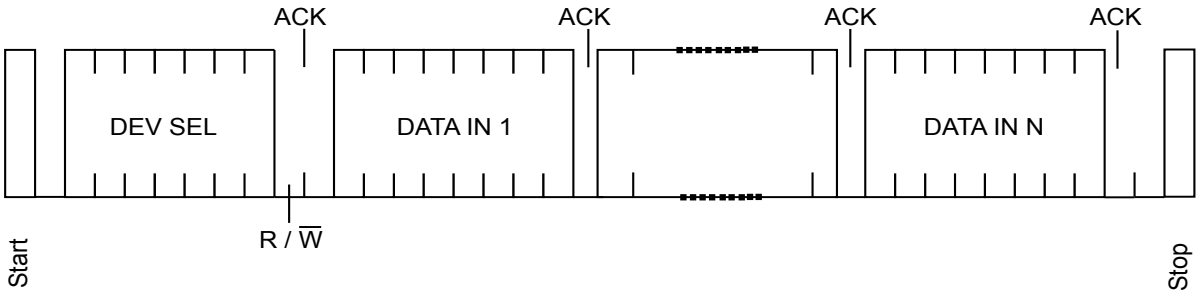
Offset	Name	Description	Power Up Condition	Type
0x05	TX_SET[7:0] for port4	TMDS Output Setting [7] TMDS output control "0" : Open drain "1" : Double termination [6:4] TMDS output Pre-emphasis control "000" : 0 dB "001" : 1.5 dB "010" : 2.5 dB "011" : 3.5 dB "1xx" : 6 dB (750 mVpp swing) [3:2] Reserved by test only. TMDS output swing setting "00" : 500 mV as default "01" : -10% "10" : +10% "11" : +20% [1:0] Reserved by test adjust. TMDS output slew rate setting "00" : Default Setting "01"/"10" : + 5% "11" : +10%	0x00	R/W
0x06	HPD_SINKx[7:0]	[7] HPD_SRC output logic function (with external 1 kOhm pull-up resistor) "1" : HPD_SRC = /HPD_SINKx "0" : HPD_SRC = HPD_SINKx [6:4] Reserved b[3] : HPD_SINK4 status as read only b[2] : HPD_SINK3 status as read only b[1] : HPD_SINK2 status as read only b[0] : HPD_SINK1 status as read only	0x00	R/W
0x07	Reserved	[7:0] Reserved	0x00	R/W

I²C Data Transfer

1. Read Sequence



2. Write Sequence



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential 4.5V

DC SIG Voltage . . . . . –0.5V to V_{DD}+0.5V

Storage Temperature . . . . . –65°C to +150°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Operation Voltage		3.0	3.3	3.6	V
I_{DD}	V_{DD} Supply Current	Output Enable (open drain, 0 dB pre-Emphasis), Port 1 Enable, HPD_SNK1 = High		160	180	mA
		Output Enable (open drain, 0 dB pre-Emphasis), All Ports Enable, HPD_SNKx = High		275	300	mA
		Output Enable (Source Termination, 0 dB pre-Emphasis), Port 1Enable, HPD_SNK1 = High		261	290	mA
		Output Enable (Source Termination, 0 dB pre-Emphasis), All Ports Enable, HPD_SNKx = High		393	430	mA
I_{DDQ}	V_{DD} Quiescent Current	OE = 1, Open Drain, No CLK input signal, All Ports Enable		99	108	mA
		OE = 1, Open Drain, No CLK input signal, Port 1 Enable		60	66	mA
		OE = 1, Source Termination, No CLK input signal, All Ports Enable		99	108	mA
		OE = 1, Source Termination, No CLK input signal, Port 1 Enable		60	66	mA
I_{STB}	Standby mode	OE = 0, All Ports Enable		0.77	0.84	mA
		OE=0, Port 1 Enable		0.71	0.78	mA
T_A	Operating Temperature	Source termination mode, 0dB pre-Emp, all ports enable	-40		70 Note 1	°C
		Open Drain Mode, 0dB pre-Emp, all port enable	-40		85	

Note 1: Please contact Pericom for application uses above 70 °C

Package Dissipation Rating

Symbol	80-pin LQFP Package	Condition Note1	Min	Typ	Max	Units
θ_{JA}	Junction to Ambient Thermal Resistance	Still air, 4-layer PCB			13.2	°C/W
θ_{JC}	Junction to Case Thermal Resistance				9.5	°C/W

Note 1: Thermal pad layout information is as following. a) Thermal pad: 6x6mm on top and 10x10mm on bottom, b) 36 thermal vias on 6x6mm thermal pad: Via diameter 0.3mm and pitch 1.0mm, c) Cu trace thickness on top and bottom: 2oz, d) Cu plane thickness: 1oz

DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
TMDS Differential Pins						
V_{OH}	Single-ended high level output voltage	V_{DD} = 3.3 V, Rout=50 Ω	V_{DD}-10		V_{DD}+10	mV
V_{OL}	Single-ended low level output voltage		V_{DD}-600		V_{DD}–400	mV
Vswing	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage				180	mV
$V_{OD(U)}$	Undershoot of output differential voltage				200	mV
$V_{OC(SS)}$	Change in steady-state common- mode output voltage between logic states				5	mV
I_{OS}	Short Circuit output current		-12		12	mA
I_{OS}	Short Circuit output current at double termination mode		-24		24	mA
VI(open)	Single-ended input voltage under high impedance input or open input	I_L = 10 uA	V_{DD}-10		V_{DD}+10	mV
R_T	Input termination resistance	V_{IN} = 2.9 V	45	50	55	Ohm
I_{OZ}	Leakage current with Hi-Z I/O	V_{DD} = 3.6 V, OE = 0		30	100	µA
HPD_SINK						
I_{IH}	High level digital input current	V_{IH} = V_{DD}	-10		50	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage	V_{DD} = 3.3 V	2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
HPD_SRC						
V_{OL}	Low level digital output voltage	V_{DD} = 3.3 V, I_{OL}=4mA			0.4	V

Control pins (OE, SEL,EMP,SW,MS)						
I_{IH}	High level digital input current	$V_{IH} = V_{DD}$	-10		10	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-50		10	µA
V_{IH}	High level digital input voltage		2.4			V
V_{IL}	Low level digital input voltage		0		0.8	V

AC Specifications

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
TMDS Differential Pins						
t_{pd}	Propagation delay				2000	ps
t_r	Differential output signal rise time (20% - 80%), 0 dB / Open drain	V_{DD} = 3.3 V, R_{OUT} = 50 Ohm		140		ps
t_f	Differential output signal fall time (20% - 80%), 0 dB / Open drain			140		ps
$t_{sk(p)}$	Pulse Skew			15	50	ps
$t_{sk(D)}$	Intra-pair Differential Skew			25	50	ps
$t_{sk(O)}$	Inter-pair Differential Skew				100	ps
t_{sx}	Select to switch output				550	ns
t_{en}	Enable Time			1	10	us
t_{dis}	Disable Time				50	ns
$t_{jit\_clk(pp)}$	Peak-to-peak output jitter CLK residual jitter	Data: 3.4 Gb data pattern Clock: 340 MHz		10		ps
$t_{jit\_data(pp)}$	Peak-to-peak output jitter Date residual jitter			28		ps
DDC I/O Pins (HPD_SINK)						
$t_{pd(HPD)(tphl)}$	Propagation Delay (from active port HPD_SINK to HPD_SRC)	C_L = 10 pF		2	6.0	ns
$t_{pd(HPD)(tphl)}$	Switching Time (from port select to the latest)			3	6.5	ns

Note

1. Overshoot of output differential voltage $V_{OD(O)} = (V_{SWING(MAX)} * 2) * 15\%$
2. Undershoot of output differential voltage $V_{OD(O)} = (V_{SWING(MIN)} * 2) * 25\%$

Output Eye Opening

Input Equalization Control Settings versus Input Trace Lengths, Vdd= 3.3V, 25C

Test Setup Conditions:

Data Rate : 3.4Gbps, Pattern : PRBS2^7-1, Swing : 500mV, No Pre-emphasis, 300Mhz on CLK Channel for Squelch Feature

Additional Setup Information:

EV Board Input and Output Traces : 2.5" Roger material, Input Trace Connection : 24" Coax + FR4 Trace Card, Output Trace Connection : 12" Coax Cable (Bias voltage of 3.05V pull up),

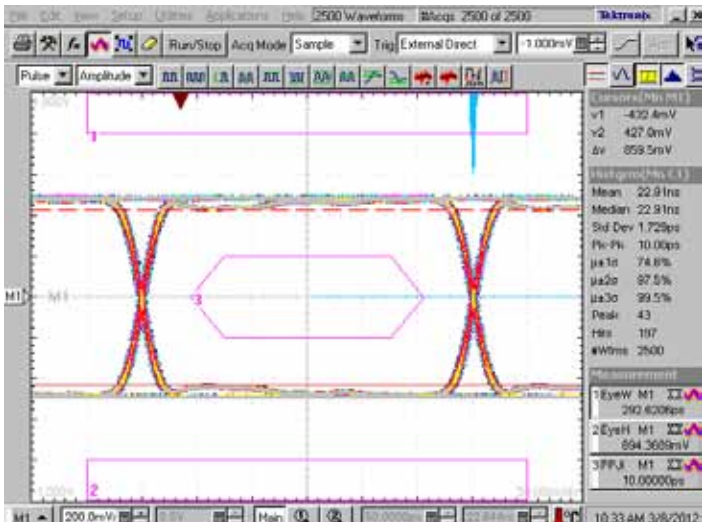
Input Level : 1V differential peak-peak (500mV at the test equipment, i.e. TMDS swing of clock and data channel)

	No Input Trace				48-inch Input Trace			
	Open Drain		Double Termination		Open Drain		Double Termination	
	Eye width (UI)	Eye height (mV)	Eye width (UI)	Eye Weight (mV)	Eye width (UI)	Eye height (mV)	Eye width (UI)	Eye Weight (mV)
2.5dB	0.894	886	0.914	919	0.631	697	0.673	811
5.0dB	0.868	892	0.888	919	0.779	832	0.815	897
7.5 dB	0.848	903	0.868	919	0.852	870	0.871	914
10.0 dB	0.825	903	0.852	919	0.845	892	0.858	914
12.5 dB	0.819	903	0.829	919	0.809	892	0.819	914
15.0 dB	0.792	903	0.805	919	0.769	892	0.776	914
17.5 dB	0.759	903	0.779	919	0.730	892	0.746	908
20.0 dB	0.697	849	0.723	919	0.697	849	0.697	908

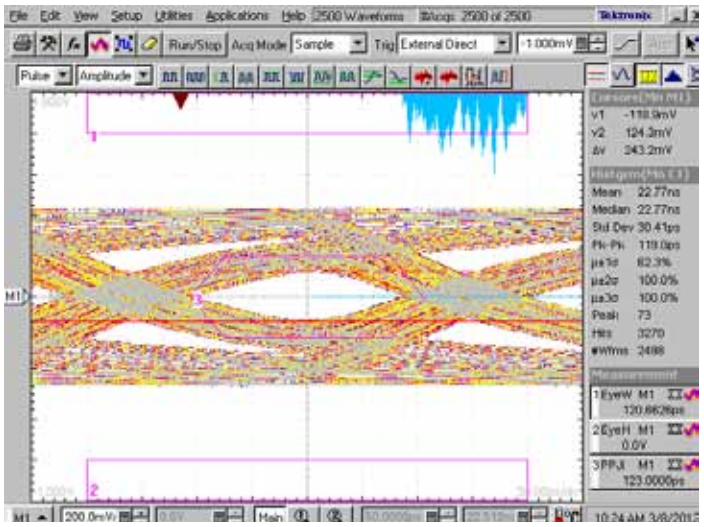
Note:

1. Equipment: HP Power Supply, Agilent JBERT, DSA8200 and PI3HDMIX414 EV Board. Input eye diagram (with 0" input trace) is hooked up 36 inch SMA coaxial cable alone

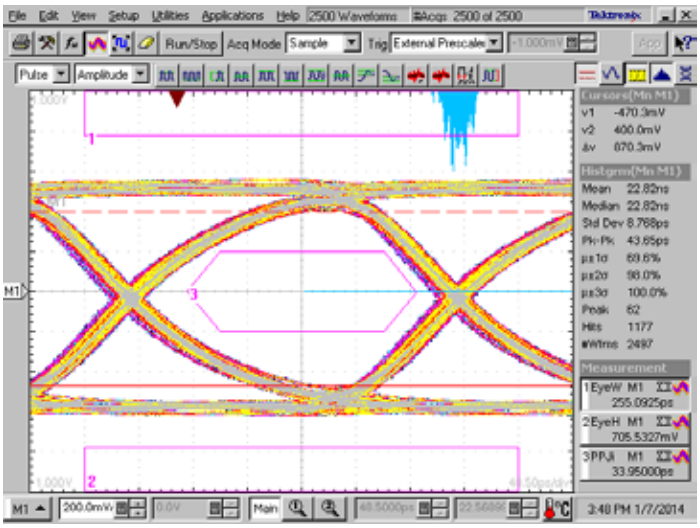
2. 48-inch Trace Card loss information is about -10.21dB at 3.4Gbps, 1.7Ghz condition



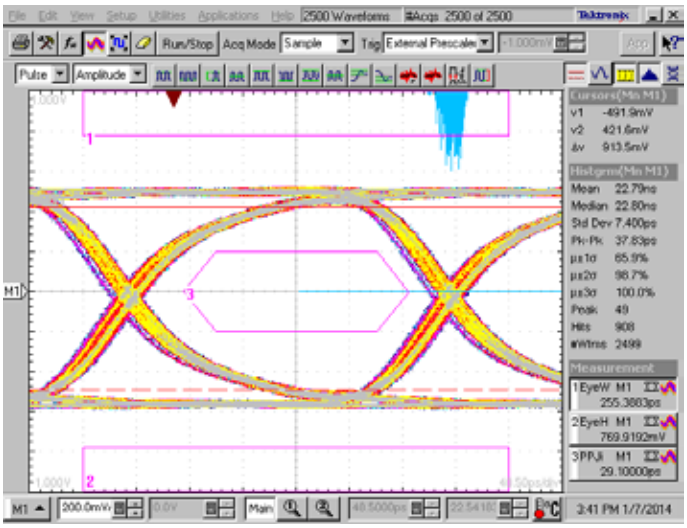
0" Input Trace: No DUT
PI3HDMIX414 Input Eye Opening, 3.4Gbps. PRBS^7-1 Pattern.
Input Trace: 24" Coax + FR4 Trace Card
Output Trace : 24" Coax, Input Swing = 1000mVd



48" Input Trace: No DUT
PI3HDMIX414 Input Eye Opening, 3.4Gbps. PRBS^7-1 Pattern.
Input Trace: 24" Coax + FR4 Trace Card
Output Trace : 24" Coax, Input Swing = 1000mVd



48" Input Trace: Open Drain
PI3HDMIX414 Eye Opening with EQ = 7.5dB Settings, 3.4Gbps, Vdd=3.3V, 25C. Eye Diagram Setup: DEM=0dB, D1x Channel, PRBS2^7, Input Swing=1000mVd

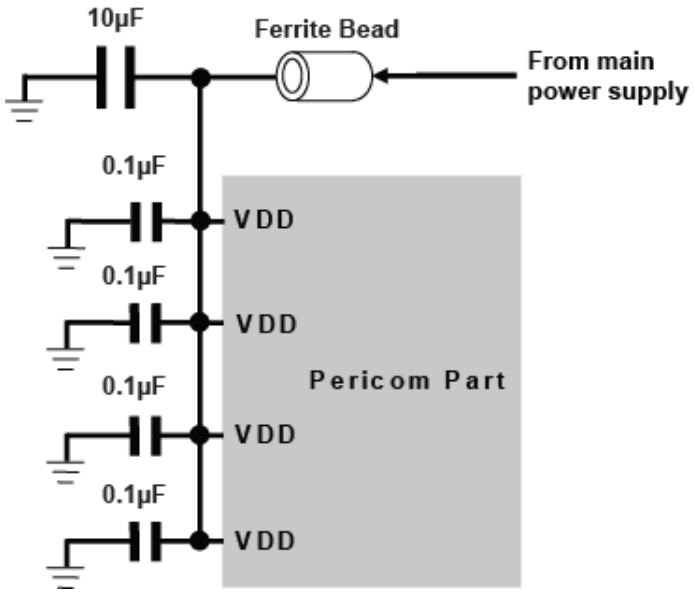


48" Input Trace: Double Termination
PI3HDMIX414 Eye Opening with EQ = 7.5dB Settings, 3.4Gbps, Vdd=3.3V, 25C. Eye Diagram Setup: DEM=0dB, D1x Channel, PRBS2^7, Input Swing=1000mVd

Recommended System Design for Power Supply

Power Supply Decoupling Circuit

It is recommended to put 0.1 µF decoupling capacitors on each VDD pins of our part, there are four 0.1 µF decoupling capacitors are put in Figure 1 with an assumption of only four VDD pins on our part, if there is more or less VDD pins on our Pericom parts, the number of 0.1 µF decoupling capacitors should be adjusted according to the actual number of VDD pins. On top of 0.1 µF decoupling capacitors on each VDD pins, it is recommended to put a 10 µF decoupling capacitor near our part's VDD, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.



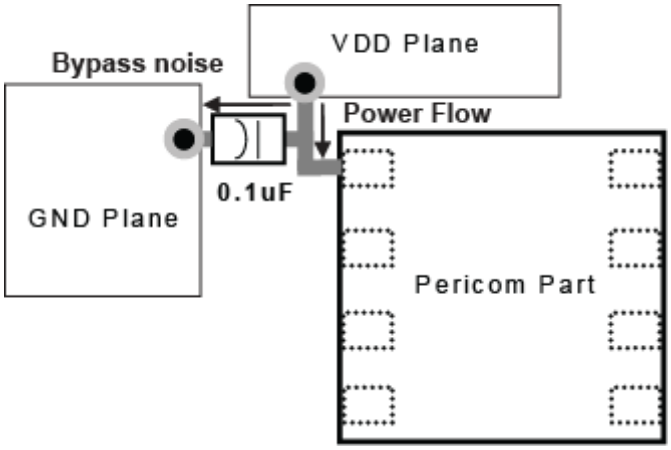
Recommended Power Supply Decoupling Capacitor Diagram

Requirements on the De-coupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

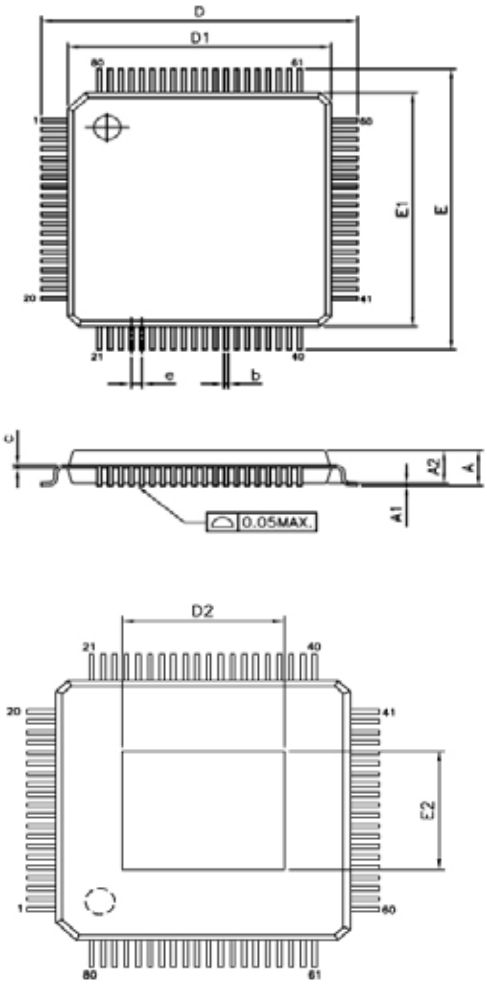
Layout and Decoupling Capacitor Placement Consideration

- ➔ Each 0.1 µF decoupling capacitor should be placed as close as possible to each VDD pin.
- ➔ VDD and GND planes should be used to provide a low impedance path for power and ground.
- ➔ Via holes should be placed to connect to VDD and GND planes directly.
- ➔ Trace should be as wide as possible
- ➔ Trace should be as short as possible.
- ➔ The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- ➔ 10 µF Capacitor should also be placed closed to our part and should be placed in the middle location of 0.1 µF capacitors.
- ➔ Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.



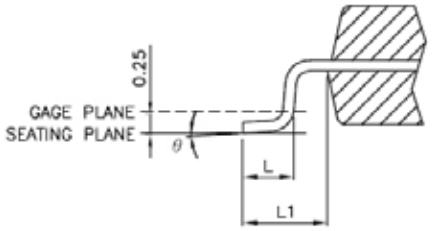
Decoupling Capacitor Placement Diagram

Package Mechanical: 80-pin LQFP (FCE80)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
D2	4.71	--	5.54
E2	3.88	--	4.57
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



Notes:
1 All dimensions are in millimeters, angles in degrees
2 Ref JEDEC: MS-026/BCE
3 Package outline exclusive of mold flash and metal burr

Note:
• For latest package info, please check: http://www.pericom.com/support/packaging

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDX414FCEEX	FCE80(EPAD)	Low Profile Flat Package

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- FCE = Package Code
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel

Related Products

Part Number	Product Description
PI3HDX412BD	HDMI 1.4b Splitter 1:4 with Signal Conditioning for 3.4 Gbps Application
PI3HDX511A/611	HDMI 1.4b Redriver and DP++ Level Shifter for 3.4 Gbps Application (top/bottom PCB mount)
PI3WVR12412	Wide Voltage Range DP & HDMI Video Switch for 6 Gbps application
PI3HDX1204-B	HDMI 2.0 ReDriver for 6 Gbps Application
PI3EQXDP1201	DisplayPort 1.2 ReDriver with built-in AUX listener
PI3HDMI521/621	HDMI 1.4b 2-to-1 Switch with Signal Conditioning for 3.4 Gbps Application (top/bottom PCB mount)
PI3VDP3212	2-Lane DisplayPort 1.2 Compliant Switch
PI3VDP12412	4-Lane DisplayPort 1.2 Compliant Switch
PI3HDMI336	HDMI 3-to-1 Switch with Signal Conditioning for 2.5 Gbps Application

PRODUCT STATUS DEFINITIONS

Datasheet Identification	Product Status	Definition
Advanced Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Pericom Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Pericom Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Pericom Semiconductor. The datasheet is for reference information only.

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