Dual Bidirectional I3C/I²C-bus Voltage-level Translator

Description

The DIODES PI3CLS9606 is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation for traditional I2C-bus/SMBus applications, and 12.5 MHz I3C-bus applications. It features two 1-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins (V_{CCA} and V_{CCB}). V_{CCA} can be supplied at any voltage between 0.72V and 1.98V and V_{CCB} can be supplied at any voltage between 0.72V and 1.98V. V_{CCA} must be ≤ V_{CCB} to ensure proper operation.

PI3CLS9606 can be used for both open drain as well as push-pull application which allows for level translation applications using I3C and I2C protocols.

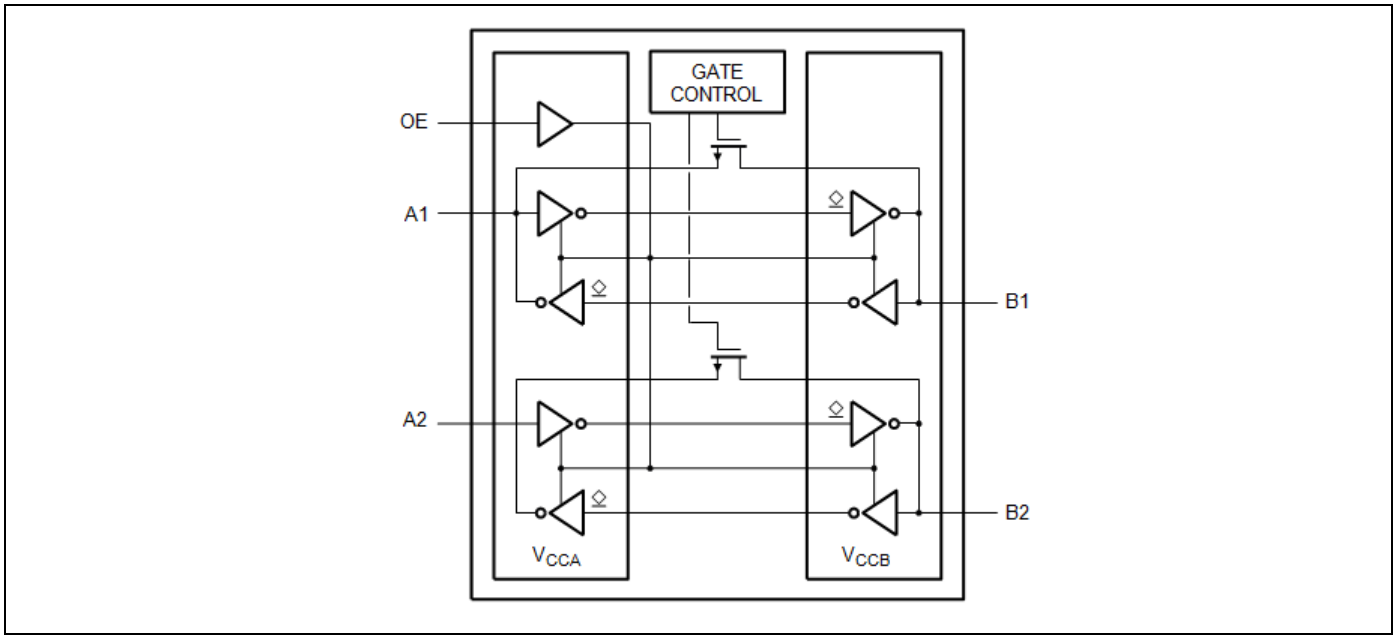
Port A is referenced to V_{CCA} and port B is referenced to V_{CCB}. The active HIGH OE pin is referenced to V_{CCA} and controllable by a signal in either VCCA or VCCB domain. A LOW level at pin OE causes the outputs to be in a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is in powered down.

Features

- I3C/I²C-bus and SMBus bi-directional level translator
- Port A operating supply voltage V_{CCA} range of 0.72V to 1.98V; Port B operating supply voltage V_{CCB} range of 0.72V to 1.98V. $V_{CCA} \leq V_{CCB}$
- Active HIGH repeater enable input
- Lock-up free operation
- Powered-off high-impedance I²C-bus pins
- ESD protection exceeds 8KV HBM per JESD22-A114
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions
- Packaging (Pb-free & Green available):
  - 8-Lead, 1.4mm x 1.0mm (HK)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

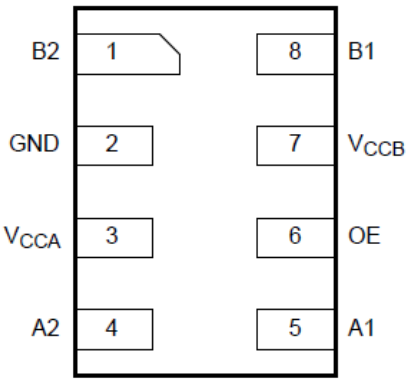
Block Diagram



Function Table

OE	Function
H	An = Bn
L	Disconnect

Pin Configuration



DFN1410-8L (Top View)

Pin Description

Pin#	Name	Description
1	B2	Data input or output (referenced to V_{CCB})
2	GND	Supply ground (0V)
3	V_{CCA}	Port A supply voltage (0.72V to 1.98V)
4	A2	Data input or output (referenced to V_{CCA})
5	A1	Data input or output (referenced to V_{CCA})
6	OE	Output enable input (active HIGH, referenced to V_{CCA})
7	V_{CCB}	Port B supply voltage (0.72V to 1.98V)
8	B1	Data input or output (referenced to V_{CCB})

Maximum Ratings

Storage Temperature	-55°C to +125°C
Supply Voltage port A	-0.5V to +2.5V
Supply Voltage port B	-0.5V to+2.5V
DC Input Voltage	-0.5V to +2.5V
Control Input Voltage (OE)	-0.5V to+2.5V
Total Power Dissipation	125mW
Input/Output Current (Port A & B)	±50mA
Input Current (V_{CCA}, V_{CCB}, GND)	100mA
ESD: HBM Mode	8kV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCA}	Supply voltage A	$V_{CCA} \leq V_{CCB}$	0.72	1.98	V
V_{CCB}	Supply voltage B	$V_{CCA} \leq V_{CCB}$	0.72	1.98	V
V_I	Input voltage	A port, B port and OE	0	1.98	V
V_O	Output voltage	Power-down or 3-state mode; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V			
		A port	0	1.98	V
		B port	0	1.98	V
T_{amb}	Ambient temperature		-40	+125	°C
T_J	Junction temperature[2]		-40	+125	°C
$\Delta t/\Delta V$	Input transition rise and fall rate	V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V	-	<5.3	ns/V

Typical Static Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V); Tamb = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{OH}	HIGH-level output voltage	A port; V_{CCA} = 1.2V; I_O = -20µA		1.1		V
V_{OL}	LOW-level output voltage	A port; V_{CCA} = 1.2V; I_O = 20µA		0.09		V
I_I	Input leakage current	OE input; V_I = 0V or 1.98V; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 7.98V			±1	µA
I_{OZ}	OFF-state output current	A or B port; V_O = 0V to V_{CCO}(1); V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V			±1	µA
I_{OFF}	Power-off leakage current	A port; V_I or V_O = 0V to 1.98V; V_{CCA} = 0V; V_{CCB} = 0V to 1.98V			±1	µA
		B port; V_I or V_O = 0V to 1.98V; V_{CCB} = 0V; V_{CCA} = 0V to 1.98V			±1	
I_{CC}	Supply current	V_I = 0V or V_{CCI}(2); I_O = 0V				
		$I_{CC(A)}$; V_{CCA} = 0.72V; V_{CCB} = 0.72V to 1.98V		0.05		µA
		$I_{CC(B)}$; V_{CCA} = 0.72V; V_{CCB} = 0.72V to 1.98V		3.3		µA
		$I_{CC(A)}$+ $I_{CC(B)}$; V_{CCA} = 0.72V; V_{CCB} = 0.72V to 1.98V		3.5		µA

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
C_I	Input capacitance	OE input; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		1.0		pF
$C_{I/O}$	Input/Output capacitance	A port; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		4.0		pF
		B port; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		4.0		pF

Note:
1. V_{CCO} is the supply voltage associated with the output.
2. V_{CCI} is the supply voltage associated with the input.

DC Electrical Characteristics

VCCA, VCCB = 0.72 V to 1.98 V; GND = 0V; Tamb = -40 °C to +125 °C; unless otherwise specified

Parameter	Description	Test Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min.	Max.	Min.	Max.	
A port or B port							
V_{IH}	HIGH-level input voltage	V_{CCA} = 0.72V to 0.9V; V_{CCB} = 0.72V to 0.9V	V_{CCI} – 0.2 [1]		V_{CCI} -0.2		V
		V_{CCA} = 0.9V to 1.98V; V_{CCB} = 0.9V to 1.98V	V_{CCI} -0.4		V_{CCI} -0.4		V
V_{IL}	LOW-level input voltage	V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		$0.3V_{CCA}$		$0.3V_{CCA}$	V
V_{OH}	HIGH-level output voltage	I_O = -20µA; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V	V_{CCO} - 0.4 [2]		V_{CCO} - 0.4		V
V_{OL}	LOW-level output voltage	I_O = 20µA; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		0.3		0.3	V
I_{LI}	Input leakage current	OE input, V_{CCA} = 0.72V to 1.98V, V_{CCB} = 0.72V to 1.98V.		±2		±5	µA
I_{OZ}	OFF-state output current	V_O = 0V or V_{CCO}; V_{CCA} = 0.72V to 1.98V V_{CCB} = 0.72V to 1.98V		±2		±10	µA
I_{OFF}	Power Off Leakage current	A port; V_I or V_O = 0V to 1.98V; V_{CCA} = 0V; V_{CCB} = 0V to 1.98V		±2		±10	µA
		B port; V_I or V_O = 0V to 1.98V; V_{CCB} = 0V; V_{CCA} = 0V to 1.98V		±2		±10	µA
I_{CCA}	Supply Current	V_I = 0V or V_{CCI}; I_O = 0A; OE = LOW; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		5		15	µA
		V_I = 0V or V_{CCI}; I_O = 0A; OE = HIGH V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		6		20	µA
		V_{CCA} = 1.98V; V_{CCB} = 0V		3.5		15	µA
		V_{CCA} = 0V; V_{CCB} = 1.98V		-2		-15	µA

Parameter	Description	Test Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min.	Max.	Min.	Max.	
I_{CCB}	Supply Current	V_I = 0V or V_{CCI}; I_O = 0A; OE = LOW; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		8		29	µA
		V_I = 0V or V_{CCI}; I_O = 0A; OE = HIGH V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		11		36	µA
		V_{CCA} = 1.98V; V_{CCB} = 0V		-2		-15	µA
		V_{CCA} = 0V; V_{CCB} = 1.98V		6	-	20	µA
I_{CCA} + I_{CCB}	Supply Current	OE = LOW; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		16		56	µA
Enable							
V_{IH}	HIGH-level input voltage	V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V	0.65V_{CCA}		0.65V_{CCA}		V
V_{IL}	LOW-level input voltage	V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72V to 1.98V		0.3V_{CCA}		0.3V_{CCA}	V
I_{LI}	Input leakage current	V_I = 0V to 1.98V; V_{CCA} = 0.72V to 1.98V; V_{CCB} = 0.72Vto 1.98V		±2		±5	µA

Notes:

1. V_{CCI} is the supply voltage associated with the input.
2. V_{CCO} is the supply voltage associated with the output.

Dynamic Characteristics

V_{CCA} = 0.8V ± 10%; GND = 0V; Tamb = -40℃ to +85℃; unless otherwise specified. [1][2]

Symbol	Parameter	Test Conditions	V_{CCB} = 1.2V ± 10%			V_{CCB} = 1.8V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD} [1]	propagation delay	A to B, C_L = 15pF		5.6	7.7		3.9	5.3	ns
		B to A, C_L = 15pF		10.6	19.9		9.6	17.2	
t_{EN}	Enable time	OE to A, B; C_L = 15pF		125	150		120	160	ns
t_{DIS}	Disable time	OE to A, No external load [2]			25			25	ns
		OE to B, No external load [2]			25			25	ns
		OE to A; C_L = 15pF			50			50	ns
		OE to B; C_L = 15pF			50			50	ns
tt	transition time	A port; C_L = 15pF		8.5	17.5		9	15.4	ns
		B port; C_L = 15pF		4	5.8		1.5	2.1	
t_{SKO}	Output Skew time	Delta between channel [3]	0	0.2	0.4	0	0.2	0.4	ns
t_W	Pulse Width	Data input	37			37			ns
f_{DATA}	Data rate		0.064		26	0.064		26	Mbps

Notes:

1. t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.
2. Guaranteed by design. Delay between OE going LOW and when the outputs are actually disabled.
3. Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

V_{CCA} = 1.2V ± 10%; GND = 0V; Tamb = -40℃ to +85℃; unless otherwise specified.

Symbol	Parameter	Test Conditions	V_{CCB} = 1.2V ± 10%			V_{CCB} = 1.8V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD}	propagation delay	A to B, C_L = 15pF		4.5	6.1		2.5	3.5	ns
		B to A, C_L = 15pF		3.9	5.3		2.8	3.9	ns
t_{PDC}	propagation delay	A to B, C_L = 80pF	NA	NA	NA		4.9	7	ns
		B to A, C_L = 30pF	NA	NA	NA		3.4	5	ns
t_{EN}	Enable time	OE to A, B; C_L = 15pF		50	100		50	100	ns
t_{DIS}	Disable time	OE to A, No external load			25			25	ns
		OE to B, No external load			25			25	ns
		OE to A; C_L = 15pF			50			50	ns
		OE to B; C_L = 15pF			50			50	ns
tt	transition time	A port; C_L = 15pF		2.6	3.5		1.5	2.5	ns
		B port; C_L = 15pF		3.6	5.1		1.3	2.2	ns
ttC	transition time	A port; C_L = 30pF	NA	NA	NA		2.2	3.6	ns
		B port; C_L = 80pF	NA	NA	NA		4.3	6.3	ns
t_{SKO}	Output Skew time	Delta between channel	0.0	0.1	0.2	0.0	0.1	0.3	ns
t_W	Pulse Width	Data input	15			13.5			ns
f_{DATA}	Data rate		0.064		52	0.064		52	Mbps

V_{CCA} = 1.8V ± 10%; GND = 0V; Tamb = -40℃ to +85℃; unless otherwise specified. (1)(2)

Symbol	Parameter	Test Conditions	V_{CCB} = 1.8V ± 10%			Unit
			Min.	Typ.	Max.	
t_{PD}	propagation delay	A to B, C_L = 15pF		2.5	3.4	ns
		B to A, C_L = 15pF		2.3	3	ns
t_{EN}	Enable time	OE to A, B; C_L = 15pF		25	50	ns
t_{DIS}	Disable time	OE to A, No external load			25	ns
		OE to B, No external load			25	ns
		OE to A; C_L = 15pF			50	ns
		OE to B; C_L = 15pF			50	ns
tt	transition time	A port; C_L = 15pF		1.2	1.7	ns
		B port; C_L = 15pF		1.7	2.5	ns
t_{SKO}	Output Skew time	Delta between channel [3]	0	0.1	0.2	ns
t_W	Pulse Width	Data input	13.5			ns
f_{DATA}	Data rate		0.064		52	Mbps

V_{CCA} = 0.8V ± 10%; GND = 0V; Tamb = -40℃ to +125℃; unless otherwise specified. (1)(2)

Symbol	Parameter	Test Conditions	V_{CCB} = 1.2V ± 10%			V_{CCB} = 1.8V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD} [1]	propagation delay	A to B, C_L = 15pF		5.6	7.7		3.9	5.3	ns
		B to A, C_L = 15pF		10.6	19.9		9.6	17.2	ns
t_{EN}	Enable time	OE to A, B; C_L = 15pF		125	150		120	160	ns
t_{DIS}	Disable time	OE to A, No external load [2]			25			25	ns
		OE to B, No external load [2]			25			25	ns
		OE to A; C_L = 15pF			50			50	ns

Symbol	Parameter	Test Conditions	V_{CCB} = 1.2V ± 10%			V_{CCB} = 1.8V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
		OE to B; C_L = 15pF			50			50	ns
t_t	transition time	A port; C_L = 15pF		8.5	17.5		9	15.4	ns
		B port; C_L = 15pF		4	5.8		1.5	2.1	ns
t_{SKO}	Output Skew time	Delta between channel [3]	0	0.2	0.4	0	0.2	0.4	ns
t_W	Pulse Width	Data input	37			37			ns
f_{DATA}	Data rate		0.064		26	0.064		26	Mbps

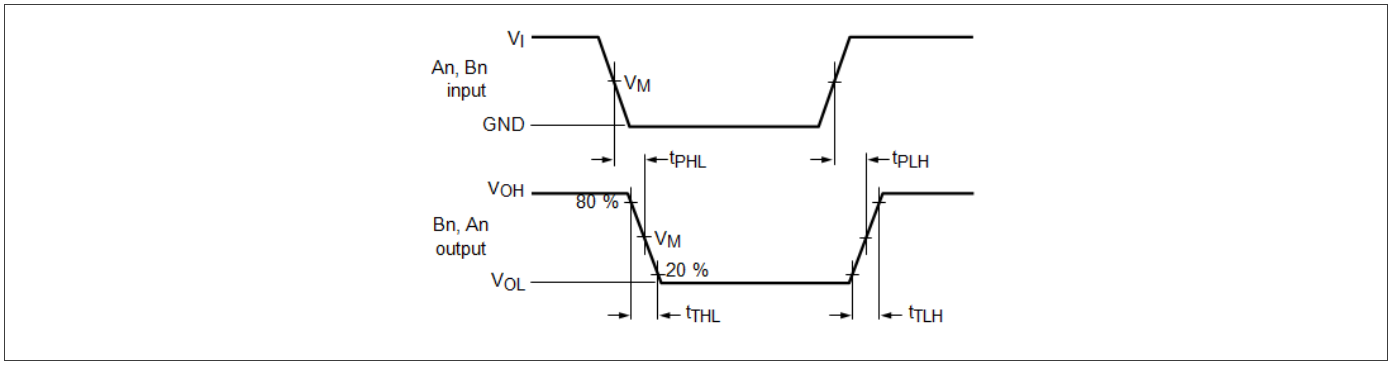
Notes:
1. t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.
2. Guaranteed by design. Delay between OE going LOW and when the outputs are actually disabled.
3. Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

V_{CCA} = 1.2V ± 10%; GND = 0V; Tamb = -40℃ to +125℃; unless otherwise specified. (1)(2)

Symbol	Parameter	Test Conditions	V_{CCB} = 1.2V ± 10%			V_{CCB} = 1.8V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD}	propagation delay	A to B, C_L = 15pF		4.5	6.2		2.5	3.6	ns
		B to A, C_L = 15pF		3.9	5.4		2.8	4.0	ns
t_{PDC}	propagation delay	A to B, C_L = 80pF	NA	NA	NA		4.9	7.4	ns
		B to A, C_L = 30pF	NA	NA	NA		3.4	5.3	ns
t_{EN}	Enable time	OE to A, B; C_L = 15pF		50	100		50	100	ns
t_{DIS}	Disable time	OE to A, No external load			25			25	ns
		OE to B, No external load			25			25	ns
		OE to A; C_L = 15pF			50	-		50	ns
		OE to B; C_L = 15pF			50	-		50	ns
tt	transition time	A port; C_L = 15pF		2.6	3.5		1.5	2.6	ns
		B port; C_L = 15pF		3.6	5.1		1.3	2.3	ns
ttC	transition time	A port; C_L = 30pF	NA	NA	NA		2.2	3.8	ns
		B port; C_L = 80pF	NA	NA	NA		4.3	6.9	ns
t_{SKO}	Output Skew time	Delta between channel	0	0.1	0.2	0	0.1	0.3	ns
t_W	Pulse Width	Data input	15			13.5			ns
f_{DATA}	Data rate		0.064		52	0.064		52	Mbps

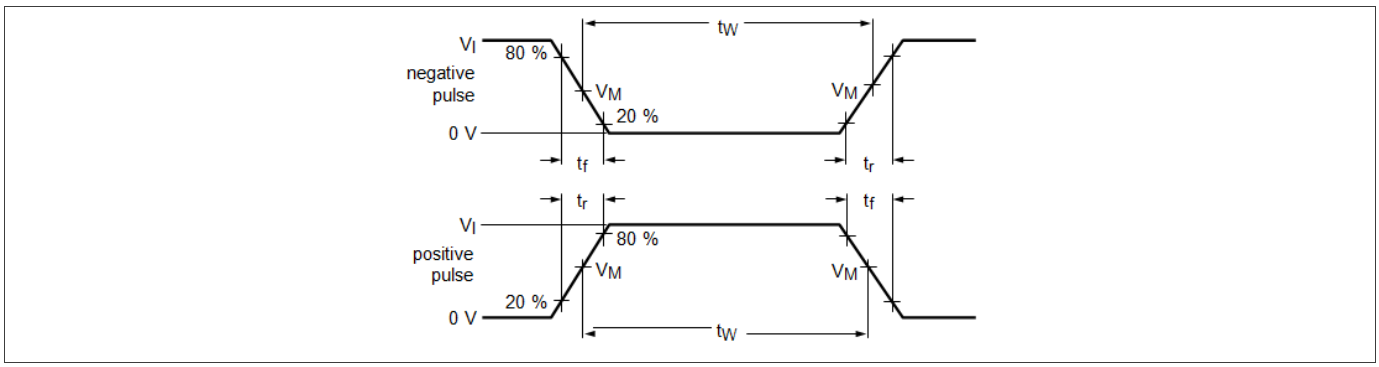
V_{CCA} = 1.8V ± 10%; GND = 0V; Tamb = -40℃ to +125℃; unless otherwise specified. (1)(2)

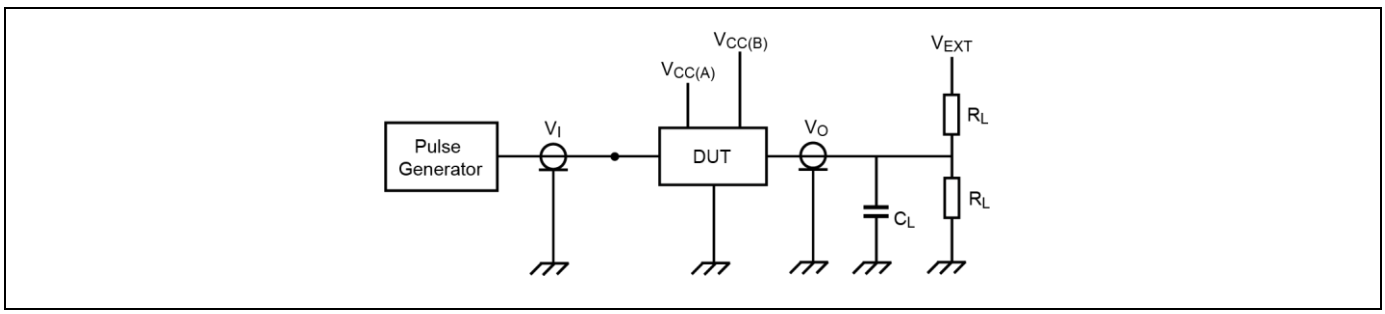
Symbol	Parameter	Test Conditions	V_{CCB} = 1.8V ± 10%			Unit
			Min.	Typ.	Max.	
t_{PD}	propagation delay	A to B, C_L = 15pF		2.5	3.5	ns
		B to A, C_L = 15pF		2.3	3.1	ns
t_{EN}	Enable time	OE to A, B; C_L = 15pF		25	50	ns
t_{DIS}	Disable time	OE to A, No external load			25	ns
		OE to B, No external load			25	ns
		OE to A; C_L = 15pF			50	ns
		OE to B; C_L = 15pF			50	ns
tt	transition time	A port; C_L = 15pF		1.2	1.7	ns
		B port; C_L = 15pF		1.7	2.6	ns
t_{SKO}	Output Skew time	Delta between channel [3]	0	0.1	0.2	ns
t_W	Pulse Width	Data input	13.5			ns
f_{DATA}	Data rate		0.064		52	Mbps



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Supply Voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
0.8 V ± 10 %	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.08 V	V_{OH} - 0.08 V
1.2 V ± 10 %	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.12 V	V_{OH} - 0.12 V
1.8 V ± 10 %	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.18 V	V_{OH} - 0.18 V





All input pulses are supplied by generators having the following characteristics: PRR ≤ 26 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ ns.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.V_{EXT} = External voltage for measuring switching times.

Supply Voltage		Input		Load		V_{EXT}		
V_{CCA}	V_{CCB}	V_I	$\Delta t/\Delta V$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}(3)
0.72V to 1.98V	0.72V to 1.98V	V_{CCI}	≤ 1.0 ns/V	15pF	50kΩ, 1MΩ	Open	Open	$2V_{CCO}$

1. V_{CCI} is the supply voltage associated with the input.
2. For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 kΩ.
3. V_{CCO} is the supply voltage associated with the output.

Input Driver Requirements

The continuous DC current sinking or sourcing capability is determined by the external system-level; open-drain or push-pull drivers that are interfaced to the PI3CLS9606 IO pins.
The high bandwidth of these IO circuits used to facilitate this fast change from an input to an output and an output to an input, they have a modest sourcing capability of hundreds of micro-amperes, as determined by the pull-up resistor.
The fall time of a signal depends on the edge-rate and output impedance of the external driving the PI3CLS9606 data IOs, as well as the capacitive loading at the data lines.

Power-up and Power-down

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. There is no special power-up sequencing required. The PI3CLS9606 includes circuitry that disables all output ports and puts the device into a power-down mode when either V_{CCA} or V_{CCB} is switched off.

Enable and Disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND, OE pin should not be left floating in any condition.
OE V_{IL} and V_{IH} are referenced to V_{CCA}. The OE can be controlled by an external device that is powered by either V_{CCA} or V_{CCB}. As V_{CCB} is required to be greater than V_{CCA}, the OE pin has been designed to withstand a voltage equal to V_{CCB} (up to 1.98V per recommended functional voltage range)

Application Information

The PI3CLS9606 can be used to interface between devices or systems operating at different supply voltages. See the figures below for a typical operating circuit using the PI3CLS9606.

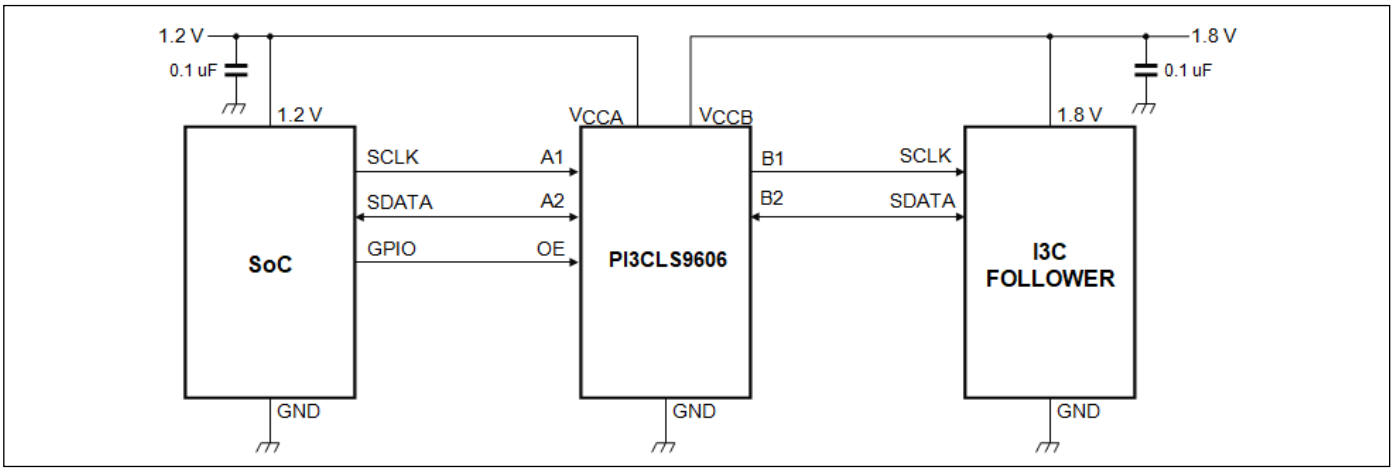


Figure 1. I3C Application

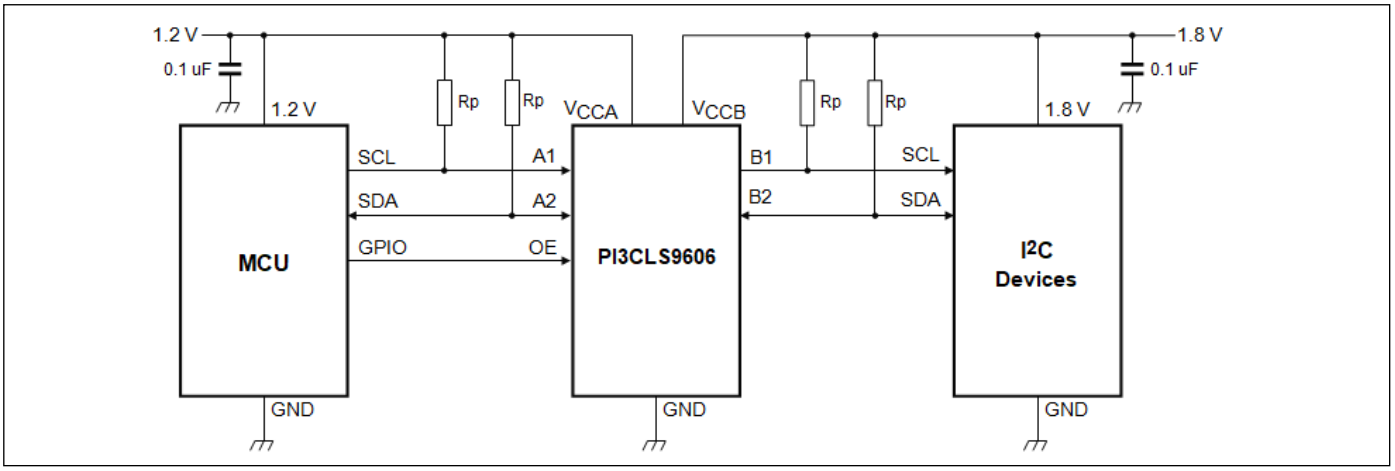
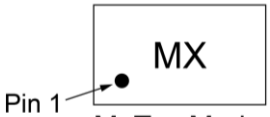


Figure 2. I2C Application

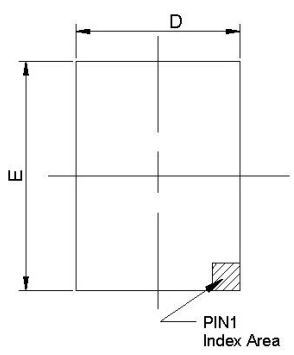
Part Marking



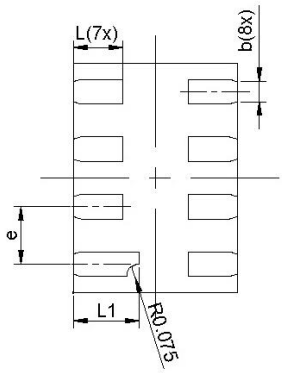
M: Top Mark
X: One Character Shorted Date Code

Mechanical Information

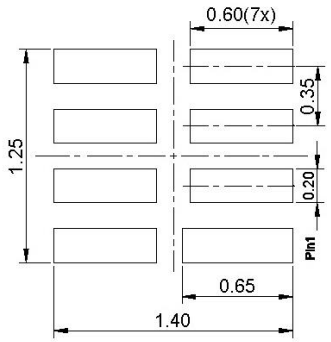
8-X1-DFN1410-8 (HK)



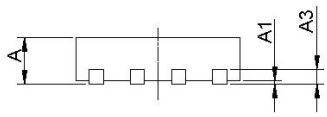
TOP VIEW



Bottom VIEW



RECOMMENDED LAND PATTERN(unit:mm)



SIDE VIEW

PKG. DIMENSIONS(MM)			
SYMBOL	Min	Nom	Max
A	0.36	0.40	0.43
A1	0	0.02	0.05
A3		0.13 REF	
D	0.95	1.00	1.05
E	1.35	1.40	1.45
b	0.12	0.15	0.20
e		0.35 BSC	
L	0.25	0.30	0.35
L1	0.35	0.40	0.45

Notes:
1. Ref: JEDEC MO-288
2. LAND PATTERN REFERENCE DIODES X2-DFN1410-8 PACKAGE INFORMATION

DATE: 12/10/20

DESCRIPTION: 8-Pin, X1-DFN1410-8

PACKAGE CODE: HK (HK8)

DOCUMENT CONTROL#: PD-2264 REVISION:--

20-0540

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Number	Package Code	Description
PI3CLS9606HKEX	HK	8-Pin, X1-DFN1410

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
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