A Product Line of
Diodes Incorporated

PI2MEQX2505

MIPI CSI-2/DSI D-PHY ReDriver

Features

- MIPI D-PHY 1.2 Specification Compliant
- Supports 4 lanes at 2.5Gbps in D-PHY
- Supports ULPS and LP power states and sub-mW in shutdown state
- Supports MIPI DSI Bi-directional LP mode
- Programmable and pin adjustable on Receiver Equalization and transmitter edge rate
- Programmable Output swing and Pre-emphasis levels
- Industrial temperature range: –40 °C to 85 °C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 28-contact, TQFN (ZH), 5.5 x 3.5 mm

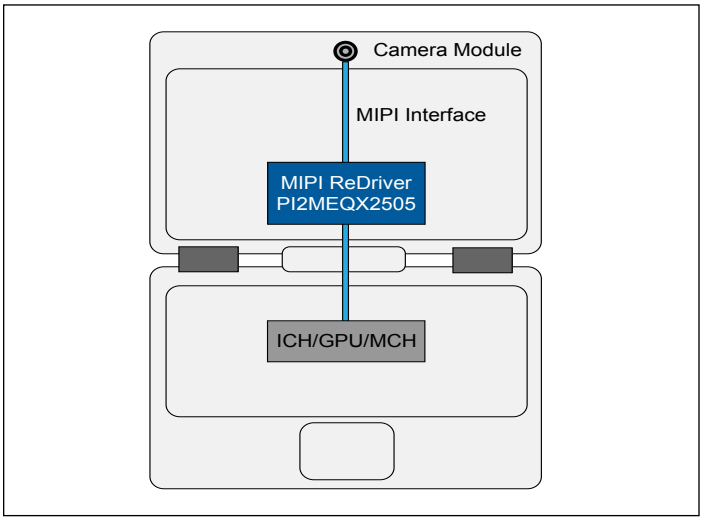
Description

The PI2MEQX2505 is a low power, high performance 2.5Gbps four lanes data and clock MIPI D-PHY ReDriver™ designed specifically for MIPI D-PHY 1.2 protocol.

The device provides programmable equalization, output swing and pre-emphasis to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI2MEQX2505 supports MIPI D-PHY 1.2 standard with 100Ω differential CML data I/O between CSI-2 Source and CSI-2 Sink, over cable, or to extend the signals across other distant data pathways on the user’s platform. It also supports pin adjustable on receiver equalization and edge rate on transmitter rise and fall time.

PI2MEQX2505 is optimized for mobile applications, and contains activity detection circuitry on the D-PHY Link interface that can transit into a lower power mode when in ULPS and LP states.

Typical MIPI Re-Driver in NB Application



Applications

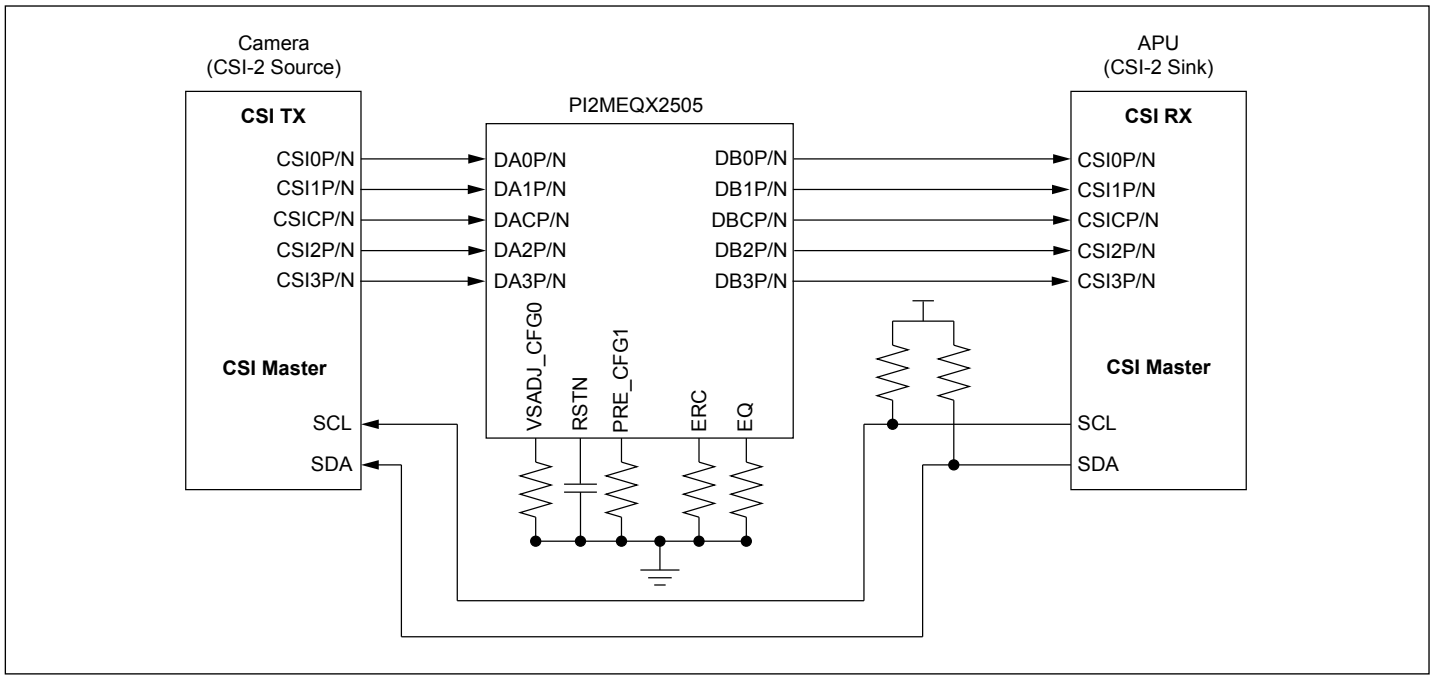
- Notebook PC
- Clamshell
- Tablets
- Camera

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

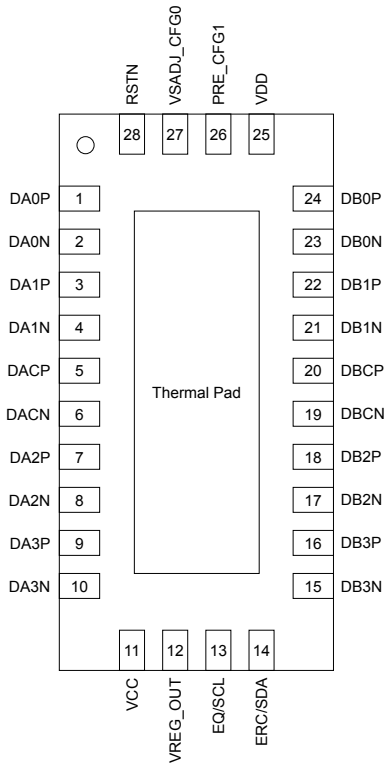
ReDriver is a trademark of Diodes Incorporated.

Block Diagram



Pin Configuration

ZH28 (TQFN)



Pin Description

Pin#	Pin Name	Type		Description
1	DA0P	100Ω Differential Input		CSI-2/DSI Lane 0 Differential positive Input. Supports DSI LP Backchannel. If unused, this pin should be tied to GND.
2	DA0N			CSI-2/DSI Lane 0 Differential negative Input. Supports DSI LP Backchannel. If unused, this pin should be tied to GND.
3	DA1P	100Ω Differential Input		CSI-2/DSI Lane 1 Differential positive Input. If unused, this pin should be tied to GND.
4	DA1N			CSI-2/DSI Lane 1 Differential negative input. If unused, this pin should be tied to GND.
5	DACP	100Ω Differential Input		CSI-2/DSI Differential Clock positive Input
6	DACN			CSI-2/DSI Differential Clock negative Input

Pin Description Cont.

Pin#	Pin Name	Type		Description
7	DA2P	100Ω Differential Input		CSI-2/DSI Lane 2 Differential positive Input. If unused, this pin should be tied to GND.
8	DA2N			CSI-2/DSI Lane 2 Differential negative Input. If unused, this pin should be tied to GND.
9	DA3P	100Ω Differential Input		CSI-2/DSI Lane 3 Differential positive Input. If unused, this pin should be tied to GND.
10	DA3N			CSI-2/DSI Lane 3 Differential negative Input. If unused, this pin should be tied to GND.
11	VCC	Power		1.8V (±10%) Supply.
12	VREG_OUT	Power		1.2V Regulator Output. Requires a 0.1 µF capacitor to GND.
13	EQ/SCL	I (3-level)	Pullup/ Pull-down (100K)	RX Equalization Select. Pin state sampled on rising edge of RSTN. This pin also functions as I2C SCL pin. EQ/SCL = V_{IL}: Equalization = 3dB EQ/SCL = V_{IM}: Equalization = 6dB EQ/SCL = V_{IH}: Equalization = 9dB
14	ERC/SDA	I/O (3-level)	Pullup/ Pull-down (100K)	Edge Rate Control for DB[4:0]P/N High speed transmitter rise and fall time. Pin state sampled on rising edge of RSTN. This pin also functions as I2C SDA pin. ERC/SDA = V_{IL}: Edge rate = 200ps ERC/SDA = V_{IM}: Edge rate = 150ps ERC/SDA = V_{IH}: Edge rate = 250ps
15	DB3N	100Ω Differential Output		CSI-2/DSI Lane 3 Differential negative Output. If unused, this pin should be left unconnected.
16	DB3P			CSI-2/DSI Lane 3 Differential positive Output. If unused, this pin should be left unconnected.
17	DB2N	100Ω Differential Output		CSI-2/DSI Lane 2 Differential negative Output. If unused, this pin should be left unconnected.
18	DB2P			CSI-2/DSI Lane 2 Differential positive Output. If unused, this pin should be left unconnected.
19	DBCN	100Ω Differential Output		CSI-2/DSI Differential Clock negative Output
20	DBCP			CSI-2/DSI Differential Clock positive Output
21	DB1N	100Ω Differential Output		CSI-2/DSI Lane 1 Differential negative Output. If unused, this pin should be left unconnected.
22	DB1P			CSI-2/DSI Lane 1 Differential positive Output. If unused, this pin should be left unconnected.

Pin Description Cont.

Pin#	Pin Name	Type		Description
23	DB0N	100Ω Differential Output		CSI-2/DSI Lane 0 Differential negative Output. Supports DSI LP Back channel. If unused, this pin should be left unconnected.
24	DB0P			CSI-2/DSI Lane 0 Differential positive Output. Supports DSI LP Back channel. If unused, this pin should be left unconnected.
25	VDD	Power		This pin must be connected to the VREG_OUT pin through at least a 10-mil trace and a 0.1 µF capacitor to ground.
26	PRE_CFG1	I (3-level)	Pullup/ Pull-down (100K)	Controls DPHY TX HS pre-emphasis level and the LP TX rise and fall times. Pin state is sampled on the rising edge of RSTN. PRE_CFG1 = V_{IL}: Pre-emphasis level = 0 dB PRE_CFG1 = V_{IM}: Pre-emphasis level = 1 dB PRE_CFG1 = V_{IH}: Pre-emphasis level = 3 dB
27	VSADJ_CFG0	I (3-level)	Pullup/ Pull-down (100K)	Controls output voltage swing for DB HS transmitters and the LP TX rise and fall times. Pin state is sampled on the rising edge of RSTN. VSADJ_CFG0 = V_{IL}: Swing = 225 mV VSADJ_CFG0 = V_{IM}: Swing = 250 mV VSADJ_CFG0 = V_{IH}: Swing = 275 mV
28	RSTN	I		Reset, active low. When low, all internal CSR are reset to default and PI2MEQX2505 is placed in low power state.
Center Pad	GND	GND		Ground.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . . –65°C to +150°C
Supply Voltage to Ground Potential . . . . . –0.3V to +2.175V
Voltage Range
D-PHY Lane I/O Differential Voltage . . . . . –0.3V to +1.4V
RSTN . . . . . –0.3V to +2.175V
All Other Terminals . . . . . –0.3V to +2.175V
Max Junction Temperature . . . . . 105°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD Rating

Symbol	Parameter	Conditions	Value	Units
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	V

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage		1.62	1.8	1.98	V
T_A	Operating free-air temperature		-40		85	°C

Electrical Characteristics, Power Supply

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PACTIVE1	Power under normal operation for 4 data lanes + clock.	D-PHY Lanes at 2.5 Gbps; V_{CC} supply stable, V_{CC} = 1.8 V		135	200	mW
PACTIVE2	Power under normal operation for 2 data lanes + clock.	D-PHY Lanes 2.5 Gbps; V_{CC} supply stable, V_{CC} = 1.8 V		80	120	mW
P_LP11	LP11 Power	All D-PHY lanes in LP11; V_{CC} supply stable; V_{CC} = 1.8 V		2	5	mW
P_STB	Standby mode power	RSTN held in asserted state (low); V_{CC} supply stable; V_{CC} = 1.8 V		0.02	0.2	mW
P_ULPS	ULPS mode power	IC stay in ULPS mode; V_{CC} supply stable; V_{CC} = 1.8 V		2	5	mW

Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Standard IO (RSTN, ERC, EQ, CFG[1:0])						
V_{IL}	Low-level control signal input voltage		0		0.14xV_{CC}	V
V_{IM}	Mid-level control signal input voltage		0.45xV_{CC}	V_{CC}/2	0.55xV_{CC}	V
V_{IH}	High-level control signal input voltage		0.86xV_{CC}		VCC	V
V_F	Floating Voltage	V_{IN} = High Impedance		V_{CC}/2		V
V_{OL}	Low level output voltage (open-drain). ERC (SDA) only	At I_{OL} max.			0.2xV_{CC}	V
I_{OL}	Low Level Output Current				3	mA
I_{IH}	High level input current				±36	µA
I_{IL}	Low level input current				±36	µA
R_{PU}	Internal pull-up resistance			100		kΩ
R_{PD}	Internal pull-down resistance			100		kΩ
$R_{(RSTN)}$	RSTN control input pullup resistor			300		kΩ
SCL, SDA						
V_{IL}	Low-level I2C signal input voltage				0.3xV_{CC}	V
V_{IH}	High-level I2C signal input voltage		0.7xV_{CC}			V
MIPI D-PHY HS Receiver Interface (DA0P/N, DA1P/N, DA2P/N, DA3P/N, DACP/N)						
$V_{(CM-RX\_DC)}$	Differential Input Common-mode voltage HS Receive mode	$V_{(CM-RX)} = (V_{A\,x\,P} + V_{A\,x\,N})/2$	70		330	mV
$\lvert V_{ID} \rvert$	HS Receiver input differential voltage	$\lvert V_{ID} \rvert = \lvert V_{A\,x\,P} - V_{A\,x\,N} \rvert$ <1.5 Gbps	70			mV
		$\lvert V_{ID} \rvert = \lvert V_{A\,x\,P} - V_{A\,x\,N} \rvert$ >1.5 Gbps	40			mV
$V_{IH(HS)}$	Single-ended input high voltage				460	mV
$V_{IL(HS)}$	Single-ended input low voltage		-40			mV
$R_{(DIFF-HS)}$	Differential input impedance		75	100	125	Ω
$V_{(RXEQ0)}$	Rx EQ gain when EQ/SCL pin ≤ V_{IL}			3		dB
$V_{(RXEQ1)}$	Rx EQ gain when EQ/SCL pin = V_{IM}	At 1250 MHz		6		dB
$V_{(RXEQ2)}$	Rx EQ gain when EQ/SCL pin ≥ V_{IH}	At 1250 MHz		9		dB

Electrical Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
MIPI D-PHY LP Receiver Interface (DA0P/N, DA1P/N, DA2P/N, DA3P/N, DACP/N, DB0P/N)						
$V_{(LPIH)}$	LP Logic 1 Input Voltage		880			mV
$V_{(LPIL)}$	LP Logic 0 Input voltage				550	mV
$V_{(HYST)}$	LP Input Hysteresis		25			mV
MIPI D-PHY HS Transmitter Interface (DB0P/N, DB1P/N, DB2P/N, DB3P/N, DBCP/N)						
$V_{(CMTX)}$	HS Transmit static common-mode voltage, VSADJ_CFG0 = VIL	$V_{(CMTX)} = (V_{(BP)} + V_{(BN)}) /2$	150	200	250	mV
$\lvert\Delta V_{(CMTX)(1,0)}\rvert$	VCMTX mismatch when output is differential-1 or differential-0	$\Delta V_{(CMTX)(1,0)} = (V_{(CMTX)(1)} - V_{(CMTX)(0)}) /2$			5	mV
$\lvert V_{OD(VD0)}\rvert$	HS Transmit differential voltage, VSADJ_CFG0 = VIL	$\lvert V_{OD}\rvert = \lvert V_{(DP)} - V_{(DN)}\rvert$	140	200	270	mV
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is differential-1 or differential-0	$\Delta V_{OD} = \lvert\Delta V_{O(D1)}\rvert - \lvert\Delta V_{O(D0)}\rvert$			14	mV
$V_{OH(HS)}$	HS Output high voltage for non-transition bit	CFG0 ≥ V_{IH} HS Pre = 3 dB			430	mV
$V_{(PRE1)}$	Pre-emphasis Level for HSTX_PRE_CFG1 = VIM	PRE = 20 x LOG ($V_{OD(TBx)}$ / $V_{OD(VDX)}$), See Figure 1.		1		dB
$V_{(PRE2)}$	Pre-emphasis level for HSTX_PRE_CFG1 = VIH	PRE = 20 x LOG ($V_{OD(TBx)}$ / $V_{OD(VDX)}$), See Figure 1.		3		dB
$R_{pd(HS)}$	Pull down resistor when RSTN = 0 V			300		kΩ
LP Mode Switch Interface						
R_{ON_LP}	I_{ON} = -8 mA, DA0P/N, DA1P/N, DA2P/N, DA3P/N, DCP/N = 1.2 V	V_{CC} = 1.8 V		30	60	Ω
ΔR_{ON_LP}	I_{ON} = -8 mA, DA0P/N, DA1P/N, DA2P/N, DA3P/N, DCP/N = 1.2 V	V_{CC} = 1.8 V		0.1	0.5	Ω
C_{ON}		V_{CC} = 1.8 V		7		pF
-3db BW		V_{CC} = 1.8 V; DC bias = 0 V		800		MHz

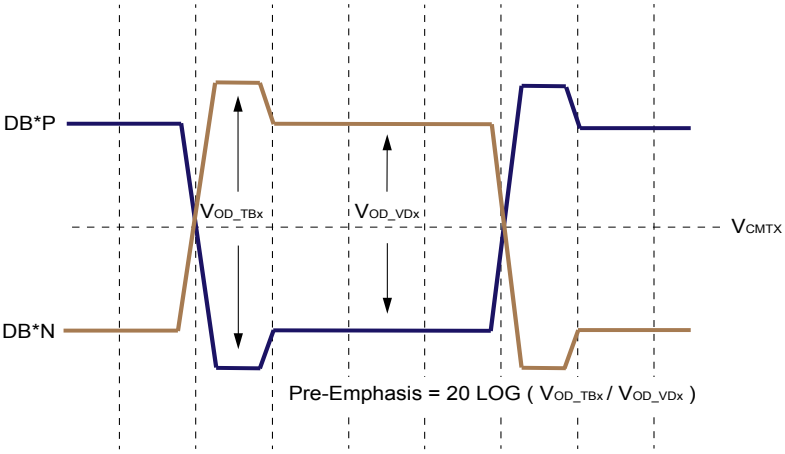


Figure 1. DPHY HS TX Pre-emphasis

Timing Requirements

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I2C (ERC (SDA), EQ (SCL))						
$t_{HD;STA}$	Hold Time (repeated) START condition. After this period, the first clock pulse is generated		4			µs
t_{LOW}	Low period of SCL clock		4.7			µs
t_{HIGH}	High period of SCL clock		4			µs
$t_{SU;STA}$	Setup time for a repeated START condition		4.7			µs
$t_{HD;DAT}$	Data hold time		5			µs
$t_{SU;DAT}$	Data setup time		4			µs
$t_{SU;STO}$	Setup time for STOP condition		4			µs
t_{BUF}	Bus free time between a STOP and START condition		4.7			µs
RSTN						
t_{D1}	V_{CC} stable before de-assertion of RSTN		100			µs
t_{SU2}	Setup of VSADJ_CFG0, PRE_CFG1, EQ and ERC pin before de-assertion of RSTN		0			µs
t_{h2}	Hold of VSADJ_CFG0, PRE_CFG1, EQ and ERC pin after de-assertion of RSTN		250			µs
t_{VCC_RAMP}	V_{CC} supply ramp requirements		0.2		100	ms
Delay Time for HS Mode						
t_{HSPD}	Propagation delay from DA to DB. In HS mode			1		ns

Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.(1)	Max.	Units
I2C (ERC (SDA), EQ (SCL))						
$F_{(SCL)}$	I2C Clock Frequency				100	kHz
t_{F_I2C}	Fall time of both SDA and SCL signals	Load of 350 pF with 2-K pullup resistor. Measure at 30% - 70%			300	ns
t_{R_I2C}	Rise Time of both SDA and SCL signals				1000	ns
D-PHY Link						
$F_{(BR)}$	Bit Rate				2.5	Gbps
$F_{(HSCLK)}$	HS Clock Input range		100		1250	MHz
MIPI D-PHY HS Receiver Interface (DACP/N, DA0P/N, DA1P/N, DA2P/N, DA3P/N)						
$\Delta V_{(CMRX\_HF)}$	Common-mode Interface beyond 450 MHz				100	mV
		>1.5 GHz			50	mV
$\Delta V_{(CMRX\_LF)}$	Common-mode interference 50 MHz – 450 MHz		-50		50	mV
MIPI D-PHY HS Transmitter Interface (DBCP/N, DB0P/N, DB1P/N, DB2P/N, DB3P/N)						
$\Delta V_{(CMTX\_HF)}$	Common-level variations above 450 MHz				15	mVrms
$\Delta V_{(CMTX\_LF)}$	Common-level variation between 50 MHz – 450 MHz				25	mVpeak
t_R and t_F	20% - 80% rise time and fall time	Datarate ≤ 1 Gbps			0.3	UI
		Datarate > 1 Gbps and ≤ 1.5 Gbps			0.35	UI
		Datarate > 1.5 Gbps			0.4	UI
		Datarate ≤ 1.5 Gbps	100			ps
		Datarate > 1.5 Gbps	50			ps
D-PHY LP Receiver Interface (DACP/N, DA0P/N, DA1P/N, DA2P/N, DA3P/N, DB0P/N)						
e_{SPIKE}	Input Pulse rejection				300	V ps
$t_{MIN(RX)}$	Minimum pulse width response		20			ns
$V_{(INT)}$	Peak interference amplitude				200	mV
$F_{(INT)}$	Interference Frequency		450			MHz
MIPI D-PHY LP Transmitter Interface (DBCP/N, DB0P/N, DB1P/N, DB2P/N, DB3P/N)						
t_{REOT}	30% - 85% rise time and fall time	Measured at end of HS transmission.			35	ns

Note:

1. All typical values are at V_{CC} = 1.8V, and T_A = 25°C.

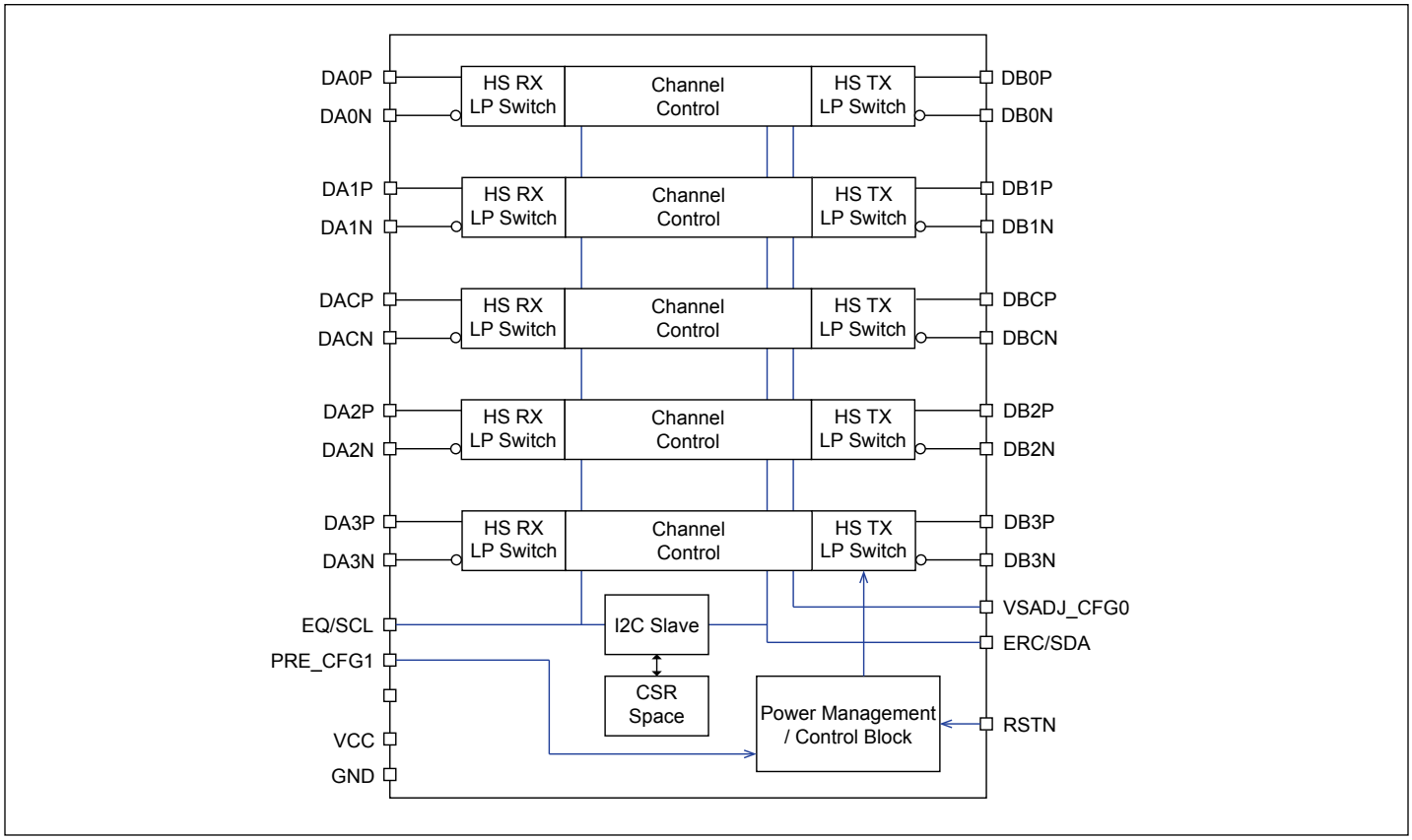
Detailed Description

Overview

The PI2MEQX2505 is a one to four lane and clock MIPI D-PHY ReDriver™ that regenerates the D-PHY signaling. The device complies with MIPI D-PHY 1.2 standard and can be used in either a MIPI CSI-2 or MIPI DSI application at datarates of up to 2.5 Gbps in D-PHY.

The device compensates for PCB, connector, and cable related frequency loss and switching related loss to provide the optimum electrical performance from a CSI2/DSI source to sink. The PI2MEQX2505 D-PHY inputs feature configurable equalizers.
The PI2MEQX2505 output swing and edge rate can be adjusted by changing the state of the VSADJ_CFG0 pin and ERC pin respectively.
The PI2MEQX2505 is optimized for mobile applications, and contains activity detection circuitry on the D-PHY Link interface that can transition into a lower power mode when in ULPS and LP states.
The device is characterized for an extended operational temperature range from –40°C to 85°C.

Functional Block Diagram



Feature Description

HS Receive Equalization

The PI2MEQX2505 supports three levels of receive equalization to compensate for ISI loss in the channel. These three levels are 3 dB, 6 dB, and 9 dB at 1250Mhz. The equalization level used by the PI2MEQX2505 is determined by the state of the EQ/SCL pin at the rising edge of RSTN. If necessary, the receiver equalization level can also be set through writing to the RXEQ register via the local I2C interface.

Table 1. EQ/SCL Pin Function

EQ/SCL Pin	HS Rx Equalization
≤ V_{IL}	3 dB
V_{IM}	6 dB
≥ V_{IH}	9 dB

HS TX Edge Rate Control

Table 2. HS TX Edge Rate Control

ERC/SDA Pin	HS Rise/Fall Times
≤ V_{IL}	200 ps typical
V_{IM}	150 ps typical
≥ V_{IH}	250 ps typical

I2C Slave Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
1	1	0	1	1	0	0	0/1

Register Map

Address	Register	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Device ID	Read	Device ID (PI2MEQX2505): (reset value: 00000101b)							
01h	Version ID	Read	Version ID (Version 0): (reset value: 00000000b)							
02h	EQ	Read/Write	Reserved (reset value: 0000b)				EQ <3>	EQ <2>	EQ <1>	EQ <0>
03h	ERC	Read/Write	Reserved (reset value: 00000b)					ERC <2>	ERC <1>	ERC <0>
04h	Reserved	Read	Reserved (reset value: 00001000b)							
05h	Output Pre-emphasis & Swing	Read/Write	Reserved (reset value: 0110b)				PREEMP LEVEL <1>	PREEMP LEVEL <0>	VSADJ <1>	VSADJ <0>

Register Setting for EQ/ERC/PRE_CFG1/VSADJ_CFG0

EQ<3:0> (Register 02h<3:0>)	EQ Gain at 500MHz	EQ Gain at 1250MHz
0000	0dB	0dB
0010	2dB	3dB
0110	4dB	6dB
1011	6dB	9dB
Others	Reserved	Reserved

ERC<2:0> (Register 03h<2:0>)	Edge Rate Control
001	250ps
011	200ps
111	150ps
Others	Reserved

PREEMP LEVEL<1:0> (Register 05h<3:2>)	Pre-emphasis Level
00	0dB
01	1dB
11	3dB
Others	Reserved

VSADJ<1:0> Register 05h<1:0>	Output Voltage Swing
00	200mV
01	225mV
10	250mV
11	275mV

Bus Transaction

Writing to the Registers

Data is transmitted to the PI2MEQX2505 by sending the device address and setting the least significant bit to a logic 0. The register sub-address byte is sent after the address and determines which register will receive the data following the sub-address byte.

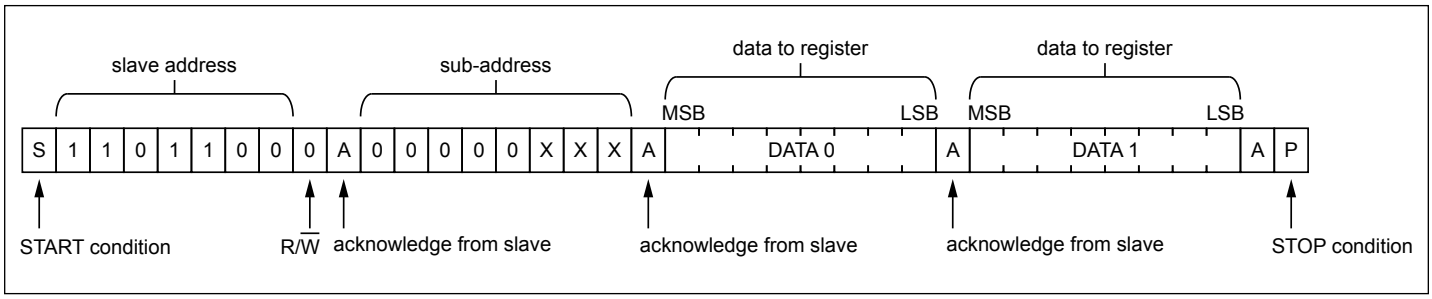


Figure 2. Write to Register

Reading the Register

In order to read data from the PI2MEQX2505, the bus master must first send the PI2MEQX2505 address with the least significant bit set to a logic 0. The sub-address byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the lease significant bit is set to a logic 1. Data from the register defined by the sub-address byte will then be sent by the PI2MEQX2505. Data is clocked into the register on the falling edge of the acknowledge clock pulse.

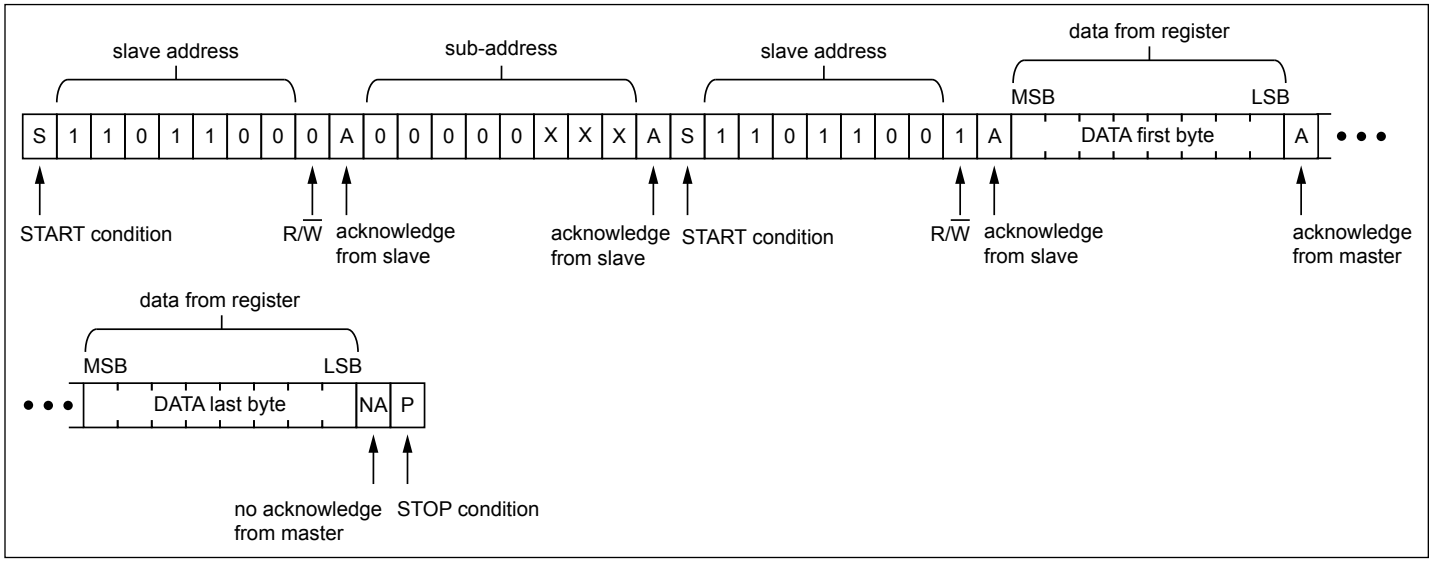
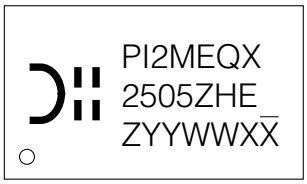


Figure 3. Read from Register

Part Marking

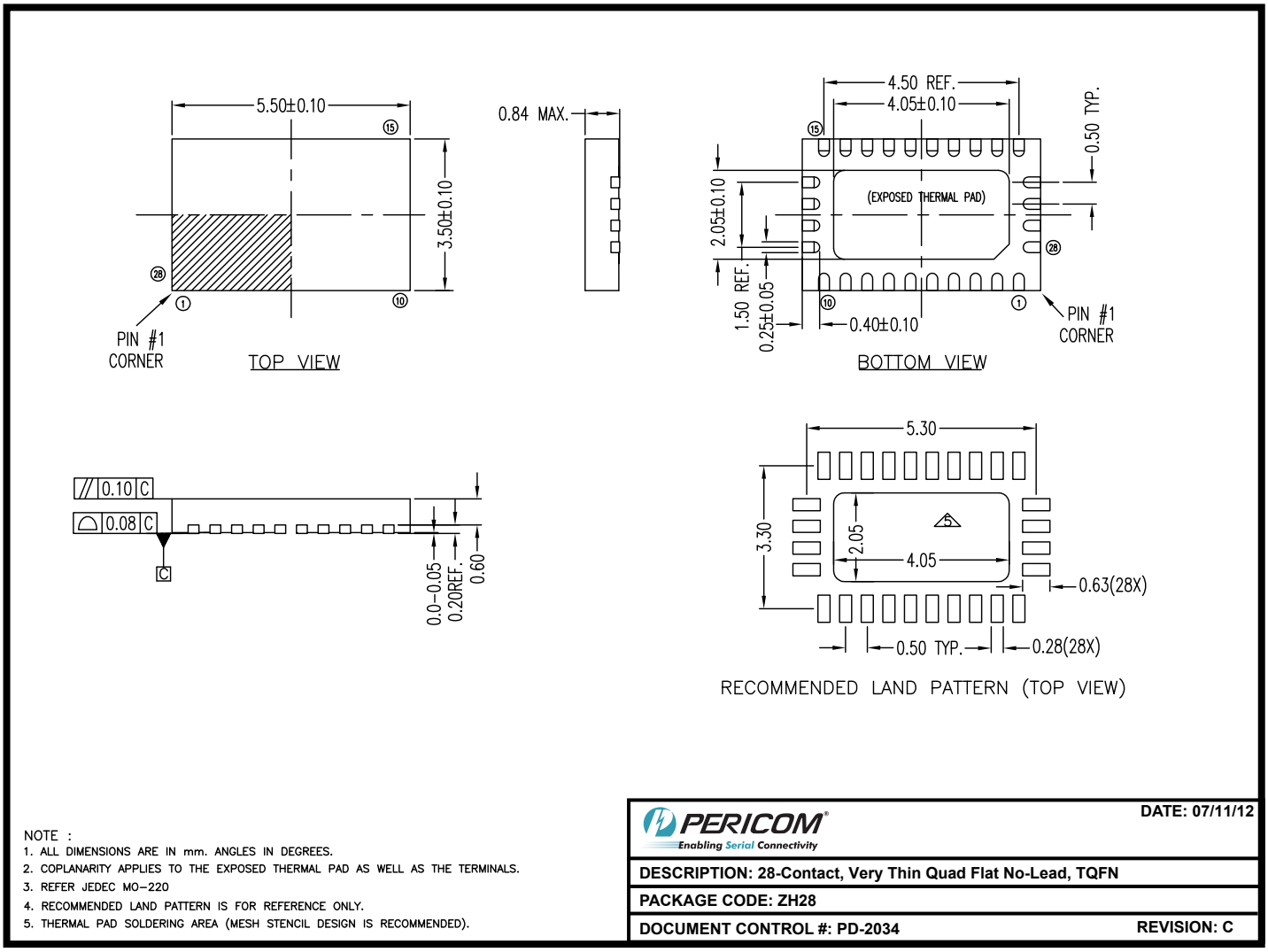
28-TQFN (ZH)



Z: Die Rev
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code
Bar above 2nd “X” means Cu wire

Packaging Mechanical

28-TQFN (ZH)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity

DATE: 07/11/12

DESCRIPTION: 28-Contact, Very Thin Quad Flat No-Lead, TQFN

PACKAGE CODE: ZH28

DOCUMENT CONTROL #: PD-2034 REVISION: C

12-0419

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Number	Package Code	Package Description
PI2MEQX2505ZHEX	ZH	28-contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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