

**2-BITS BIDIRECTIONAL LEVEL TRANSLATOR
 OPEN-DRAIN AND PUSH-PULL APPLICATIONS**

Description

The LSF0102 is a 2-channel bidirectional multi-voltage level translator for open-drain and push-pull applications. This device is a universal level translator that A port operates from 0.65V to 4.5V (Vref_A) and B port 1.8V to 5.5V (Vref_B). This range allows for bidirectional voltage translations between 0.65V and 5.0V. Be aware that Vref_B is recommended to be at 1.0V higher than Vref_A for best signal integrity.

The EN pin is used to activate the device. When EN is HIGH, the translator switch is on. Otherwise, EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by Vref_B via an external Rpu (pullup resistor, typ 200kΩ) and the EN must be LOW during power-up or power-down to avoid miss operation.

Be aware that external Rpu (pullup resistor) is required on each signal in both A and B ports for push-pull application because a pull-high state can avoid miss operation during power-up or power-down. As same as open-drain application, the smaller Rpu results in the larger driving current. For bidirectional signal flows, there is no need for a direction pin to minimize system effort. This device supports 5V tolerant I/O pins in a variety of applications which require different voltage translation levels.

Features

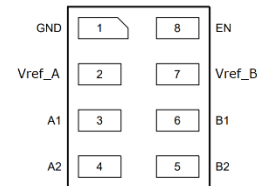
- External Rpu (Pullup Resistor) Sets Driving Current in Both Push-Pull and Open-Drain Applications
- Maximum Data Rate is Dominated by the System Capacitance and Pullup Resistors
 - $\leq 100\text{MHz}$; $C_L = 15\text{pF}$, 30pF , $R_{PU} \leq 300\Omega$
 - $\leq 50\text{MHz}$; $C_L = 50\text{pF}$, $R_{PU} \leq 300\Omega$
- Bidirectional Voltage Level Translation Between:
 - 0.65V and 1.5V, 1.8V, 2.5V, 3.3V and 5.0V
 - 1.2V and 1.8V, 2.5V, 3.3V and 5.0V
 - 1.8V and 2.5V, 3.3V and 5.0V
 - 2.5V and 3.3V and 5.0V
 - 3.3V and 5.0V
- ESD Protection Exceeds JESD 22
 - 4000V HBM (A114)
 - 1500V CDM (C101)
- Latch-Up Exceeds 100mA per JESD 17
- Specified from -40°C to $+125^\circ\text{C}$
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.**

<https://www.diodes.com/quality/product-definitions/>

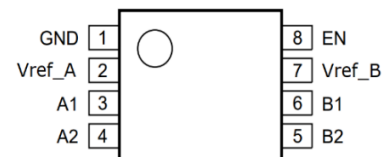
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain $<900\text{ppm}$ bromine, $<900\text{ppm}$ chlorine ($<1500\text{ppm}$ total Br + Cl) and $<1000\text{ppm}$ antimony compounds.

Pin Assignments

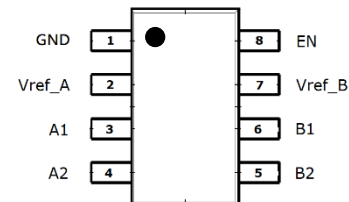
(Top View)



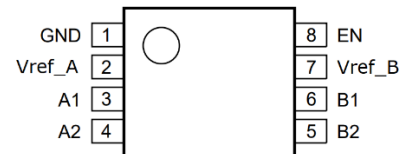
X2-DFN1410-8



SSOP-8



SOT28



VSSOP-8 / MSOP-8

Applications

- GPIO, MDIO, SDIO, SVID, UART
- PMBus, SMBus, I2C, and other interfaces
- Telecom infrastructure
- Industrial
- High-performance computing
- Wide array of products such as:
 - PCs, networking, notebooks
 - Smart phones
 - Tablets

Pin Descriptions

Pin Number	Pin Name	Function
1	GND	Ground
2	Vref_A	Reference supply voltage; A port
3	A1	Input/output
4	A2	Input/output
5	B2	Input/output
6	B1	Input/output
7	Vref_B	Reference supply voltage; B port
8	EN	Enable input (active HIGH)

Absolute Maximum Ratings (Note 4)

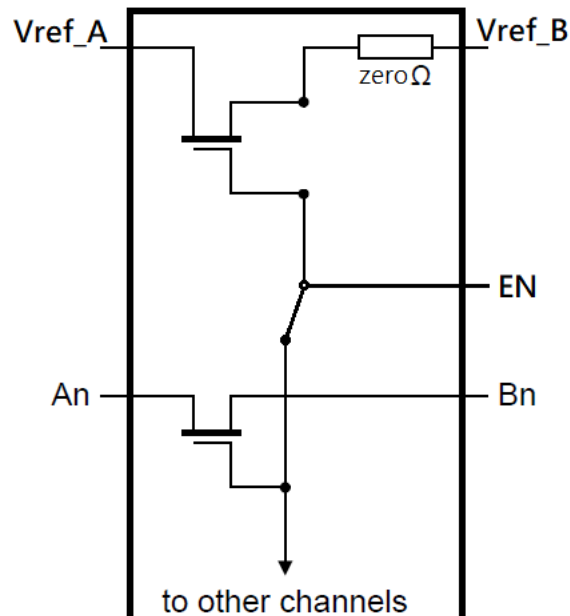
Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	±4	kV
ESD CDM	Charged Device Model ESD Protection	±1.5	kV
VREF	Supply Reference Voltage Range	-0.5 to +6.0	V
VI	Input Voltage Range	-0.5 to +6.0	V
VO	Voltage Range Applied to Any Output in the High-Z or Power-Off State	-0.5 to +6.0	V
ICH	Continuous Channel Current	128	mA
IIK	Input Clamp Current, VI < 0	-50	mA
TJ	Operating Junction Temperature	-40 to +150	°C
TSTG	Storage Temperature	-65 to +150	°C

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Functional Diagram

NOTE: See load circuit.

EN pin is shorted to Vref_B with an external pull up resistor for gate bias voltage.
Recommend: 200 kΩ



Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vref_A	Reference Voltage, A Port	0.65	4.5	V
Vref_B	Reference Voltage, B Port, when Vref_A >= 1V	Vref_A + 0.6	5.5	V
	Reference Voltage, B Port, when Vref_A < 1V	Vref_A + 0.8	5.5	V
V _{I/O}	Input/Output Voltage	0	5.5	V
V _{EN}	Enable Voltage when Vref_A >= 1V	Vref_A + 0.6	5.5	V
	Enable Voltage when Vref_A < 1V	Vref_A + 0.8	5.5	V
I _{PASS}	Pass Transistor Current	—	64	mA
T _A	Operating Free-Air Temperature	-40	+125	°C

Electrical Characteristics (All typical values are measured at T_A = +25 °C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
Vref_A	A Port Supply Voltage	What if config to be low-voltage side	0.65	—	4.5	V	
Vref_B	B Port Supply Voltage	What if config to be high-voltage side	1.8	—	5.5	V	
V _{IK}	Input Clamping Voltage	I _I = -18mA, V _{EN} = 0	-1.2	—	—	V	
I _L	Leakage Current	Pins An, Bn, Vref_A, Vref_B and EN; V _I = GND to 5.0V	—	1.0	5.0	μA	
I _{CC}	Supply Current	Vref_B = EN = 5.5V, Vref_A = 4.5V, I _O = 0, V _I = 0 or V _{CC}	—	6	—	μA	
C _{IO(off)}	I/O Pin Off-State Capacitance	V _O = 3V or 0, EN = 0	—	5	6	pF	
C _{IO(on)}	I/O Pin On-State Capacitance	V _O = 3V or 0, EN = 3V	—	10	13	pF	
C _{I(Vref_A/B/EN)}	Reference Voltage Pin and Enable Pin Input Capacitance	V _O = 3V or 0	—	10	—	pF	
V _{IL} (EN)	Device Turn-Off Threshold of EN Pin	—	—	—	Vref_A	V	
V _{IH} (EN)	Device Turn-On Threshold of EN Pin	When Vref_A >= 1V. See load circuit.	Vref_A + 0.6	—	5.5	V	
		When Vref_A < 1V. See load circuit.	Vref_A + 0.8	—	5.5	V	
R _{on}	On-State Resistance (Note 5)	V _I = 0, I _O = 64mA	Vref_A = 3.3V; Vref_B = EN = 5V	—	5	—	Ω
			Vref_A = 1.8V; Vref_B = EN = 5V	—	6	—	
			Vref_A = 1.0V; Vref_B = EN = 5V	—	9	—	
		V _I = 0, I _O = 32mA	Vref_A = 1.8V; Vref_B = EN = 5V	—	8	—	Ω
			Vref_A = 2.5V; Vref_B = EN = 5V	—	6	—	
		V _I = 1.8V, I _O = 15mA, Vref_A = 3.3V; Vref_B = EN = 5V	—	8	—	Ω	
		V _I = 1.0V, I _O = 10mA, Vref_A = 1.8V; Vref_B = EN = 3.3V	—	14	—	Ω	
		V _I = 0, I _O = 10mA, Vref_A = 1.0V; Vref_B = EN = 3.3V	—	10	—	Ω	
		V _I = 0, I _O = 10mA, Vref_A = 1.0V; Vref_B = EN = 1.8V	—	12	—	Ω	
		V _I = 0, I _O = 10mA, Vref_A = 0.65V; Vref_B = EN = 1.5V	—	15	—	Ω	

Note: 5. Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

Translating Down Switching Characteristics (T_A = +25°C, unless otherwise specified.) (Note 6)

Translating Down, 5.0V to 1.8V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50pF	C _L = 30pF	C _L = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	B	A	0.4	0.3	0.2	ns
t _{PHL}			1.0	0.7	0.5	ns
Test Conditions: Vref_A = 1.8V, VPU = VIH = 5.0V, VM = 2.15V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 3.3V to 1.8V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50pF	C _L = 30pF	C _L = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	B	A	0.4	0.3	0.2	ns
t _{PHL}			1.0	0.7	0.5	ns
Test Conditions: Vref_A = 1.8V, VPU = VIH = 3.3V, VM = 1.15V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 3.3V to 1.2V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50pF	C _L = 30pF	C _L = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	B	A	0.6	0.4	0.2	ns
t _{PHL}			1.1	0.8	0.6	ns
Test Conditions: Vref_A = 1.2V, VPU = VIH = 3.3V, VM = 0.85V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.8V to 1.2V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50pF	C _L = 30pF	C _L = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	B	A	0.8	0.5	0.3	ns
t _{PHL}			1.6	1.4	1.1	ns
Test Conditions: Vref_A = 1.2V, VPU = VIH = 1.8V, VM = 0.65V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.8V to 0.8V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50pF	C _L = 30pF	C _L = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	B	A	0.8	0.5	0.3	ns
t _{PHL}			1.6	1.2	1.0	ns
Test Conditions: Vref_A = 0.8V, VPU = VIH = 1.8V, VM = 0.55V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.5V to 0.65V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50pF	C _L = 30pF	C _L = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	B	A	1.0	0.6	0.4	ns
t _{PHL}			1.9	1.5	1.1	ns
Test Conditions: Vref_A = 0.65V, VPU = VIH = 1.5V, VM = 0.4V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Note: 6. All typical values are measured at T_A = +25°C. Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz; Z_O = 50Ω. Definitions test circuit: C_L = load capacitance including jig and probe capacitance; R_L = load resistance = 300Ω; R_{PU} = ext. pullup resistance = 200kΩ.

Translating Up Switching Characteristics (T_A = +25°C, unless otherwise specified.) (Note 6)

Translating Up, 1.8V to 5.0V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL = 50pF	CL = 30pF	CL = 15pF	UNIT
			Typ	Typ	Typ	
tPLH	A	B	0.4	0.3	0.3	ns
tPHL			1.9	1.4	1.0	ns
Test Conditions: VIH = Vref_A = 1.8V, VEXT = VPU = 5.0V, RL = 300Ω, VM = 2.05V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 1.8V to 3.3V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL = 50pF	CL = 30pF	CL = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	A	B	0.4	0.3	0.3	ns
t _{PHL}			1.9	1.4	1.0	ns
Test Conditions: V _{IH} = V _{ref_A} = 1.8V, V _{EXT} = V _{PU} = 3.3V, R _L = 300Ω, V _M = 0.9V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 1.2V to 3.3V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL = 50pF	CL = 30pF	CL = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	A	B	0.4	0.3	0.2	ns
t _{PHL}			3.2	2.4	1.6	ns
Test Conditions: V _{IH} = V _{ref_A} = 1.2V, V _{EXT} = V _{PU} = 3.3V, R _L = 300Ω, V _M = 0.75V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 1.2V to 1.8V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL = 50pF	CL = 30pF	CL = 15pF	UNIT
			Typ	Typ	Typ	
tPLH	A	B	0.6	0.3	0.2	ns
tPHL			2.8	2.2	1.6	ns
Test Conditions: VIH = Vref_A = 1.2V, VEXT = VPU = 1.8V, RL = 300Ω, VM = 0.6V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 0.8V to 1.8V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL = 50pF	CL = 30pF	CL = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	A	B	0.6	0.3	0.2	ns
t _{PHL}			3.7	2.9	2.1	ns
Test Conditions: V _{IH} = V _{ref_A} = 0.8V, V _{EXT} = V _{PU} = 1.8V, R _L = 300Ω, V _M = 0.55V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 0.65V to 1.5V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50pF	C _L = 30pF	C _L = 15pF	UNIT
			Typ	Typ	Typ	
t _{PLH}	A	B	0.7	0.3	0.2	ns
t _{PHL}			5.0	3.8	2.7	ns
Test Conditions: V _{IH} = Vref_A = 0.65V, V _{EXT} = V _{PU} = 1.8V, R _L = 300Ω, V _M = 0.4V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Note: 6. All typical values are measured at T_A = +25°C. Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz; Z_O = 50Ω. Definitions test circuit: C_L = load capacitance including jig and probe capacitance; R_L = load resistance = 300Ω; R_{PU} = ext. pullup resistance = 200kΩ.

Parameter Measurement Information

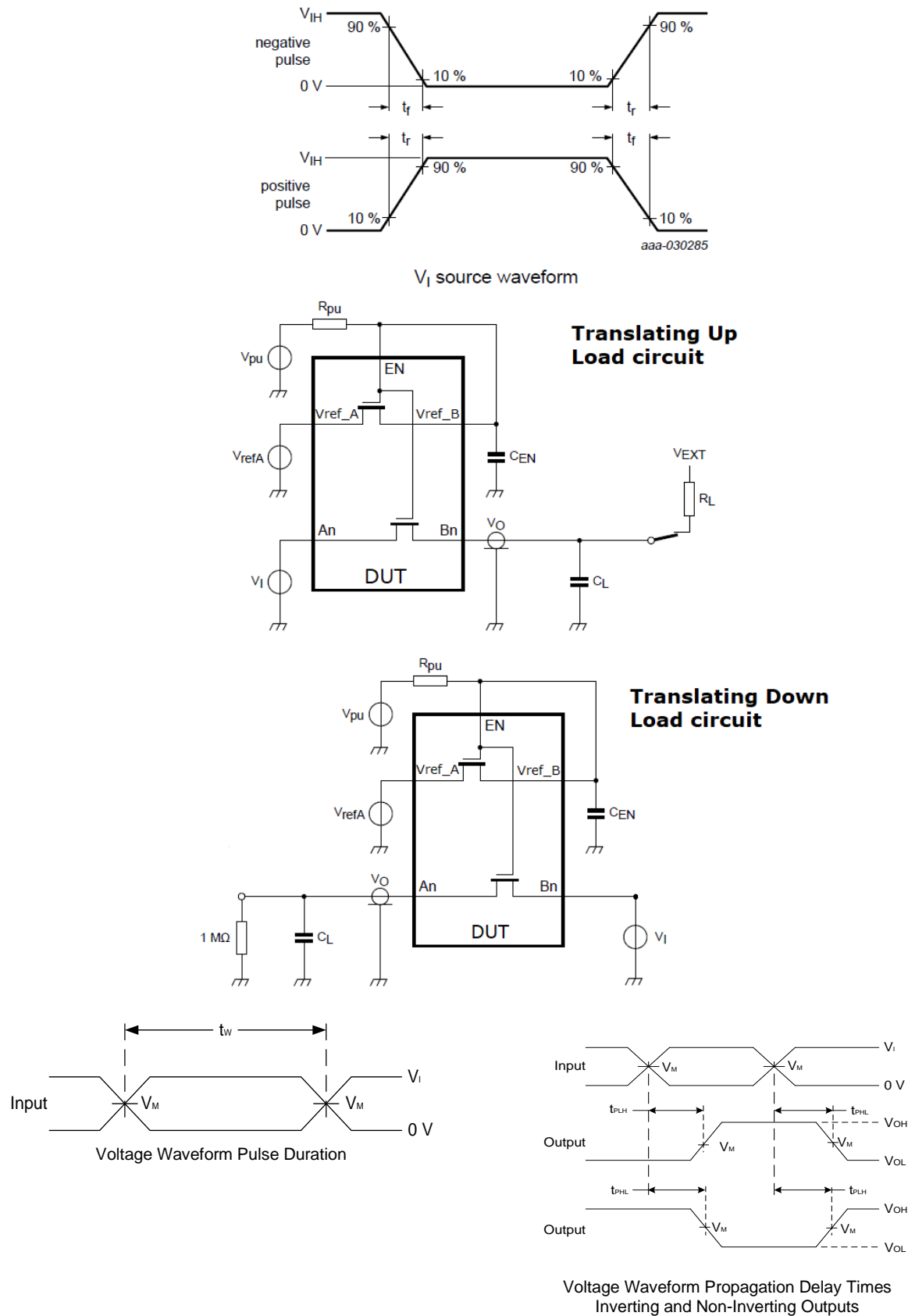


Figure 1. Load Circuit and Voltage Waveforms, $R_{PU} = 200k\Omega$, $C_{EN} = 0.1\mu F$, $R_L = 300\Omega$, $C_L = 15pF, 30pF, 50pF$

Application Circuit Information

I2C or I3C protocol typically occurs in a modern application as shown in Figure 2. For the I2C or I3C voltage translation up or down, consideration should be taken for I3C because it is using higher speeds, which require careful design and attention to signal integrity to ensure reliable communication.

Since I3C uses open-drain mode when necessary for compatibility of I2C, but switches to push-pull outputs whenever possible. The existing I2C devices can be connected to an I3C bus but still have the bus able to switch to a higher data rate for communication at higher speeds between compliant I3C devices. Always refer to the I3C specifications and device datasheets for detailed information and recommendations to ensure reliable communication. Especially at higher speeds, which involve proper PCB layout, termination resistors, and cable selection based on your specific application requirements.

- Standard data rate (SDR): this is the default mode of I3C and operates at 11Mbps or 12.5Mbps.
- High data rate (HDR): this mode of I3C supports speeds up to 25Mbps where it is further enhanced to reach up to 33Mbps.
- Voltage levels: I3C supports a variety of voltage levels including 1.8V, 2.5V, 3.3V, and 5V.
- Output type: I3C utilizes both open-drain and push-pull outputs for SCL, offering flexibility for different voltage level combinations.
- Rise time and fall time: I3C defines minimum rise and fall times for the SCL signal to ensure proper signal integrity at different speeds.
- SCL is a conventional digital clock signal, driven with a push-pull output by the current bus controller during data transfers. When communication with known I3C targets occurs, the bus controller may switch to a higher frequency and/or alter the duty cycle.
- SDA carries the serial data stream, which may be driven by either a controller or target, but is driven at a rate determined by the controller's SCL signal. For compatibility with the I2C protocol, each transaction begins with SDA operating as an open-drain output, which limits the transmission speed. For messages addressed to an I3C target, the SDA driver mode switches to push-pull after the first few bits in the transaction, allowing the clock to be further increased.

Therefore, this presents a challenge with LSF0102 for I3C because the LSF0102 relies on a pullup resistor to translate the voltage up from the low-voltage side. The pullup resistor selected shall be not only strong enough to meet the timing requirements, but also not so strong that it violates the V_{IL} requirements of the I3C devices. So, the pullup resistors are needed on both sides for the normal translation setup. This means that the pullup resistors are required to pull the bus voltage on the high-voltage side from V_{PU_1} to V_{PU_2} .

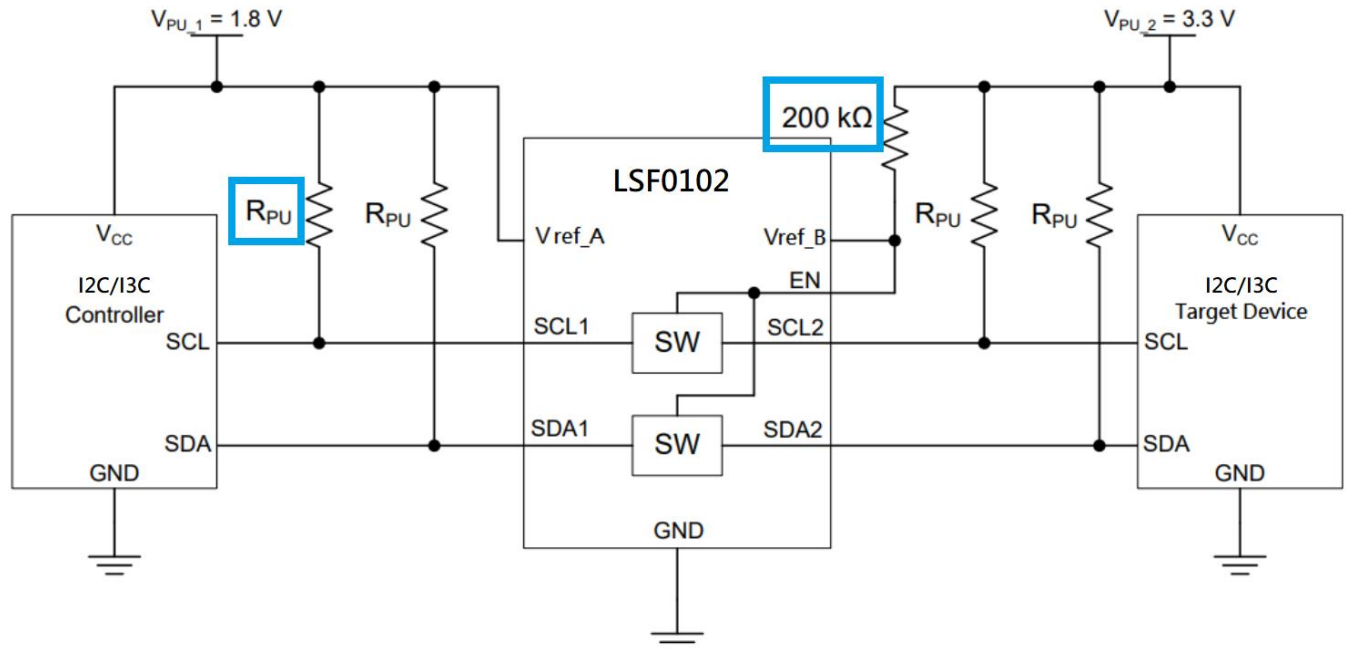


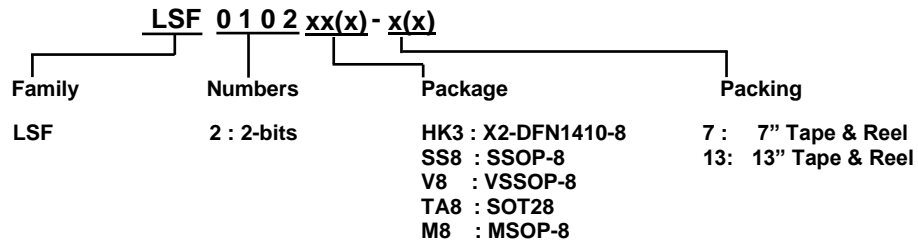
Figure 2. Typical Application Circuit for I2C or I3C Bus Voltage Translation

Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	X2-DFN1410-8	(Note 7)	—	235	—	°C/W
		SSOP-8		—	202	—	
		VSSOP-8		—	185	—	
		SOT28		—	225	—	
		MSOP-8		—	158	—	
θ_{JC}	Thermal Resistance Junction-to-Case	X2-DFN1410-8	(Note 7)	—	158	—	
		SSOP-8		—	52	—	
		VSSOP-8		—	54	—	
		SOT28		—	121	—	
		MSOP-8		—	32	—	

Note: 7. Test condition for each of the 3 package types: Device mounted on JEDEC standard PCB per JESD51, with minimum recommended pad layout.

Ordering Information



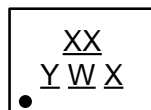
Orderable Part Number	Part Number Suffix	Package Code	Package	Packing (Note 8)	
				Qty.	Carrier
LSF0102HK3-7	-7	HK3	X2-DFN1410-8	5000	7" Tape and Reel
LSF0102SS8-7	-7	SS8	SSOP-8	3000	7" Tape and Reel
LSF0102V8-7	-7	V8	VSSOP-8	3000	7" Tape and Reel
LSF0102TA8-7	-7	TA8	SOT28	3000	7" Tape and Reel
LSF0102M8-13	-13	M8	MSOP-8	2500	13" Tape and Reel

Note: 8. The taping orientation is located on our website at <https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf>.

Marking Information

(1) X2-DFN1410-8

(Top View)



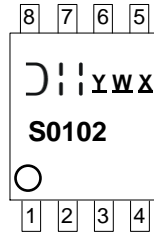
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
LSF0102HK3-7	X2-DFN1410-8	J8

Marking Information (continued)

(2) SSOP-8

(Top View)

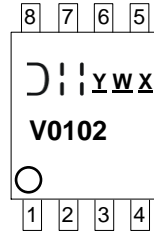


Y : Year : 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Packaging	Identification Code
LSF0102SS8-7	SSOP-8	S0102

(3) VSSOP-8

(Top View)

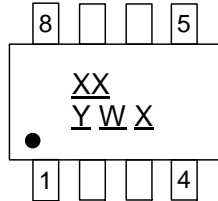


Y : Year : 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
LSF0102V8-7	VSSOP-8	V0102

(4) SOT28

(Top View)

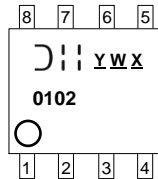


XX : Identification Code
Y : Year 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
LSF0102TA8-7	SOT28	J8

(5) MSOP-8

(Top View)



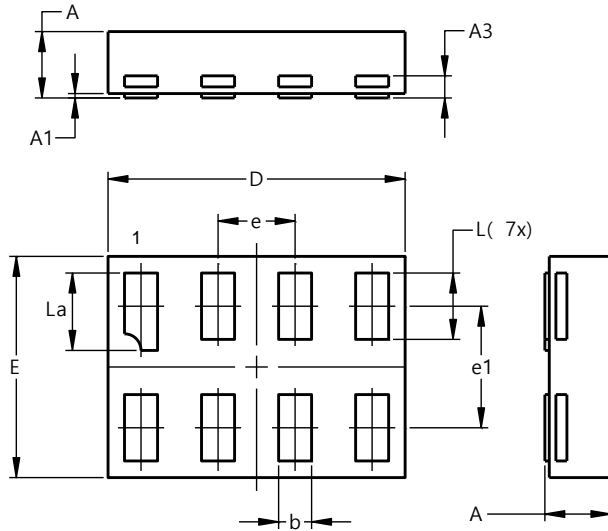
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
LSF0102M8-13	MSOP-8	0102

Package Outline Dimensions

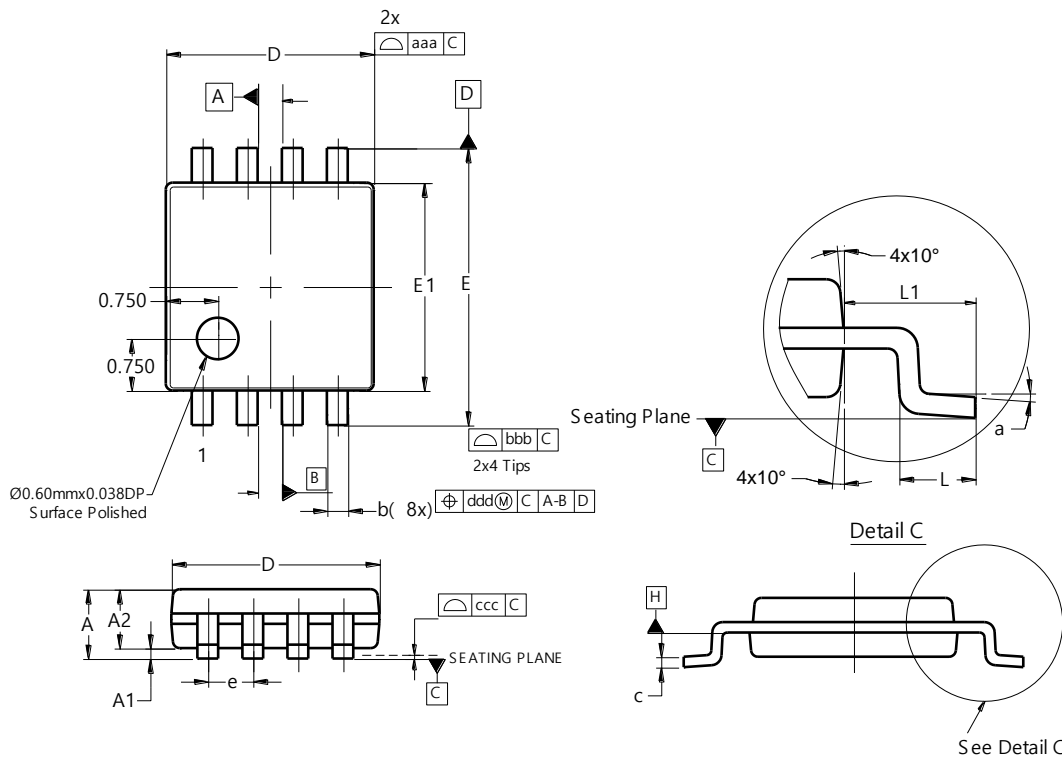
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) X2-DFN1410-8



X2-DFN1410-8			
Dim	Min	Max	Typ
A	0.30	0.35	0.33
A1	0.00	0.03	0.02
A3	--	--	0.10
b	0.12	0.20	0.15
D	1.30	1.40	1.35
E	0.95	1.05	1.00
e	--	--	0.35
e1	--	--	0.55
L	0.27	0.35	0.30
L1	0.32	0.40	0.35
All Dimensions in mm			

(2) SSOP-8

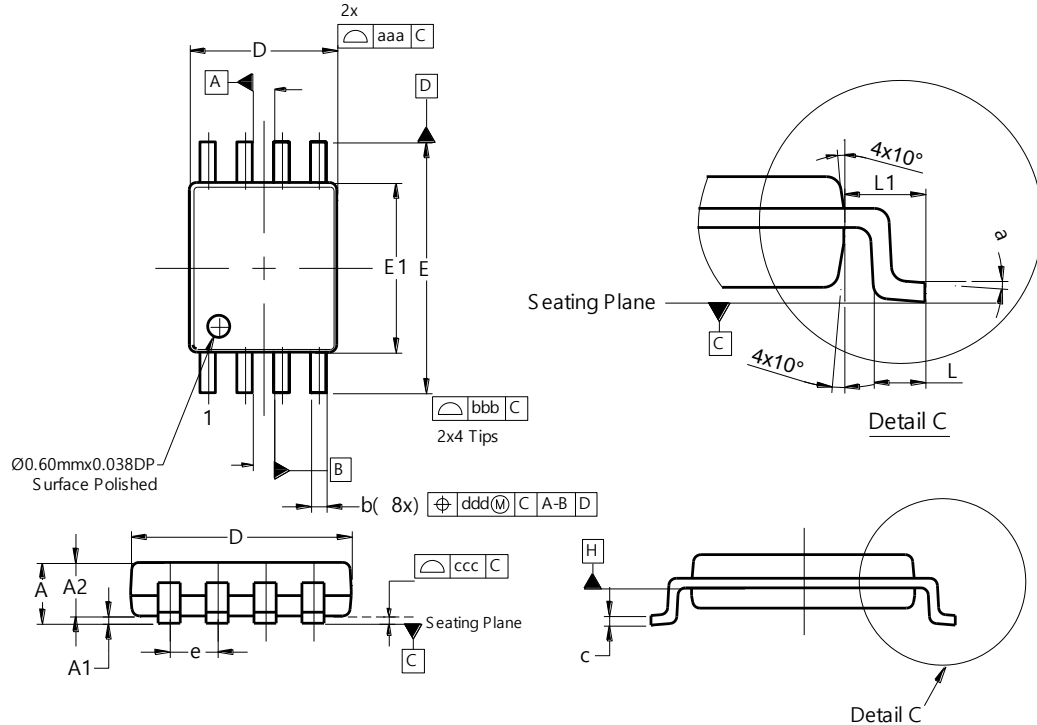


SSOP-8			
Dim	Min	Max	Typ
A	--	1.30	--
A1	0.05	0.15	--
A2	0.95	1.20	1.05
b	0.15	0.30	0.225
c	0.08	0.23	--
D	2.75	3.15	2.95
E	3.75	4.25	4.00
E1	2.70	2.90	2.80
e	--	--	0.65
L	0.20	0.60	0.40
L1	0.525	0.675	0.60
a	0°	8°	4°
aaa	0.20		
bbb	0.25		
ccc	0.10		
ddd	0.13		
All Dimensions in mm			

Package Outline Dimensions (continued)

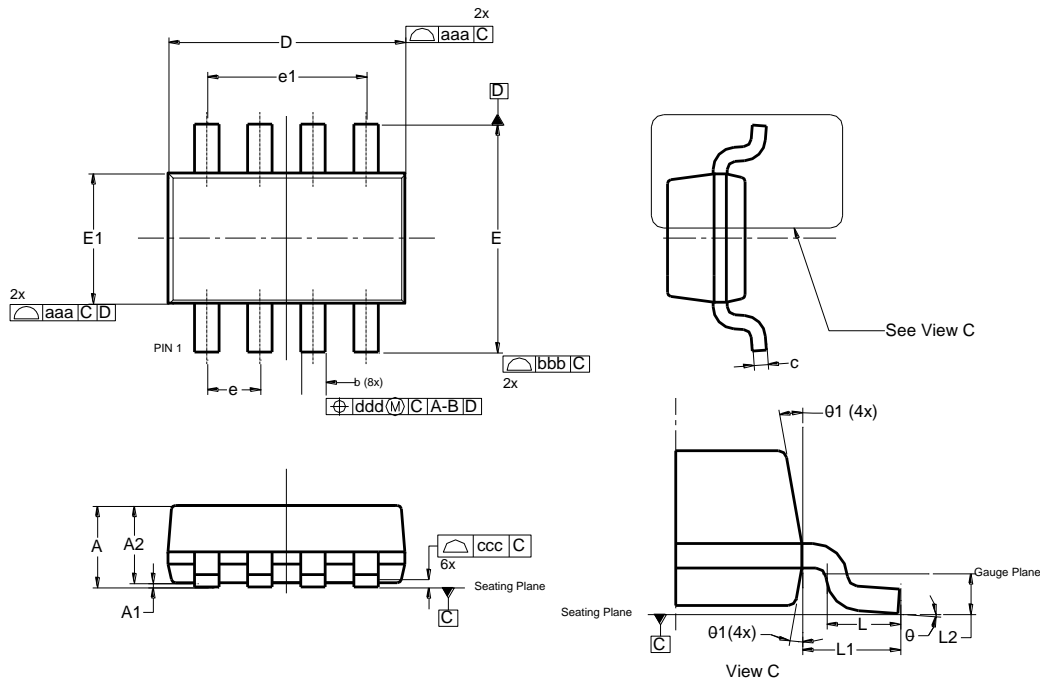
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(3) VSSOP-8



VSSOP-8			
Dim	Min	Max	Typ
A	0.60	0.90	--
A1	--	0.10	--
A2	0.60	0.80	--
b	0.17	0.25	0.21
c	0.08	0.13	--
D	1.90	2.10	2.00
E	3.20	3.60	3.40
E1	2.20	2.40	2.30
e	--	--	0.50
L	0.30	0.40	0.35
L1	0.50	0.60	0.55
a	0°	6°	3°
aaa	0.20		
bbb	0.25		
ccc	0.10		
ddd	0.13		
All Dimensions in mm			

(4) SOT28

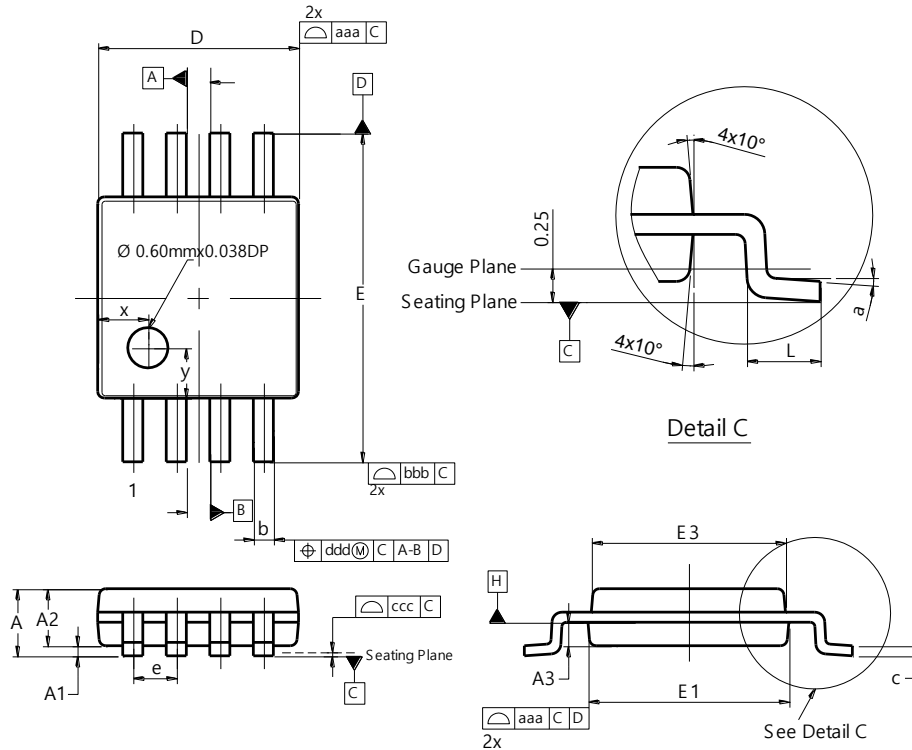


SOT28			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.10	--
A2	--	--	0.95
b	0.20	0.40	0.30
c	0.08	0.20	--
D	2.85	2.95	2.90
E	2.65	2.95	2.80
E1	1.55	1.65	1.60
e	0.65 BSC		
e1	1.95 BSC		
L	0.30	0.60	0.45
L1	0.60 REF		
L2	0.25 BSC		
θ	0°	8°	--
θ1	9°	11°	10°
aaa	0.15		
bbb	0.25		
ccc	0.10		
ddd	0.20		
All Dimensions in mm			

Package Outline Dimensions (continued)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(5) MSOP-8

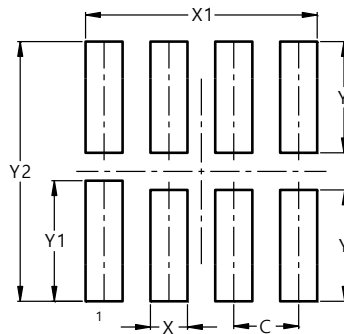


MSOP-8			
Dim	Min	Max	Typ
A	--	1.10	--
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E3	2.85	3.05	2.95
e	--	--	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	--	--	0.750
y	--	--	0.750
aaa	0.20		
bbb	0.25		
ccc	0.10		
ddd	0.13		
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) X2-DFN1410-8

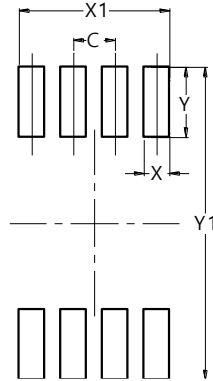


Dimensions	Value (in mm)
C	0.350
X	0.200
X1	1.250
Y	0.600
Y1	0.650
Y2	1.400

Suggested Pad Layout (continued)

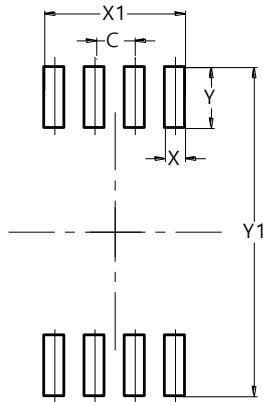
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(2) SSOP-8



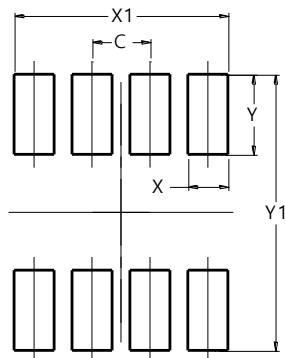
Dimensions	Value (in mm)
C	0.650
X	0.400
X1	2.350
Y	1.100
Y1	4.900

(3) VSSOP-8



Dimensions	Value (in mm)
C	0.500
X	0.250
X1	1.750
Y	0.750
Y1	4.050

(4) SOT28

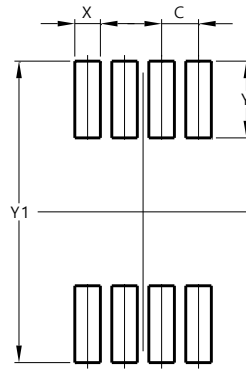


Dimensions	Value (in mm)
C	0.950
G	1.600
X	0.700
Y	0.900
Y1	3.400

Suggested Pad Layout (continued)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(5) MSOP-8



Dimensions	Value (in mm)
C	0.650
X	0.450
Y	1.350
Y1	5.300

Mechanical Data

X2-DFN1410-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.004 grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

SSOP-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.018 grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

VSSOP-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.018 grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

SOT28

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.018 grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

MSOP-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.025 grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

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