

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _C = +25°C (Note 4)
40V	7.6mΩ @ V _{GS} = 10V	100A

Description

This new generation n-channel enhancement mode MOSFET is designed to minimize R_{DS(ON)} yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switches.

Applications

- Power management
- DC-DC converters
- Motor controls

Features

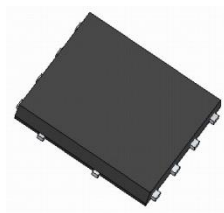
- Rated to +175°C – Ideal for High Ambient Temperature Environments
- Thermally Efficient Package-Cooler Running Applications
- High-Conversion Efficiency
- Low R_{DS(ON)} – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- < 1.1mm Package Profile – Ideal for Thin Applications
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. “Green” Device (Note 3)**
- This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.**
<https://www.diodes.com/quality/product-definitions/>
- An automotive-compliant part is available under separate datasheet ([DMTH4007SPSQ](#))**

Mechanical Data

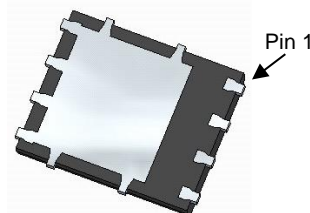
- Package: PowerDI[®]5060-8
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.097 grams (Approximate)

Site 1:

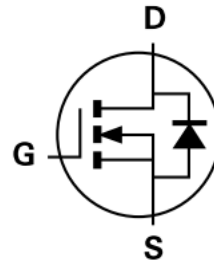
PowerDI5060-8



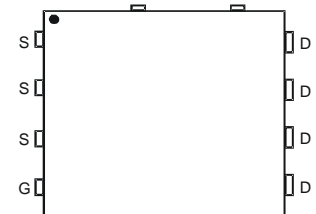
Top View



Bottom View



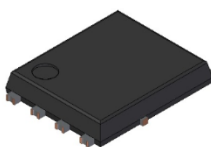
Internal Schematic



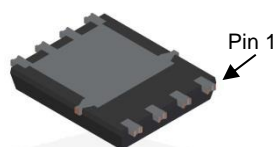
Top View
Pin Configuration

Site 2:

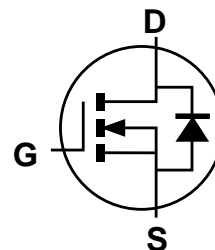
PowerDI5060-8/SWP (Type UX)



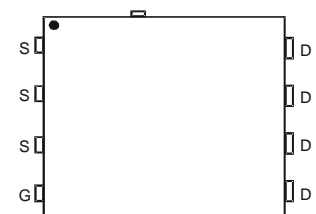
Top View



Bottom View



Internal Schematic



Top View
Pin Configuration

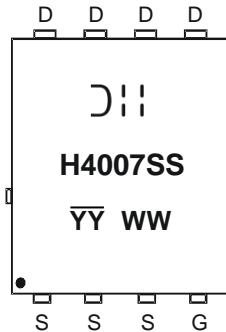
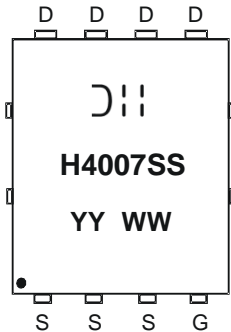
- Notes:
- EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 - See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 - Package limited.


Ordering Information (Note 5)

Part Number	Package	Packing	
		Qty.	Carrier
DMTH4007SPS-13	PowerDI5060-8	2,500	Tape & Reel
	PowerDI5060-8/SWP (Type UX)	2,500	Tape & Reel

Note: 5. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



 = Manufacturer's Marking
 H4007SS = Product Type Marking Code
 YYWW = Date Code Marking
 YY or YY = Last Two Digits of Year (ex: 23 = 2023)
 WW = Week Code (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V _{DSS}	40	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (Note 6)	T _A = +25°C T _A = +70°C	I _D	15.7 13.1	A
Continuous Drain Current (Note 7)	T _C = +25°C (Note 4)	I _D	100	A
	T _C = +100°C		77	
Maximum Continuous Body Diode Forward Current (Note 7)		I _S	100	A
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)		I _{DM}	200	A
Avalanche Current, L = 0.3mH		I _{AS}	20	A
Avalanche Energy, L = 0.3mH		E _{AS}	60	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P _D	2.8	W
Thermal Resistance, Junction to Ambient (Note 6)	R _{θJA}	53	°C/W
Total Power Dissipation (Note 7)	P _D	136	W
Thermal Resistance, Junction to Case (Note 7)	R _{θJC}	1.1	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +175	°C

Notes: 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
 7. Thermal resistance from junction to soldering point (on the exposed drain pad).

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	40	—	—	V	V _{GS} = 0V, I _D = 1mA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 32V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	2	—	4	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	4.9	7.6	mΩ	V _{GS} = 10V, I _D = 20A
Diode Forward Voltage	V _{SD}	—	—	1.2	V	V _{GS} = 0V, I _S = 20A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	2,082	—	pF	V _{DS} = 25V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	790	—		
Reverse Transfer Capacitance	C _{rss}	—	113	—		
Gate Resistance	R _g	—	0.46	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _g	—	41.9	—	nC	V _{DS} = 30V, I _D = 20A, V _{GS} = 10V
Gate-Source Charge	Q _{gs}	—	10	—		
Gate-Drain Charge	Q _{gd}	—	11.5	—		
Turn-On Delay Time	t _{D(ON)}	—	7	—	ns	V _{DD} = 30V, V _{GS} = 10V I _D = 20A, R _g = 3Ω
Turn-On Rise Time	t _R	—	11.5	—		
Turn-Off Delay Time	t _{D(OFF)}	—	15.6	—		
Turn-Off Fall Time	t _F	—	8.8	—	ns	I _F = 20A, dI/dt = 100A/μs
Body Diode Reverse Recovery Time	t _{RR}	—	29.9	—		
Body Diode Reverse Recovery Charge	Q _{RR}	—	23	—	nC	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

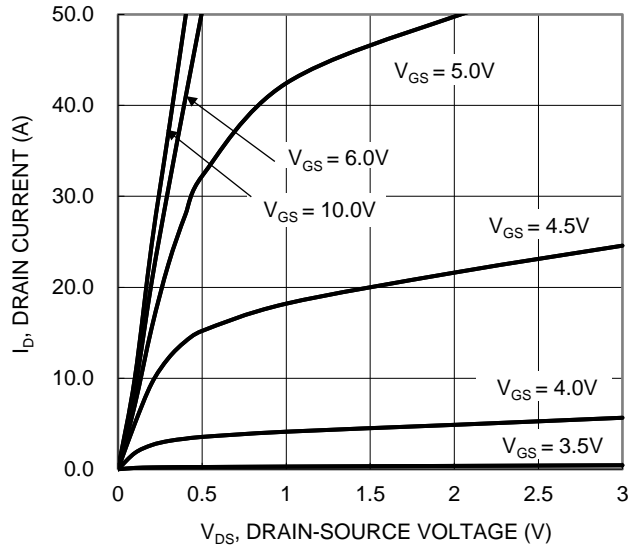


Figure 1. Typical Output Characteristic

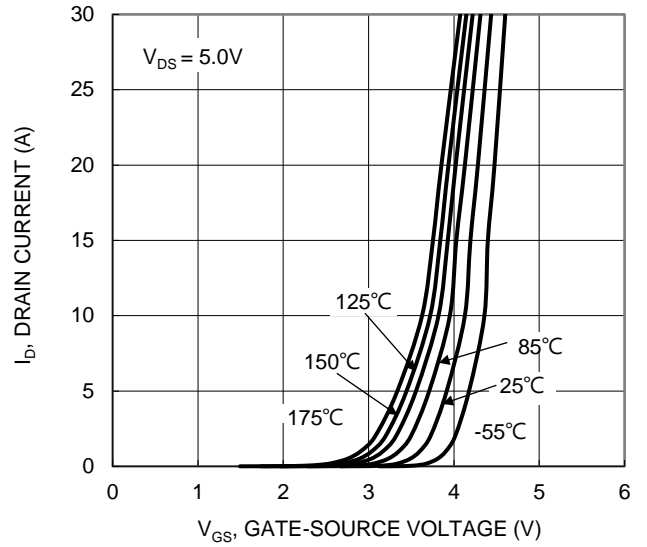


Figure 2. Typical Transfer Characteristic

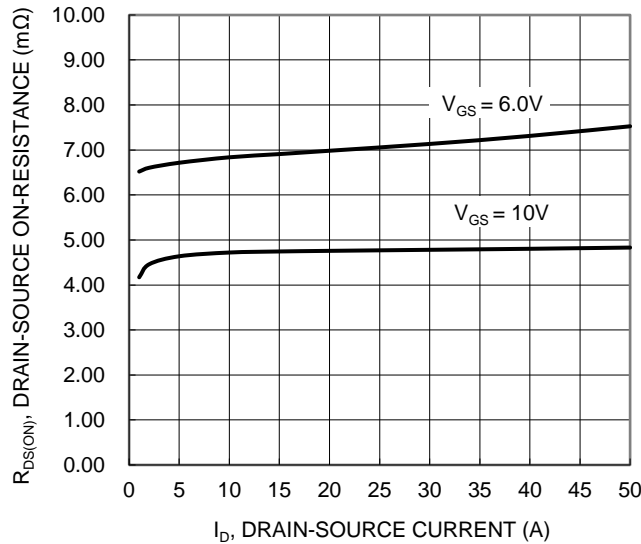


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

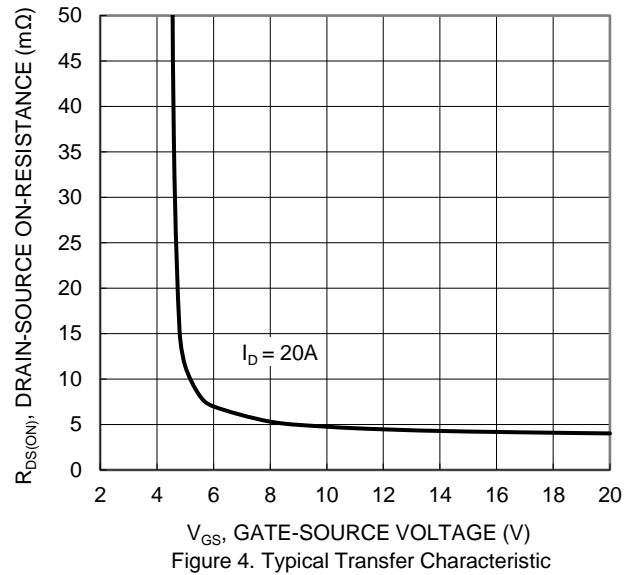


Figure 4. Typical Transfer Characteristic

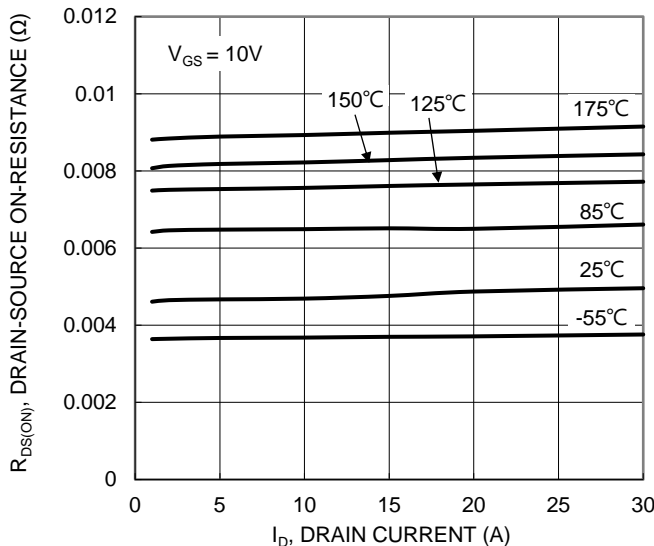


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

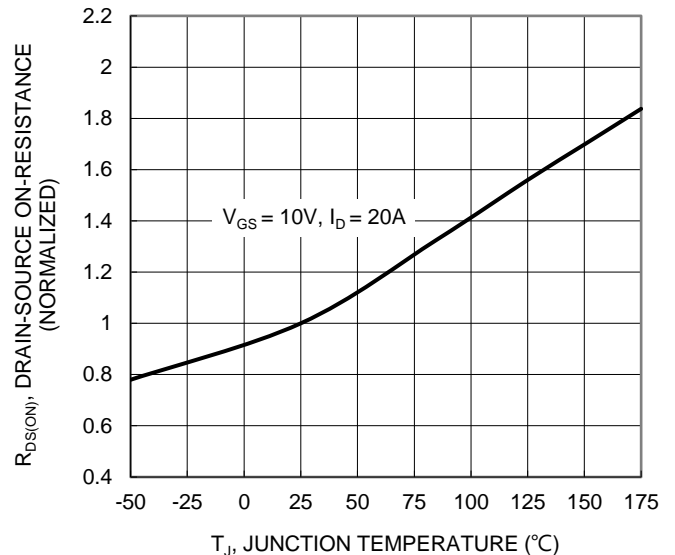


Figure 6. On-Resistance Variation with Temperature

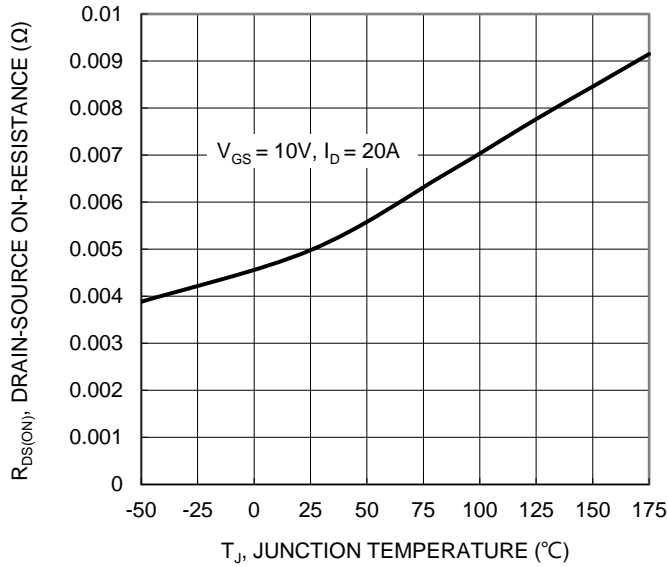


Figure 7. On-Resistance Variation with Temperature

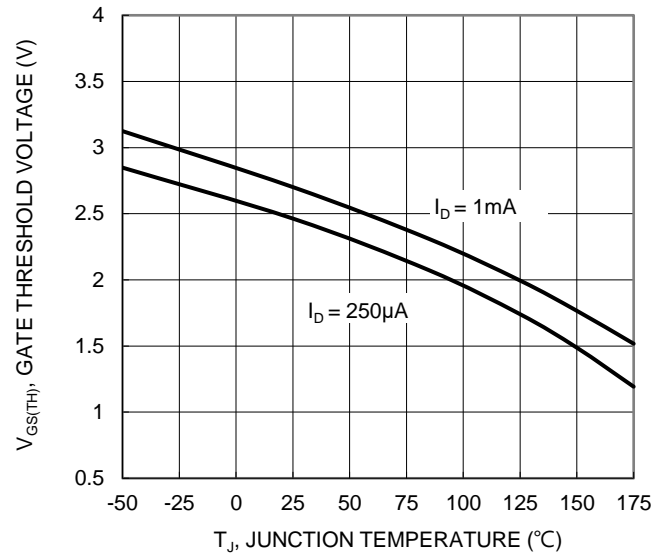


Figure 8. Gate Threshold Variation vs. Temperature

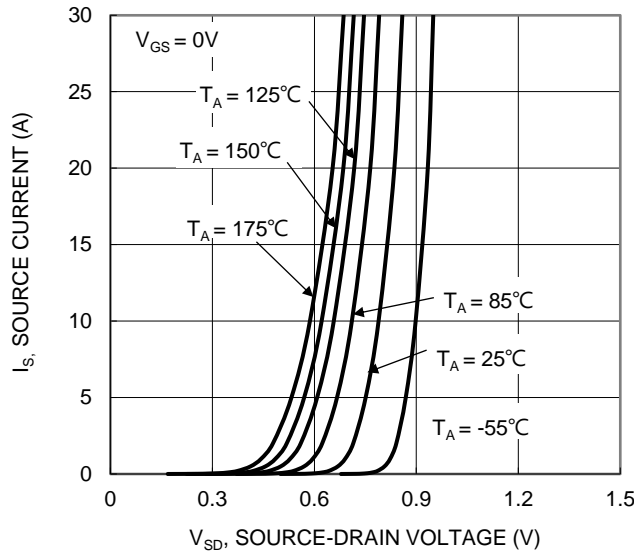


Figure 9. Diode Forward Voltage vs. Current

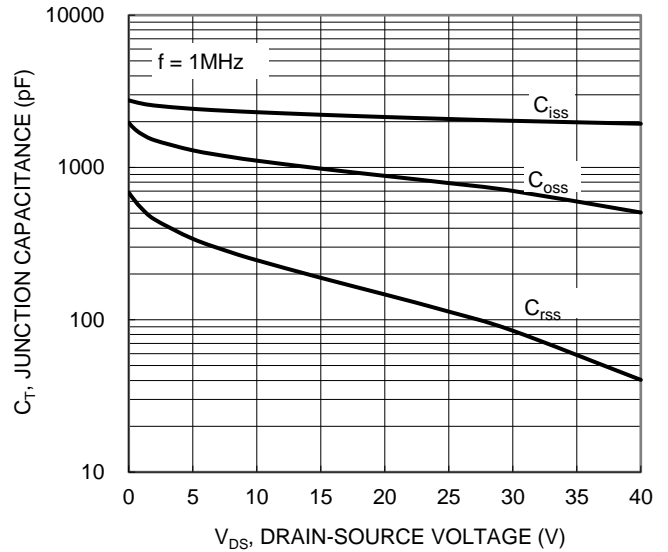


Figure 10. Typical Junction Capacitance

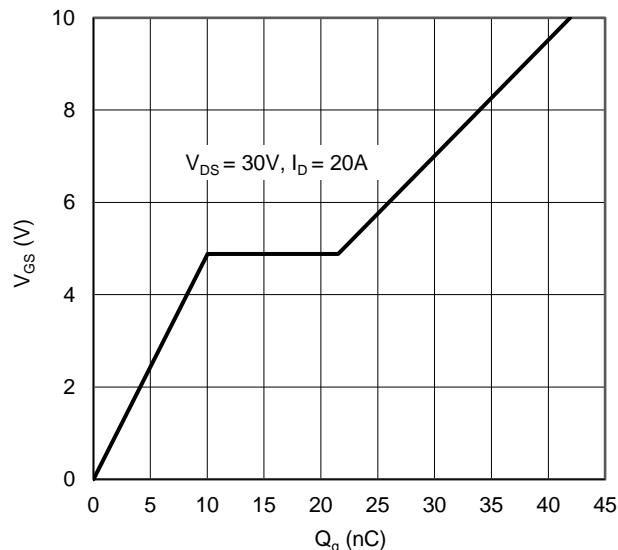


Figure 11. Gate Charge

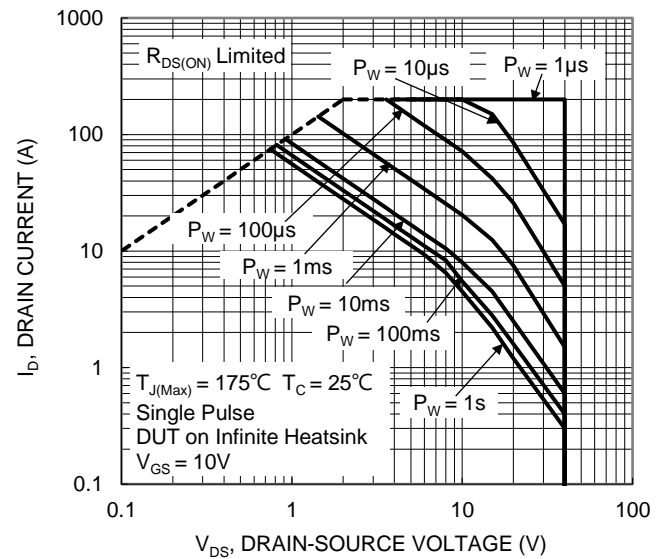


Figure 12. SOA, Safe Operation Area

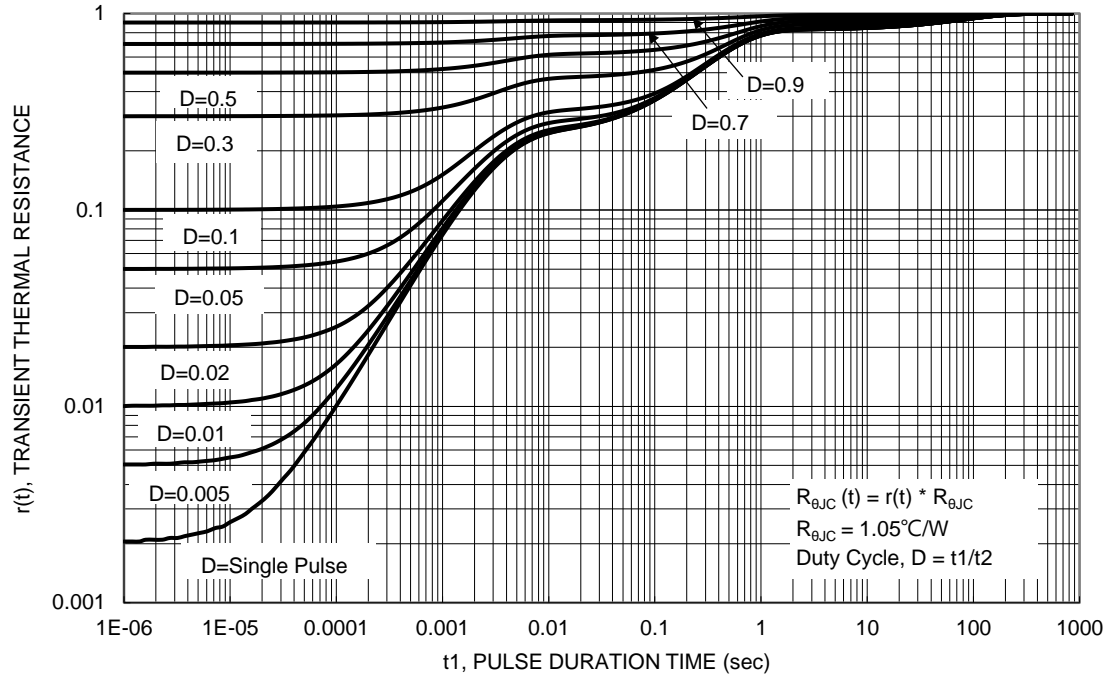
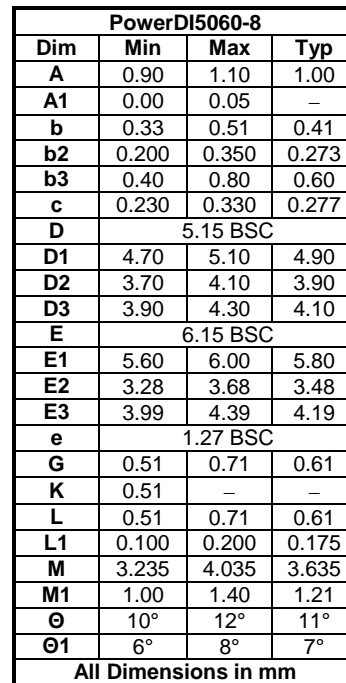


Figure 13. Transient Thermal Resistance

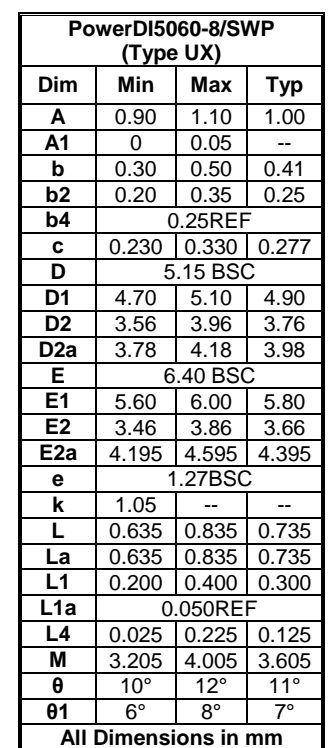
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

Site 1:

PowerDI5060-8



Site 2:

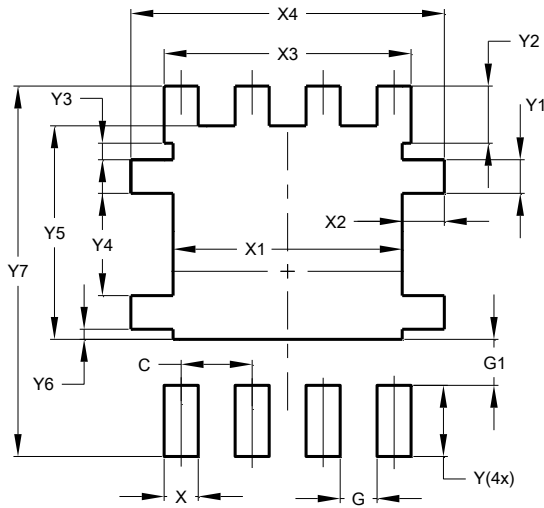
PowerDI5060-8/SWP (Type UX)

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

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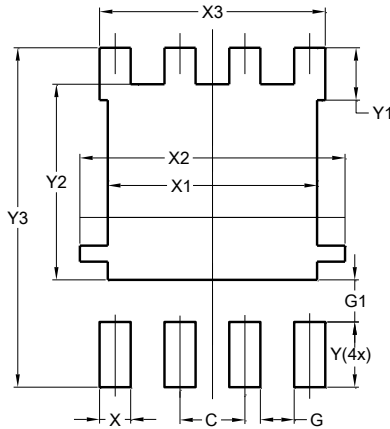
PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

Site 2:

PowerDI5060-8/SWP (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	5.190
X3	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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