



150V N-CHANNEL ENHANCEMENT MODE MOSFET PowerDI5060-8

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _C = +25°C	
150V	66mΩ @ V _{GS} = 10V	24A	

Features and Benefits

- 100% Unclamped Inductive Switching (UIS) Test in Production –
 Ensures More Reliable and Robust End Application
- Thermally Efficient Package-Cooler Running Applications
- Low Rds(ON) Minimizes On-State Losses
- Low Q_g Minimizes Switching Losses
- < 1.1mm Package Profile Ideal for Thin Applications (PowerDI[®])
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The DMT15H053SPSWQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.

https://www.diodes.com/quality/product-definitions/

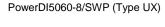
Description and Applications

This new generation MOSFET features low on-resistance and fast switching, making it ideal for high-efficiency power-management applications.

- Power-management functions
- DC-DC converters
- Backlighting

Mechanical Data

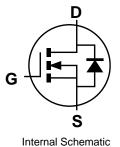
- Package: PowerDI5060-8
- Package Material: Molded Plastic, "Green" Molding Compound UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminals: Finish Matte Tin Annealed over Copper Lead-Frame.
 Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.097 grams (Approximate)

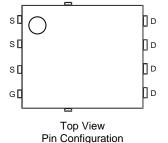






Top View Bottom View





Ordering Information (Note 4)

Part Number	Paskaga	Packing		
Part Number	Package	Qty.	Carrier	
DMT15H053SPSWQ-13	PowerDI5060-8/SWP (Type UX)	2,500	Tape & Reel	

Notes:

- 1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.



Marking Information



Dil = Manufacturer's Marking
T1553SW = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 23 = 2023)
WW = Week Code (01 to 53)

Maximum Ratings (@ T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	150	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Dunin Courset V	Steady State	Tc = +25°C		24	Δ.
Continuous Drain Current V _{GS} = 10V (Note 5)		$T_C = +25^{\circ}C$ $T_C = +70^{\circ}C$	ID	19	А
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			lдм	96	Α
Maximum Continuous Body Diode Forward Current (Note 5)			Is	24	Α
Pulsed Body Diode Current (10µs Pulse, Duty Cycle = 1%)			Іѕм	96	Α
Avalanche Current, L = 1mH			las	11.7	Α
Avalanche Energy, L = 1mH			E _{AS}	68.4	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)	T _A = +25°C	PD	1.9	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	Reja	65	°C/W
Total Power Dissipation (Note 7)	T _A = +25°C	PD	3.3	W
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	R _{0JA}	38	°C/W
Total Power Dissipation (Note 5)	Tc = +25°C	PD	90	W
Thermal Resistance, Junction to Case (Note 5)		Rejc	1.4	1.4
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

Notes:

- 5. Thermal resistance from junction to soldering point (on the exposed drain pad).
- 6. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
- 7. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.



Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BV _{DSS}	150	_	_	V	V _G S = 0V, I _D = 10mA	
Zero Gate Voltage Drain Current	IDSS	-	_	1	μA	V _{DS} = 120V, V _{GS} = 0V	
Gate-Source Leakage	Igss	1	_	±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	Vgs(th)	2	3.2	4	>	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance	R _{DS(ON)}	_	46	66	mΩ	V _{GS} = 10V, I _D = 20A	
Diode Forward Voltage	V _{SD}	1	0.9	1	V	$V_{GS} = 0V, I_{S} = 20A$	
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance	Ciss		814			$V_{DS} = 75V$, $V_{GS} = 0V$ f = 1MHz	
Output Capacitance	Coss		84		pF		
Reverse Transfer Capacitance	Crss		3.7				
Gate Resistance	Rg	_	0.6	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge	Qg	-	11.5	_		75)/ 1 444	
Gate-Source Charge	Qgs	1	4.6	_	nC	$V_{DS} = 75V, I_{D} = 4.1A$ $V_{GS} = 10V$	
Gate-Drain Charge	Q_{gd}	1	2.8	_		vG3 = 10v	
Turn-On Delay Time	tD(ON)	1	5.7	_		$V_{DS} = 75V, V_{GS} = 10V$ $I_{D} = 4.1A, R_{g} = 6\Omega$	
Turn-On Rise Time	t _R	_	17.7	_	20		
Turn-Off Delay Time	tD(OFF)		15.7	_	ns		
Turn-Off Fall Time	tF		12.7				
Reverse Recovery Time	trr	_	47	_	ns	I= - 4.1	
Reverse Recovery Charge	Q _{RR}	_	87	_	nC	I _F = 4.1A, di/dt = 100A/μs	

Notes:

^{8.} Short duration pulse test used to minimize self-heating effect. 9. Guaranteed by design. Not subject to product testing.





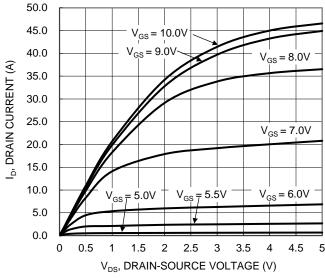


Figure 1. Typical Output Characteristic

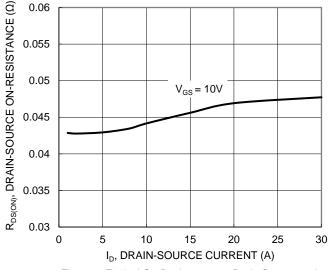


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

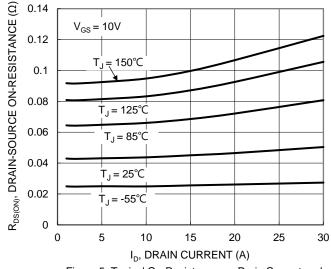


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

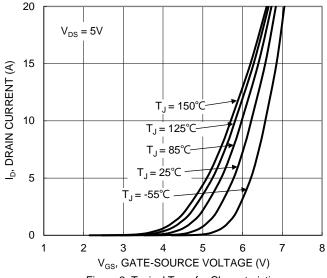


Figure 2. Typical Transfer Characteristic

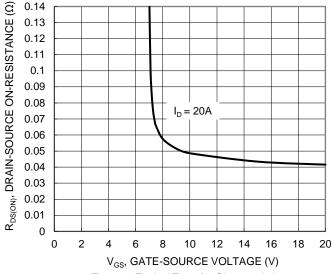


Figure 4. Typical Transfer Characteristic

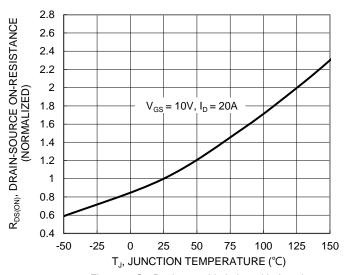


Figure 6. On-Resistance Variation with Junction Temperature





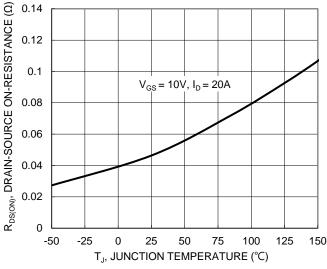


Figure 7. On-Resistance Variation with Junction Temperature

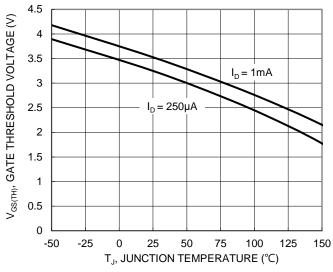


Figure 8. Gate Threshold Variation vs. Junction Temperature

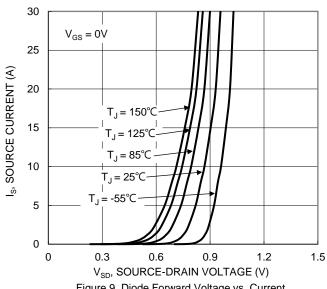
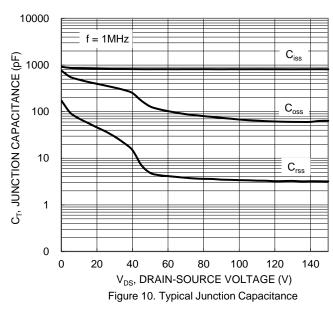


Figure 9. Diode Forward Voltage vs. Current



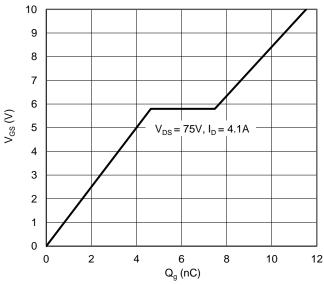


Figure 11. Gate Charge

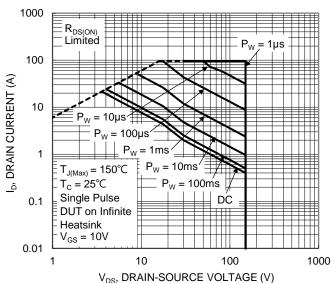


Figure 12. SOA, Safe Operation Area



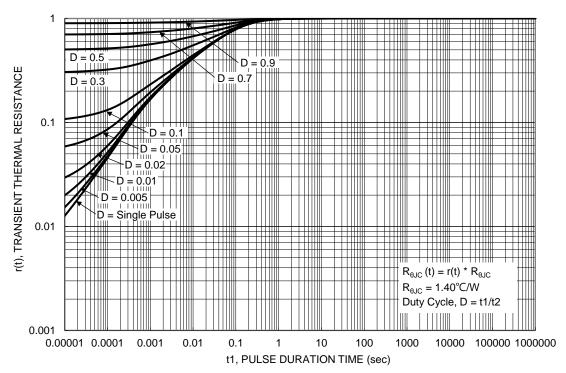


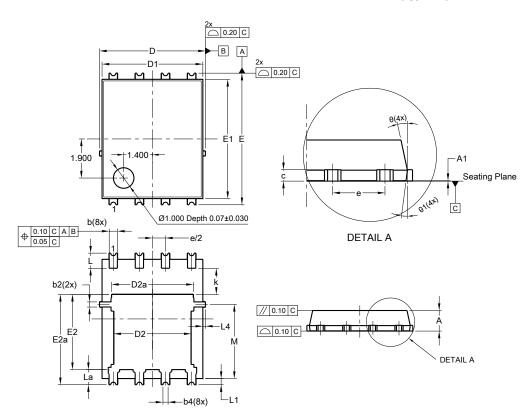
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8/SWP (Type UX)

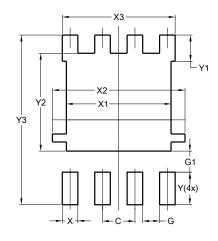


PowerDI5060-8/SWP (Type UX)					
Dim	Min	Max	Тур		
Α	0.90	1.10	1.00		
A1	0	0.05			
b	0.30	0.50	0.41		
b2	0.20	0.35	0.25		
b4	C).25REF			
С	0.230	0.330	0.277		
D	5	.15 BS0	2		
D1	4.70	5.10	4.90		
D2	3.56	3.96	3.76		
D2a	3.78	4.18	3.98		
Е	6	.40 BS0	3		
E1	5.60	6.00	5.80		
E2	3.46	3.86	3.66		
E2a	4.195	4.595	4.395		
е	1.27BSC				
k	1.05				
L	0.635	0.835	0.735		
La	0.635	0.835	0.735		
L1	0.200	0.400	0.300		
L4	0.025	0.225	0.125		
M	3.205	4.005	3.605		
θ	10°	12°	11°		
θ1	6°	8°	7°		
All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8/SWP (Type UX)



Dimensions	Value (in mm)		
С	1.270		
G	0.660		
G1	0.820		
X	0.610		
X1	4.100		
X2	5.190		
Х3	4.420		
Y	1.270		
Y1	1.020		
Y2	3.810		
Y3	6.610		



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