

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D $T_A = +25^\circ C$
-60V	150m Ω @ $V_{GS} = -10V$	-3A
	185m Ω @ $V_{GS} = -4.5V$	-2.7A

Description

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Motor Control
- Transformer Driving Switch
- DC-DC Converters
- Power Management Functions
- Uninterrupted Power Supply

Features and Benefits

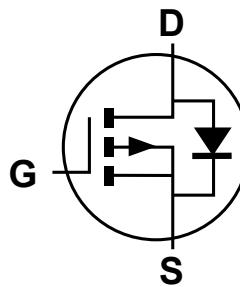
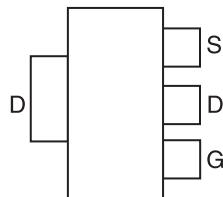
- 100% Unclamped Inductive Switch (UIS) test in production
- Low on-resistance
- Fast switching speed
- **Lead-Free Finish; RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SOT223
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 
- Weight: 0.112 grams (approximate)



Top View



Equivalent Circuit

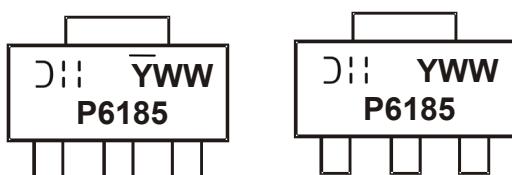
Ordering Information (Note 4)

Part Number	Qualification	Case	Packaging
DMP6185SE-13	Standard	SOT223	2,500 / Tape & Reel

Notes:

1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



DII = Manufacturer's Marking

P6185 = Marking Code

YWW = Date Code Marking for SAT (Shanghai Assembly/ Test site)

YWW = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Y or Y= Year (ex: 3 = 2013)

WW = Week (01 - 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source voltage	V_{DSS}	-60	V
Gate-Source voltage	V_{GS}	± 20	V
Continuous Drain current (Note 6) $V_{GS} = -10\text{V}$	I_D	-3	A
$T_A = +70^\circ\text{C}$		-2.4	
Maximum Body Diode Continuous Current	I_S	-2	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)	I_{DM}	-15	A
Single Pulsed Avalanche Current (Note 7)	I_{AS}	-16	A
Single Pulsed Avalanche Energy (Note 7)	E_{AS}	13	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	1.2	W
$T_A = +70^\circ\text{C}$		0.8	
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	104	°C/W
$t < 10\text{s}$		51	
Total Power Dissipation (Note 6)	P_D	2.2	W
$T_A = +70^\circ\text{C}$		1.4	
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	60	°C/W
$t < 10\text{s}$		30	
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	7.6	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-60	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -48\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(\text{th})}$	-1	—	-3	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	110	150	$\text{m}\Omega$	$V_{GS} = -10\text{V}, I_D = -2.2\text{A}$
			130	185		$V_{GS} = -4.5\text{V}, I_D = -1.8\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.75	-0.95	V	$V_{GS} = 0\text{V}, I_S = -1\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	708	—	pF	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	39	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	32	—	pF	
Gate Resistance	R_g	—	17	28	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = -4.5\text{V}$)	Q_g	—	6.2	—	nC	$V_{DS} = -30\text{V}, I_D = -12\text{A}$
Total Gate Charge ($V_{GS} = -10\text{V}$)	Q_g	—	14	—	nC	
Gate-Source Charge	Q_{gs}	—	2.8	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.1	—	nC	
Turn-On Delay Time	$t_{D(\text{on})}$	—	5.2	—	ns	$V_{DS} = -30\text{V}, R_L = 2.5\Omega$
Turn-On Rise Time	t_r	—	23	—	ns	
Turn-Off Delay Time	$t_{D(\text{off})}$	—	33	—	ns	
Turn-Off Fall Time	t_f	—	39	—	ns	
Body Diode Reverse Recovery Time	t_{rr}	—	22	—	ns	$I_F = -12\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{rr}	—	17	—	nC	

Notes:

- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
- Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
- UIS in production with $L = 0.1\text{mH}$, starting $T_A = +25^\circ\text{C}$.
- Short duration pulse test used to minimize self-heating effect.
- Guaranteed by design. Not subject to product testing.

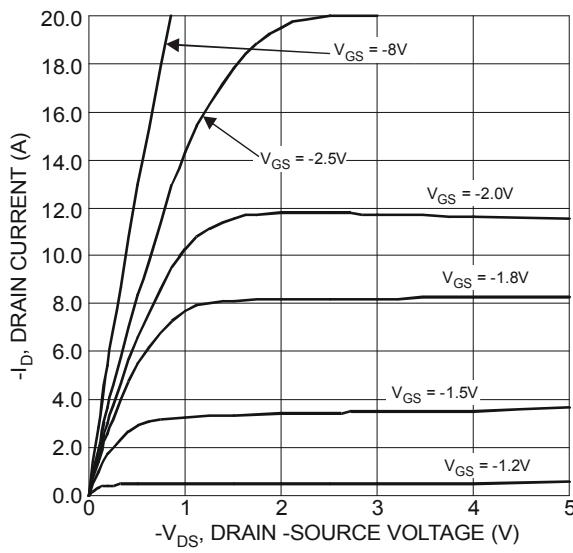


Figure 1 Typical Output Characteristics

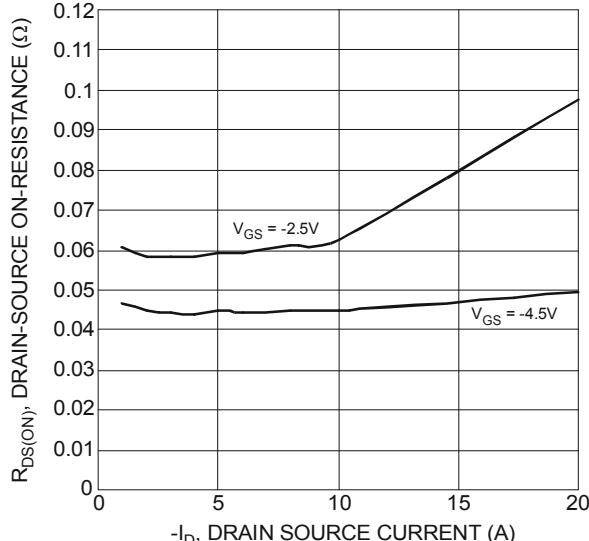


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

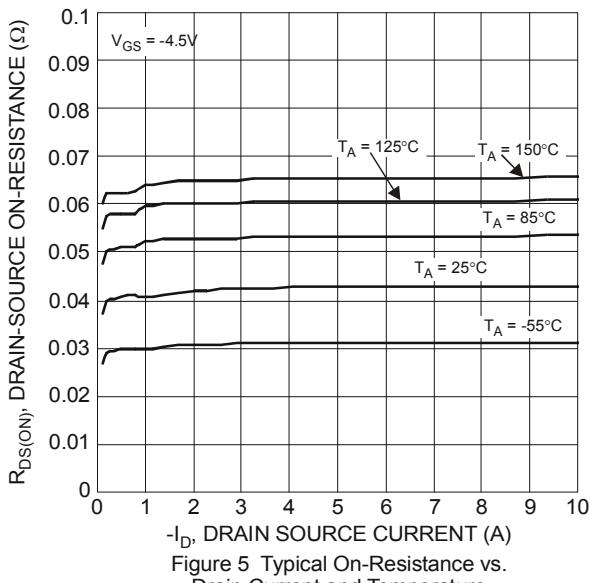


Figure 5 Typical On-Resistance vs.
Drain Current and Temperature

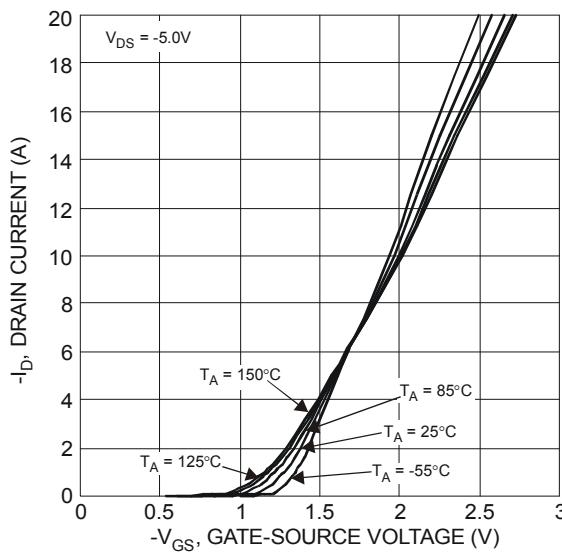


Figure 2 Typical Transfer Characteristics

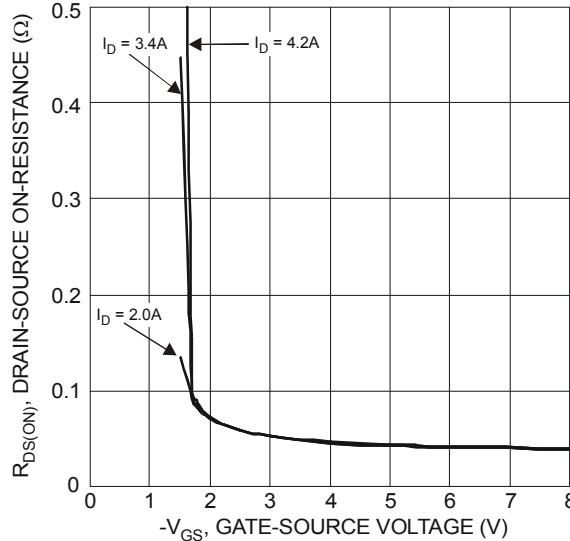


Figure 4 Typical Transfer Characteristics

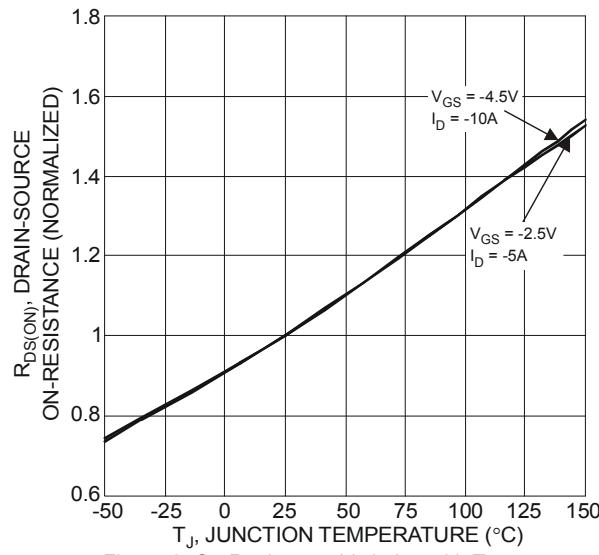
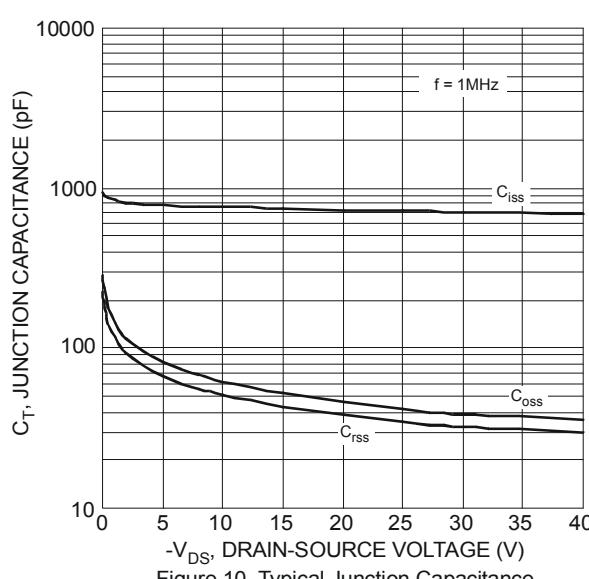
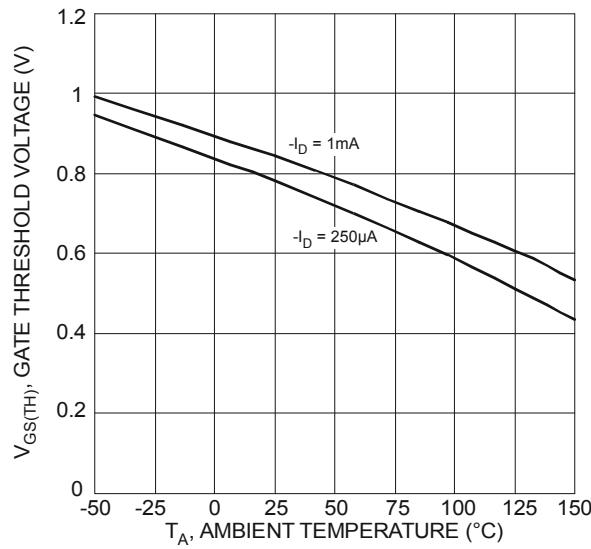
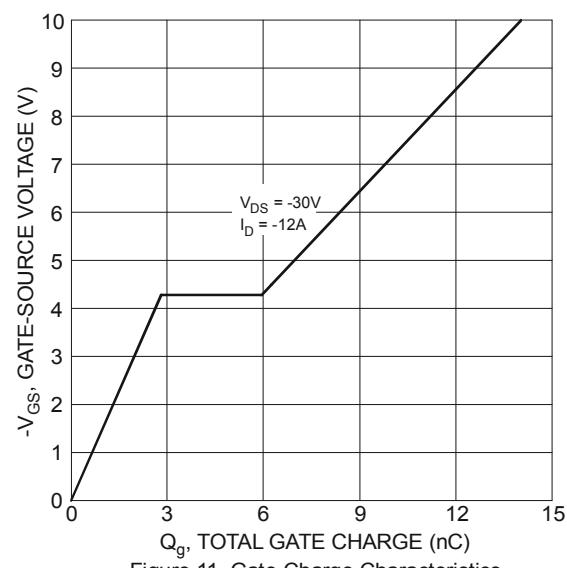
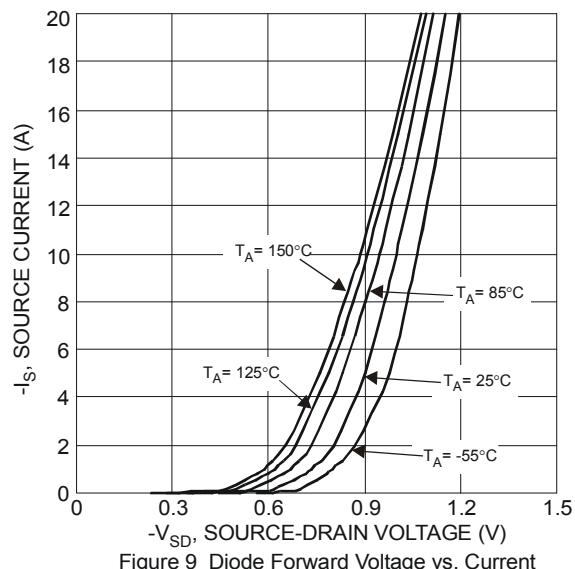
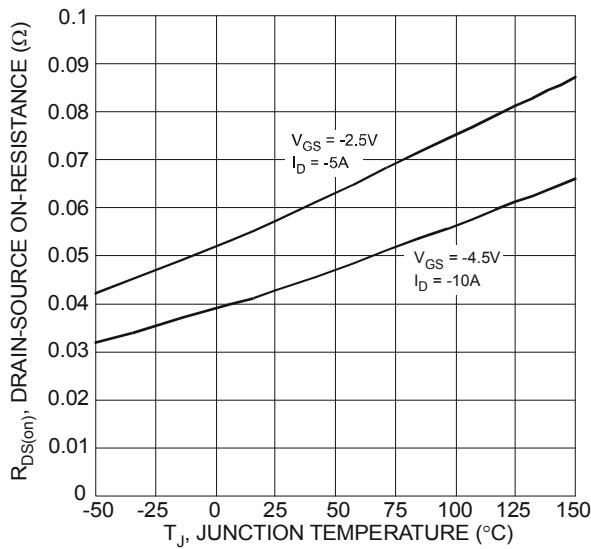
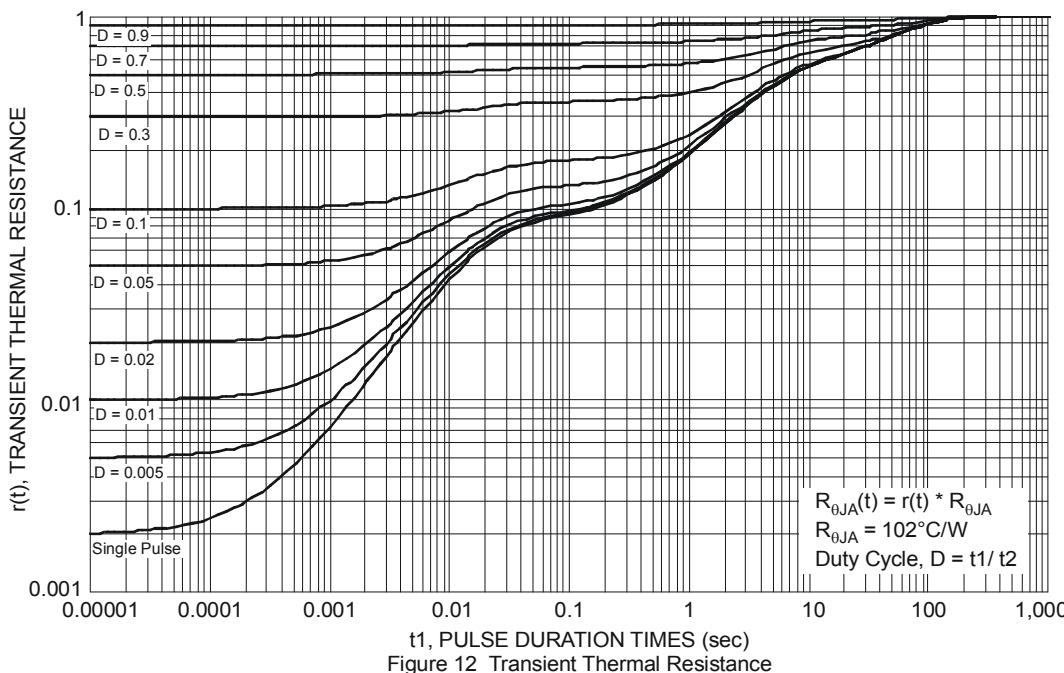


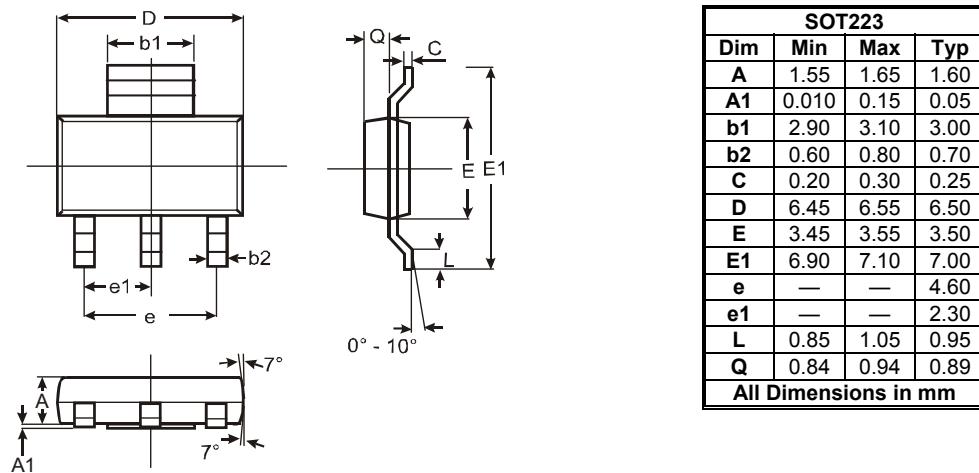
Figure 6 On-Resistance Variation with Temperature





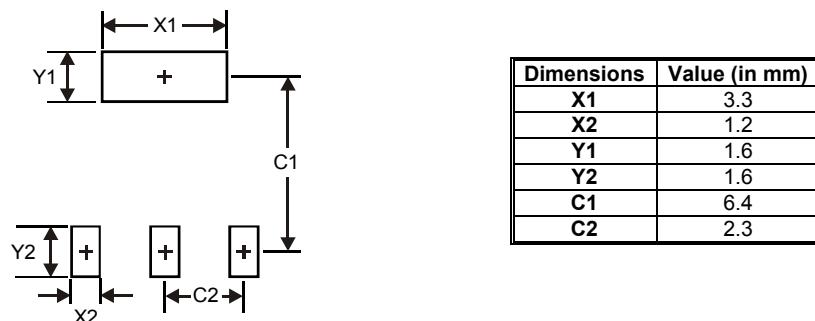
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



Suggested Pad Layout

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