Product Summary

V_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
-8V	9.9mΩ @ V_{GS} = -4.5V	-10A

Description

This new generation Lateral MOSFET (LD-MOS) is designed to minimize on-state losses and switch ultra-fast, making it ideal for high-efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal $R_{DS(ON)}$ per footprint area.

Applications

- Battery protections
- Battery managements
- Load switches

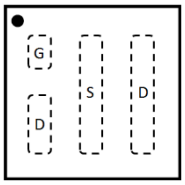
Features

- LD-MOS Technology with the Lowest Figure of Merit:
  - $R_{DS(ON)}$ = 9.9mΩ to Minimize On-State Losses
  - Q_g = 7.0nC for Ultra-Fast Switching
- $V_{GS(TH)}$ = -0.80V typ. for a Low Turn-On Potential
- CSP with Footprint 1.2mm × 1.2mm
- Height = 0.35mm for Low Profile
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

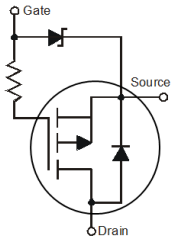
Mechanical Data

- Package: X2-DSN1212-4
- Terminal Connections: See Diagram Below
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Material: Finish – NiAu. Solderable per MIL-STD-202, Method 208e4
- Weight: 0.00092 grams (Approximate)

X2-DSN1212-4
(Note 4)



Top-View
Pin Configuration



Equivalent Circuit

Ordering Information (Note 5)

Part Number	Package	Packing	
		Qty.	Carrier
DMP1010UCA4-7	X2-DSN1212-4	3,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Device with exposed silicon sidewall is non-isolated area.
5. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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Marking Information

X2-DSN1212-4

FA = Product Type Marking Code
YW = Date Code Marking
Y or $\overline{Y}$ = Year (ex: 3 = 2023)
W or $\overline{W}$ = Week (ex: a = Week 27; z Represents Week 52 and 53)

Date Code Key

Year	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034
Code	3	4	5	6	7	8	9	0	1	2	3	4

Week	1-26	27-52	53
Code	A-Z	a-z	z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-8	V
Gate-Source Voltage			V_{GSS}	-6	V
Continuous Drain Current (Note 6) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-6 -4.8	A
Continuous Drain Current (Note 7) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-10 -8	A
Pulsed Drain Current (Pulse Duration 10µs, Duty Cycle ≤1%)			I_{DM}	-60	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P_D	0.63	W
Total Power Dissipation (Note 7)	P_D	1.75	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	200.0	°C/W
Thermal Resistance, Junction to Ambient (Note 7)	$R_{\theta JA}$	71.7	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-8	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current @T_C = +25°C	I_{DSS}	—	—	-1	µA	V_{DS} = -6.4V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	-100	nA	V_{GS} = -6.0V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.4	-0.80	-1.05	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	8.4	9.9	mΩ	V_{GS} = -4.5V, I_D = -1A
			11.6	15		V_{GS} = -2.5V, I_D = -1A
			17.2	40		V_{GS} = -1.8V, I_D = -1A
			30	—		V_{GS} = -1.5V, I_D = -0.2A
Diode Forward Voltage (Note 7)	V_{SD}	—	-0.66	-1	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	699	—	pF	V_{DS} = -4V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	463	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	109	—	pF	
Series Gate Resistance	R_G	—	21.5	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (-4.5V)	Q_g	—	7.0	—	nC	V_{DS} = -4.0V, I_D = -1A
Gate-Source Charge	Q_{gs}	—	1.0	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.0	—	nC	
Gate Charge at V_{TH}	$Q_{g(th)}$	—	0.7	—	nC	
Output Charge	$Q_{g(OSS)}$	—	2.2	—	nC	V_{DS} = -4.0V, V_{GS} = 0V
Turn-On Delay Time	$t_{D(ON)}$	—	17.5	—	ns	V_{DS} = -4V, V_{GS} = -4.5V, I_D = -1A, R_G = 0Ω
Turn-On Rise Time	t_R	—	4.6	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	46.0	—	ns	
Turn-Off Fall Time	t_F	—	17.5	—	ns	
Reverse Recovery Charge	Q_{RR}	—	5.7	—	nC	V_{DS} = -4V, I_F = -1A, di/dt = 200A/µs
Reverse Recovery Time	t_{RR}	—	17.6	—	ns	

Notes: 6. Device mounted on FR-4 PCB with minimum recommended pad layout.
7. Device mounted on FR-4 material with 1-inch^2 (6.45cm^2), 2oz (0.071mm thick) Cu.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

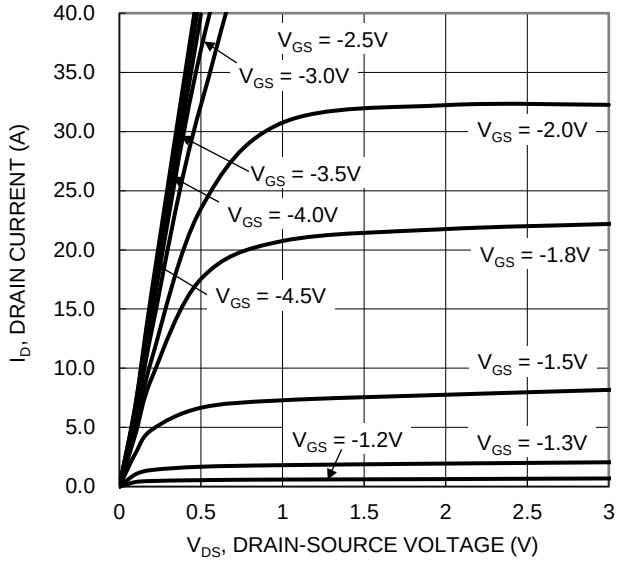


Figure 1. Typical Output Characteristic

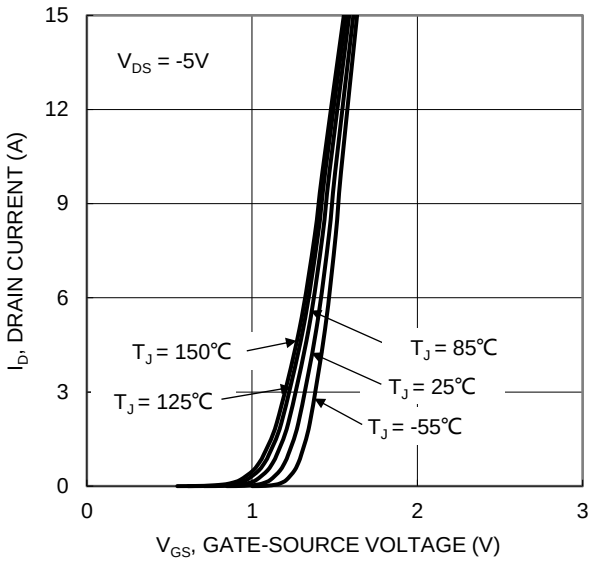


Figure 2. Typical Transfer Characteristic

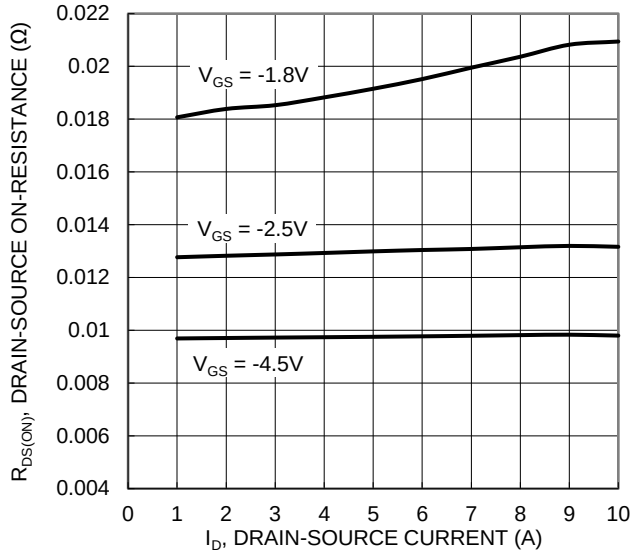


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

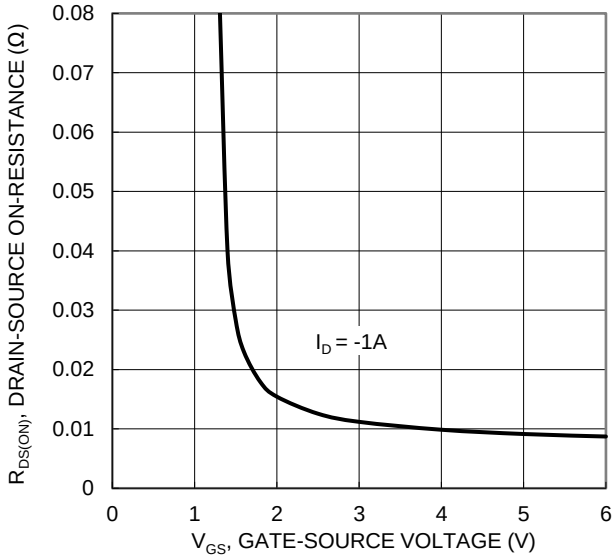


Figure 4. Typical Transfer Characteristic

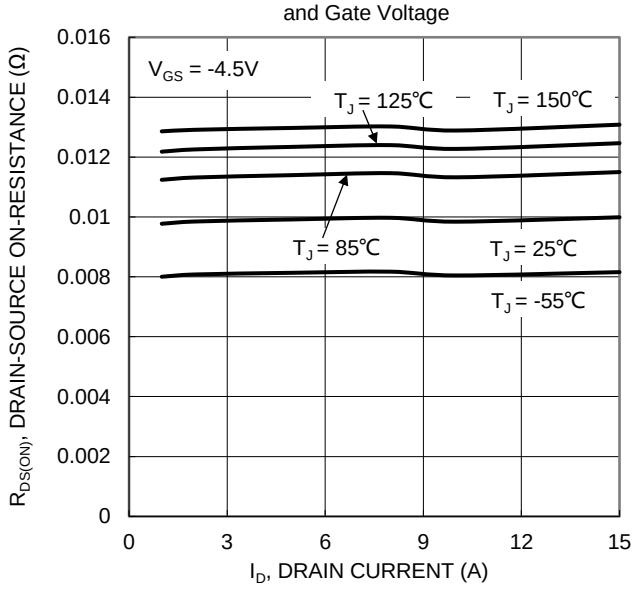


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

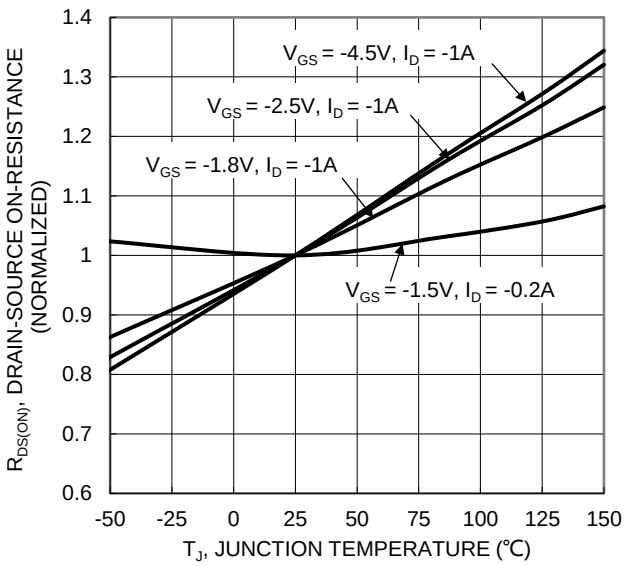


Figure 6. On-Resistance Variation with Junction Temperature

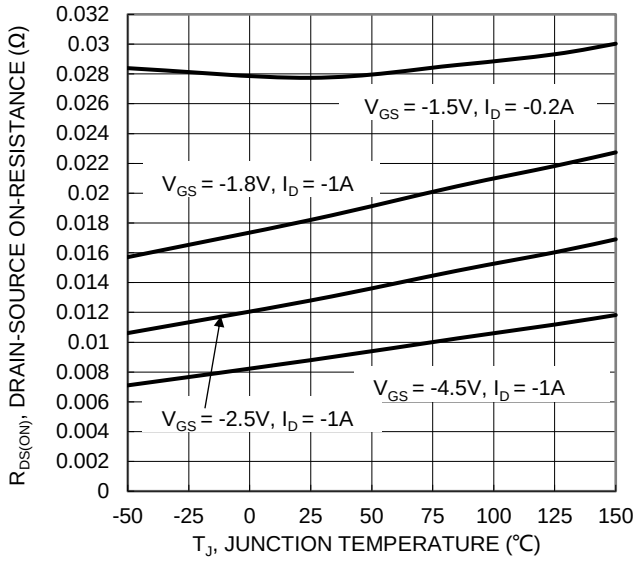


Figure 7. On-Resistance Variation with Junction Temperature

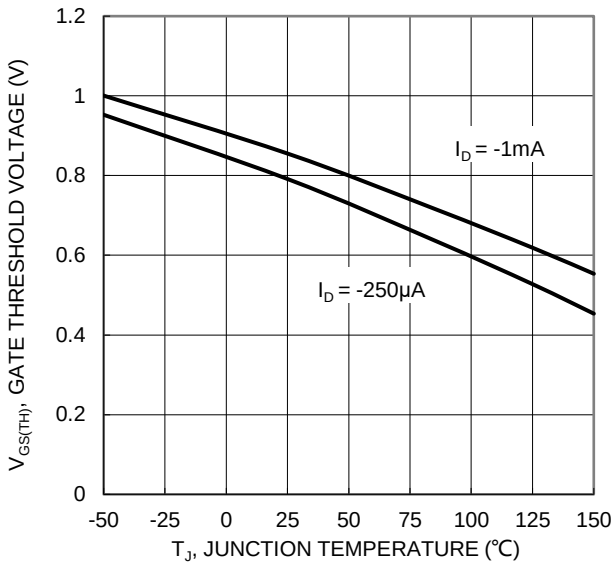


Figure 8. Gate Threshold Variation vs. Junction Temperature

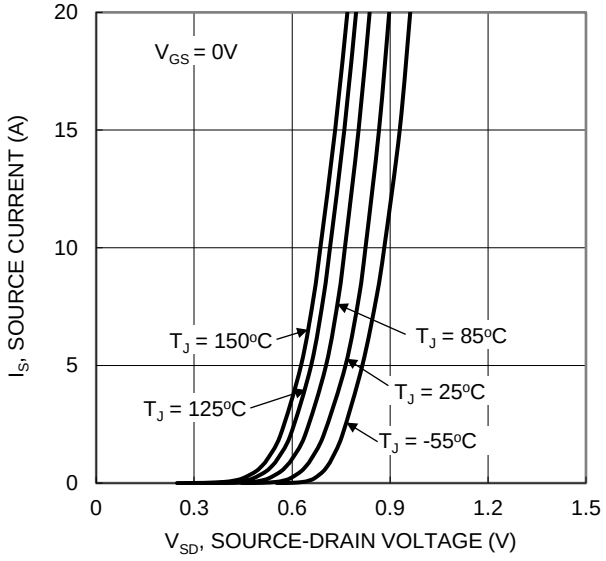


Figure 9. Diode Forward Voltage vs. Current

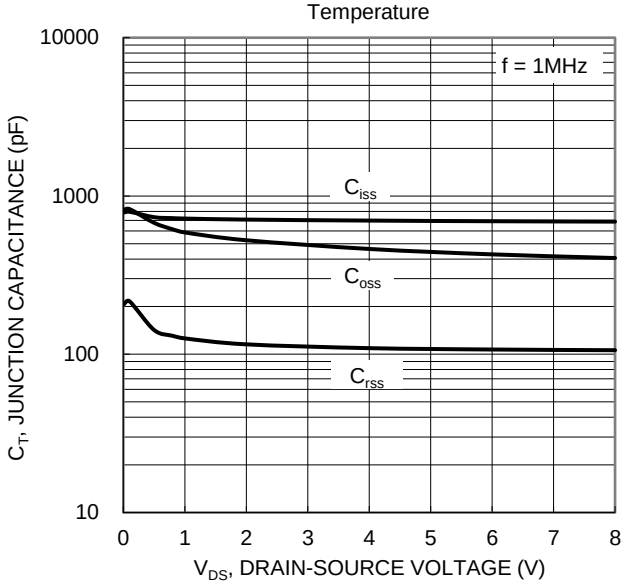


Figure 10. Typical Junction Capacitance

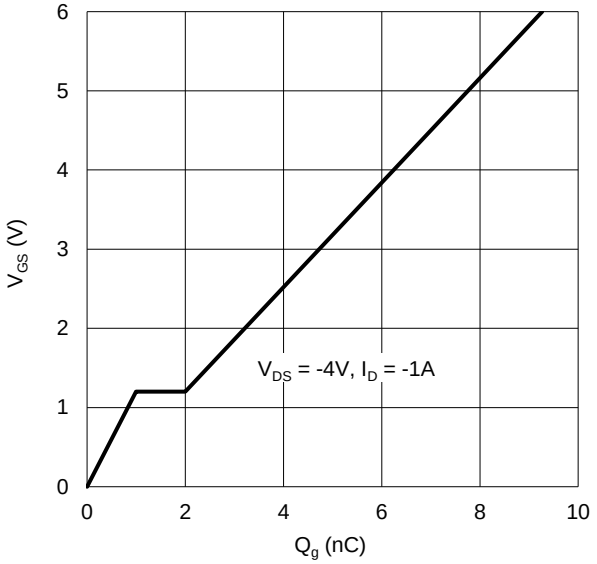


Figure 11. Gate Charge

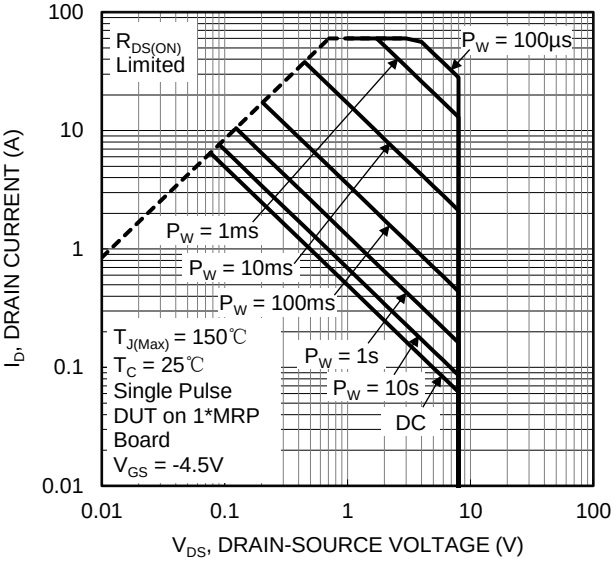


Figure 12. SOA, Safe Operation Area

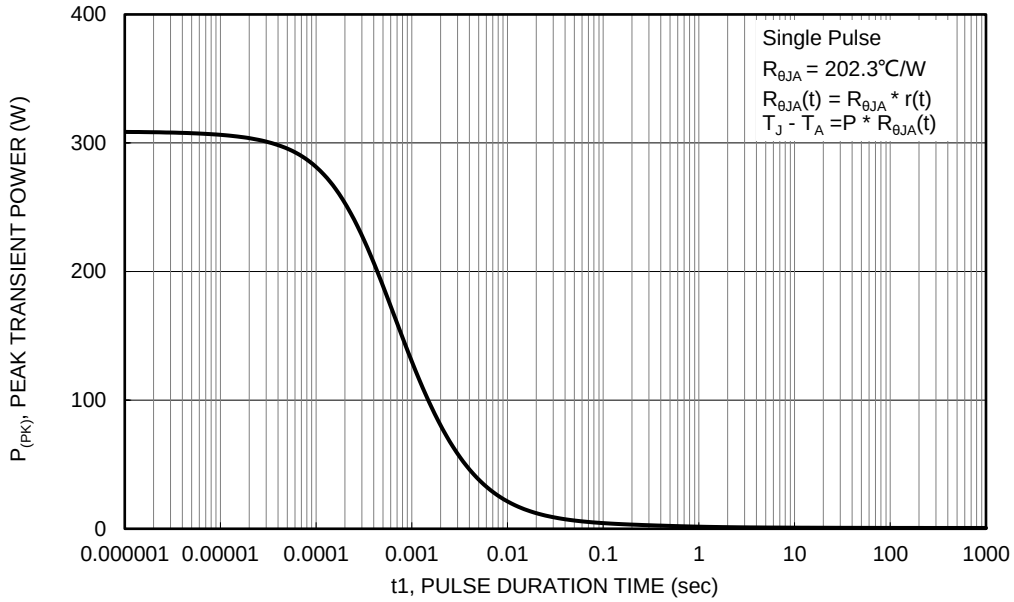


Figure 13. Single Pulse Maximum Power Dissipation

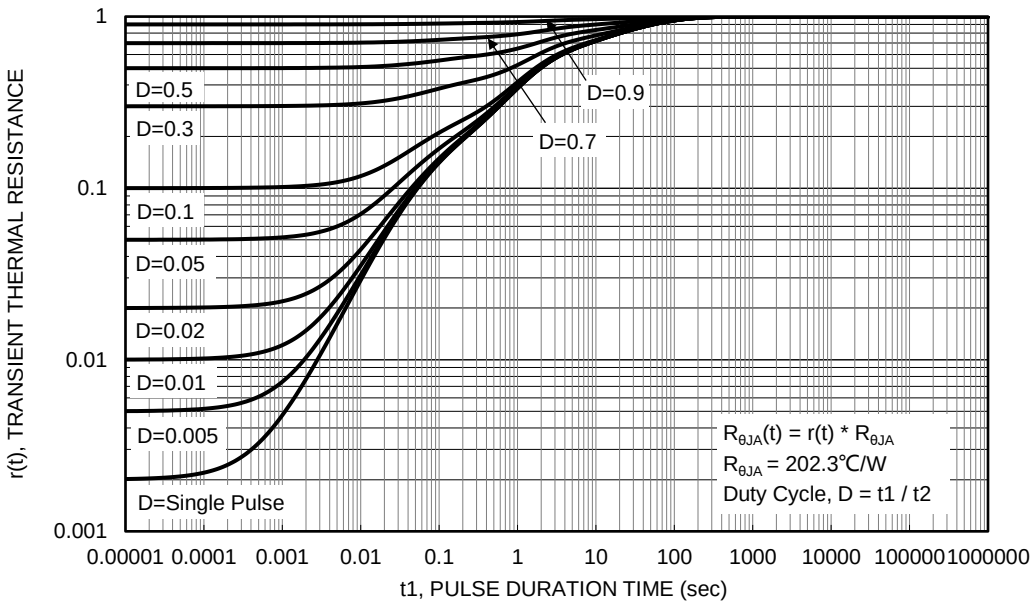
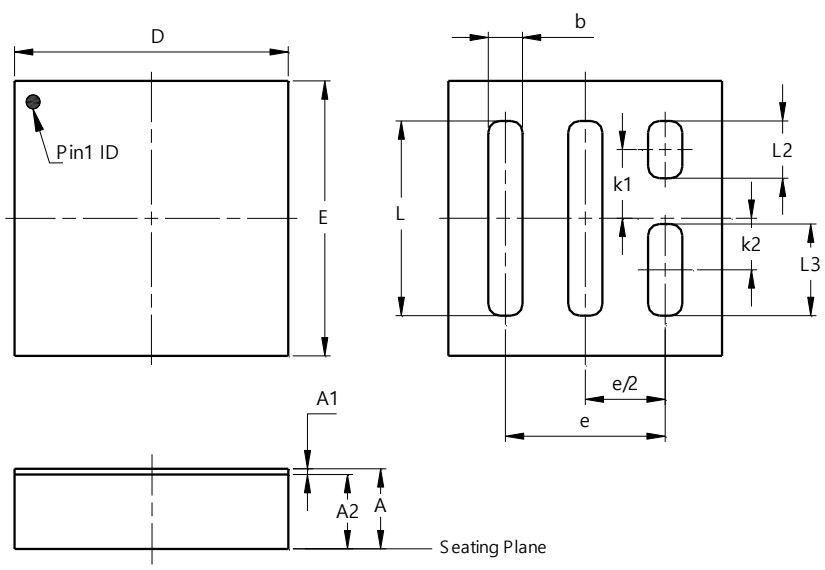


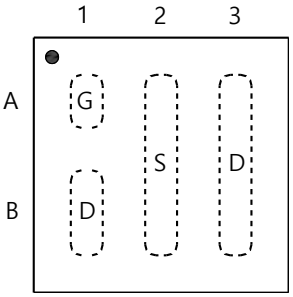
Figure 14. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DSN1212-4





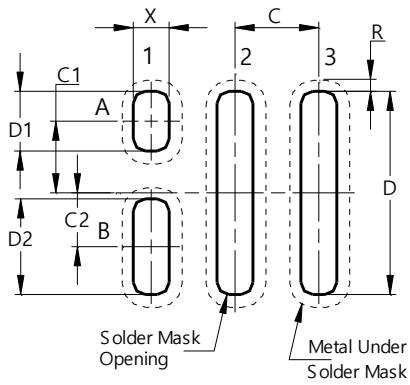
Pin Assignment	
A1	G
A2/B2	S
A3/B3	D
B1	D

X2-DSN1212-4			
Dim	**Min**	**Max**	**Typ**
A	--	0.35	0.30
A1	--	--	0.025
A2	--	--	0.275
b	0.14	0.16	0.15
D	1.12	1.20	1.16
E	1.12	1.20	1.16
e	--	--	0.70
k1	--	--	0.30
k2	--	--	0.225
L	0.84	0.86	0.85
L2	0.24	0.26	0.25
L3	0.39	0.41	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DSN1212-4



Dimensions	Value (in mm)
C	0.35
C1	0.30
C2	0.225
D	0.85
D1	0.25
D2	0.40
X	0.15
R	0.05 Min

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