

Description

The AP65251 is an adaptive constant on-time mode synchronous buck converter providing high efficiency, excellent transient response and high DC output accuracy for low-voltage regulation in digital TVs, set-top-boxes, and network systems.

The constant-on-time control scheme handles wide input/output voltage ratios and provides low external component count. The internal proprietary circuit enables the device to adopt ultra-low ESR ceramic capacitors.

The adaptive on-time control supports seamless transition between continuous conduction mode (CCM) at higher load conditions and discontinuous conduction mode (DCM) at lighter load conditions.

DCM allows AP65251 to maintain high efficiency at light load conditions. The AP65251 also features UVLO, OTP, and OCP to protect the circuit.

This IC is available in TSOT26 package.

Features

- V_{IN} 4.5V to 16V
- 2A Continuous Output Current, 2.5A Valley
- Efficiency Up to 95%
- Automated Light Load improvement
- V_{OUT} Adjustable to 0.6 to 6V
- 500kHz Switching Frequency
- Internal Soft-Start
- Enable Pin
- Over current Protection (OCP) with Hiccup
- Thermal Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

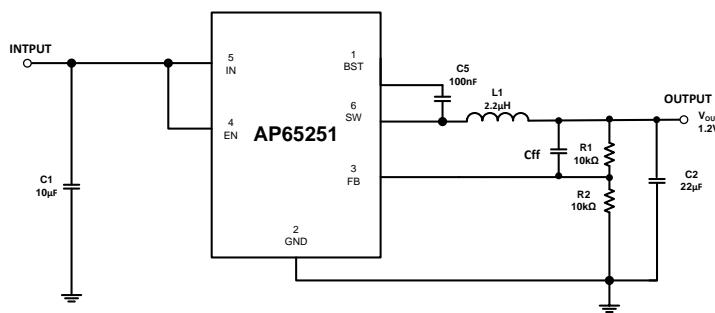
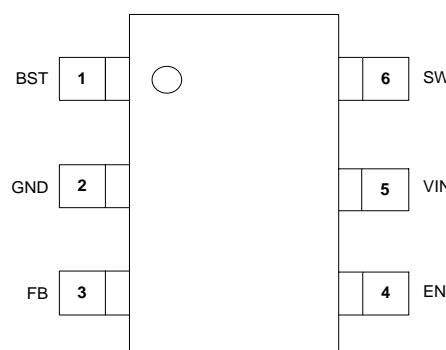


Figure 1. Typical Application Circuit

Pin Assignments

Top View



TSOT26

Applications

- Gaming Consoles
- Flat Screen TV sets and Monitors
- Set Top Boxes
- Distributed power systems
- Home Audio
- Consumer electronics
- Network Systems
- FPGA, DSP and ASIC Supplies
- Green Electronics

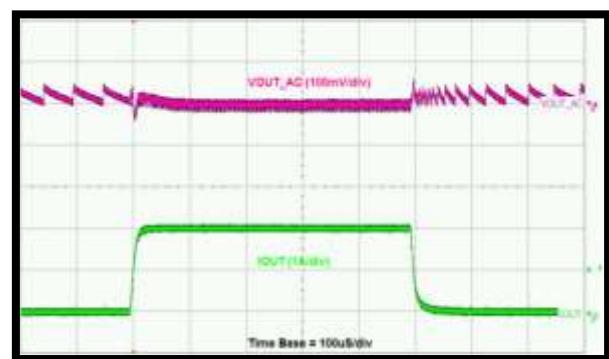


Figure 2. Load Transient 0 to 2A

Pin Descriptions

Pin Name	Pin Number	Function
TSOT26		
BST	1	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel MOSFET a 0.01 μ F or greater capacitor from SW to BST to power the high side switch.
GND	2	Power Ground.
FB	3	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See Setting the Output Voltage.
EN	4	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. Attach to IN with a 100k Ω pull up resistor for automatic startup.
VIN	5	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.5V to 16V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
SW	6	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.

Functional Block Diagram

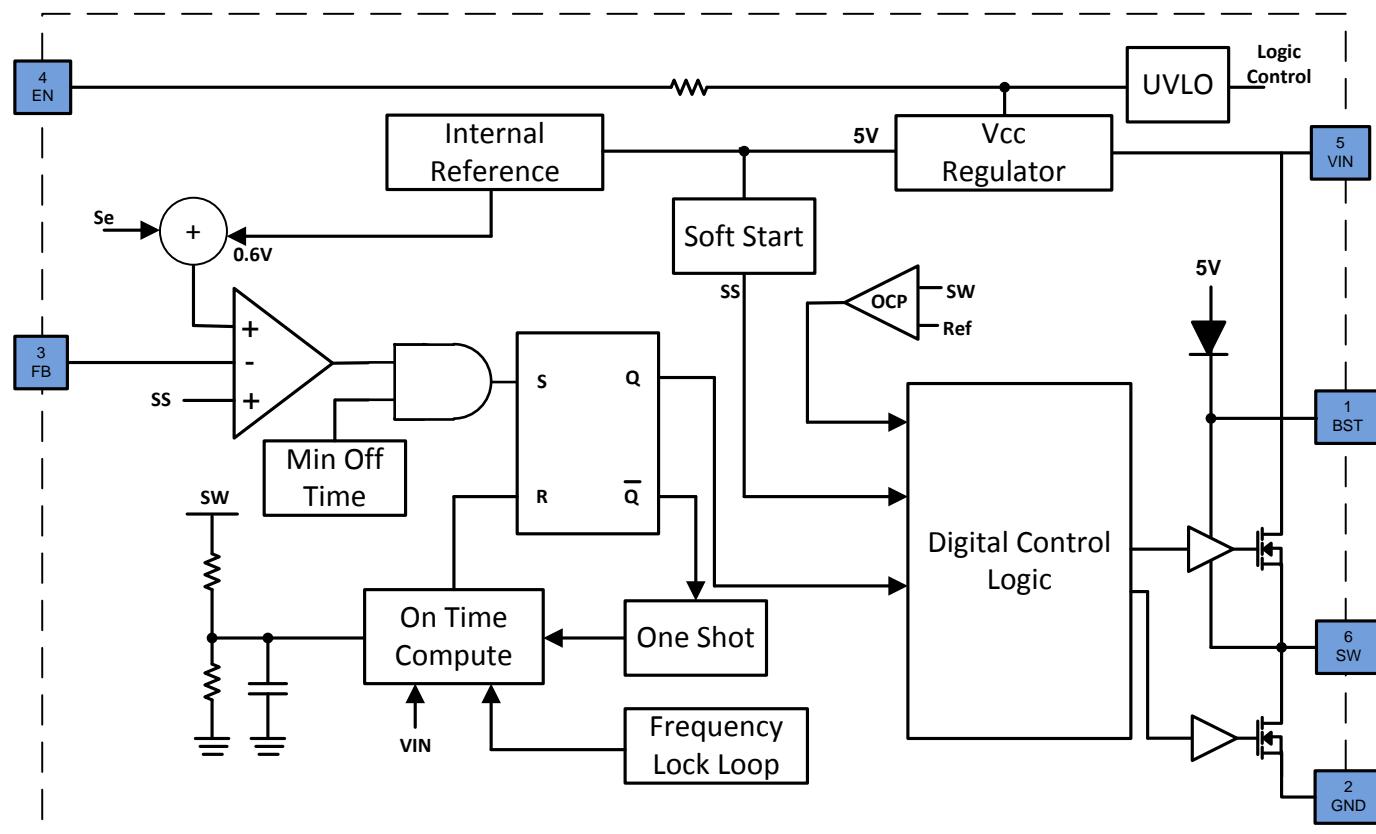


Figure 2. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to 20	V
V_{SW}	Switch Node Voltage	-1.0 to $V_{IN} + 0.3$	V
V_{BST}	Bootstrap Voltage	$V_{SW} - 0.3$ to $V_{SW} + 6.0$	V
V_{FB}	Feedback Voltage	-0.3V to +6.0	V
V_{EN}	Enable/UVLO Voltage	-0.3V to +16.0	V
T_{ST}	Storage Temperature	-65 to +150	$^\circ\text{C}$
T_J	Junction Temperature	+160	$^\circ\text{C}$
T_L	Lead Temperature	+260	$^\circ\text{C}$
ESD Susceptibility (Note 5)			
HBM	Human Body Mode	2000	V
CDM	Charge Device Model	1000	V

Notes:

4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	TSOT26	122	$^\circ\text{C}/\text{W}$
θ_{JC}	Junction to Case	TSOT26	28	$^\circ\text{C}/\text{W}$

Note: 6. Test condition for SOT26: Device mounted on FR-4 substrate, single-layer PC board, 2oz copper, with minimum recommended pad layout

Recommended Operating Conditions (Note 7) (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	4.5	16	V
T_A	Operating Ambient Temperature Range	-40	+85	$^\circ\text{C}$

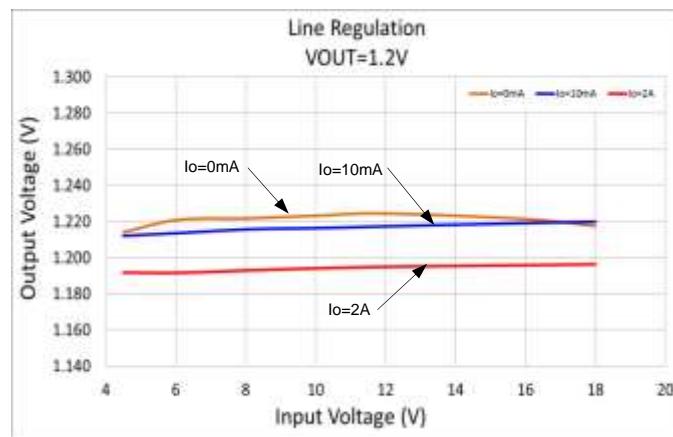
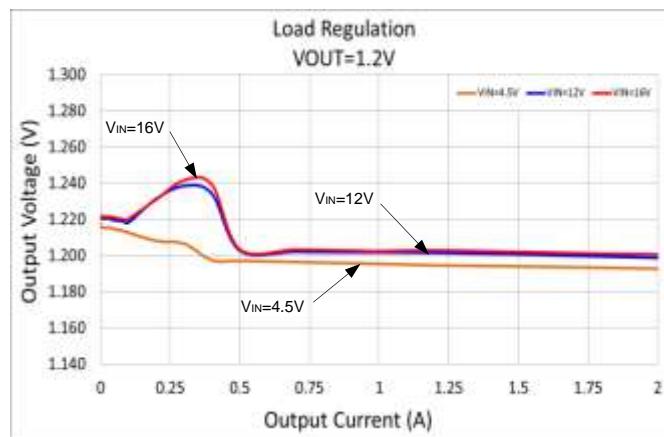
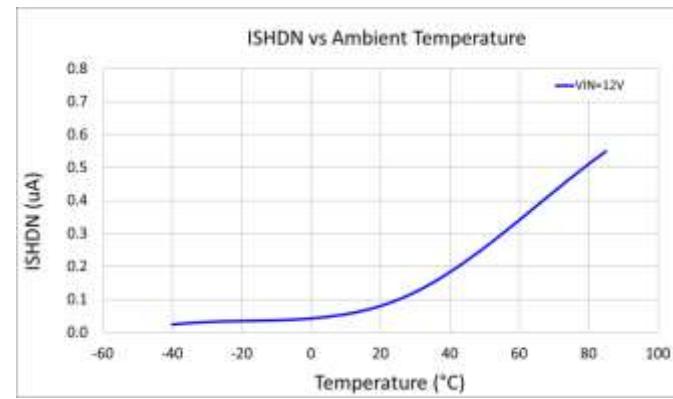
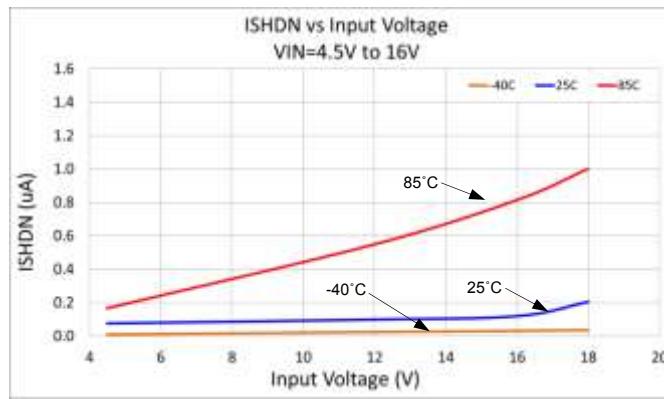
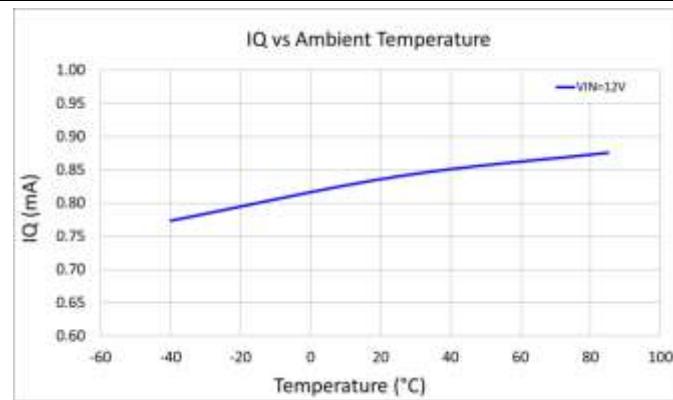
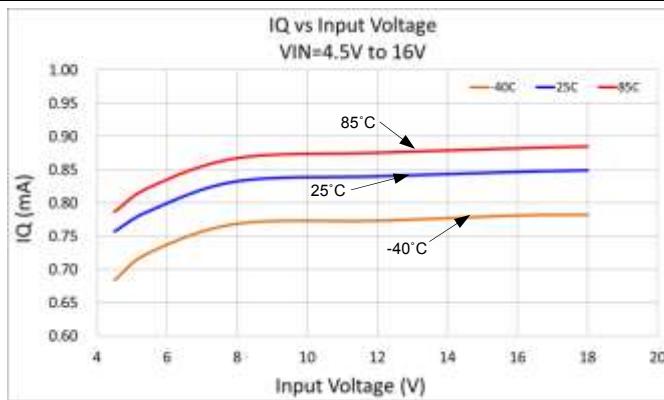
Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, unless otherwise specified.)

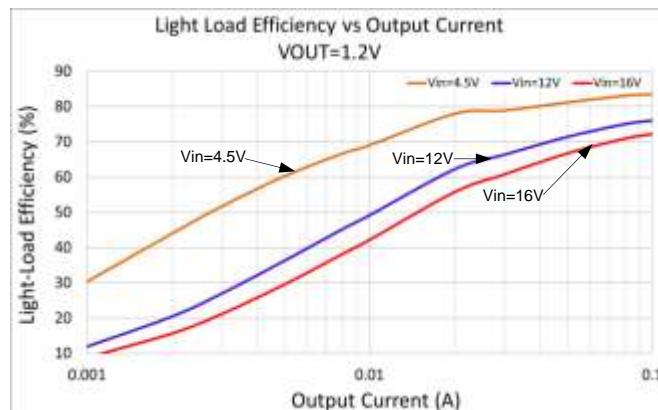
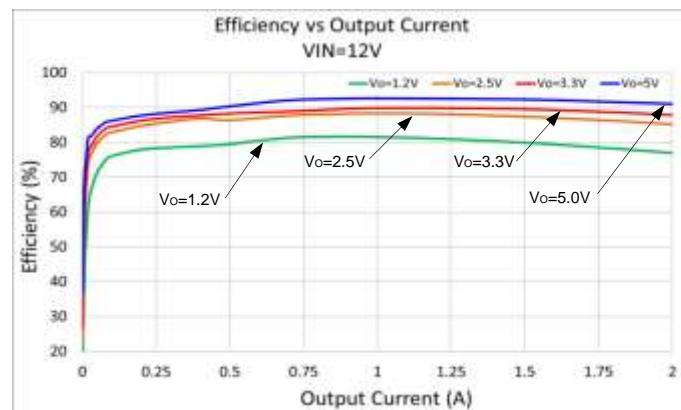
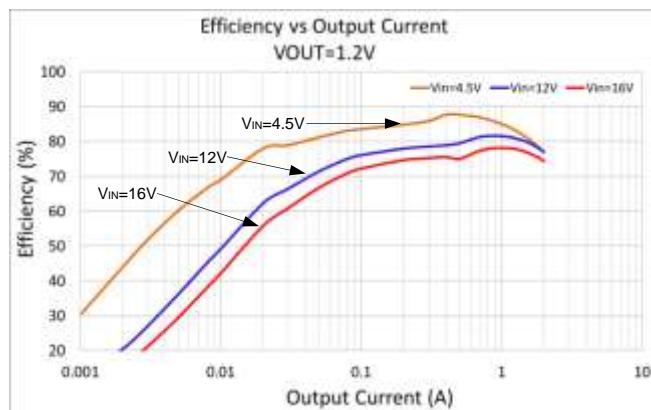
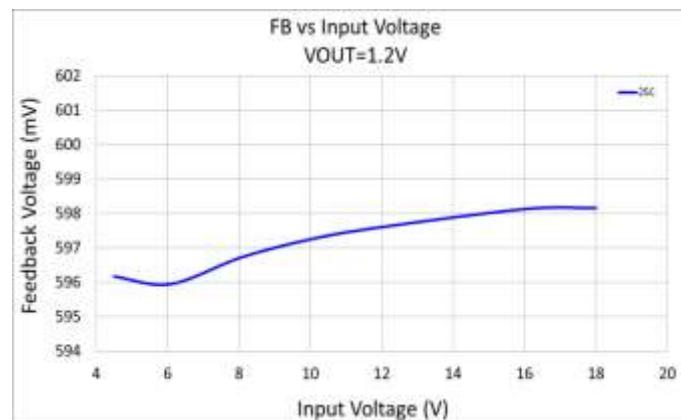
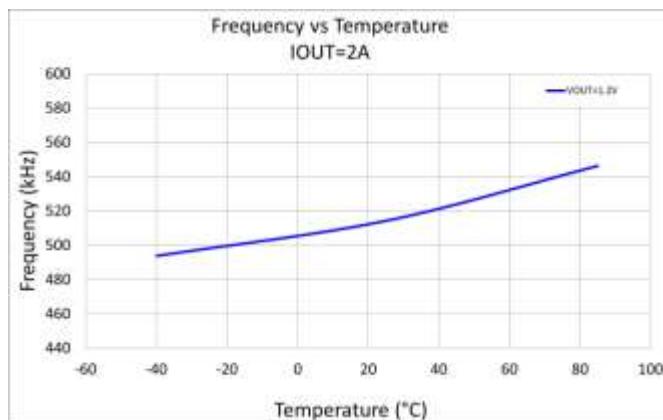
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	$V_{EN} = 0\text{V}$		0.1	1.0	μA
I_Q	Supply Current (Quiescent)	$V_{EN} = 2.0\text{V}$, $V_{FB} = 1.0\text{V}$		0.8		mA
$R_{DS(ON)1}$	High-Side Switch On-Resistance (Note 8)			150		$\text{m}\Omega$
$R_{DS(ON)2}$	Low-Side Switch On-Resistance (Note 8)			90		$\text{m}\Omega$
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.9	2.5	3	A
F_{SW}	Oscillator Frequency			500		kHz
D_{MAX}	Maximum Duty Cycle			75		%
T_{ON}	Minimum On Time			130		ns
V_{FB}	Feedback Voltage	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, CCM	591	600	609	mV
V_{EN_H}	EN Logic High		1.8			V
V_{EN_L}	EN Logic Low				0.4	V
I_{EN}	EN Input Current	$V_{EN} = 2\text{V}$		6		μA
		$V_{EN} = 0\text{V}$		0		μA
UVLO	V_{IN} Under Voltage Threshold Rising	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.55	3.9	4.25	V
	V_{IN} Under Voltage Threshold Hysteresis			300		mV
T_{SS}	Soft-Start Period			0.8		ms
T_{SD}	Thermal Shutdown (Note 8)			150		$^\circ\text{C}$
	Thermal Hysteresis (Note 8)			20		$^\circ\text{C}$

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, unless otherwise specified.)

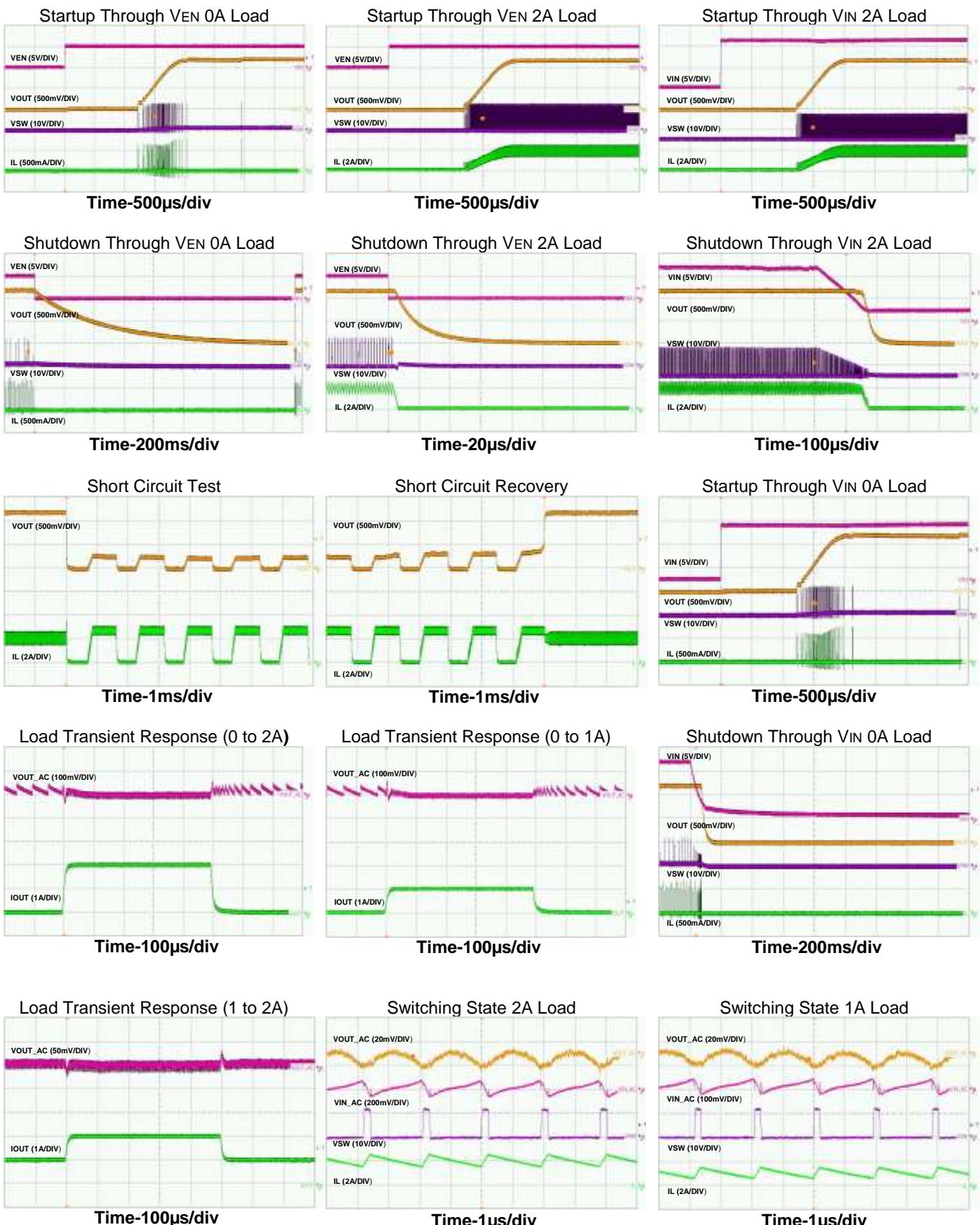


Typical Performance Characteristics (cont.) (@ $T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, unless otherwise specified.)



Typical Performance Characteristics (cont.)

(@ $T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, $L = 2.2\mu\text{H}$, $C1 = 10\mu\text{F}$, $C2 = 22\mu\text{F}$, unless otherwise specified.)



Application Information

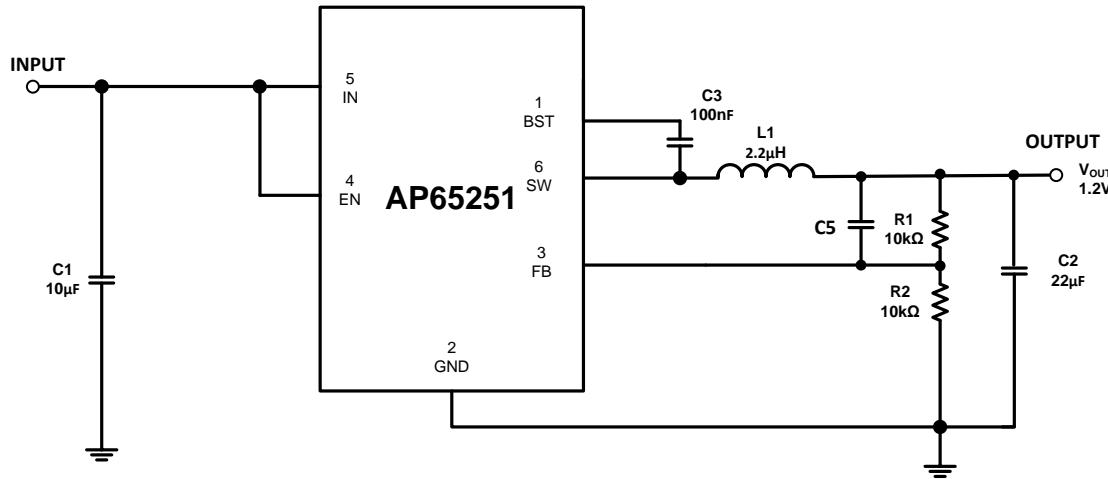


Figure 3. Typical Application of AP65251

PWM Operation and Adaptive On-time Control

The AP65251 is a synchronous step-down converter with internal power MOSFETs. Adaptive constant on time (aCOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot timer, ON-time period. This one shot is calculated by the converter's input voltage (V_{IN}) and the output voltage (V_{OUT}) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The high-side MOSFET turned off after the fixed on time expire and turn on the low-side MOSFET. Once the output voltage dropped below the output regulation, the low-side turned off. The one-shot timer then reset and the high-side MOSFET is turned on again.

AP65251 uses an adaptive on-time control scheme and does not have a dedicated in board oscillator. It runs with a pseudo-constant frequency of 650kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f}$$

V_{OUT} is the output voltage

V_{IN} is the input voltage

f is the switching frequency

After an ON-time period, the AP65251 goes into the OFF-time period. The OFF-time period length depends on VFB in most case. It will end when the FB voltage decreases below 0.6V, then the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is about 260ns typical.

Power Save Mode

The AP65251 is designed with Power Save Mode (PSM) at light load conditions for high efficiency. The AP65251 automatically reduces the switching frequency and changes the Ton time to T_{min-on} time during a light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually its valley comes close to zero current, which is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only by output capacitor, when FB voltage is lower than 0.6V, the next ON cycle begins. The on-time is the minimum on time that benefits for decreasing V_{OUT} ripple at light load condition. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following equation:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON}$$

T_{ON} is on-time

Application Information (cont.)

Enable

Above the 'EN high-level input voltage', the internal regulator is turned on and the quiescent current can be measured above this threshold. The enable (EN) input allows the user to control turning on or off the regulator. To enable the AP65251, EN must be pulled above the 'EN high-level input voltage.' To disable the AP65251, EN must be pulled below 'EN low-level input voltage.'

In Figure 3, EN is a high voltage input that can be safely connected to VIN (up to 16V) directly or through a 100KΩ pull-up to VIN for automatic start-up.

Over Current Protection (OCP)

Figure 4 shows the over current protection (OCP) scheme of AP65351. In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between GND pin and SW pin is lower than the over current trip level, V_{LIMIT} , the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin when the measured voltage is higher than limit voltage. After 6μs, the internal OCL (Over Current Logic) threshold is set to a lower level and internal SS is discharged such that output is 0V. Then the switching action is blanked out for 0.6ms before soft start re-initiated and OCP threshold is restored to higher value.

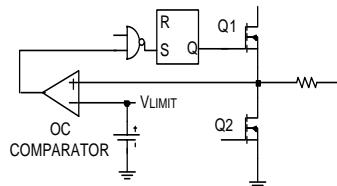


Figure 4 Overcurrent Protection Scheme

Under Voltage Lockout

Undervoltage Lockout is implemented to prevent the IC from insufficient input voltages. The AP65251 has a UVLO comparator that monitors the input voltage and the internal bandgap reference. If the input voltage falls below 3.9V, the AP65251 will disable. In this event, both high-side and low-side MOSFETs are turned off.

Thermal shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 150°C, the AP65251 shuts itself off, and both HMOS and LMOS will be turned off. The output is discharged with the internal transistor. When the junction cools to the required level (130°C nominal), the device initiates soft-start as during a normal power-up cycle.

Power Derating Characteristics

To prevent the regulator from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by:

$$T_{RISE} = PD \cdot (\theta_{JA})$$

Where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J , is given by:

$$T_J = T_A + T_{RISE}$$

T_A is the ambient temperature of the environment. For TSOT26 package, the θ_{JA} is 70°C/W. The actual junction temperature should not exceed the absolute maximum junction temperature of 125°C when considering the thermal design. The plot below is a typical derating curve versus ambient temperature.

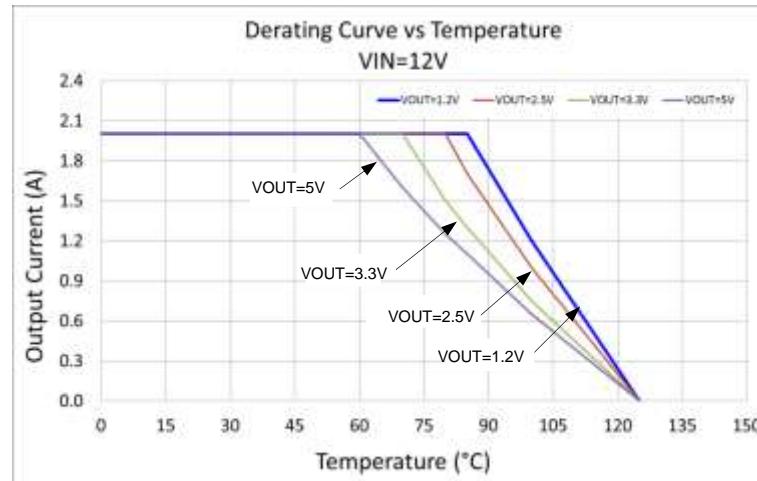


Figure 5 Output Current Derating Curve vs Temperature

Application Information (cont.)

Setting the Output Voltage

The output voltage can be adjusted from 0.6V using an external resistor divider. An optional C5, in figure 3, of 10pF to 47pF used to improve the transient response. Resistor R1 is selected based on a design tradeoff between efficiency and output voltage accuracy. Table 2 shows a list of resistor selection for common output voltages. For high values of R1 there is less current consumption in the feedback network. R1 can be determined by the following equation:

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{0.6} - 1 \right)$$

Output Voltage (V)	Cout (uF)	L(μH)	C5 (pF)	R1 (KΩ)	R2 (KΩ)
1.2	22	2.2	NC	10	10
2.5	22	3.6	NC	25.5	8.06
3.3	22	3.6	20-33	115	25.5
5	22	4.7	20-39	110	15

Table 1 Recommended Components Selection

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{SW}}$$

Where ΔI_L is the inductor ripple current and f_{SW} is the buck converter switching frequency.

Choose the inductor ripple current to be 30% to 50% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence choosing an inductor with appropriate saturation current rating is important.

A 2.2μH to 4.7μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor's DC resistance should be less than 100mΩ. Use a larger inductance for improved efficiency under light load conditions.

Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on time on the upper MOSFET. It must have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has RMS rating greater than half of the maximum load current.

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used it must be surge protected, otherwise, capacitor failure could occur. For most applications greater than 10μF, ceramic capacitor is sufficient.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshoot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

Maximum capacitance required can be calculated from the following equation:

ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated from the equation below:

$$V_{out_Ripple} = \Delta I_{inductor} * ESR$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 22μF to 68μF ceramic capacitor will be sufficient. To meet the load transient requirement, C_o should be greater than the following:

Application Information (cont.)

$$C_o = \frac{L(I_{out} + \frac{\Delta I_{inductor}}{2})^2}{(\Delta V + V_{out})^2 - V_{out}^2}$$

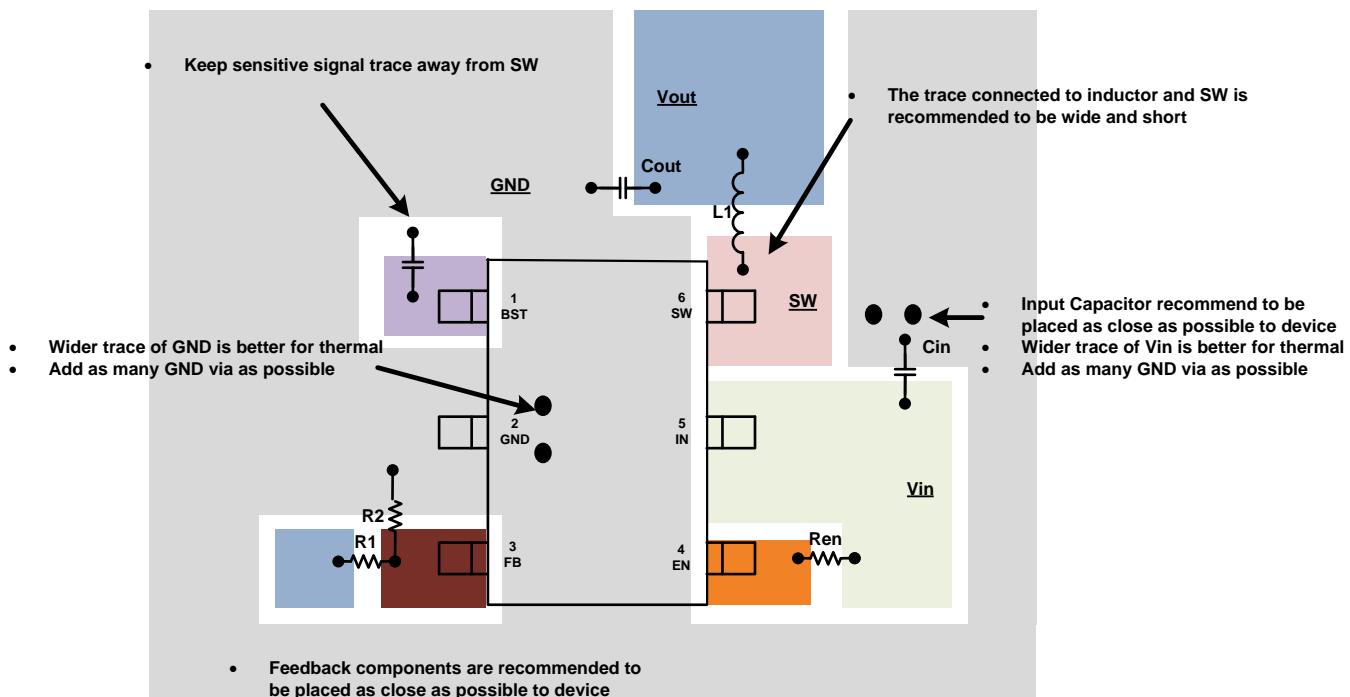
Where ΔV is the maximum output voltage overshoot.

Bootstrap Capacitor

To ensure the proper operation, a ceramic capacitor must be connected between the VBST and SW pin. A $0.1\mu F$ ceramic capacitor is sufficient.

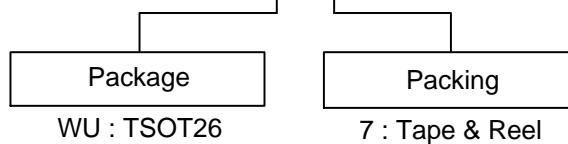
PC Board Layout

1. The AP65251 works at 2A load current, heat dissipation is a major concern in layout the PCB. A 2oz Copper in both top and bottom layer is recommended.
2. Provide sufficient vias in the thermal exposed pad for heat dissipate to the bottom layer.
3. Provide sufficient vias in the Output capacitor GND side to dissipate heat to the bottom layer.
4. Make the bottom layer under the device as GND layer for heat dissipation. The GND layer should be as large as possible to provide better thermal effect.
5. Make the Vin capacitors as close to the device as possible.
6. Make the VREG5 capacitor as close to the device as possible.



Ordering Information

AP65251 WU - 7

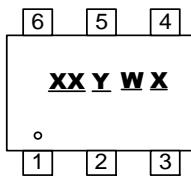


Part Number	Package Code	Part Marking	Identification Code	Tape and Reel	
				Quantity	Part Number Suffix
AP65251WU-7	WU	TSOT26	SB	3000	-7

Marking Information

TSOT26

(Top View)



XX : Identification Code

XX Flashcards

W : Week : A-Z : 1~26 week;
a-z : 27~52 week; z represents
52 and 53 week

X : Internal Code

Part Number	Package	Identification Code
AP65251WU-7	TSOT26	SB

Mechanical Data

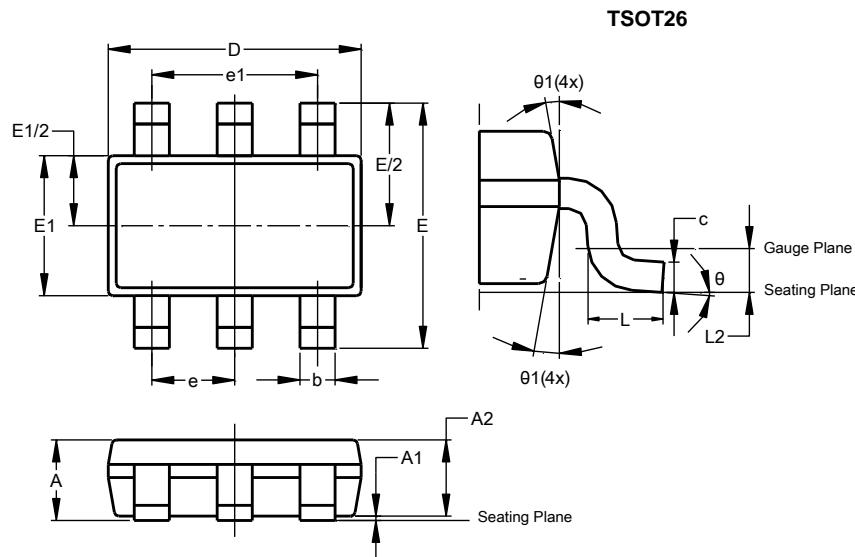
- Surface Mount Package
- Case Material: Molded Plastic, UL Flammability Classification Rating 94V-0
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208^(e3)
- Weight: 0.013 grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

Package View



Top View

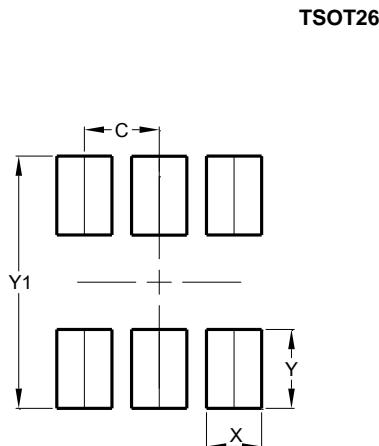
Package Outline Dimensions



TSOT26			
Dim	Min	Max	Typ
A	–	1.00	–
A1	0.010	0.100	–
A2	0.840	0.900	–
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	–
c	0.120	0.200	–
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	–
L2	0.250 BSC		
θ	0°	8°	4°
θ1	4°	12°	–

All Dimensions in mm

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These dimensions may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the 'Z' dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for International grid details, please see document IEC, Publication 97.

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

Minimum Packing Quantity

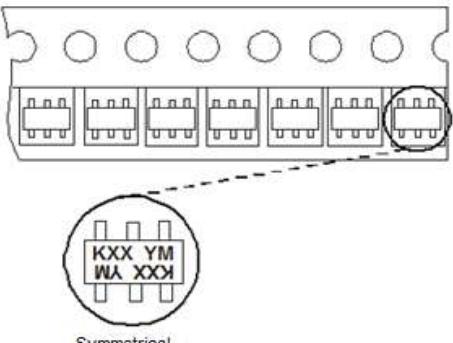
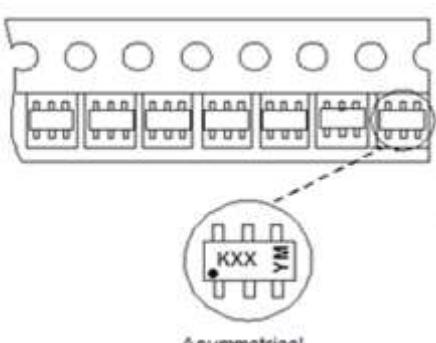
	Quantity	Tape Width	Part Number Suffix
7" Reel	3,000	8mm	-7
13" Reel	10,000	8mm	-13

Note: Package quantities given are for minimum packaging quantity only, not minimum order quantity. For minimum order quantity, please contact Sales Department.

Note: No mixed date codes or partial quantity (less than minimum packaging quantity) per packaging is allowed.

Note: In no case shall there be two or more consecutive components missing from any reel for any reason.

Device Tape Orientation

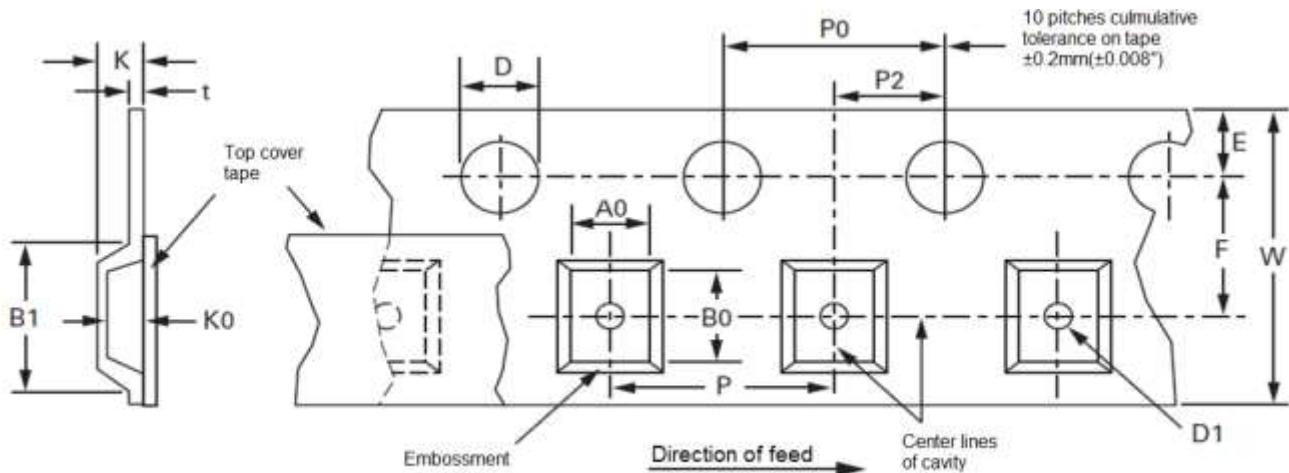
Tape Width	Part Number Suffix	Tape Orientation	
8mm	-7 -13	 Symmetrical	 Asymmetrical

Direction of feed 

Note: For part marking, refer to product datasheet.

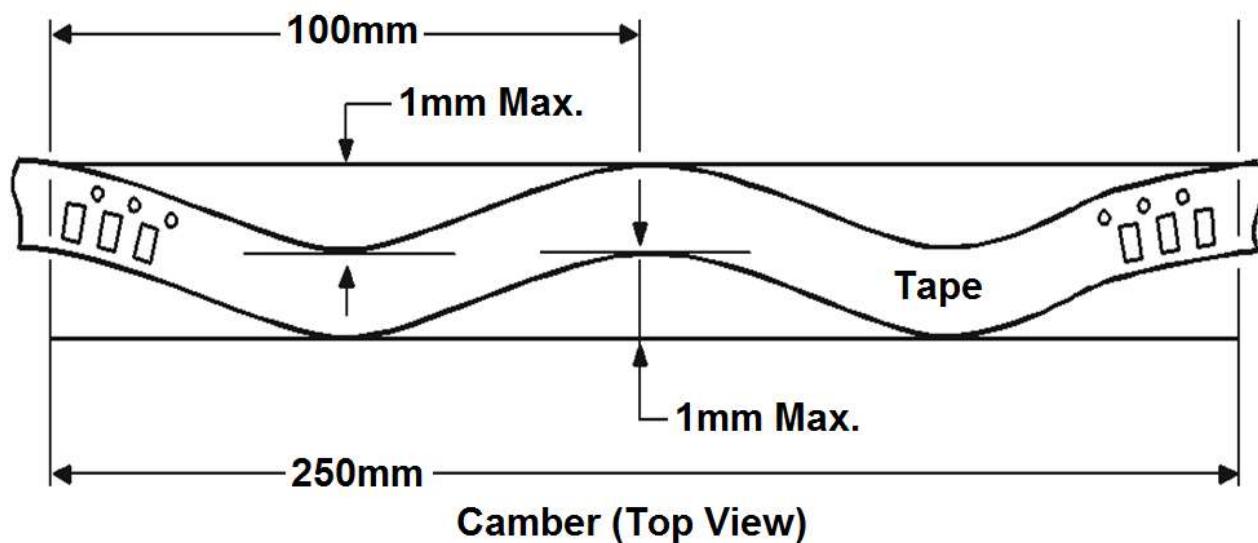
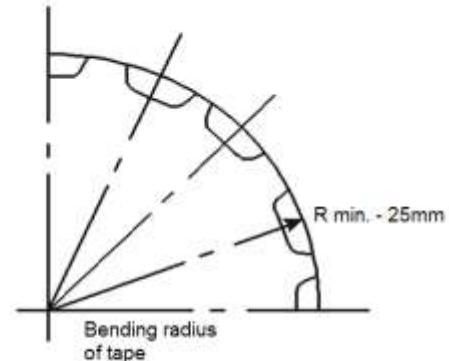
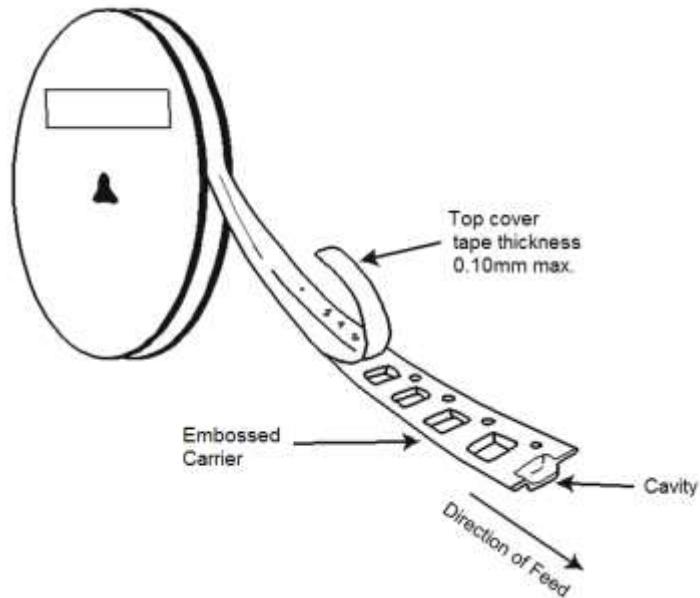
Note: Tape and package drawings are not to scale and are shown for device tape orientation only.

Embossed Carrier Tape Specifications



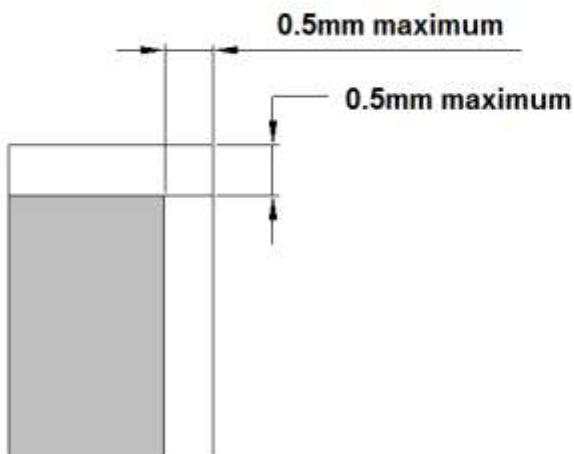
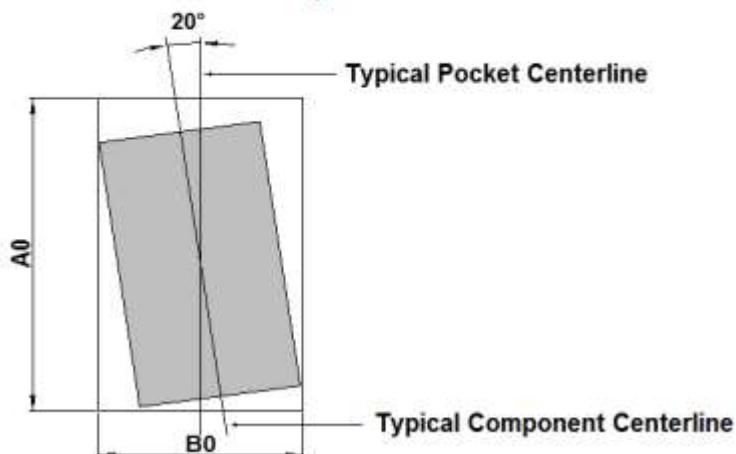
Tape Width (W)	Dimension	Value (mm)	Dimension	Value (mm)	Dimension	Value (mm)
8mm	B1	4.5 max.	F	3.5 ± 0.05	P2	2.0 ± 0.05
	D	$1.5 + 0.10 - 0.0$	K	2.4 max.	t	0.40 max.
	D1	0.35 min.	P	4.0 ± 0.10	W	8 ± 0.30
	E	1.75 ± 0.10	P0	4.0 ± 0.10		
	A0 B0 K0	Determined by component size. The clearance between the component and the cavity must comply to the rotational and lateral movement requirement provided in figures in the "Maximum Component Movement in Tape Pocket" section.				

Embossed Carrier Tape Specifications (Continued)

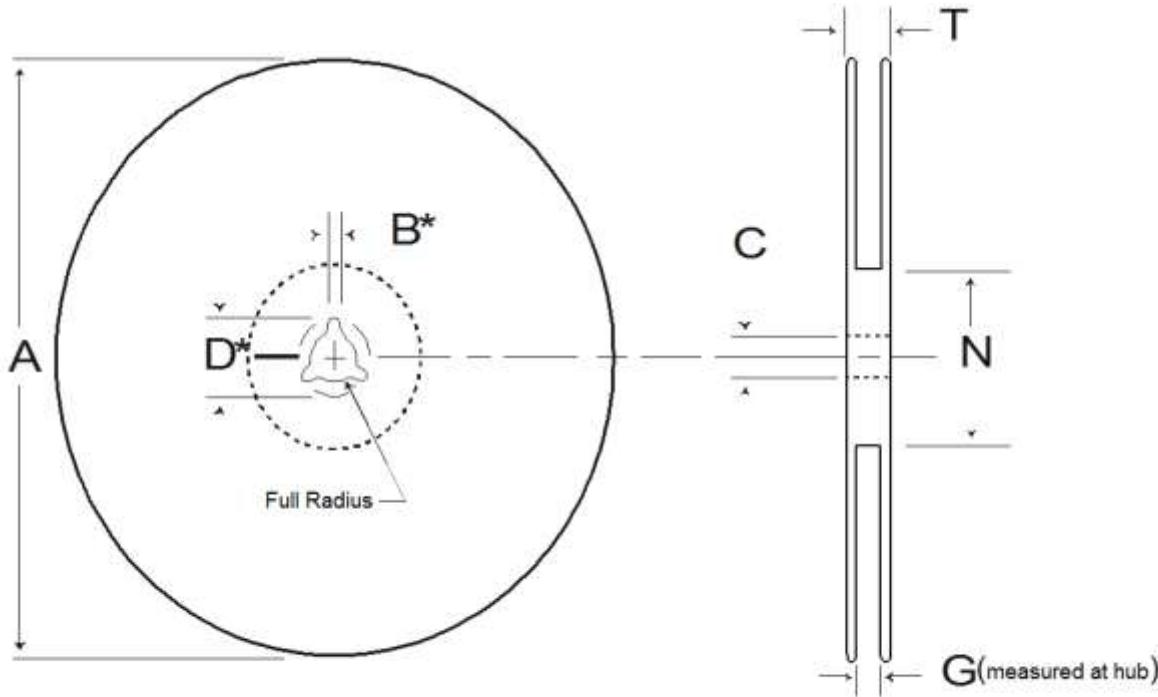


Allowable camber to be 1mm/100mm tape, non-cumulative

Maximum Component Movement in Tape Pocket

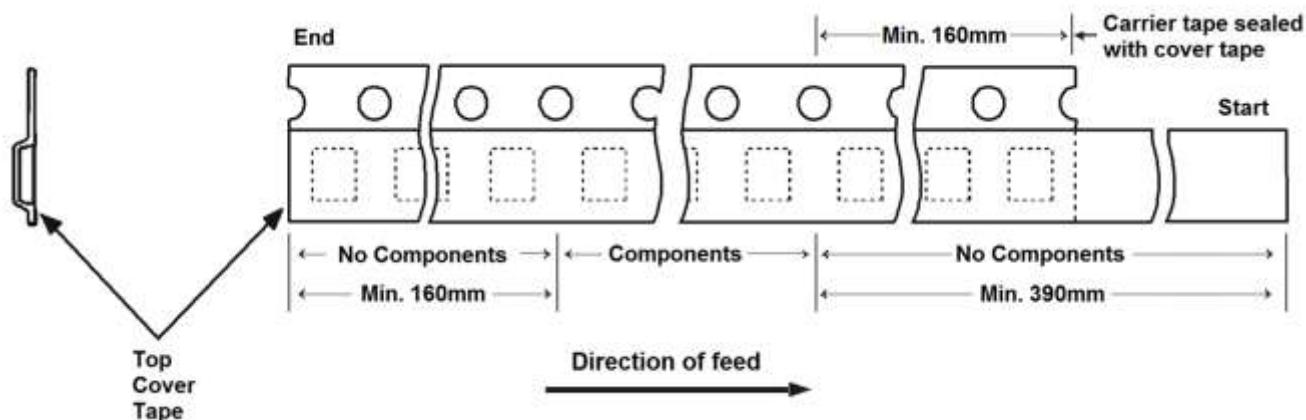
Component Lateral Movement**8mm Tape****Maximum Component Rotation
Top View****Maximum Component Rotation
Side View**

Surface Mount Reel Specifications



Tape Width	Reel Size	A (mm)	B Max (mm)	C (mm)	D Max (mm)	N Min (mm)	G (mm)	T Max (mm)
8mm	7"	178 \pm 2	2.0 +0.5 -0	13 +0.5 -0.2	20.5 \pm 0.2	55 \pm 5	8.4 +1.5 -0.0	14.4
	13"	330 \pm 2	2.0 +0.5 -0	13 +0.5 -0.2	20.5 \pm 0.2	100 \pm 2	8.4 +1.5 -0.0	14.4

Tape Leader and Trailer Specifications



Note: There shall be a leader of at least 230mm which may consist of carrier tape and/or cover tape or a start tape followed by at least 160mm of empty carrier tape sealed with cover tape.

Note: There shall be a trailer of at least 160mm of empty carrier tape sealed with cover tape. The entire carrier tape must release from the reel hub as the last portion of the tape unwinds from the reel without damage to the carrier tape and the remaining components in the cavities.

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