TRIPLE BUFFER WITH OPEN-DRAIN OUTPUTS

Description

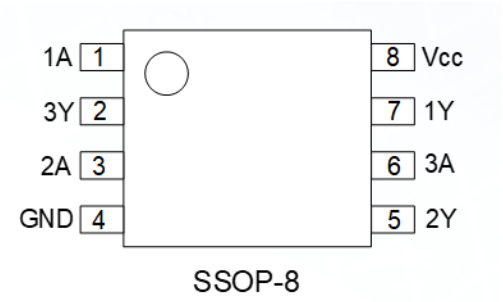
The 74LVC3G07 is a triple buffer with open-drain outputs. The device is designed for operation with a power supply range of 1.65V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output preventing damaging current backflow when the device is powered down.

Each of the buffers performs the positive Boolean function:

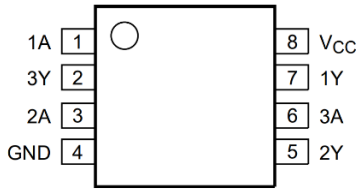
$Y = A$

A pullup resistor is required for a logical HIGH output.

Pin Assignments



SSOP-8



VSSOP-8

Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- -24mA Output Drive at 3.3V
- CMOS Low-Power Consumption
- I_{OFF} Supports Partial Power Down Mode Operation
- Inputs Accept up to 5.5V
- ESD Protection Tested per JESD 22
  Exceeds 2,000V Human Body Model (A114)
  Exceeds 1,000V Charged Device Model (C101)
- Latch-Up Exceeds 100mA per JESD 78, Class I
- Range of Package Options
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Applications

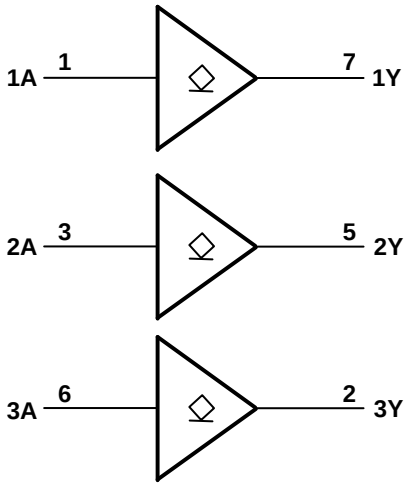
- Voltage-level shifting
- General-purpose logic
- Power down signal isolation
- Wide array of products such as:
  - PCs, networking, notebooks, netbooks, PDAs
  - Computer peripherals, hard drives, CD/DVD ROM
  - TV, DVD, DVR, set top boxes
  - Cell phones, personal navigation/GPS
  - MP3 players, cameras, video recorders

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Descriptions

Pin Name	Pin NO.	Description
1A	1	Data Input
3Y	2	Data Output
2A	3	Data Input
GND	4	Ground
2Y	5	Data Output
3A	6	Data Input
1Y	7	Data Output
V_{CC}	8	Supply Voltage

Logic Diagram



Function Table

Inputs	Output
A	**Y**
H	Z
L	L

Absolute Maximum Ratings (Notes 4, 5)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
V_{CC}	Supply Voltage Range	-0.5 to 6.5	V
V_I	Input Voltage Range	-0.5 to 6.5	V
V_O	Voltage Applied to Output in High Impedance or I_{OFF} State	-0.5 to 6.5	V
V_O	Voltage Applied to Output in High or Low State	-0.5 to 6.5	V
I_{IK}	Input Clamp Current $V_I < 0$	-50	mA
I_{OK}	Output Clamp Current $V_O < 0$	-50	mA
I_O	Continuous Output Current	±50	mA
I_{CC}, I_{GND}	Continuous Current Through V_{CC} or GND	±100	mA
T_J	Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C

Notes: 4. Stresses beyond the absolute maximum can result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.
5. Forcing the maximum allowed voltage could cause a condition exceeding the maximum current or conversely forcing the maximum current could cause a condition exceeding the maximum voltage. The ratings of both current and voltage must be maintained within the controlled range.

Recommended Operating Conditions (Note 6)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Operating Voltage	Operating	1.65	5.5	V
		Data Retention Only	1.5	—	V
V_{IH}	High-Level Input Voltage	V_{CC} = 1.65V to 1.95V	0.65 X V_{CC}	—	V
		V_{CC} = 2.3V to 2.7V	1.7	—	
		V_{CC} = 3V to 3.6V	2	—	
		V_{CC} = 4.5V to 5.5V	0.7 X V_{CC}	—	
V_{IL}	Low-Level Input Voltage	V_{CC} = 1.65V to 1.95V	—	0.35 X V_{CC}	V
		V_{CC} = 2.3V to 2.7V	—	0.7	
		V_{CC} = 3V to 3.6V	—	0.8	
		V_{CC} = 4.5V to 5.5V	—	0.3 X V_{CC}	
V_I	Input Voltage	—	0	5.5	V
V_O	Output Voltage	—	0	V_{CC}	V
I_{OL}	Low-Level Output Current	V_{CC} = 1.65V	—	4	mA
		V_{CC} = 2.3V	—	8	
		V_{CC} = 3V	—	16	
			—	24	
		V_{CC} = 4.5V	—	32	
Δt/ΔV	Input Transition Rise or Fall Rate	V_{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V	—	20	ns/V
		V_{CC} = 1.65V to 2.7V	—	10	
		V_{CC} = 2.7V to 5V	—	5	
T_A	Operating Free-Air Temperature	—	-40	+125	ºC

Note: 6. Unused inputs should be held at V_{CC} or Ground for device proper operation.

Electrical Characteristics

Symbol	Parameter	Test Conditions	V_{CC}	-40°C to +85°C		-40°C to +125°C		Unit
				Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage	I_{OL} = 100µA	1.65V to 5.5V	—	0.1	—	0.1	V
		I_{OL} = 4mA	1.65V	—	0.45	—	0.45	
		I_{OL} = 8mA	2.3V	—	0.3	—	0.3	
		I_{OL} = 16mA	3V	—	0.4	—	0.4	
		I_{OL} = 24mA		—	0.55	—	0.75	
		I_{OL} = 32mA	4.5V	—	0.55	—	0.75	
I_I	Input Current	V_I = 5.5V or GND	0 to 5.5V	—	±5	—	±5	µA
I_{OFF}	Power Down Leakage Current	V_I or V_O = 5.5V	0	—	±10	—	±10	µA
I_{CC}	Supply Current	V_I = 5.5V or GND, I_O = 0	1.65V to 5.5V	—	10	—	10	µA
ΔI_{CC}	Additional Supply Current	Input at V_{CC} – 0.6V	3V to 5.5V	—	500	—	500	µA
C_I	Input Capacitance	V_I = V_{CC} or GND	3.3V	—	3.5 (Typ)	—	—	pF

Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Typ	Max	Unit
Θ_{JA}	Thermal Resistance Junction-to-Ambient	SSOP-8	Note 7	—	130	—	°C/W
		VSSOP-8	Note 7	—	155	—	°C/W
Θ_{JC}	Thermal Resistance Junction-to-Case	SSOP-8	Note 7	—	36	—	°C/W
		VSSOP-8	Note 7	—	38	—	°C/W

Note: 7. Test condition: Device mounted on JEDEC 2s2p High-K board, FR-4 substrate PCB, 2oz copper with minimum recommended pad layout.

Operating Characteristics (T_A = +25°C, V_{CC} = 3.3V)

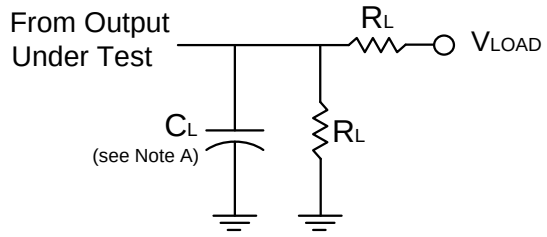
Symbol	Parameter	Test Conditions	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	Unit
			Typ	Typ	Typ	Typ	
C_{PD}	Power Dissipation Capacitance	f = 10MHz, 1 Input Switching	3	3	4	5	pF

Switching Characteristics

Figure 1

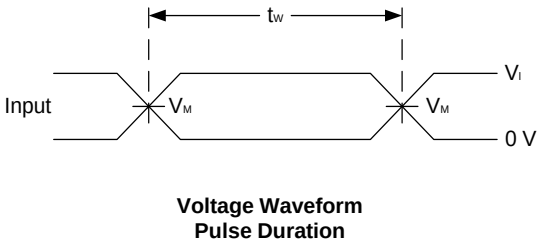
Parameter	From Input	To Output	V_{CC}	T_A = -40°C to +85°C		T_A = -40°C to +125°C		Unit
				Min	Max	Min	Max	
t_{PD}	A	Y	1.8V ± 0.15V	1.5	7.8	1.5	8.3	ns
			2.5V ± 0.2V	1	4.3	1	4.8	
			3.3V ± 0.3V	1	3.7	1	4.2	
			5.0V ± 0.5V	1	2.9	1	3.4	

Parameter Measurement Information (Notes B, C)

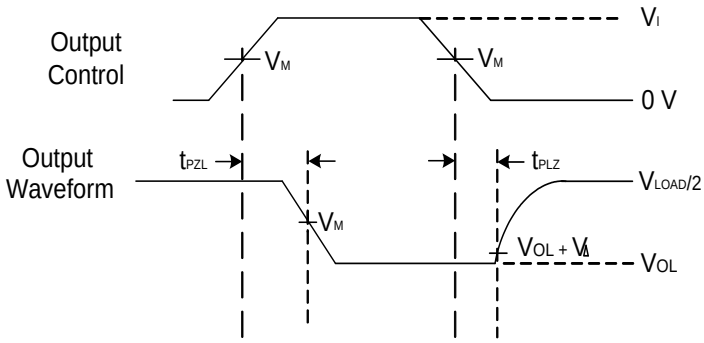


TEST	Condition
t_{PLZ} (see Notes D and F)	V_{LOAD}
t_{PZL} (see Notes D and E)	V_{LOAD}

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8V ± 0.15V	V_{CC}	≤2ns	V_{CC} / 2	2 X V_{CC}	30pF	1kΩ	0.15V
2.5V ± 0.2V	V_{CC}	≤2ns	V_{CC} / 2	2 X V_{CC}	30pF	500Ω	0.15V
3.3V ± 0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V ± 0.5V	V_{CC}	≤2.5ns	V_{CC} / 2	2 X V_{CC}	50pF	500Ω	0.3V



Voltage Waveform
Pulse Duration

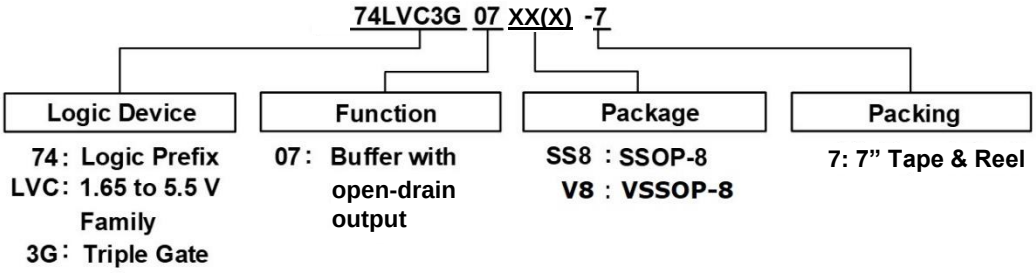


Voltage Waveform
Propagation Delay Time

Figure 1. Load Circuit and Voltage Waveforms

Notes:
A. Includes test lead and test apparatus capacitance.
B. All pulses are supplied at pulse repetition rate ≤ 10MHz.
C. The inputs are measured one at a time with one transition per measurement.
D. For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD}.
E. t_{PZL} is measured at V_M.
F. t_{PLZ} is measured at $V_{OL} + V_\Delta$.

Ordering Information



Part Number	Package Code	Package	Packing	
			Qty.	Carrier
74LVC3G07SS8-7	SS8	SSOP-8	3000	7" Tape and Reel (Note 8)
74LVC3G07V8-7	V8	VSSOP-8	3000	7" Tape and Reel (Note 8)

Note: 8. The taping orientation is located on our website at http://www.diodes.com/package-outlines.html.

Marking Information

SSOP-8

(Top View)

Y : Year : 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents 52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
74LVC3G07SS8-7	SSOP-8	S3G07

VSSOP-8

(Top View)

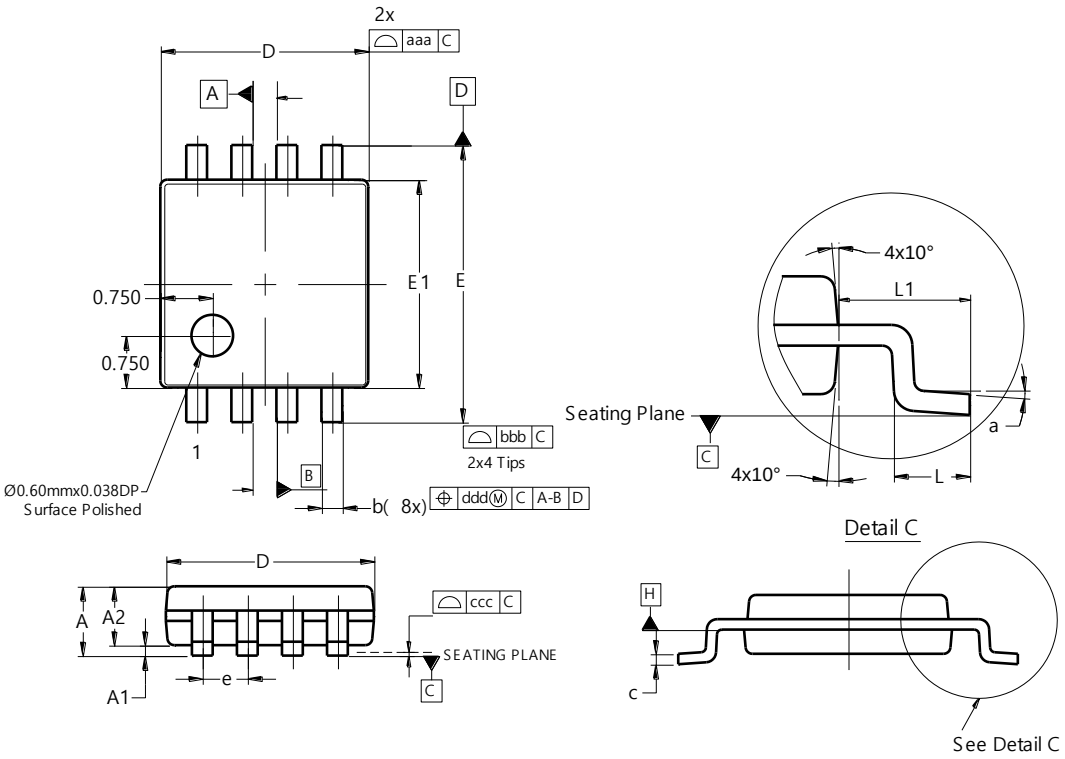
Y : Year : 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents 52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
74LVC3G07V8-7	VSSOP-8	V3G07

Package Outline Dimensions

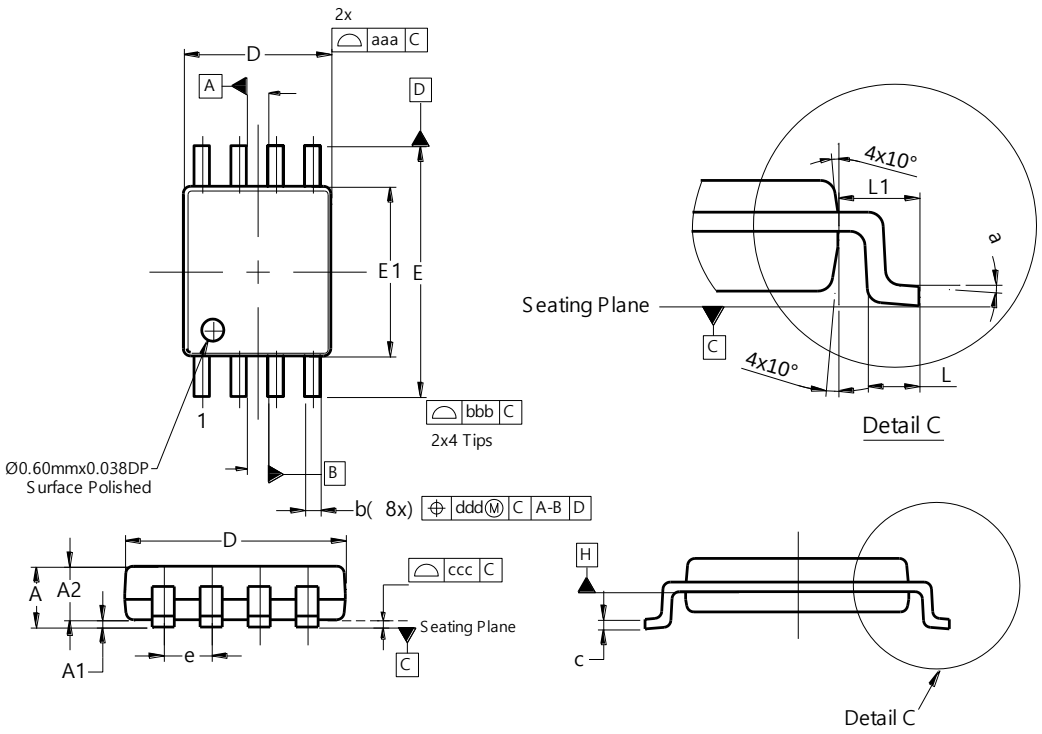
Please see http://www.diodes.com/package-outlines.html for the latest version.

SSOP-8



SSOP-8			
Dim	**Min**	**Max**	**Typ**
A	--	1.30	--
A1	0.05	0.15	--
A2	0.95	1.20	1.05
b	0.15	0.30	0.225
c	0.08	0.23	--
D	2.75	3.15	2.95
E	3.75	4.25	4.00
E1	2.70	2.90	2.80
e	--	--	0.65
L	0.20	0.60	0.40
L1	0.525	0.675	0.60
a	0°	8°	4°
aaa	0.20		
bbb	0.25		
ccc	0.10		
ddd	0.13		
All Dimensions in mm			

VSSOP-8

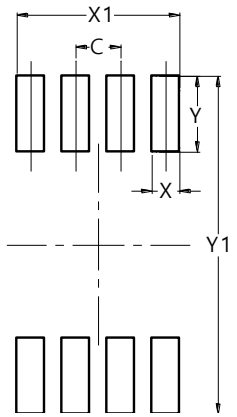


VSSOP-8			
Dim	**Min**	**Max**	**Typ**
A	0.60	0.90	--
A1	--	0.10	--
A2	0.60	0.80	--
b	0.17	0.25	0.21
c	0.08	0.13	--
D	1.90	2.10	2.00
E	3.20	3.60	3.40
E1	2.20	2.40	2.30
e	--	--	0.50
L	0.30	0.40	0.35
L1	0.50	0.60	0.55
a	0°	6°	3°
aaa	0.20		
bbb	0.25		
ccc	0.10		
ddd	0.13		
All Dimensions in mm			

Suggested Pad Layout

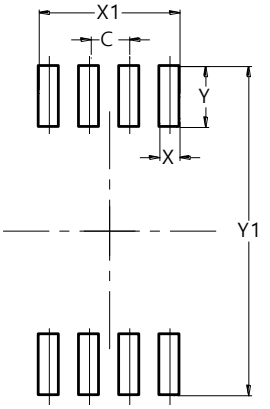
Please see http://www.diodes.com/package-outlines.html for the latest version.

SSOP-8



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	2.350
Y	1.100
Y1	4.900

VSSOP-8



Dimensions	Value (in mm)
C	0.500
X	0.250
X1	1.750
Y	0.750
Y1	4.050

Mechanical Data

SSOP-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Mate Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.0169 grams (Approximate)

VSSOP-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Mate Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.011 grams (Approximate)

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