

## Double-Data-Rate Octal SPI PSRAM

### Specifications

- Single Supply Voltage:
  - $V_{DD} = 1.62$  to  $1.98V$
  - $V_{DDQ} = 1.62$  to  $1.98V$
- Interface: Octal SPI with DDR mode, two bytes transfers per one clock cycle
- Performance: Clock rate up to 200MHz, (400MBps read/write throughput)
- Organization: 256Mb, 32M x 8bits with 2048 bytes per page
  - Column address: AY0 to AY10
  - Row address: AX0 to AX13
- Refresh: Self-managed
- Operating temperature range
  - TC =  $-40^{\circ}C$  to  $+85^{\circ}C$  (standard range)\*
  - TC =  $-40^{\circ}C$  to  $+105^{\circ}C$  (extended range)\*
- Typical mean Room Standby Current:
  - $90\mu A$  @  $25^{\circ}C$  (Standby mode)
  - $40\mu A$  @  $25^{\circ}C$  (Half Sleep Mode with data retained)
- Maximum Standby Current:
  - $1100\mu A$  @  $105^{\circ}C$
  - $680\mu A$  @  $85^{\circ}C$

\* please refer to Table 1

### Features

- Low Power Features:
  - Partial Array Self-Refresh (PASR)
  - Auto Temperature Compensated Self-Refresh (ATCSR) self-managed by a built-in temperature sensor
  - Ultra Low Power Half Sleep mode with data retention.
- Software reset
- Reset pin available
- Output driver LVCMOS with programmable drive strength
- Data mask (DM) for write operation
- Data strobe (DQS) for high speed read operation
- Write burst length, maximum 2048 Byte, minimum 2 Byte.
- Wrap & hybrid burst in 16/32/64/2K lengths.
- Linear Burst Command
- Row Boundary Crossing (RBX) read operations enabled via Mode Register

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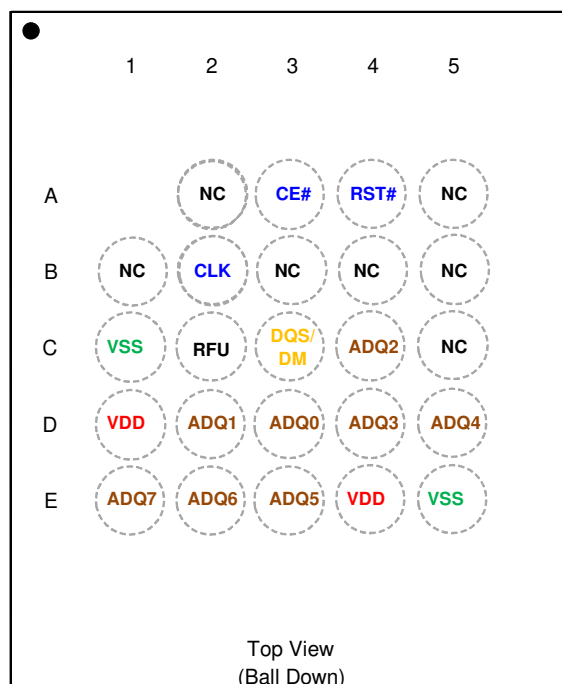
8	Change Log.....	29
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## 2 Package Information

### 2.1 Package Types : BGA 24b X8 (BD)

The APS25608N-OB Rx is available in mini-BGA 24L package 6 x 8 x 1.2mm, ball pitch 1.0mm, ball size 0.4mm, package code "BD".

- Ball Assignment for MINIBGA 24L



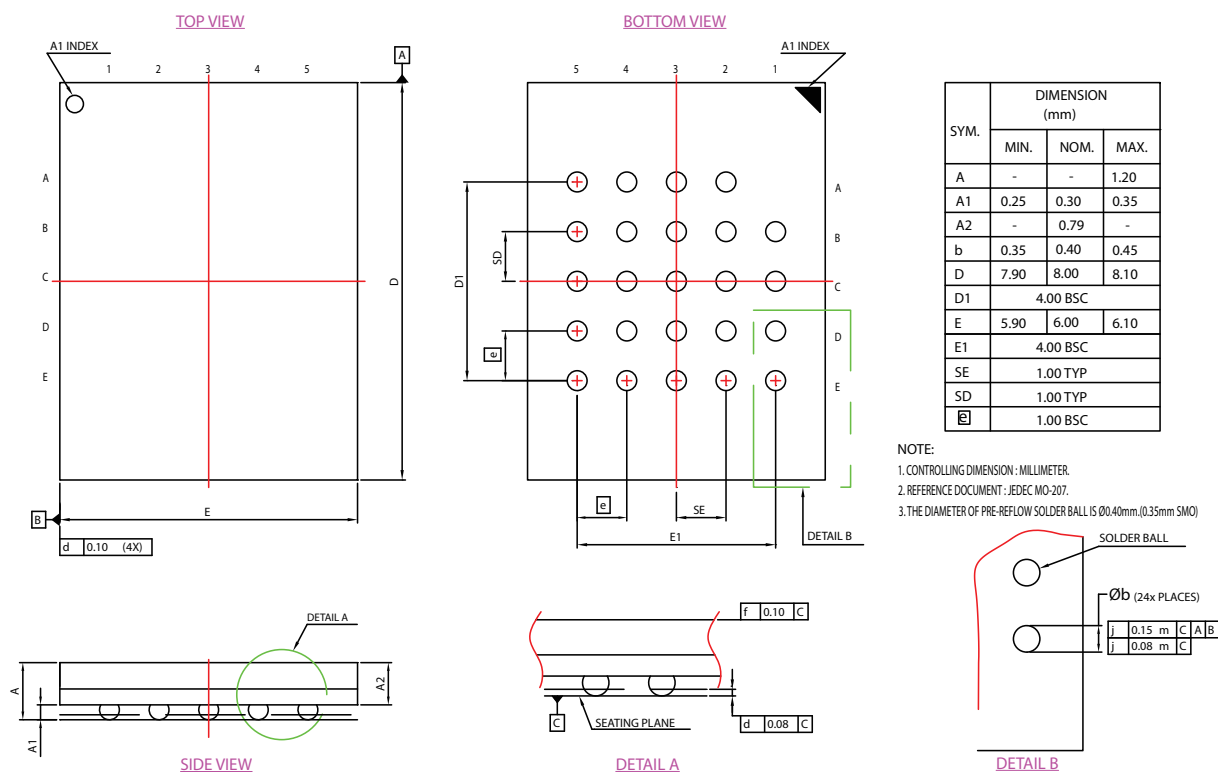
(6x8x1.2mm)(P1.0)(B0.4)

Note:

1. Part Number APS25608N-OB Rx-BD for 256Mb.
2. RFU: Reserved for Future Use, which is reserved for 2nd CE#.
3. NC: No Internal connection

## 2.2 Package Outline Drawing

### 2.2.1 BGA 24b, package code BD



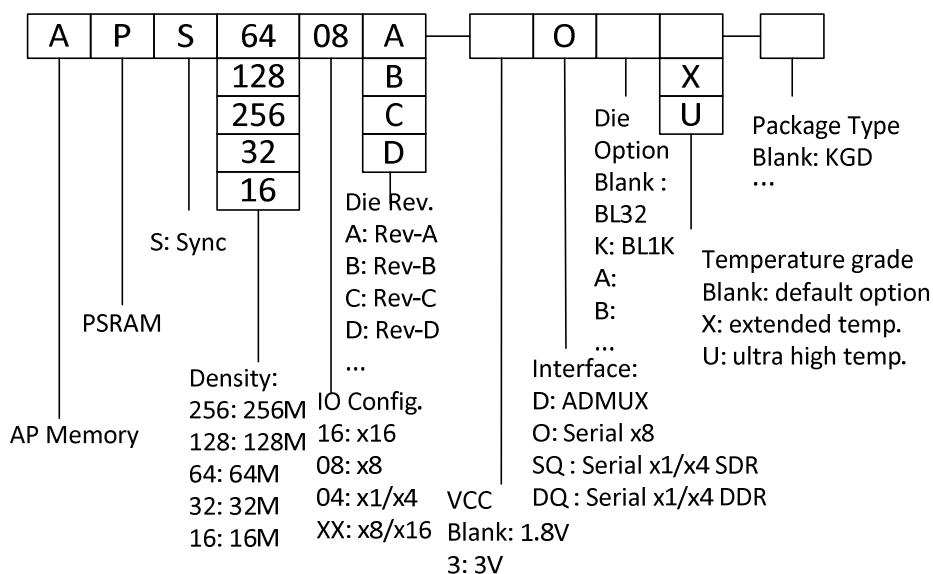
### 3 Ordering Information

**Table 1: Ordering Information**

Part Number	IO	Temperature Range	Max Frequency	Note
APS25608N-OB R	X8	Tj=-40°C to +85°C	200 MHz	Bare die
APS25608N-OB RX	X8	Tj=-40°C to +105°C	200 MHz	Bare die
APS25608N-OB R-BD	X8	Tc=-40°C to +85°C	200 MHz	BGA 24b
APS25608N-OB RX-BD	X8	Tc=-40°C to +105°C	200 MHz	BGA 24b

Note for “x”

- OB R is standard part. PN example of 24b BGA is APS25608N-OB R-BD for normal temperature grade.



## 4 Signal Table

All signals are listed in Table 2.

**Table 2: Signals Table**

<b>Symbol</b>	<b>Type</b>	<b>Description</b>	<b>Comments</b>
V <sub>DD</sub>	Power	Core & IO supply 1.8V	V <sub>DDQ</sub> short to V <sub>DD</sub> internally.
V <sub>SS</sub>	Ground	Core& IO supply ground	
A/DQ[7:0]	IO	Address/Data bus [7:0]	
DQS/DM	IO	DQ strobe clock for DQ[7:0] during all reads, Data mask for DQ[7:0] during memory writes. DM is active high. DM=1 means “do not write”.	
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state.	
CLK	Input	Input clock	
RESET#	Input	Reset signal, active low. Optional, as the pad is internally tied to a weak pull-up and can be left floating.	May not be available for all package types

## 5 Power-Up Initialization

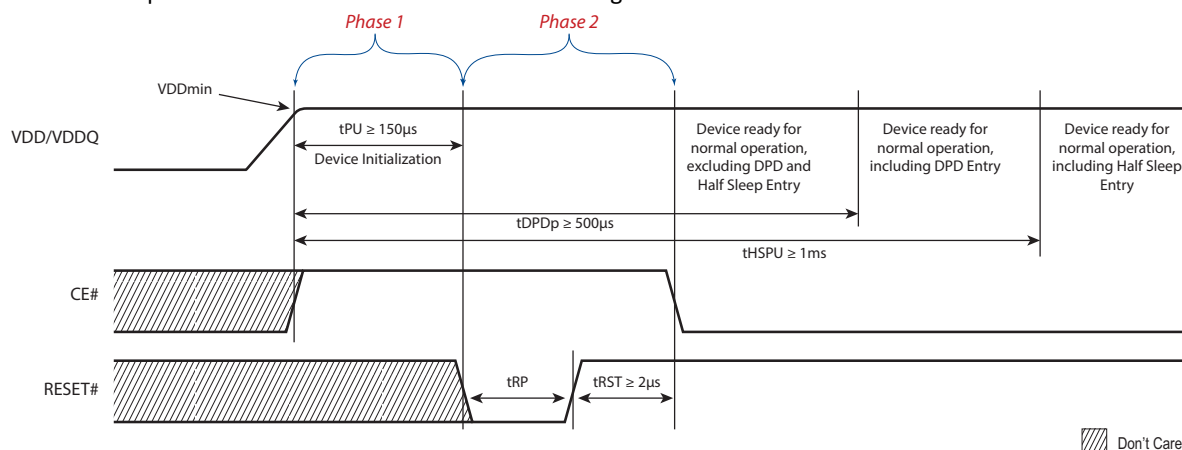
Octal DDR products include an on-chip voltage sensor used to start the self-initialization process.  $V_{DD}$  and  $V_{DDQ}$  must be applied simultaneously. When they reach a stable level at or above minimum  $V_{DD}$ , the device is in Phase 1 and it requires  $150\mu s$  to complete its self-initialization process. System host can then proceed to Phase 2 of the initialization described in section 5.1.

During Phase 1 CE# should remain HIGH (track  $V_{DD}$  within 200mV); CLK should remain LOW.

After Phase 2 is complete the device is ready for operation, however Half Sleep entry and Deep Power Down (DPD) entry are not available until Half Sleep Power Up ( $t_{HSPU}$ ) or DPD Power Up ( $t_{DPDp}$ ) durations are observed.

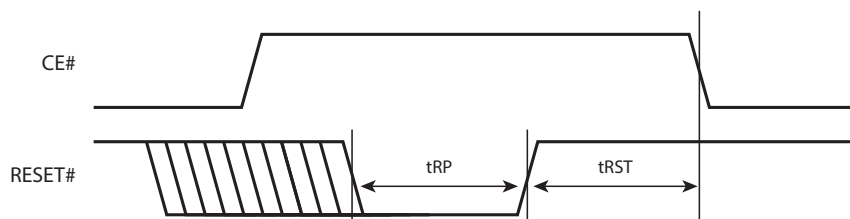
### 5.1 Power-Up Initialization Method 1 (via. RESET# pin)

The RESET# pin can be used to initialize the device during Phase 2 as follows:



**Figure 1: Power-Up Initialization Method 1 RESET#**

The RESET# pin can also be used at any time after the device is initialized to reset all register contents. Memory content is not guaranteed. Timing requirements for RESET# usage are shown below.

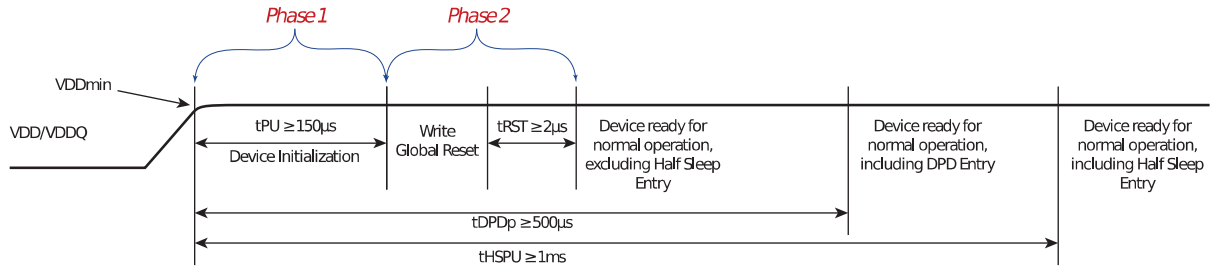


**Figure 2: RESET# Timing**



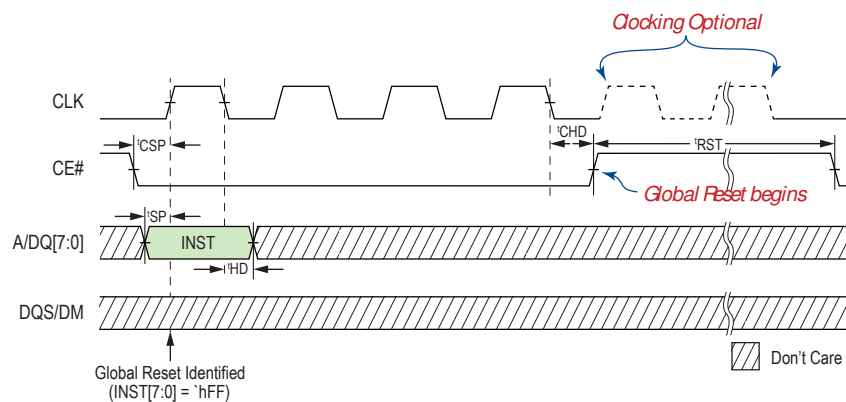
## 5.2 Power-Up Initialization Method 2 (via. Global Reset)

As an alternate power-up initialization method, after the Phase 1 150 $\mu$ s period the Global Reset command can also be used to reset the device in Phase 2 as follows:



**Figure 3. Power-Up Initialization Method 2 Timing with Global Reset**

The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is made of 4 clocked CE# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below.



**Figure 4: Global Reset**

## 6 Interface Description

### 6.1 Address Space

Octal DDR PSRAM device is byte-addressable. Memory accesses must start on even addresses (A[0]='0'). Mode Register accesses can start on even or odd address.

### 6.2 Burst Type & Length

Read and write operations are default Hybrid Wrap 32 mode. Other burst lengths of 16, 32, 64 or 2K bytes in standard or Hybrid wrap modes are register configurable (see Table 19). The device also includes command burst options for Linear Bursting. Bursts can start on any even address. Write burst length requires a minimum of 2 bytes. Read has no minimum length. Both write and read have no restriction on maximum burst length as long as tCEM is met.

### 6.3 Command/Address Latching







After CE# goes LOW, instruction code is latched on 1<sup>st</sup> CLK rising edge. Access address is latched on the 3<sup>rd</sup>, 4<sup>th</sup>, 5<sup>th</sup> & 6<sup>th</sup> CLK edges (2<sup>nd</sup> CLK rising edge, 2<sup>nd</sup> CLK falling edge, 3<sup>rd</sup> CLK rising edge, 3<sup>rd</sup> CLK falling edge).

### 6.4 Command Truth Table

The Octal DDR PSRAM recognizes commands listed in the following table. Instruction and address are input through A/DQ[7:0] pins. Host must send correct instruction and address format according to the following table.

Note that Linear Burst commands, 20h and A0h, ignore burst setting defined by MR8[2:0].

Note that only Linear Burst Read command is capable of performing row boundary crossing (RBX) read function.

Command	1st CLK		2nd CLK		3rd CLK	
						
Sync Read	00h		A3	A2	A1	A0
Sync Write	80h		A3	A2	A1	A0
Linear Burst Read	20h		A3	A2	A1	A0
Linear Burst Write	A0h		A3	A2	A1	A0
Mode Register Read	40h		x			MA
Mode Register Write	C0h		x			MA
Global Reset	FFh		x			

Remarks: x = don't care ( $V_{IH}/V_{IL}$ )

A3 = 7'bx, RA[13] {unused address bits are reserved}

A2 = RA[12:5]

A1 = RA[4:0], CA[10:8]

A0 = CA[7:0]

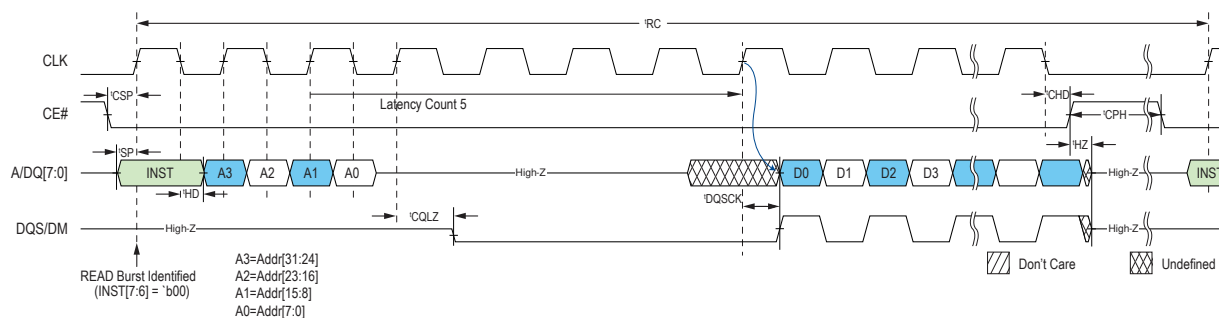
MA = Mode Register Address

## 6.5 Read Operation

After address latching, the device initializes DQS/DM to '0 from CLK rising edge of the 3<sup>rd</sup> clock cycle (A1). See Figure 5 below.

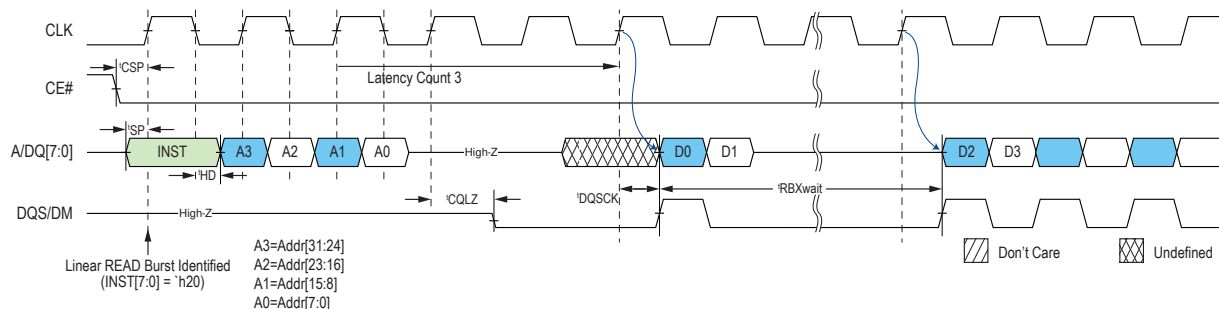
Output data is available after LC latency cycles, as shown in Figure 7 & Figure 8 . LC is latency configuration code defined in Table 5 and Table 6. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 9. Synchronous timing parameters are shown in Table 29 & Table 30.

In case of internal refresh insertion, variable latency output data may be delayed by **up to** (LCx2) latency cycles as shown in Figure 7. True variable refresh pushout latency can be anywhere **between** LC to LCx2. The 1<sup>st</sup> DQS/DM rising edge after read pre-amble indicates the beginning of valid data.

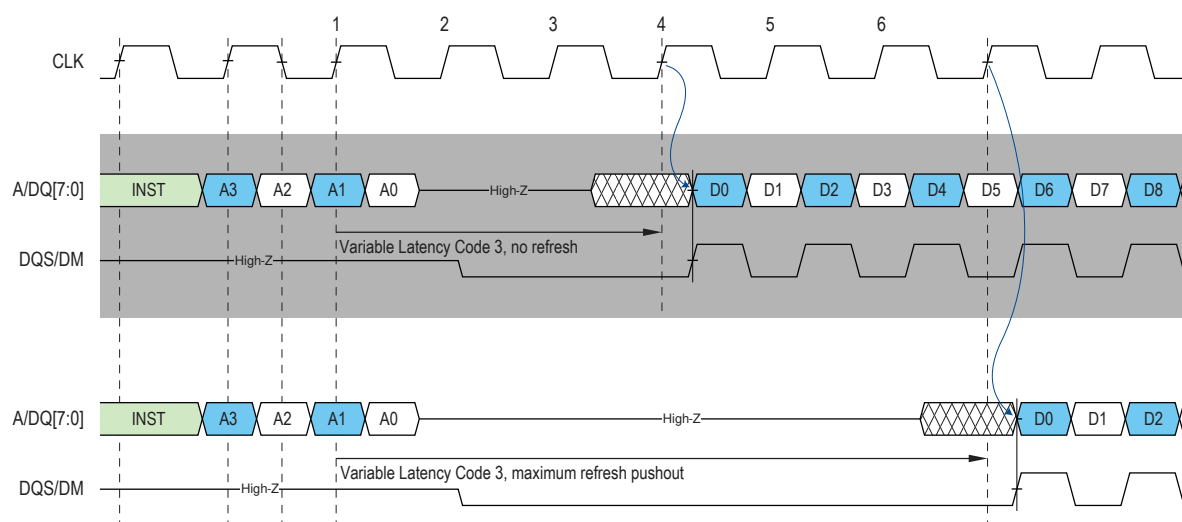


**Figure 5: Synchronous Read**

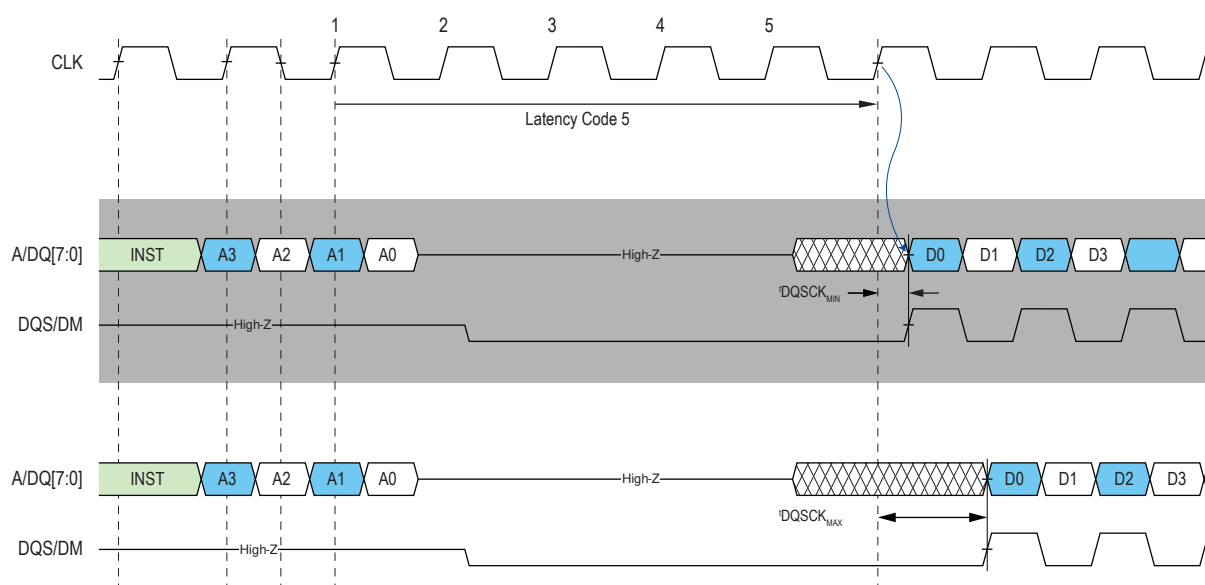
If RBX is enabled (MR8[3] written to 1) and a Linear Burst Read Command ('h20) is issued, read operation may cross row boundaries as shown in Figure 6.



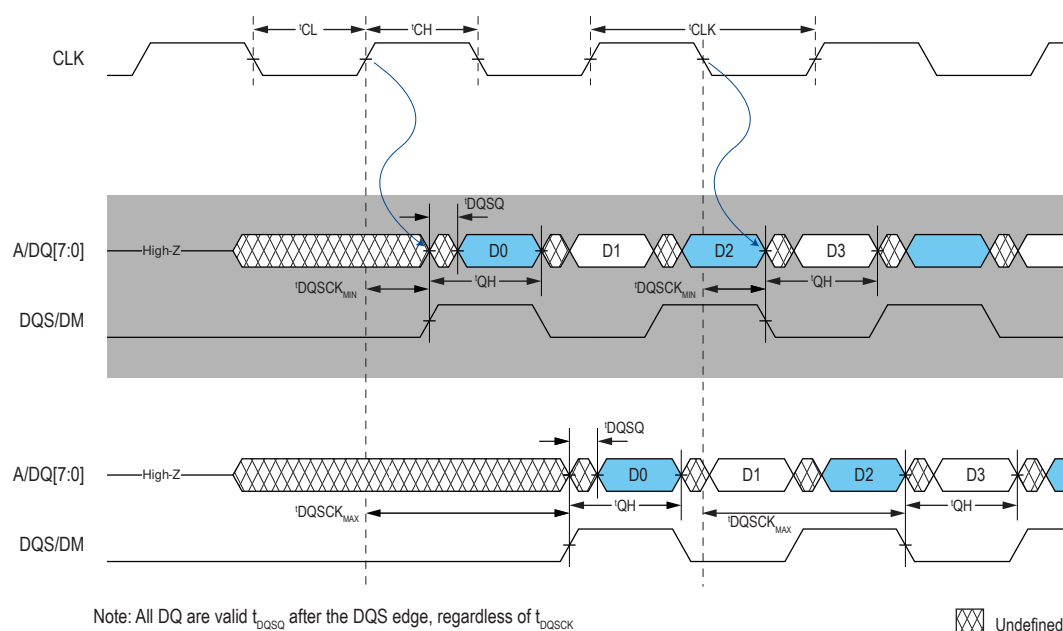
**Figure 6: Linear Burst Read with RBX (Starting address '7FE)**



**Figure 7: Variable Read Latency Refresh Pushout**



**Figure 8: Read Latency & tDQSCK**



**Figure 9: Read DQS/DM & DQ timing**

## 6.6 Write Operation

A minimum of 2 bytes of data must be input in a write operation. In the case of consecutive short burst writes,  $t_{RC}$  must be met by issuing additional CE# high time between operations. Single-byte write operations can be done by masking through DQS/DM pin as shown in Figure 10.

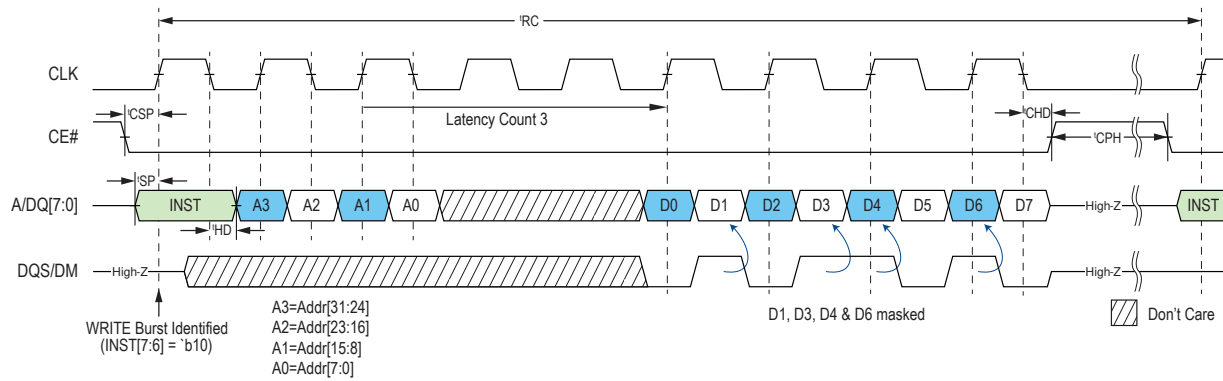


Figure 10: Synchronous Write followed by any Operation

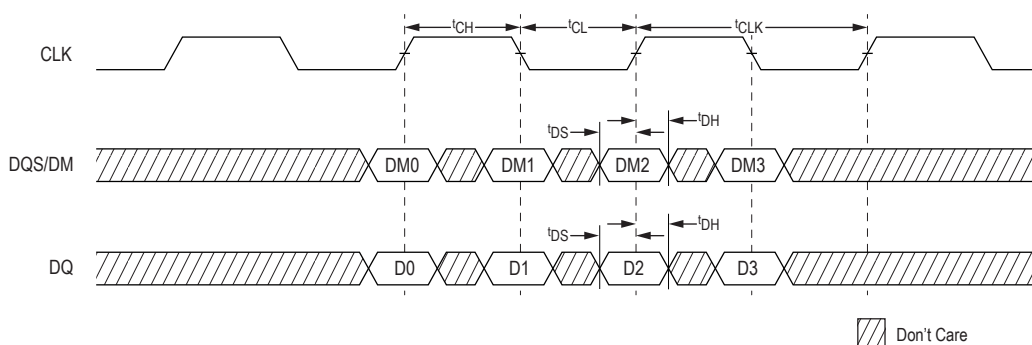


Figure 11: Write DQS/DM & DQ Timing

## 6.7 Control Registers

Register Read is shown below. Mode Address in command determines which Mode Register is read from as Data0 (see chart in the Figure below).

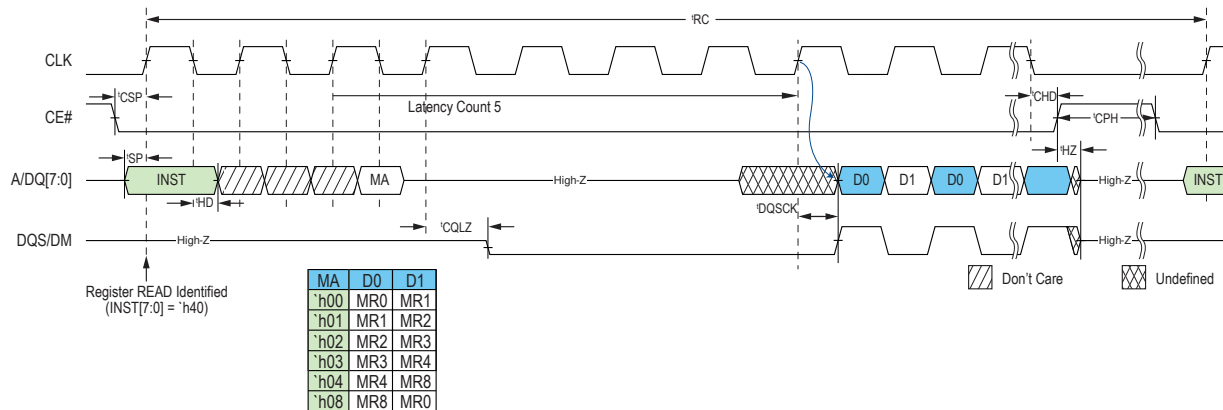


Figure 12: Register Read

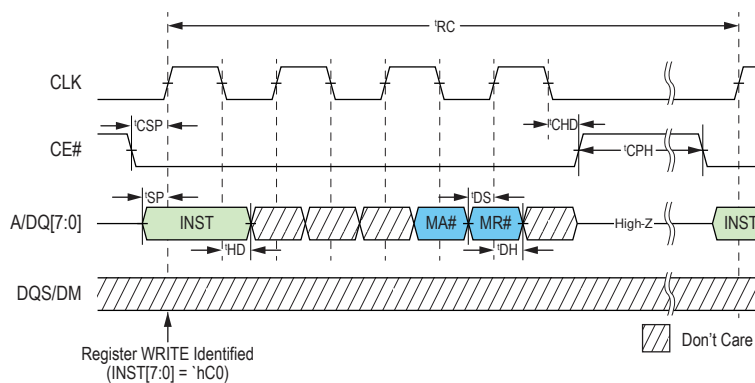


Figure 13: Register Write

Register Writes are always latency 1. Write Latency Code, MR4[7:5] does not apply to Register writes. Register Reads follow the same read latency settings, defined in MR0[4:2] (see Table 6).

Registers 0, 4 & 8 are read and writable. Registers 1, 2 and 3 are read-only. Register 6 is write-only.

Register mapping is shown in Table 3. All MR0 or MR8 writes must have MR0[7:6] or MR8[7:6] written to '0(s).

**Table 3: Mode Register Table**

MR No.	MA[7:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h00	R/W	'00'		LT	Read Latency Code			Drive Str.	
1	`h01	R	ULP	rsvd.		Vendor ID				
2	`h02	R	KGD			Dev ID		Density		
3	`h03	R	RBXen	0	SRF		rsvd.			
4	`h04	R/W	Write Latency Code			RF rate		PASR		
6	`h06	W	Half Sleep				rsvd.			
8	`h08	R/W	'0'	'0'	rsvd		RBX	BT	BL	

**Table 4: Read Latency Type MR0[5]**

Latency Type	
MR0[5]	LT
0	Variable (default)
1	Fixed

**Table 5: Read Latency Codes MR0[5:2]**

	VL Codes (MR0[5]=0)		FL Codes (MR0[5]=1)	Max Input CLK Freq (MHz)	
MR0[4:2]	Latency (LC)	Max push out (LCx2)	Latency (LCx2)	Standard	Extended
000	3	6	6	66	66
001	4	8	8	109	109
010	5 (default)	10	10	133	133
011	6	12	12	166	166
100	7	14	14	200	200
others	reserved			-	-

**Table 6: Operation Latency Code Table**

Type	Operation	VL (default)		FL
		No Refresh	Refresh	
Memory	Read	LC	Up to LCx2	LCx2
	Write	WLC		WLC
Register	Read	LC		LC
	Write	1		1

\*Note: see Table 15 for WLC settings.



**Table 7: Drive Strength Codes MR0[1:0]**

<b>Codes</b>	<b>Drive Strength</b>
'00	Full (25Ω default)
'01	Half (50Ω)
'10	1/4 (100Ω)
'11	1/8 (200Ω)

**Table 8: Ultra Low Power Device mapping MR1[7]**

<b>ULP</b>	
'0	Non-ULP (no Half Sleep)
'1	ULP (Half Sleep supported)

**Table 9: Vendor ID mapping MR1[4:0]**

<b>Vendor ID</b>
01101: APM

**Table 10: Good-Die Bit MR2[7:5]\***

<b>Codes</b>	<b>Good Die ID</b>
'110	PASS
others	FAIL

\*Note: Default is FAIL die, and only mark PASS after all tests passed.

**Table 11: Device ID MR2[4:3]**

<b>Codes</b>	<b>Device ID</b>
'00	Generation 1
'01	Generation 2
'10	Generation 3
'11	Generation 4 (default)

**Table 12: Device Density mapping MR2[2:0]**

<b>MR2[2:0]</b>	<b>Density</b>
'101	128Mb
'111	256Mb
'110	512Mb
others	reserved

**Table 13: Row Boundary Crossing Enable MR3[7]**

<b>MR3[7] (read-only)</b>	<b>RBXen</b>
0	RBX not supported
1	RBX supported via MR8[3]=1

**Table 14: Self Refresh Flag MR3[5:4]**

MR3[5:4] indicates current device refresh rate. Refresh rate depends on temperature and refresh frequency configuration, set by MR4[4:3].

<b>MR3[5:4] (read-only)</b>	<b>Self Refresh Flag</b>
01	0.5x Refresh
00	1x Refresh
10	4x Refresh
11	reserved

**Table 15: Write Latency MR4[7:5]**

Write latency, WLC, is default to 5 after power up. Use MR Write to set write latencies according to write latency table. When operating frequency exceeding Fmax listed in the table will result in write data corruption.

<b>MR4[7:5]</b>	<b>Write Latency Codes (WLC)</b>	<b>Fmax (MHz)</b>
000	3	66
100	4	109
010	5 (default)	133
110	6	166
001	7	200
Others	reserved	-

**Table 16: Refresh Frequency setting MR4[4:3]**

<b>MR4[4:3]</b>	<b>Refresh Frequency</b>
x0	Always 4x Refresh (default)
01	Enables 1x Refresh when temperature allows
11	Enable 0.5x Refresh when temperature allows

Note: x= don't care

**Table 17: PASR MR4[2:0]**

The PASR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

<b>256Mb X8</b>				
<b>Codes</b>	<b>Refresh Coverage</b>	<b>Address Space</b>	<b>Size</b>	<b>Density</b>
'000	Full array (default)	0000000h-1FFFFFFh	32M X8	256Mb
'001	Bottom 1/2 array	0000000h-0FFFFFFh	16M X8	128Mb
'010	Bottom 1/4 array	0000000h-07FFFFFFh	8M X8	64Mb
'011	Bottom 1/8 array	0000000h-03FFFFFFh	4M X8	32Mb
'100	None	0	0M	0Mb
'101	Top 1/2 array	1000000h-1FFFFFFh	16M X8	128Mb
'110	Top 1/4 array	1800000h-1FFFFFFh	8M X8	64Mb
'111	Top 1/8 array	1C00000h-1FFFFFFh	4M X8	32Mb

**Table 18: Half Sleep MR6[7:0]**

<b>MR6[7:0]</b>	<b>ULP Modes</b>
'hF0	Half Sleep
'hC0	Deep Power Down
others	reserved

Note: see 6.8 Half Sleep Mode; 6.9 Deep Power Down Mode for more information.

**Table 19: Burst Type MR8[2], Burst Length MR8[1:0]**

By default the device powers up in 32 Byte Hybrid Wrap. In non-Hybrid burst (MR8[2]=0), MR8[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid burst wrap is selected (MR8[2]=1), the device will burst through the initial wrapped burst length once, then continue to burst incrementally up to maximum column address (2K) before wrapping around within the entire column address space. Burst length (MR8[1:0]) can be set to 16,32,64 & 2K Lengths.

<b>MR8[2]</b>	<b>MR8[1:0]</b>	<b>Burst Length</b>	<b>Example of Sequence of Bytes During Wrap</b>	
			<b>Starting</b>	<b>Burst Address Sequence</b>
'0	'00	16 Byte Wrap	4	[4,5,6,...15,0,1,2,...]
'0	'01	32 Byte Wrap	4	[4,5,6,...31,0,1,2,...]
'0	'10	64 Byte Wrap	4	[4,5,6,...63,0,1,2,...]
'0	'11	2K Byte Wrap	4	[4,5,6,...2047,0,1,2,...]
'1	'00	16 Byte Hybrid Wrap	2	[2,3,4,...15,0,1],16,17,18,...2047,0,1,...
'1	'01	32 Byte Hybrid Wrap (default)	2	[2,3,4,...31,0,1],32,33,34,...2047,0,1,...
'1	'10	64 Byte Hybrid Wrap	2	[2,3,4,...63,0,1],64,65,66,...2047,0,1,...
'1	'11	2K Byte Wrap	2	[2,3,4,...2047,0,1,2,...]

The Linear Burst Commands (INST[5:0]=6'b10\_0000) forces the current array read or write command to do 2K Byte Wrap (equivalent to having MR8[1:0] set to 2'b11). For non-RBX Enabled devices the burst command read/writes linearly from the starting address and wraps back to the beginning of the page upon reaching the end of the page. To access a different page, host must issue a new command.

**Table 20: Row Boundary Crossing Read Enable MR8[3]**

This register setting applies to Linear Burst reads only on RBX enabled devices (MR3[7]=1). Default write and read burst behavior is limited within 2K page (row) address space (CA='h000 -> 'h7FF). Setting this bit high will allow Linear Burst Read command to cross over into the next Row (RA+1).

<b>MR8[3]</b>	<b>RBX Read</b>
0	Reads stay within page (row) boundary
1	Allow reads cross page (row) boundary

## 6.8 Half Sleep Mode

Half Sleep Mode puts the device in an ultra-low power state, while the stored data is retained. Half Sleep Mode Entry is entered by writing 8'hF0 into MR6. CE# going high initiates the Half Sleep mode and must be maintained for the minimum duration of Half Sleep time, t<sub>HS</sub>. The Half Sleep Entry command sequence is shown below.

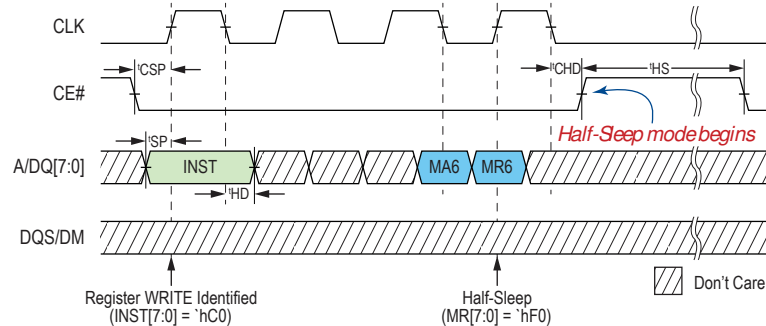


Figure 14: Half Sleep Entry Write (latency same as Register Writes, WL1)

Half Sleep Exit is initiated by a low pulsed CE#. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum Half Sleep Exit time, t<sub>XHS</sub>).

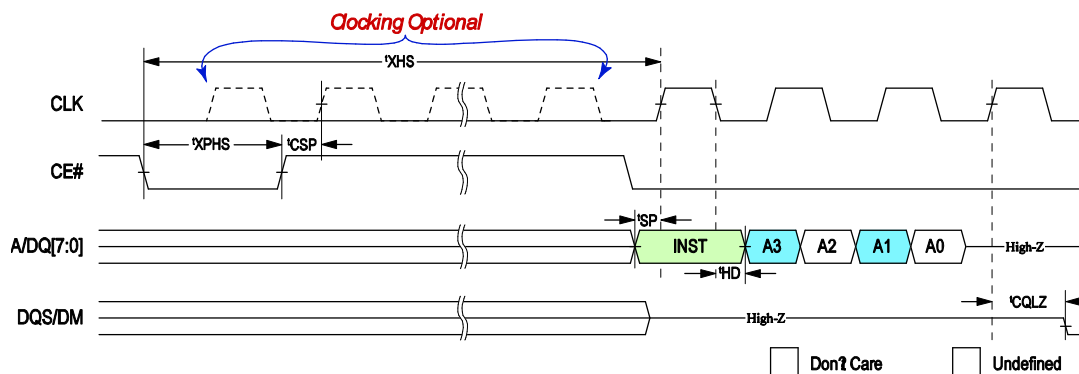


Figure 15: Half Sleep Exit (Read Operation shown as example)

## 6.9 Deep Power Down Mode

Deep Power Down Mode (DPD) puts the device into power down state. DPD Mode Entry is entered by writing 8'hC0 into MR6. CE# going high initiates the DPD Mode and must be maintained for the minimum duration of Deep Power Down time, tDPD. The Deep Power Down Entry command sequence is shown below.

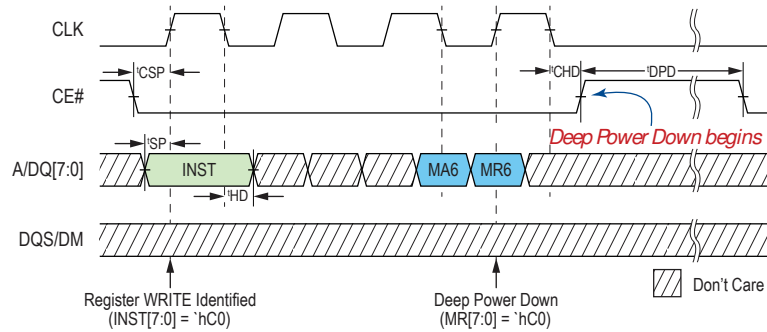


Figure 16: Deep Power Down Entry

Deep Power Down Exit is initiated by a low pulsed CE#. After a CE# DPD exit, CE# must be held high with or without clock toggling until the first operation begins (observing minimum Deep Power Down Exit time, tXDPD).

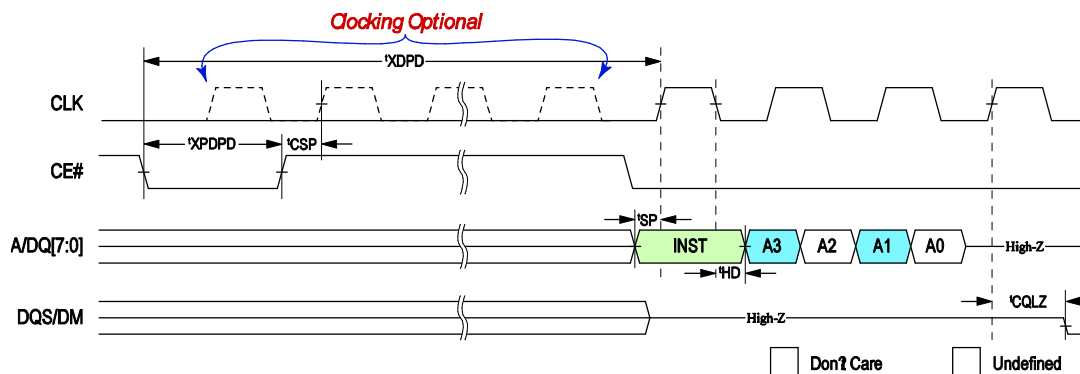


Figure 17: Deep Power Down Exit (Read Operation shown as example)

Register values and memory content are not retained in DPD Mode. After DPD mode register values will reset to defaults. tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial powerup to the first DPD entry.

## 7 Electrical Specifications:

### 7.1 Absolute Maximum Ratings

**Table 21: Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit	Notes
Voltage to any ball except $V_{DD}$ , $V_{DDQ}$ relative to $V_{SS}$	VT	-0.4 to $V_{DD}/V_{DDQ}+0.4$	V	
Voltage on $V_{DD}$ supply relative to $V_{SS}$	$V_{DD}$	-0.4 to +2.45	V	
Voltage on $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DDQ}$	-0.4 to +2.45	V	
Storage Temperature	$T_{STG}$	-55 to +150	°C	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### 7.2 Pin Capacitance

**Table 22: Bare Die Pin Capacitance**

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		1	pF	VIN=0V
Output Pin Capacitance	COUT		2	pF	VOU=0V

Note 1: spec'd at 25°C.

**Table 23: Package Pin Capacitance**

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		TBD	pF	VIN=0V
Output Pin Capacitance	COUT		TBD	pF	VOU=0V

Note 1: spec'd at 25°C.

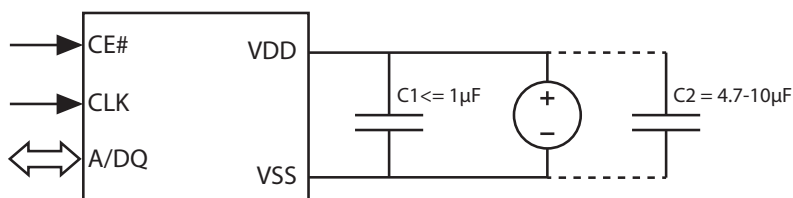
**Table 24: Load Capacitance**

Parameter	Symbol	Min	Max	Unit	Notes
Load Capacitance	$C_L$		15	pF	

Note 1: System  $C_L$  for the use of package

### 7.3 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



#### 7.3.1 Low ESR cap C1:

It is recommended to place a low ESR decoupling capacitor of  $\leq 1\mu\text{F}$  close to the device to absorb transient peaks.

#### 7.3.2 Large cap C2:

Though half-sleep average current is small (less than  $100\mu\text{A}$ ), its peak current from internal periodical burst refresh can reach up to the level of  $25\text{mA}$ . The peak current duration can last for few tens of microseconds. During this period if the system regulator cannot supply such large peaks, it is important to place a  $4.7\mu\text{F}$ - $10\mu\text{F}$  cap to cover the burst refresh current demand and replenish the cap before the next burst of refresh.

If needed, contact AP Memory for further decoupling solution assistance.

### 7.4 Operating Conditions

**Table 25: Operating Characteristics**

Parameter	Min	Max	Unit	Notes
Operating Temperature (extended)	-40	105	°C	1
Operating Temperature (standard)	-40	85	°C	

Note 1: Extended temp range of -40 to 105°C is only characterized; test condition is -32 to 105°C.



## 7.5 DC Characteristics

**Table 26: DC Characteristics**

Symbol	Parameter	Min	Max	Unit	Notes
V <sub>DD</sub>	Supply Voltage	1.62	1.98	V	
V <sub>DDQ</sub>	I/O Supply Voltage	1.62	1.98	V	
V <sub>IH</sub>	Input high voltage	V <sub>DDQ</sub> -0.4	V <sub>DDQ</sub> +0.3	V	
V <sub>IL</sub>	Input low voltage	-0.3	0.4	V	
V <sub>OH</sub>	Output high voltage (I <sub>OH</sub> =-0.2mA)	0.8 V <sub>DDQ</sub>		V	
V <sub>OL</sub>	Output low voltage (I <sub>OL</sub> =+0.2mA)		0.2 V <sub>DDQ</sub>	V	
I <sub>LI</sub>	Input Pin leakage current		1	μA	
I <sub>LO</sub>	Output Pin leakage current		1	μA	
ICC	Read/Write @13MHz		5	mA	1
	Read/Write @133MHz		19	mA	1
	Read/Write @166MHz		22	mA	1
	Read/Write @200MHz		26	mA	1
ISB <sub>EXT</sub>	Standby current (extended temp)		1100	μA	2
ISB <sub>STD</sub>	Standby current (standard temp)		680	μA	2
ISB <sub>STDroom</sub>	Standby current (room temp)			μA	2,3,4
ISB <sub>STDHS</sub>	Standby current (half sleep 25°C)			μA	2,3,5,6
ISB <sub>STD DP</sub>	Standby current (Deep Power Down -40°C to 85°C)		20	μA	7

Note 1: Current is only characterized.

Note 2: Without CLK toggling. ISB will be higher if CLK is toggling.

Note 3: 0.5x Refresh.

Note 4: **Typical mean ISB<sub>STDROOM</sub> 90uA.**

Note 5: Current is only guaranteed after 150ms into Half Sleep mode.

Note 6: **Typical mean ISB<sub>STDHS</sub> 40uA**

Note 7: **Typical mean ISB<sub>STD DP</sub> 8uA at 25°C**

## 7.6 ISB Partial Array Refresh Current

Table 27: Typical-mean PASR Current @ 25°C

Standby Current @ 25°C			
PASR	ISB –typical mean	Unit	Notes
Full	90	μA	1, 2
1/2	80	μA	1, 2
1/4	75	μA	1, 2
1/8	72	μA	1, 2
Half Sleep Current @ 25°C			
PASR	I Half Sleep-typical mean	Unit	Notes
Full	40	μA	1,2,3
1/2	30	μA	1,2,3
1/4	25	μA	1,2,3
1/8	22	μA	1,2,3

Table 28: Typical-mean PASR Current @ 105°C /85°C

Standby Current @ 85°C			
PASR	ISB –typical mean	Unit	Notes
Full	530	μA	2
1/2	370	μA	2
1/4	290	μA	2
1/8	250	μA	2
Half Sleep Current @ 85°C			
PASR	I Half Sleep-typical mean	Unit	Notes
Full	440	μA	2, 3
1/2	300	μA	2, 3
1/4	230	μA	2, 3
1/8	190	μA	2, 3

Note1: Current at 25°C is only attainable by enabling 0.5x Refresh Frequency (see Table 17)

Note2: PASR Current is only characterized without CLK toggling.

Note3: Spec'd Half Sleep current is only guaranteed after 150ms into Half Sleep mode.

## 7.7 AC Characteristics

**Table 29: READ/WRITE Timing**

		<b>KGD/BGA 1.8V Only</b>							
		<b>-7(133MHz)</b>		<b>-6(166MHz)</b>		<b>-5(200MHz)</b>			
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>	<b>Notes</b>
tCLK	CLK period	7.5		6		5		ns	
tCH/tCL	Clock high/low width	0.45	0.55	0.45	0.55	0.45	0.55	tCLK	
tKHL	CLK rise or fall time		1.2		1		0.8	ns	
tCPH	CE# HIGH between subsequent burst operations	15		18		24		ns	
tCEM	CE# low pulse width (excluding Half Sleep exit)		2		2		2	μs	Standard temp
			0.5		0.5		0.5	μs	Extended temp
tCEM	CE# low pulse width	3		3		3		tCLK	Minimum 3
tCSP	CE# setup time to CLK rising edge	2		2		2		ns	
tCHD	CE# hold time from CLK falling edge	2		2		2		ns	
tSP	Setup time to active CLK edge	0.8		0.6		0.5		ns	
tHD	Hold time from active CLK edge	0.8		0.6		0.5		ns	Max 0.75*tCLK
tHZ	Chip disable to DQ/DQS output high-		6		6		6	ns	
tRBWait	Row Boundary Crossing Wait Time	30	65	30	65	30	65	ns	
tRC	Write Cycle	60		60		60		ns	
tRC	Read Cycle	60		60		60		ns	
tHS	Minimum Half Sleep duration	150		150		150		μs	
tXHS	Half Sleep Exit CE# low to CLK setup time	150		150		150		μs	
tXPHS	Half Sleep Exit CE# low pulse width	60		60		60		ns	
			2		2		2	μs	Standard temp
			0.5		0.5		0.5	μs	Extended temp
tDPD	Minimum DPD duration	500		500		500		μs	
tDPDp	Minimum period between DPD	500		500		500		μs	
tXDPD	DPD CE# low to CLK setup time	150		150		150		μs	
tXPDPD	DPD Exit CE# low pulse width	60		60		60		ns	
tPU	Device Initialization	150		150		150		μs	
tRP	RESET# low pulse width	1		1		1		μs	
tRST	Reset to CMD valid	2		2		2		μs	

**Table 30: DDR timing parameters**

		<b>KGD/BGA 1.8V Only</b>							
		<b>-7(133MHz)</b>		<b>-6(166MHz)</b>		<b>-5(200MHz)</b>			
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>	<b>Notes</b>
tCQLZ	Clock rising edge to DQS low	1	6	1	6	1	6	ns	
tDQSCK	DQS output access time from CLK	2	6.5	2	6.5	2	6.5	ns	
tDQSQ	DQS – DQ skew		0.6		0.5		0.4	ns	
tDS	DQ and DM input setup time	0.8		0.6		0.5		ns	
tDH	DQ and DM input hold time	0.8		0.6		0.5		ns	
tHP	Half Period	= min (tCH, tCL)						ns	
tQHS	Datahold skew factor		0.75		0.6		0.5	ns	
tQH	DQ output hold time from DQS	= tHP - tQHS						ns	

## 8 Change Log

Version	Date	Description
0.29	Jul 08, 2019	Initial Version derived from E7 XX 0.29; Update table 28
0.3	Jul 16, 2019	Update ball assignment, tXPHS
0.31	Jul 17, 2019	Update VDDQ information
0.32	Aug 2, 2019	Updated note for RFU, NC, and DC Characteristics; Updated Deep Power Down Mode description and PASR table
0.33	Aug 23, 2019	Updated tHS, package code, note for ball assignment
0.34	Aug 29, 2019	Updated note for DC Characteristics
0.35	Dec 12, 2019	Updated Figure 15 and Figure 17
0.40	Jun 11, 2020	Drive strength: 25 Ohm (default). Remove all room temperature maximum spec.(Standby mode & Half Sleep mode).
1.00	Jul 27, 2020	ICC updated. Revised Typical-mean PASR Current.

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