Kneron KL520 series AI SoC

Datasheet

Revision History:

version	description	date
0.1	Initial version	2019/1/18
0.2	Re-arrange updated information	2019/2/15
0.3	Pin definition & package update	2019/3/25
1.0	Electrical characteristics & Ordering information	2019/5/31
1.1	Adding pinmux table	2019/7/1
1.2	Update 7.2 ordering information	2019/7/12
1.3	Update temperature range	2019/8/6
1.4	Update pinmux I/O description	2019/8/28
1.5	Update low power description and package/ordering/reflow information	2019/12/12
1.6	Update pinmux I/O description	2020/2/4
1.7	Update ambient temperature	2020/9/4

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1 Overview

1.1 General description

Kneron KL520 series is an AI SoC targeting smart-home and IoT segment with Kneron NPU core inside to accelerate neural network processing and enabling devices with edge AI ability to achieve Kneron's AI everywhere vision.

The NPU core is designed to accelerate major computing layers inside the convolutional neural network (CNN), to off-load the heavy computing from traditional CPU or GPU architecture. Thus Kneron AI SoC can achieve edge side AI computing with only entry level MCU accompanied with Kneron NPU core, and saves hardware cost and power consumption.

Kneron KL520 series AI SoC is suitable for door lock, access control, doorbell, web camera, smart toy, home appliance, surveillance scenarios, and ready for RGB, NIR, depth image sensors. So system makers can easily find a suitable image sensors to realize their application and achieve AI everywhere with Kneron KL520 inside.

1.2 Key specification

NPU

- Maximum Frequency @ 300 MHz
- Peak Throughput of 8-bit mode: 345 GOPS, 576MAC/cycle

CPU

- ARM Cortex-M4@200MHz for system control
- ARM Cortex-M4@250MHz as AI co-processor

SDRAM

- SIP, 32MB or 64MB, 16-bit LPDDR2-1066

External flash

- Up to 64 MB SPI NOR flash

Supporting OS

- CMSIS RTX

Power

- Average power consumption 380mW
- 1.1V core voltage
- 3.3V I/O voltage

Video in interface

- Two MIPI-CSI-2 RX port with 2-lane each
- DPI

Video out interface

- 2-lane MIPI-DSI-1.2 TX
- LCD (DPI)

- LCM

Audio Interface

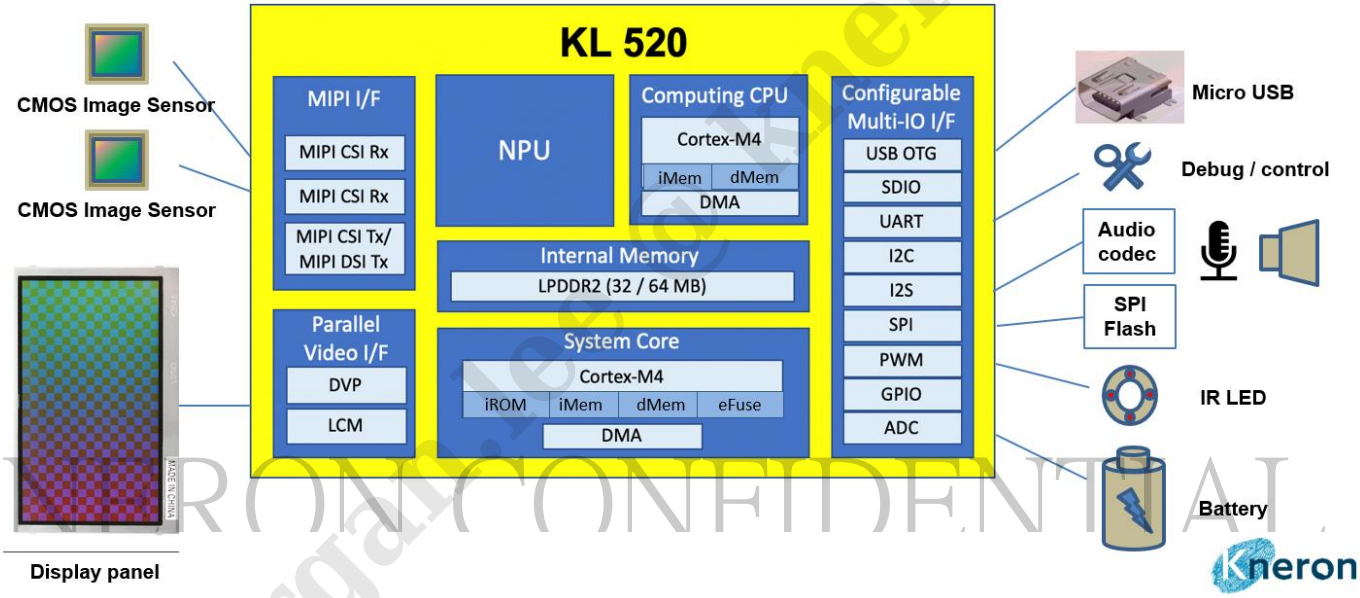
- I2S

Peripheral Interface

- I2C
- SPI
- UART
- USB 2.0 OTG interface
- PWM
- GPIO
- SDIO

1.3 Block diagram

Here is the KL520 system block diagram. Which describes the dedicated component for AI SoC.



2 Functional Description

2.1 CPU

In order to get the optimized performance and efficiency, there are two Cortex-M4 embedded in KL520-series. System CPU is designed for the chip-level operation which is equipped with i-mem of 96KB and d-mem of 96KB. Major work items are serviced RTOS, IO driver, video input and output, 3rd party application.
AI computing CPU is designed for the computer vision function with NPU to assist AI computing which is equipped with i-mem of 64KB and d-mem of 64KB. Dual CPU running by shared memory.

2.2 NPU

Kneron's self-developed 2nd generation NPU is embedded in KL520-series. It is lego-like architecture to service popular CNN models such as TinyYolo, ResNET, Mobilenet. It supports reconfigurable mechanism and can be updated on the field.

2.3 DRAM

LPDDR2 is embedded in KL520-series to reduce the power consumption. 32MB and 64MB are two capacity options for different applications. KL520 have total 2GB/s bandwidth for NPU and System processing use.

2.4 MIPI CSI RX

KL520-series provides two high-resolution, high-speed and flexible interconnects of the MIPI CSI receiver port. It is compliant with the Camera Serial Interface 2 (CSI-2) and supports the MIPI Alliance specifications. The supported data rate is up to 1.2 Gbps per data lane and it is scalable from one to two data lanes per port

2.5 MIPI CSI TX

KL520-series provides a high-resolution high-speed flexible interconnection of the MIPI CSI transceiver. It is compliant with the Camera Serial Interface 2 (CSI-2) and supports the MIPI Alliance specifications. The supported data rate is up to 1.2 Gbps per data lane and it is scalable from one to two data lanes. This feature allow KL520 behaves as a sensor with AI function for customer's SOC platform.

2.6 MIPI DSI TX

KL520-series DSI host controller provides a high-resolution, high-speed, and flexible interconnect for the display panel. It is compliant with the Display Serial Interface (DSI) and supports MIPI Alliance specifications, which include Display Pixel Interface (DPI-2), Display Bus Interface (DBI-2), Display Command Set (DCS). The supported data rate is up to 1.2 Gbps per lane and it is scalable from one to two data lanes.

2.7 DVP video interface

To link with the general parallel video interfaces Sensor/Panel in the market, KL520-series provides DPI (parallel input interface) for RGB format (RGB-888 / RGB-565) and YUV format (YUV422). Same Pin can be configured for LCD output for video output application.

For simple text message application. KL520 also provide generic LCM interface for customer easy use.

2.8 I2C

I2C in KL520-series is configurable to be able to serve as a master or slave residing on the I2C bus. The master is a active device that initiates the data transfers on the bus and generates the clock signals to conduct the transfers. During these transfers, any addressed device is considered a slave. Data are transmitted and received from the I2C bus through a buffered interface. Two wires, the serial data (SDA) and serial clock (SCL), carry information between devices connected to the bus. Max

2.9 I2S

Since I2S is a populate audio format provided by many audio devices, KL520-series provides this interface to transfer digital audio data. Both Master or Slave mode codec are supported.

2.10 UART

UART in KL520-series provides the standard communications channel for diagnosis or management purpose of this SOC chip. In UART mode, the operation is backward compatible to the 16550 which widely supported by existing system software.

2.11 USB

USB2.0 in KL520-series can be configured for host or device applications because of its OTG capability, which enable an easy connection between the USB peripherals and any USB-ready product. The high speed data rate leading to the optimal performance in applications spanning a wide variety of the consumer markets. The USB 2.0 OTG are fully compliant with the USB 2.0 specification.

3.2 Compliance with USB2.0 specification

3.2 Support high speed 480Mb/s and full speed 12Mb/s data rate

3.2 Support control, bulk, isochronous and interrupt transfer

3.2 Support UVC 1.5 & 1.0

3.2 Embedded USB transceiver and clock generator

3.2 Simple packet data transfer control

3.2 Internal DMA mode for efficient data transfer between USB controller and internal memory

2.12 SPI

KL520-series contains SPI interface controller to execute the SPI Flash command as ROM and link with other devices.

2.13 GPIO

KL520-series provides a flexible, configurable and programmable general-purpose I/O. The options to remove or add the interrupt sense, bouncing clock, and pull high/low circuits are programable. The attributes of each GPIO pin, such as input/output, bypass, interrupt sense, clock source, and pull type can be programmed to fit the user specification. GPIO also equipped with de-bouncing buffer that suitable for the noisy input environment.

2.14 SDIO

KL520-series has a host controller of the SD (Secure Digital) interface which is compliant with the SD physical layer specification, version 3.0.

2.15 PWM

KL520-series' s internal timer supports the PWM (Pulse Width Modulation) function to generate the PWM signals for the motor control or power level control.

3 Pin Descriptions

3.1 Peripheral and video I/O configuration

Package		LQFP 128		TFBGA 159		TFBGA 161	
Config. Mode (1)		Config 1	Config 2	Config 3	Config 4	Config 5	Config 6
MIPI inputs	MIPI CSI Rx	1 (2Lanx1)	2 (1Lanx1, 2Lanx1)	2 (2Lanx2)	2 (2Lanx2)	1 (2Lanx1)	1 (2Lanx1)
MIPI output	MIPI CSI Tx MIPI DSI Tx	N/A	N/A	N/A	N/A	CSI or DSI x1 (2Lanx1)	
Camera Interface	DVP	N/A	N/A	0	0	0	1(8 bit)
Display module interface	LCM (Intel 8080)	N/A	N/A	0	1 (18 bit)	0	0
USB OTG		1					
RTC		1					
ADC		x	x	4 channels			
Common IO interface (2)	I2C	1	2	3	2	3	3
	I2S	0	0	1	1	1	1
	SPI	1	1	2	0	2	1
	UART	1	0	2	1	2	1
	SDIO	0	0	1	0	1	1
	GPIO	1	1	7	1	7	2
	PWM	1	1	2	1	2	1

(1) KL520 series offer three kinds of packages with different configurations of MIPI camera (1 or 2 cam) and display panel (with or without) option.

(2) Common I/O interface is configurable with pin-mux setting. Please contact Kneron for more information.

3.2 Pin description

Pin name	LQFP 128	TFBGA 159	TFBGA 161	Description	Power Domain
RTC_IO	65	P11	P11	Clock oscillator IO in RTC power domain	RTC
RTC_IN	66	P12	P12	Clock oscillator IN in RTC power domain	RTC
PSW_NPU	58	P10	P10	Power control to enable NPU power	RTC
PSW_CPU	59	R11	R11	Power control to enable CPU power	RTC
PSW_DDRCK	62	R12	R12	Power control to enable internal DDR power	RTC
WAKEUP	61	P13	P13	Wakeup trigger to enable chip > 736us	RTC
RST_N	63	R13	R13	System reset >150us	RTC
OM	64	R14	R14	Reference pin. Pull down to GND	RTC
MPRX0_CKN	122	A3	A3	MIPI CSI-2 RX clock-	NPU
MPRX0_CKP	123	A2	A2	MIPI CSI-2 RX clock+	NPU
MPRX0_DN0	113	A6	A6	MIPI CSI-2 RX lane0 data-	NPU
MPRX0_DN1	117	B4	B4	MIPI CSI-2 RX lane1 data-	NPU
MPRX0_DP0	114	A5	A5	MIPI CSI-2 RX lane0 data+	NPU
MPRX0_DP1	118	A4	A4	MIPI CSI-2 RX lane1 data-	NPU
MPRX0_RBIAS	111	C6	C6	MIPI CSI-2 RX bias	NPU
MPRX1_CKN	7	E2	-	MIPI CSI-2 RX clock-	NPU
MPRX1_CKP	8	E1	-	MIPI CSI-2 RX clock+	NPU
MPRX1_DN0	3	C2	-	MIPI CSI-2 RX lane0 data-	NPU
MPRX1_DN1	-	D2	-	MIPI CSI-2 RX lane1 data-	NPU
MPRX1_DP0	4	C1	-	MIPI CSI-2 RX lane0 data+	NPU
MPRX1_DP1	-	D1	-	MIPI CSI-2 RX lane1 data+	NPU
MPRX1_RBIAS	1	B1	-	MIPI CSI-2 RX bias	NPU
MPTX_CKN	-	-	C1	MIPI TX clock- (CSI-2 or DSI-2)	NPU
MPTX_CKP	-	-	C2	MIPI Tx clock+ (CSI-2 or DSI-2)	NPU
MPTX_DN0	-	-	E1	MIPI TX lane0 data- (CSI-2 or DSI-2)	NPU
MPTX_DN1	-	-	D1	MIPI TX lane1 data- (CSI-2 or DSI-2)	NPU
MPTX_DP0	-	-	E2	MIPI TX lane0 data+ (CSI-2 or DSI-2)	NPU
MPTX_DP1	-	-	D2	MIPI TX lane1 data+ (CSI-2 or DSI-2)	NPU

MPTX_RBIAS	-	-	B1	MIPI TX bias (CSI-2 or DSI-2)	NPU
OTG_DM	107	A8	A8	USB2.0 OTG D-	NPU
OTG_DP	106	A9	A9	USB2.0 OTG D+	NPU
OTG_VBUS	102	A10	A10	USB2.0 OTG Vbus	NPU
OTG_RREF	108	B7	B7	USB2.0 OTG Rref	NPU
OTG_DRV_VBUS	104	E5	E5	USB2.0 OTG as host providing power to device	NPU
ADC_VRT	-	J1	J1	Analog to digital converter voltage reference	NPU
ADC_AIN0	-	K1	K1	Analog to Digital Convertor Input channel 0	NPU
ADC_AIN1	-	J2	J2	Analog to Digital Convertor Input channel 1	NPU
ADC_AIN2	-	L1	L1	Analog to Digital Convertor input channel 2	NPU
ADC_AIN3	-	K2	K2	Analog to Digital Convertor input channel3	NPU
SPI_DO	80	J14	J14	SPI DO (for SPI flash)	CPU
SPI_DI	79	L9	L9	SPI DI (for SPI flash)	CPU
SPI_CK	76	L14	L14	SPI CLK (for SPI flash)	CPU
SPI_CS_N	77	L15	L15	SPI CS (for SPI flash)	CPU
DDRUP	41	P5	P5	Ref. pin. Connect to 240 Ohm to GNDD	NPU
DDRDN	42	R6	R6	Ref. pin. Connect to 240 Ohm to V12_DDR	NPU
OSC_IO	70	P15	P15	Clock oscillator IO in CPU power domain	CPU
OSC_IN	69	R15	R15	Clock oscillator IN in CPU power domain	CPU
PIO1	84	H14	H14	Programable IO - default SPI WP_N	CPU
PIO2	83	J11	J11	Programable IO - default SPI HOLD_N	CPU
PIO3	93	E11	E11	Programable IO - default JTAG_TRST_N	CPU
PIO4	90	C15	C15	Programable IO - default JTAG_TDI	CPU
PIO5	87	E15	E15	Programable IO - default JTAG_SWDITMS	CPU
PIO6	85	F14	F14	Programable IO - default JTAG_SWCLKTCK	CPU
PIO7	91	B15	B15	Programable IO - default JTAG_TDO	CPU
PIO8	100	E6	E6	Programable IO - default UART_RX	CPU
PIO9	99	B10	B10	Programable IO - default UART_TX	CPU
PIO10	95	E10	E10	Programable IO - default I2C_SCL	CPU
PIO11	96	A15	A15	Programable IO - default I2C_SDA	CPU
PIO12	94	C14	C14	Programable IO - default PWM	CPU
PIO13	-	B11	B11	Programable IO - default LC_PCLK	CPU

PIO14	-	E7	E7	Programable IO - default LC_VS	CPU
PIO15	-	E8	E8	Programable IO - default LC_HS	CPU
PIO16	-	A11	A11	Programable IO - default LC_DE	CPU
PIO17	-	A12	A12	Programable IO - default LC_DATA[0]	CPU
PIO18	-	E9	E9	Programable IO - default LC_DATA[1]	CPU
PIO19	-	B12	B12	Programable IO - default LC_DATA[2]	CPU
PIO20	-	B13	B13	Programable IO - default LC_DATA[3]	CPU
PIO21	-	A13	A13	Programable IO - default LC_DATA[4]	CPU
PIO22	-	B14	B14	Programable IO - default LC_DATA[5]	CPU
PIO23	-	D14	D14	Programable IO - default LC_DATA[6]	CPU
PIO24	-	D15	D15	Programable IO - default LC_DATA[7]	CPU
PIO25	-	F11	F11	Programable IO - default LC_DATA[8]	CPU
PIO26	-	E14	E14	Programable IO - default LC_DATA[9]	CPU
PIO27	-	F15	F15	Programable IO - default LC_DATA[10]	CPU
PIO28	-	H11	H11	Programable IO - default LC_DATA[11]	CPU
PIO29	-	G14	G14	Programable IO - default LC_DATA[12]	CPU
PIO30	-	G11	G11	Programable IO - default LC_DATA[13]	CPU
PIO31	-	G15	G15	Programable IO - default LC_DATA[14]	CPU
PIO32	-	H15	H15	Programable IO - default LC_DATA[15]	CPU
PIO33	-	K11	K11	Programable IO - default SD_CLK	CPU
PIO34	-	J15	J15	Programable IO - default SD_CMD	CPU
PIO35	-	L10	L10	Programable IO - default SD_DAT[0]	CPU
PIO36	-	K14	K14	Programable IO - default SD_DAT[1]	CPU
PIO37	-	K15	K15	Programable IO - default SD_DAT[2]	CPU
PIO38	-	L11	L11	Programable IO - default SD_DAT[3]	CPU
KGD_ZQ	53	P8	P8	DDR reference. Connect 240 Ohm to GNDA	DDR

LQFP128 Power/Ground Pin			
Pin name	Description	Pin no.	Power Domain
V33_RTC	3.3V for RTC	57	RTC
V33_OSC	3.3V for Oscillator	68	CPU
TEST_EF	Test mode pin; Normal use: tie to GND	74	CPU
V33D_CPU	3.3V for CPU digital ckt	78, 86, 92, 98, 101	CPU
V33A_NPU	3.3V for NPU analog ckt	105	NPU
V18A_NPU	1.8V for NPU analog ckt	2, 6, 10, 112, 116, 119, 124	NPU
V18_DDR	1.8V for DDR	29, 40, 54	DDR
V12A_NPU	1.2V for NPU analog ckt	18, 22, 26, 31, 35, 38, 44, 47, 55	NPU
V12_DDR	1.2V for DDR	13, 16, 23, 30, 37, 43, 48, 50	DDR
V11D_CPU	1.1V for CPU digital ckt	72, 75, 82, 89, 97, 103	CPU
V11A_CPU	1.1V for CPU analog ckt	67, 71	CPU
V11D_NPU	1.1V for NPU digital ckt	12, 15, 19, 21, 25, 28, 32, 34, 39, 45, 51, 56, 81, 88, 110, 127	NPU
V11A_NPU	1.1V for NPU analog ckt	5, 9, 11, 14, 60, 73, 109, 115, 121, 126,128	NPU
GND	Ground	17, 20, 24, 27, 33, 36, 46, 49, 52, 120, 125	

TFBGA159 Power/Ground Pin			
Pin name		Pin no.	Power Domain
V33_RTC	3.3V for RTC	N10	RTC
V33_OSC	3.3V for Oscillator	P14	CPU
TEST_EF	Test mode pin; Normal use: tie to GND	L13	CPU
V33D_CPU	3.3V for CPU digital ckt	F9, F10, H9, H10, K9, K10	CPU
V33A_NPU	3.3V for NPU analog ckt	B8, M1	NPU
V18A_NPU	1.8V for NPU analog ckt	F2, B6	NPU
V18_DDR	1.8V for DDR	P6	DDR
V12A_NPU	1.2V for NPU analog ckt	P1, P2, R1, R2, R8, R9	NPU

V12_DDR	1.2V for DDR	M2, P4, P7	DDR
V11D_CPU	1.1V for CPU digital ckt	L7, L8	CPU
V11A_CPU	1.1V for CPU analog ckt	N13, N14	CPU
V11D_NPU	1.1V for NPU digital ckt	K5, K6, N1, N2, R3, R4	NPU
V11A_NPU	1.1V for NPU analog ckt	B3, D3, F3, G1, G2, M15, R10	NPU
GNDD	Ground for digital ckt	F5, F6, F7, F8, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, J5, J6, J7, J8, J9, J10, K7, K8, L5, L6, N3, N4, N15, P3	
GNDA	Ground for analog ckt	A1, A7, B2, B5, B9, F1, G3, H1, H2, L2, M14, P9	

TFBGA161 Power/Ground Pin			
Pin name	Description	Pin no.	Power Domain
V33_RTC	3.3V for RTC	N10	RTC
V33_OSC	3.3V for Oscillator	P14	CPU
TEST_EF	Test mode pin; Normal use: tie to GND	L13	CPU
V33D_CPU	3.3V for CPU digital ckt	F9, F10, H9, H10, K9, K10	CPU
V33A_NPU	3.3V for NPU analog ckt	B8, M1	NPU
V18A_NPU	1.8V for NPU analog ckt	B2, B6	NPU
V18_DDR	1.8V for DDR	P6	DDR
V12A_NPU	1.2V for NPU analog ckt	P1, P2, R1, R2, R8, R9	NPU
V12_MPTX	1.2V for MIPI Tx	E3	NPU
V12_DDR	1.2V for DDR	M2, P4, P7	DDR
V11D_CPU	1.1V for CPU digital ckt	L7, L8	CPU
V11A_CPU	1.1V for CPU analog ckt	N13, N14	CPU
V11D_NPU	1.1V for NPU digital ckt	K5, K6, N1, N2, R3, R4	NPU
V11A_NPU	1.1V for NPU analog ckt	B3, D3, F2, F3, G1, G2, M15, R10	NPU
GNDD	Ground for digital ckt	F5, F6, F7, F8, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, J5, J6, J7, J8, J9, J10, K7, K8, L5, L6, N3, N4, N15, P3	
GNDA	Ground for analog ckt	A1, A7, B5, B9, C3, F1, G3, H1, H2, L2, M14, P9	

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	GNDA	MPRX0_CKP	MPRX0_CKN	MPRX0_DP1	MPRX0_DP0	MPRX0_DN0	GNDA	OTG_DM	OTG_DP	OTG_VBUS	PIO16	PIO17	PIO21		PIO11
B	MPRX1_RBIAS	GNDA	V11A_NPU	MPRX0_DN1	GNDA	V18A_NPU	OTG_RREF	V33A_NPU	GNDA	PIO9	PIO13	PIO19	PIO20	PIO22	PIO7
C	MPRX1_DP0	MPRX1_DN0				MPRX0_RBIAS								PIO12	PIO4
D	MPRX1_DP1	MPRX1_DN1	V11A_NPU											PIO23	PIO24
E	MPRX1_CKP	MPRX1_CKN			OTG_DRV_VBUS	PIO8	PIO14	PIO15	PIO18	PIO10	PIO3			PIO26	PIO5
F	GNDA	V18A_NPU	V11A_NPU		GNDD	GNDD	GNDD	GNDD	V33D_CPU	V33D_CPU	PIO25			PIO6	PIO27
G	V11A_NPU	V11A_NPU	GNDA		GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	PIO30			PIO29	PIO31
H	GNDA	GNDA			GNDD	GNDD	GNDD	GNDD	V33D_CPU	V33D_CPU	PIO28			PIO1	PIO32
J	ADC_VRT	ADC_AIN1			GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	PIO2			SPI_DO	PIO34
K	ADC_AIN0	ADC_AIN3			V11D_NPU	V11D_NPU	GNDD	GNDD	V33D_CPU	V33D_CPU	PIO33			PIO36	PIO37
L	ADC_AIN2	GNDA			GNDD	GNDD	V11D_CPU	V11D_CPU	SPI_DI	PIO35	PIO38		TEST_EF	SPI_CLK	SPI_CS_N
M	V33D_NPU	V12_DDR												GNDA	V11A_NPU
N	V11D_NPU	V11D_NPU	GNDD	GNDD						V33_RTC			V11A_CPU	V11A_CPU	GNDD
P	V12A_NPU	V12A_NPU	GNDD	V12_DDR	DDRUP	V18_DDR	V12_DDR	KGD_ZQ	GNDA	PSW_NPU	RTC_IO	RTC_IN	WAKEUP	V33_OSC	OSC_IO
R	V12A_NPU	V12A_NPU	V11D_NPU	V11D_NPU		DDRDN		V12A_NPU	V12A_NPU	V11A_NPU	PSW_CPU	PSW_DDRCK	RST_N	OM	OSC_IN

TFBGA 8x8 159io Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	GNDA	MPRX0_CKP	MPRX0_CKN	MPRX0_DP1	MPRX0_DP0	MPRX0_DN0	GNDA	OTG_DM	OTG_DP	OTG_VBUS	PIO16	PIO17	PIO21		PIO11
B	MPTX_RBIAS	V18A_NPU	V11A_NPU	MPRX0_DN1	GNDA	V18A_NPU	OTG_RREF	V33A_NPU	GNDA	PIO9	PIO13	PIO19	PIO20	PIO22	PIO7
C	MPTX_CKN	MPTX_CKP	GNDA			MPRX0_RBIAS								PIO12	PIO4
D	MPTX_DN1	MPTX_DP1	V11A_NPU											PIO23	PIO24
E	MPTX_DN0	MPTX_DP0	V12_MPTX		OTG_DRV_VBUS	PIO8	PIO14	PIO15	PIO18	PIO10	PIO3			PIO26	PIO5
F	GNDA	V11A_NPU	V11A_NPU		GNDD	GNDD	GNDD	GNDD	V33D_CPU	V33D_CPU	PIO25			PIO6	PIO27
G	V11A_NPU	V11A_NPU	GNDA		GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	PIO30			PIO29	PIO31
H	GNDA	GNDA			GNDD	GNDD	GNDD	GNDD	V33D_CPU	V33D_CPU	PIO28			PIO1	PIO32
J	ADC_VRT	ADC_AIN1			GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	PIO2			SPI_DO	PIO34
K	ADC_AIN0	ADC_AIN3			V11D_NPU	V11D_NPU	GNDD	GNDD	V33D_CPU	V33D_CPU	PIO33			PIO36	PIO37
L	ADC_AIN2	GNDA			GNDD	GNDD	V11D_CPU	V11D_CPU	SPI_DI	PIO35	PIO38		TEST_EF	SPI_CLK	SPI_CS_N
M	V33D_NPU	V12_DDR												GNDA	V11A_NPU
N	V11D_NPU	V11D_NPU	GNDD	GNDD						V33_RTC			V11A_CPU	V11A_CPU	GNDD
P	V12A_NPU	V12A_NPU	GNDD	V12_DDR	DDRUP	V18_DDR	V12_DDR	KGD_ZQ	GNDA	PSW_NPU	RTC_IO	RTC_IN	WAKEUP	V33_OSC	OSC_IO
R	V12A_NPU	V12A_NPU	V11D_NPU	V11D_NPU		DDRDN		V12A_NPU	V12A_NPU	V11A_NPU	PSW_CPU	PSW_DDRCK	RST_N	OM	OSC_IN

TFBGA 8x8 161io Ball Map

3.3 Pinmux table for programmable I/O

PAD name	PIO name	Mode0	DIR	Mode1	DIR	Mode2	DIR	Mode3	DIR	Mode4	DIR	Mode5	DIR	Mode6	DIR	Mode7	DIR
X_SPI_WP_N	PIO1	SPI_WP_N	O			SD_CLK	O	GPIO0	IO	UART2 RX	I	PWM1	O	I2C2_CLK	O	SPI1_CLK	O
X_SPI_HOLD_N	PIO2	SPI_HOLD_N	O	I2S1_BCLK	IO	SD_CMD	IO	GPIO1	IO	UART2 TX	O	PWM2	O	I2C2_DATA	IO	SPI1_CS	O
X_JTAG_TRST_N	PIO3	JTAG_TRST_N	I	I2S1_RCLK	IO	SD_DAT[0]	IO	GPIO2	IO	UART0_RX	I	SD_CLK	O	I2C3_CLK	O	I2C0_CLK	O
X_JTAG_TDI	PIO4	JTAG_TDI	I	I2S1_SDATA	IO	SPI0_CS	O	GPIO3	IO	UART0_TX	O	SD_CMD	IO	I2C3_DATA	IO	I2C0_DATA	IO
X_JTAG_SWDITMS	PIO5	JTAG_SWDITMS	I	I2S0_BCLK	IO	SPI0_CLK	O	GPIO4	IO	UART0_irda_nrts	O	SD_DAT[0]	IO	I2C1_CLK	O	SPI1_DI	I
X_JTAG_SWCLKTCK	PIO6	JTAG_SWCLKTCK	I	I2S0_RCLK	IO	SPI0_DO	O	GPIO5	IO	UART0_irda_ncts	I	PWM3	O	I2C1_DATA	IO	SPI1_DO	O
X_JTAG_TDO	PIO7	JTAG_TDO	O	I2S0_SDATA	IO	SPI0_DI	I	GPIO6	IO	UART0_irda_RX_h	I	PWM4	O				
X_LC_PCLK	PIO13	LC_PCLK	O	UART2 RX	I			GPIO7	IO	I2C3_CLK	O	DPI_DATA[12]	I				
X_LC_VS	PIO14	LC_VS	O	UART2 TX	O	I2S1_BCLK	IO	GPIO8	IO	I2C3_DATA	IO	DPI_DATA[13]	I			LCM_DB[0]	IO
X_LC_HS	PIO15	LC_HS	O	I2C2_CLK	O	I2S1_RCLK	IO	GPIO9	IO	SPI0_CLK	O	DPI_DATA[14]	I			LCM_DB[1]	IO
X_LC_DE	PIO16	LC_DE	O	I2C2_DATA	IO	I2S1_SDATA	IO	GPIO10	IO	SPI0_CS	O	DPI_DATA[15]	I			LCM_DB[2]	IO
X_LC_DATA[0]	PIO17	LC_DATA[0]	O	X_SD_CLK	O	I2S0_BCLK	IO	GPIO11	ta	SPI0_DI	I	DPI_DATA[16]	I			LCM_DB[3]	IO
X_LC_DATA[1]	PIO18	LC_DATA[1]	O	X_SD_CMD	IO	I2S0_RCLK	IO	GPIO12	IO	SPI0_DO	O	DPI_DATA[17]	I			LCM_DB[4]	IO
X_LC_DATA[2]	PIO19	LC_DATA[2]	O	X_SD_DAT[0]	IO	I2S0_SDATA	IO	GPIO13	IO	UART1 RX	I	DPI_DATA[18]	I			LCM_DB[5]	IO
X_LC_DATA[3]	PIO20	LC_DATA[3]	O	X_SD_DAT[1]	IO	UART0_irda_TX	O	GPIO14	IO	UART1 TX	O	DPI_DATA[19]	I			LCM_DB[6]	IO
X_LC_DATA[4]	PIO21	LC_DATA[4]	O	X_SD_DAT[2]	IO	UART0_irda_RX_I	I	GPIO15	IO	SPI0_CLK	O	DPI_DATA[20]	I	UART3 RX	I	LCM_DB[7]	IO
X_LC_DATA[5]	PIO22	LC_DATA[5]	O	X_SD_DAT[3]	IO	UART0_irda_RX_h	I	GPIO16	IO	SPI0_CS	O	DPI_DATA[21]	I	UART3 TX	O	LCM_DB[8]	IO
X_LC_DATA[6]	PIO23	LC_DATA[6]	O	UART2 RX	I	I2C1_CLK	O	GPIO17	IO	SPI0_DI	I	DPI_DATA[22]	I	—		LCM_DB[9]	IO
X_LC_DATA[7]	PIO24	LC_DATA[7]	O	UART2 TX	O	I2C1_DATA	IO	GPIO18	IO	SPI0_DO	O	DPI_DATA[23]	I	—		LCM_DB[10]	IO
X_LC_DATA[8]	PIO25	LC_DATA[8]	O	I2S0_BCLK	IO	SPI1_CLK	O	GPIO19	IO	UART3 RX	I	DPI_PCLK	I			LCM_DB[11]	IO
X_LC_DATA[9]	PIO26	LC_DATA[9]	O	I2S0_RCLK	IO	SPI1_CS	O	GPIO20	IO	UART3 TX	O	DPI_VS	I	—		LCM_DB[12]	IO
X_LC_DATA[10]	PIO27	LC_DATA[10]	O	I2S0_SDATA	IO	SPI1_DI	I	GPIO21	IO	UART4_RX	I	DPI_HS	I	—		LCM_DB[13]	IO
X_LC_DATA[11]	PIO28	LC_DATA[11]	O	I2C0_CLK	O	SPI1_DO	O	GPIO0	IO	UART4_TX	O	DPI_DE	I			LCM_DB[14]	IO
X_LC_DATA[12]	PIO29	LC_DATA[12]	O	I2C0_DATA	IO	PWM5	O	GPIO1	IO	SPI1_CLK	O	DPI_DATA[0]	I			LCM_DB[15]	IO

X_LC_DATA[13]	PIO30	LC_DATA[13]	O	I2S1_BCLK	IO	I2S0_BCLK	IO	GPIO2	IO	SPI1_CS	O	DPI_DATA[1]	I			LCM_DB[16]	IO
X_LC_DATA[14]	PIO31	LC_DATA[14]	O	I2S1_RCLK	IO	I2S0_RCLK	IO	GPIO3	IO	SPI1_DI	I	DPI_DATA[2]	I			LCM_DB[17]	IO
X_LC_DATA[15]	PIO32	LC_DATA[15]	O	I2S1_SDATA	IO	I2S0_SDATA	IO	GPIO4	IO	SPI1_DO	O	DPI_DATA[3]	I			LCM_CSn	I
X_SD_CLK	PIO33	SD_CLK	O	LC_DATA[16]	O	I2S1_BCLK	IO	GPIO22	IO	I2C1_CLK	O	DPI_DATA[4]	I	UART2 RX	I	LCM_WR	I
X_SD_CMD	PIO34	SD_CMD	IO	LC_DATA[17]	O	I2S1_RCLK	IO	GPIO23	IO	I2C1_DATA	IO	DPI_DATA[5]	I	UART2 TX	O	LCM_RS	I
X_SD_DAT[0]	PIO35	SD_DAT[0]	IO	LC_DATA[18]	O	I2S1_SDATA	IO	GPIO24	IO	I2C2_CLK	O	DPI_DATA[6]	I	UART3 RX	I	LCM_RD	I
X_SD_DAT[1]	PIO36	SD_DAT[1]	IO	LC_DATA[19]	O			GPIO25	IO	I2C2_DATA	IO	DPI_DATA[7]	I	UART3 TX	O	LCM_RESETn	I
X_SD_DAT[2]	PIO37	SD_DAT[2]	IO	LC_DATA[20]	O	SPI1_CLK	O	GPIO26	IO	I2C3_CLK	O	DPI_DATA[8]	I	UART4_RX	I	LCM_BLCTRL	I
X_SD_DAT[3]	PIO38	SD_DAT[3]	IO	LC_DATA[21]	O	SPI1_CS	O	GPIO27	IO	I2C3_DATA	IO	DPI_DATA[9]	I	UART4_TX	O	LCM_TP_INT1	I
X_UART0_RX	PIO8	UART0_RX	I	LC_DATA[22]	O	SPI1_DI	I	GPIO7	IO	SPI0_CLK	O	DPI_DATA[10]	I				
X_UART0_TX	PIO9	UART0_TX	O	LC_DATA[23]	O	SPI1_DO	O	GPIO28	IO	SPI0_CS	O	DPI_DATA[11]	I				
X_I2C0_SCL	PIO10	I2C0_CLK	O	UART0_irda_TX	O	I2S0_BCLK	IO	GPIO29	IO	SPI0_DI	I	I2S1_BCLK	IO				
X_I2C0_SDA	PIO11	I2C0_DATA	IO	UART0_irda_RX_l	I	I2S0_RCLK	IO	GPIO30	IO	SPI0_DO	O	I2S1_RCLK	IO				
X_PWM0	PIO12	PWM0	O	UART0_irda_RX_h	I	I2S0_SDATA	IO	GPIO31	IO			I2S1_SDATA	IO				

Pin-Mux table

3.4 Pinmux I/O description

General Name	Pin Name	Description
PWM	PWM	Pulse width modulation
GPIO	GPIO	Programmable general-purpose input/output
UART	TX	data output
	RX	data input
I2C	I2C_CLK	SCL
	I2C_DATA	SDA
SPI	SPI_CLK	serial clock
	SPI_CS	selected
	SPI_DI	Data input / IO0
	SPI_DO	data output / IO1
	SPI_WP_N	IO2(for SPI flash quad-mode)
	SPI_HOLD_N	IO3(for SPI flash quad-mode)
I2S	I2S_BCLK	Bit clock
	I2S_RCLK	Sample rate clock
	I2S_SDATA	serial data
	mclk	master mode clock
SDIO	SD_CLK	Clock
	SD_CMD	Command
	SD_DAT[0:3]	Data
IrDA	irda_nrst	Request to send
	irda_ncts	Clear to send
	irda_RX_h	Infrated Receive for FIR
LCD (display panel interface)	LC_PCLK	Pixel clock
	LC_VS	Vertical synchronization
	LC_HS	Horizontal synchronization
	LC_DE	Data enable
	LC_DATA[0:15]	Pixel data
LCM (LCD Module)	LCM_SCn	Select
	LCM_WR	Write enable

	LCM_RS	Register select
	LCM_RD	Read enable
	LCM_RESETn	Reset
	LCM_BLCTRL	Back light control
	LCM_TP_INT1	Touch panel interrupt
	LCM_DB[0:17]	data bus
DPI (Parallel Video Input)	DPI_PCLK	Pixel clock
	DPI_VS	Vertical synchronization
	DPI_HS	Horizontal synchronization
	DPI_DE	Data enable
	DPI_DATA[0:23]	Pixel data
JTAG	JTAG_TRST_N	Reset for the JTAG TAP controller
	JTAG_TDI	Test Data In
	JTAG_SWDITMS	Test Mode Select
	JTAG_SWCLKTCK	Test Clock
	JTAG_TDO	Test Data Out

Pinmux description

4 Power Mode

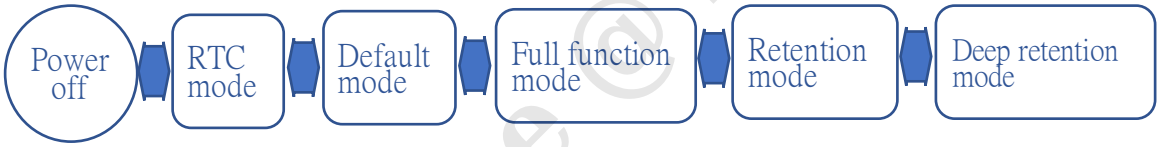
4.1 Introduction

KL520 is low-power oriented SOC chip and is capable to provide power efficient solution to our customer by partition the whole chip power into three power domains: RTC, Default and NPU. By efficient allocation of these three power partitions, we are able to provide five power modes phase in KL520 SOC – RTC, DEFAULT, Full Function, Retention and Deep Retention mode.

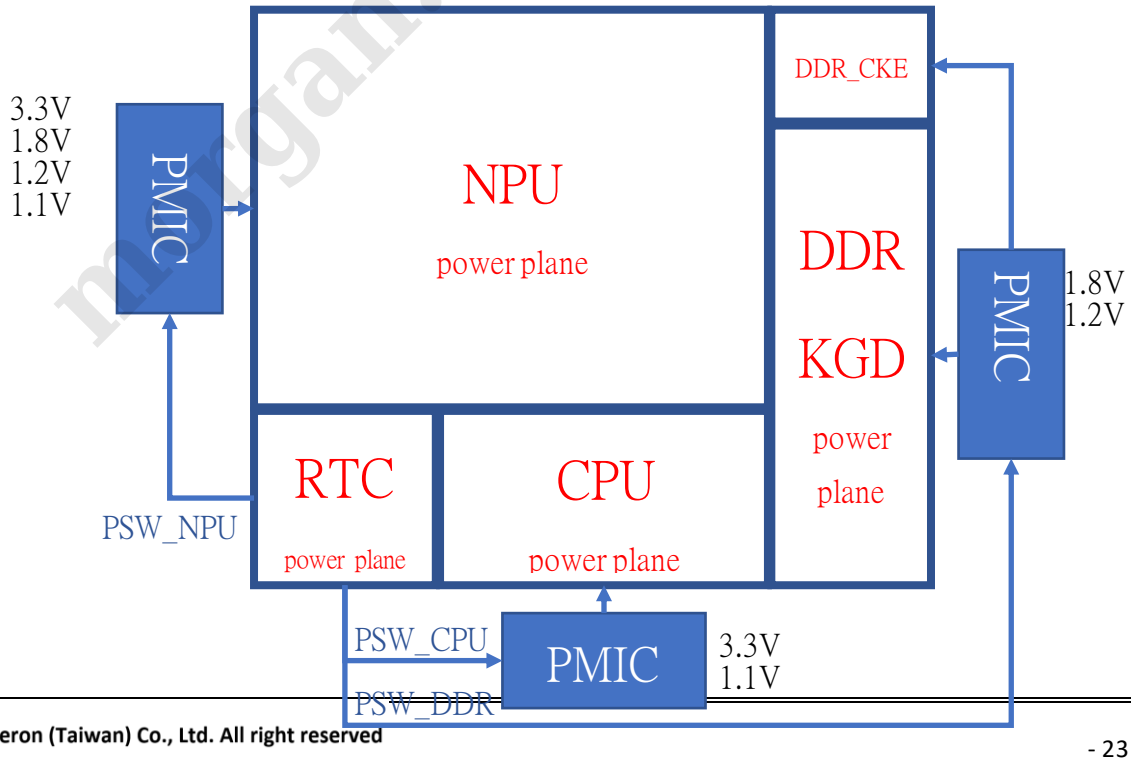
In minimum power condition, KL520 only depends on one single 3.3V power supply for RTC power domain with Real-Time-Clock circuit operation which consume only 29uW.
In other scenario, depends on different CNN model used, the peak power of KL520 are in general still under 500mW.

4.2 Power mode

4.3 Power mode



4.4 Power Partition



4.5 Power Consumption

MODE	RTC	DEFAULT	FULL_FUNC	RETENTION	DEEP_RET
POWER (mW)	0.03	268	*1	125	0.18

Note 1: This number is vary depends on the AI model and application, please contact KNERON sales for further information.

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Core Voltage	VDDmax	1.045	1.155	V
Supply IO Voltage	VDDIOmax	3.135	3.465	V
IO Signal Voltage	VIOmax	-0.5	VDDIO[1]+0.3	V
ESD (human body mode)	ESD-HBM	± 1.0		KV
ESD (machine mode)	ESD-MM	± 30		V
Latch-Up		<-100	>100	mA
Storage Temperature	Tstorage	-40	125	℃
Ambient Temperature	T_A	0	70	℃
Junction Temperature	T_J	-40	125	℃

Absolute Maximum Ratings

[1] The voltage depends on different power group

* Permanent device damage may occur if the absolute maximum ratings are exceeded

5.1 Recommended operating conditions

Power pin	Description	Min.	Typ.	Max.	Unit
V33_RTC V33_OSC V33D_CPU V33A_NPU	3.3V IO(digital IO, USB, ADC) and RTC power supply	3.135	3.3	3.465	V
V18A_NPU V18_DDR	1.8V IO(MIPI) and DDR power supply	1.71	1.8	1.89	V
V12A_NPU V12A_MPTX V12_DDR	1.2V IO(MIPI/Tx) and DDR power supply	1.14	1.2	1.26	V
V11D_CPU V11A_CPU V11D_NPU V11A_NPU	1.1V core and IO(MIPI) power supply	1.045	1.1	1.155	V

5.2 DC electrical characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Unit
V33	3.3V I/O and RTL-power domain power supply	V33_RTC V33_OSC V33D_CPU	3.135	3.3	3.465	V
T_J	Operating junction temperature		-40	25	125	°C
V_{Il}	Input low voltage	LVTTL	-	-	0.8	V
V_{Ih}	Input high voltage	LVTTL	2.0	-	-	V
V_{t-}	Schmitt-trigger negative-to threshold voltage	LVTTL	0.8	1.1	-	V
V_{t+}	Schmitt-trigger positive-to-threshold voltage	LVTTL	-	1.6	2.0	V
V_{Ol}	Output low voltage	I_{Ol} = 2mA~8mA	-	-	0.4	V
V_{Oh}	Output high voltage	I_{Oh} = 2mA~8mA	2.4	-	-	V
R_{pu}	Input pull-up resistance	V_{in} = 0V	40	75	190	Ω
R_{pd}	Input pull-down resistance	V_{in} = V33	40	75	190	Ω
I_{in}	Input leakage current	V_{in} = V33 or 0V	-	-	±10	μA
I_{oz}	Tri-state put leakage current	-	-	-	±10	μA

5.3 USB electrical characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Unit
Input levels for High-speed mode						
V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$ Measured at the connection as an application circuit	300	-	-	mV
V_{HSCM}	High-speed data signaling common-mode voltage range	-	-60	-	500	mV
V_{HSSQ}	High-speed squelch detection threshold	Squelch is detected	-	-	100	mV
		Squelch is not detected	200	-	-	mV
V_{HSDSC}	High-speed disconnection detection threshold	Disconnection is detected	625	-	-	mV
		Disconnection is not detected	-	-	525	mV
Output levels for High-speed						
V_{HSOI}	High-speed idle-level output voltage (Differential)	-	-20	-	20	mV
V_{HSOL}	High-speed low-level output voltage (Differential)	-	-20	-	20	mV
V_{HSOH}	High-speed high-level output voltage (Differential)	-	360	400	440	mV
V_{CHIRPJ}	Chirp-J output voltage (Differential voltage)	-	700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage (Differential voltage)	-	-900	-	-500	mV
$I_{DP/DM}$	Allowable output current of DP/DM lines	When the termination is 45Ω±10%	14.55	17.78	21.79	μA
Input levels for Low-speed/Full-speed						
V_{IH}	High-level input voltage	Driven	2.0	-	-	V
V_{IHZ}	High-level input voltage	Floating	2.7	-	3.6	V
V_{IL}	Low-level input voltage	-	-	-	0.8	V
V_{DI}	Differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	Differential common-mode voltage	Including V_{DI} range	0.8	-	2.5	V
Output levels for Low-speed/Full-speed						
V_{OL}	Low-level output voltage		0	-	0.3	V
V_{OH}	High-level output voltage		2.8	-	3.6	V

USB2.0 DC electrical characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Unit
Driver characteristics (High-speed mode)						
$T_{HSRDRATE}$	High-speed TX data rate	-	479.76	-	480.24	Mbps
$T_{HSRDRATE}$	High-speed RX data rate	-	479.76	-	480.24	Mbps
t_{HSR}	High-speed differential rise time	10%~90%	100	-	-	ps
t_{HSR}	High-speed differential fall time	90%~10%	100	-	-	ps
Driver characteristics (Full-speed mode)						
T_{FDRATE}	Full-speed TX data rate	-	11.994	-	12.006	Mbps
T_{FDRATE}	Full-speed RX data rate	-	11.970	-	12.030	Mbps
t_{FR}	Rise time	10%~90%	4.0	-	20	ns
t_{FF}	Fall time	90%~10%	4.0	-	20	ns
Driver characteristics (Low-speed mode)						
T_{LDRATE}	Low-speed TX data rate	-	1.49925	-	1.50075	Mbps
T_{LDRATE}	Low-speed RX data rate	-	1.47750	-	1.52250	Mbps
t_{FR}	Rise time	10%~90%	75	-	300	ns
t_{FF}	Fall time	90%~10%	75	-	300	ns

USB2.0 AC electrical characteristics

5.4 MIPI electrical characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Unit
HS receiver						
V_{CMRX}	Common-mode voltage in the HS receive mode	-	70	-	300	mV
V_{IDTH}	Differential input high threshold voltage	-	-	-	70	mV
V_{IDTL}	Differential input low threshold voltage	-	-70	-	-	mV
V_{IHHS}	Single-end input high voltage	-	-	-	460	mV
V_{ILHS}	Single-end input low voltage	-	-40	-	-	mV
$V_{TERN-EN}$	Single-end threshold voltage for HS termination enable	-	-	-	450	mV
Z_{ID}	Differential input impedance	-	80	100	125	Ω
LP receiver						
V_{IH}	Logic 1 input voltage	-	800	-	-	mV
V_{IL}	Logic 0 input voltage not at the ULP state	-	-	-	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage at the ULP state	-	-	-	300	mV
V_{HYST}	Input hysteresis	-	25	-	-	mV

MIPI Rx DC electrical characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Unit
HS transmitter						
V_{CMTX}	Static common-mode voltage	-	150	200	250	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0	-	-	-	5.0	mV
$\|V_{OD}\|$	Differential input low threshold voltage	-	140	200	270	mV
$\|\Delta V_{OD}\|$	Differential voltage of HS transmitter	-	-	-	10	mV
V_{OHHS}	HS output high voltage	-	-	-	360	mV
Z_{OS}	Single-end output impedance		40	50	62.5	Ω
ΔZ_{OS}	Single-end output impedance mismatch		-	-	10	%
LP transmitter						
V_{OH}	The venin output high level	-	1.1	1.2	1.3	V
V_{OL}	The venin output low level	-	-50	-	50	mV
Z_{OS}	Single-end output impedance		110	-	-	Ω

MIPI Tx DC electrical characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Unit
HS receiver						
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz	-	-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference between 50MHz~450MHz	-	-50	-	50	mV
C_{CM}	Common-mode termination	-	-	-	60	pF
LS receiver						
e_{SPIKE}	Input pulse rejection	-	-	-	300	Vps
T_{MIN-RX}	Minimum pulse width response	-	20	-	-	ns
V_{INT}	Peak interference amplitude	-	-	-	200	mV
f_{INT}	Interference frequency	-	450	-	-	MHz
HS transmitter						
$\Delta V_{CMTRX(HF)}$	Common-mode interference beyond 450MHz	-	-	-	15	mV_{RMS}

$DV_{CMTRX(LF)}$	Common-mode interference between 50MHz~450MHz	-	-	-	25	mV_{PEAK}
t_R and t_F	20%~80% rise time and fall time	> 1.0 Gbps	-	-	0.35	UI
			100	-	-	ps
t_R and t_F	20%~80% rise time and fall time	≤ 1.0 Gbps	-	-	0.3	UI
			150	-	-	ps
LP transmitter						
V_{OH}	The venin output high level	-	1.1	1.2	1.3	V
V_{OL}	The venin output low level	-	-50	-	50	mV
Z_{OS}	Single-end output impedance		110	-	-	Ω

MIPI AC electrical characteristics

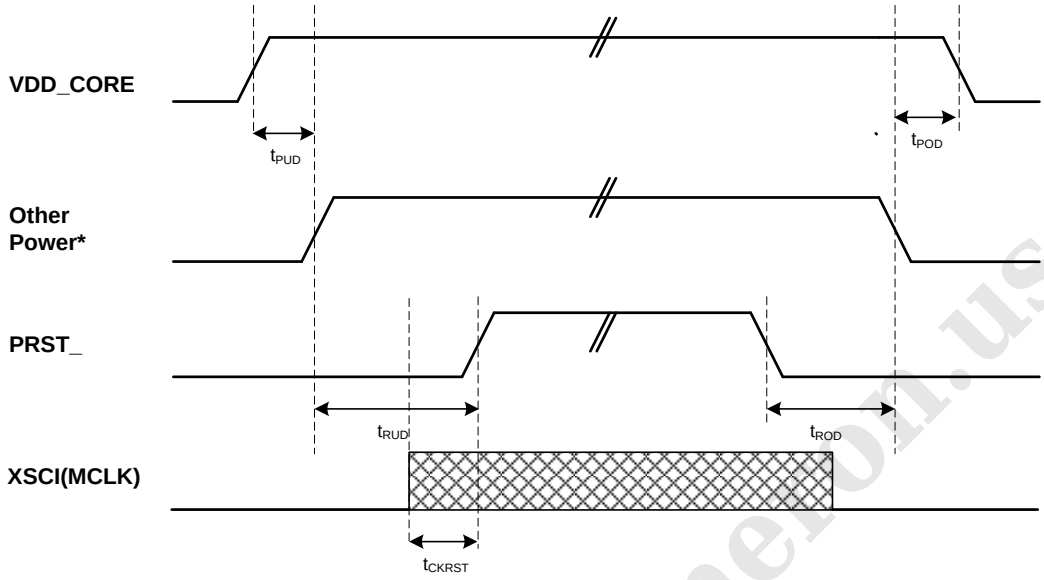
5.5 ADC electrical characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Unit
V33	3.3V power supply	V33A_NPU	3.135	3.3	3.465	V
AIN0~3	Analog input range	ADC_AIN0 ~ ADC_AIN3	0.1* V33	-	0.9* V33	V
RES	Resolution	-	-	-	10	bit
INL	Integral non-linearity error	-	-2.0	±1.0	2.0	LSB
DNL	Differential non-linearity error	-	-1.0	±0.8	1.5	LSB
Internal CLK	Clock frequency	-	1.0	-	11	MHz
Internal Sample	Sampling rate	-	-	-	1.0	MSPS
SNDR	Signal-to-noise plus distortion ratio	At analog input freq. = 100kHz	52	56	-	dB
THD	Total harmonic distortion		-	-60	-55	dB
SFDR	Spurious-free dynamic range	Clock jitter < 1.2ns rms	55	60	-	dB

5.6 Power On/Off Sequence

Symbol	Parameter	Min	Max	Unit
t_{PUD}	Core power up to IO power up delay	100	-	ns
t_{RUD}	IO power on to reset assert delay	1	-	ms
t_{POD}	IO power off to Core power off delay	100	-	ns
t_{ROD}	Reset de-assert to IO power delay	0	-	Ns
t_{CKRST}	Clock on to reset assert delay	8T	-	T=42ns(24MHz)

Power on/off sequence parameter



Power on/off timing diagram

6 Thermal information

Package	Power(W)	θJA(℃ /W)	θJB(℃ /W)	θJC(℃ /W)
TFBGA 8x8		30.3	13.68	13.3

The testing JEDEC PCB is based on 4 layers, 101.5 x 114.5 mm, 1.6 mm Thickness (**JEDEC JESD51-9)**

Package	Power(W)	θJA(℃ /W)	θJB(℃ /W)	θJC(℃ /W)
LQFP 14x14 (EP)		24.8	16.11	13.0

The testing JEDEC PCB is based on 4 layers, 76.2 x 114.3 mm, 1.6 mm Thickness **(JEDEC JESD51-5)**

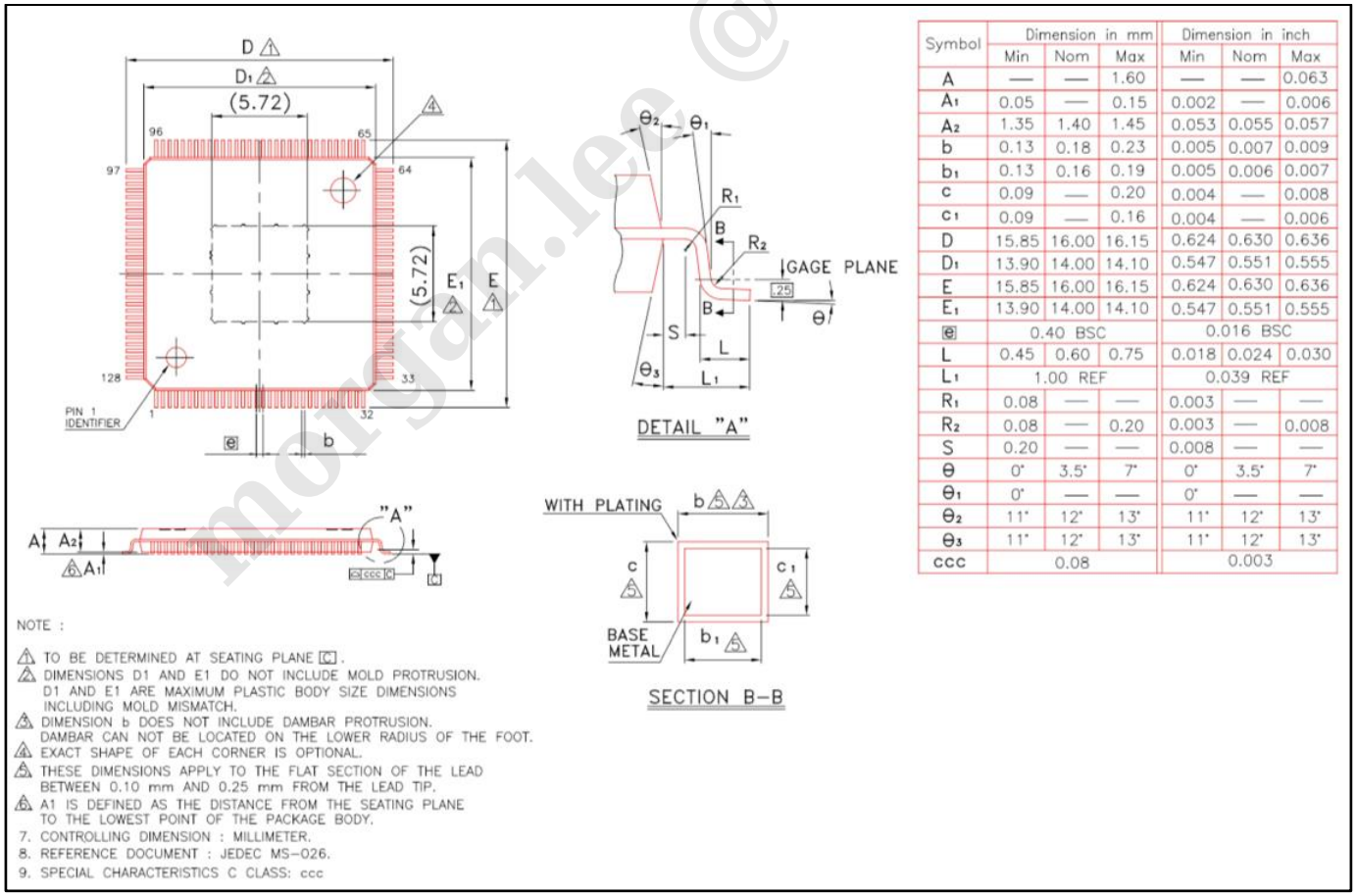
7 Package information

7.3 Package information

Kneron P/N	Package General Description	Environmental	MSL	Package Qty
KL520B1311A	TFBGA 8x8 159io, 512Mb	RoHS & REACH Compliant	Level 3	348
KL520B2311A	TFBGA 8x8 161io, 512Mb	RoHS & REACH Compliant	Level 3	348
KL520L1311A	LQFP 14x14 128L, 512Mb	RoHS & REACH Compliant	Level 3	90
KL520B1211A	TFBGA 8x8 159io, 256Mb	RoHS & REACH Compliant	Level 3	348
KL520B2211A	TFBGA 8x8 161io, 256Mb	RoHS & REACH Compliant	Level 3	348
KL520L1211A	LQFP 14x14 128L, 256Mb	RoHS & REACH Compliant	Level 3	90

7.4 Package outline

7.2.1 LQFP 14x14 128io

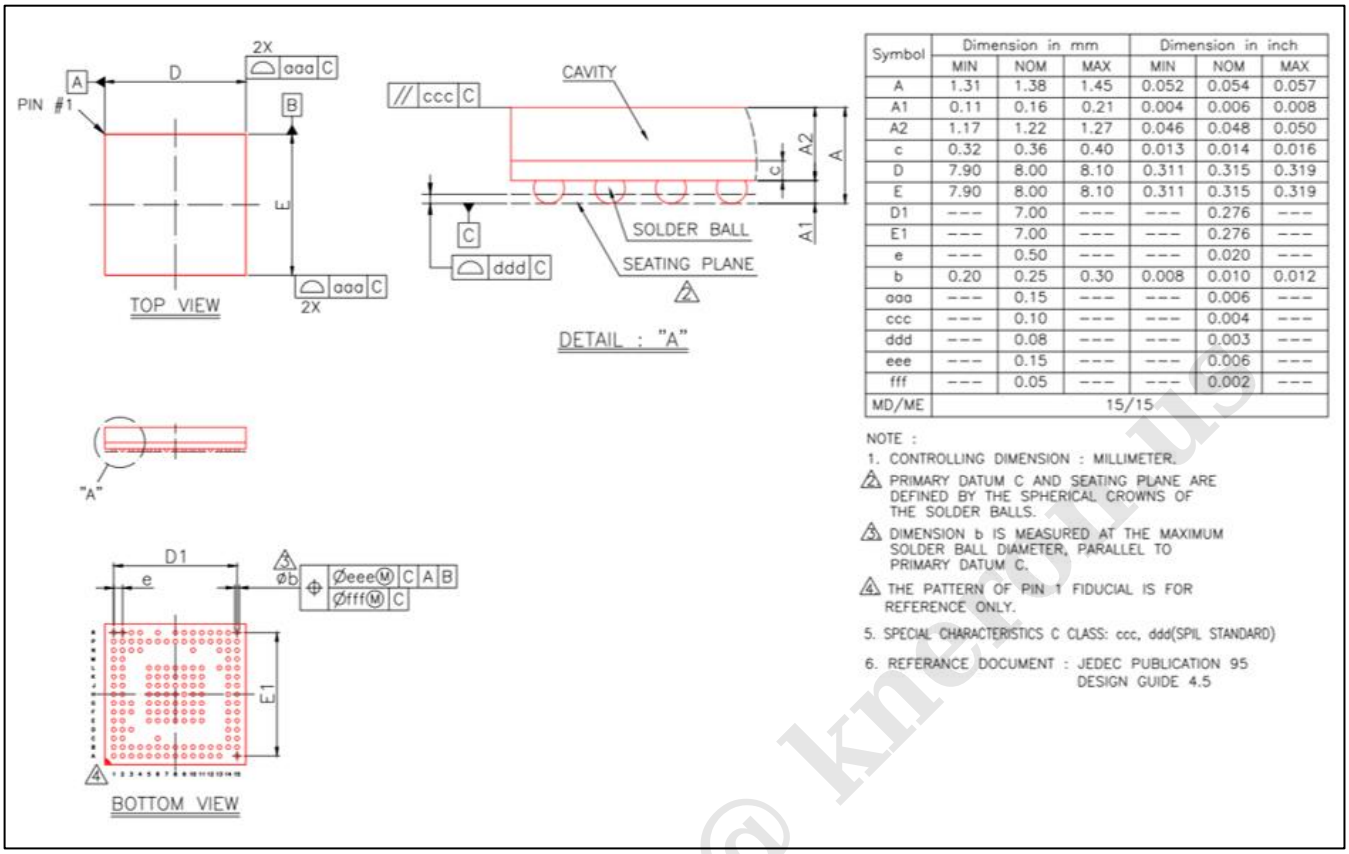


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE C.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

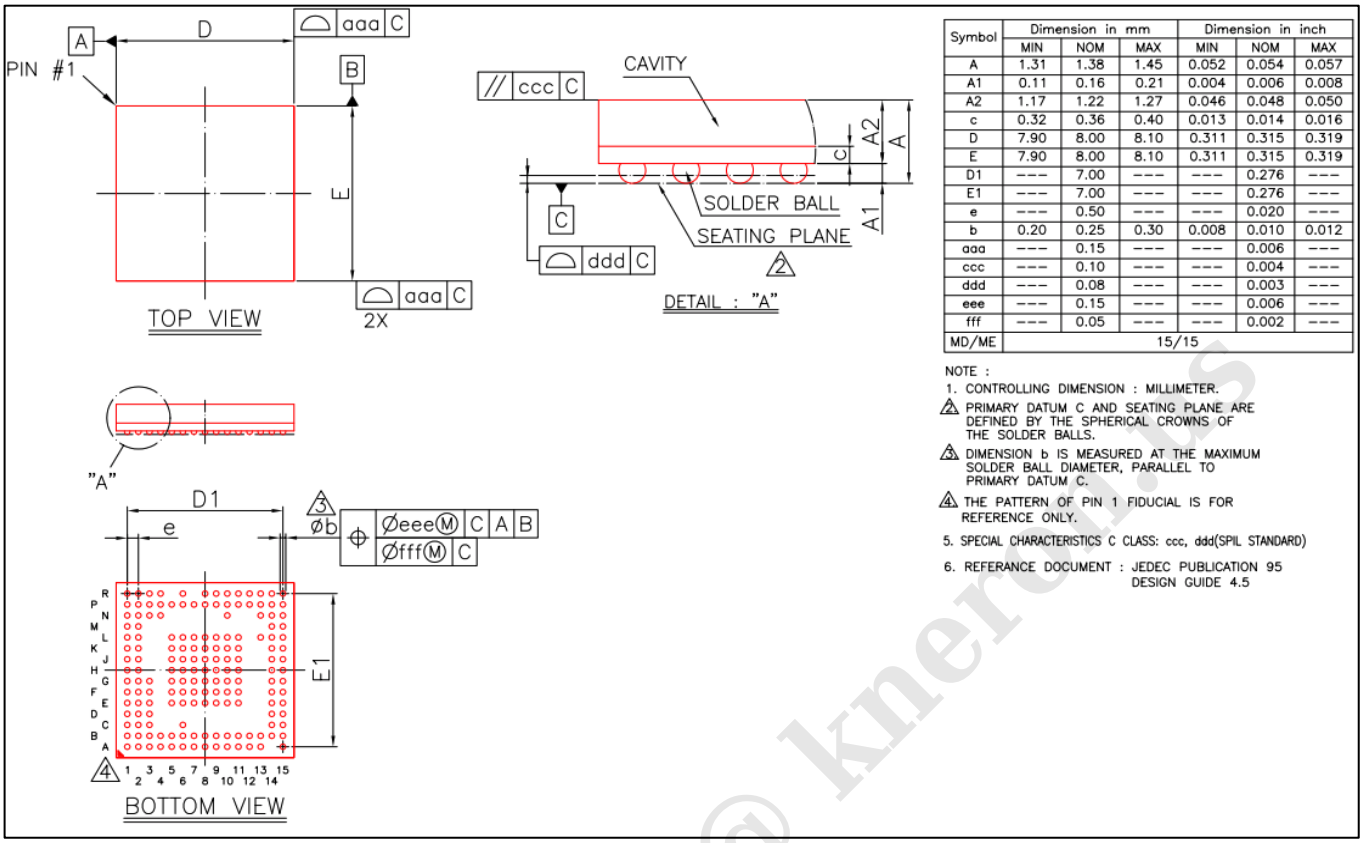
7.2.2 TFBGA 8x8 159io



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.31	1.38	1.45	0.052	0.054	0.057
A1	0.11	0.16	0.21	0.004	0.006	0.008
A2	1.17	1.22	1.27	0.046	0.048	0.050
c	0.32	0.36	0.40	0.013	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
D1	---	7.00	---	---	0.276	---
E1	---	7.00	---	---	0.276	---
e	---	0.50	---	---	0.020	---
b	0.20	0.25	0.30	0.008	0.010	0.012
aaa	---	0.15	---	---	0.006	---
ccc	---	0.10	---	---	0.004	---
ddd	---	0.08	---	---	0.003	---
eee	---	0.15	---	---	0.006	---
fff	---	0.05	---	---	0.002	---
MD/ME	15/15					

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. SPECIAL CHARACTERISTICS C CLASS: ccc, ddd(SPIL STANDARD)
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

7.2.3 TFBGA 8x8 161io

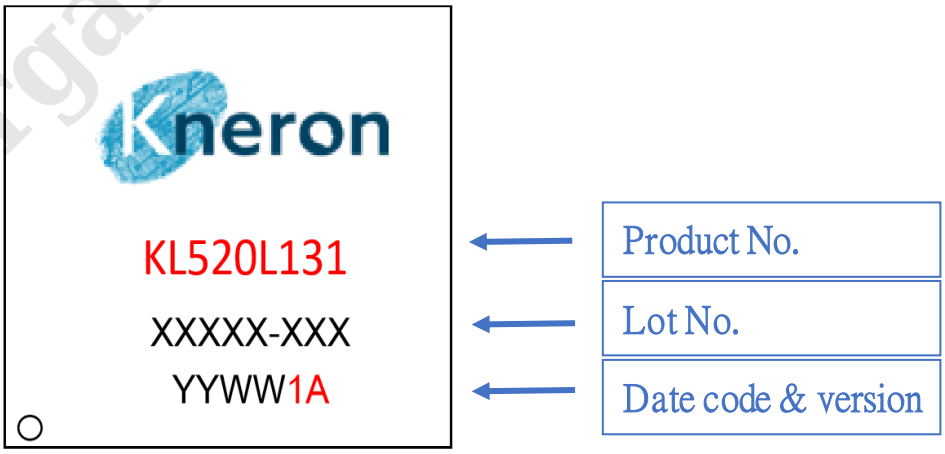


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.31	1.38	1.45	0.052	0.054	0.057
A1	0.11	0.16	0.21	0.004	0.006	0.008
A2	1.17	1.22	1.27	0.046	0.048	0.050
c	0.32	0.36	0.40	0.013	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
D1	---	7.00	---	---	0.276	---
E1	---	7.00	---	---	0.276	---
e	---	0.50	---	---	0.020	---
b	0.20	0.25	0.30	0.008	0.010	0.012
aaa	---	0.15	---	---	0.006	---
ccc	---	0.10	---	---	0.004	---
ddd	---	0.08	---	---	0.003	---
eee	---	0.15	---	---	0.006	---
fff	---	0.05	---	---	0.002	---
MD/ME	15/15					

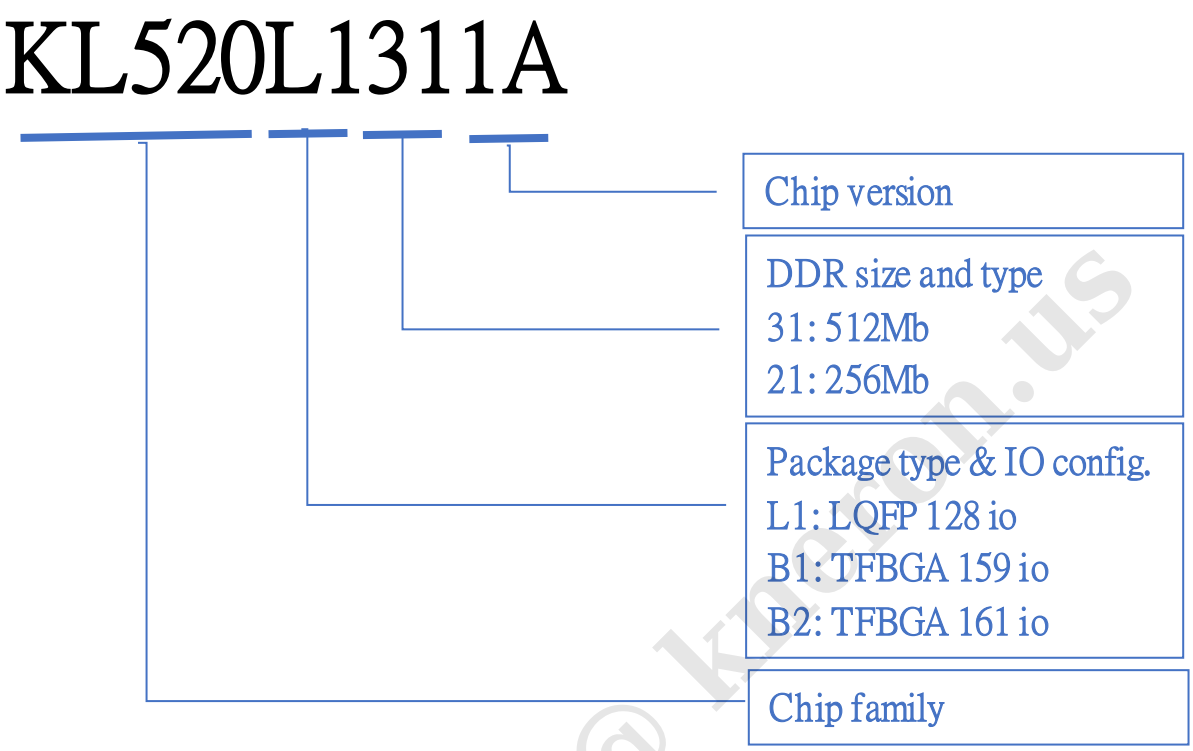
NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. SPECIAL CHARACTERISTICS C CLASS: ccc, ddd(SPIL STANDARD)
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

8 Ordering information

8.3 Top marking

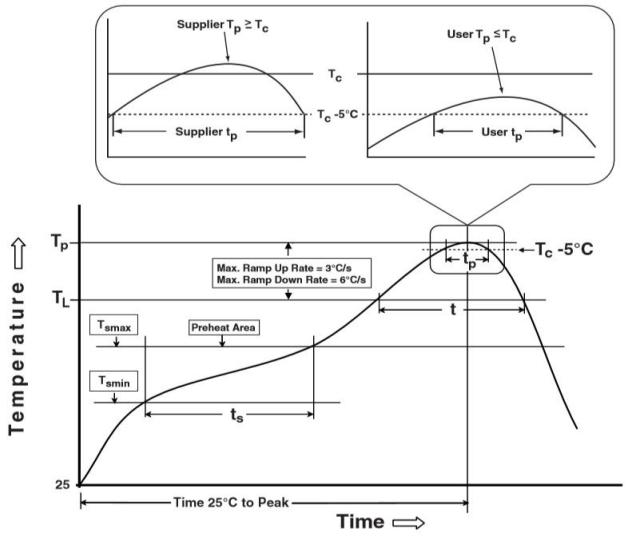


8.4 Ordering information



9 Appendix

9.3 Reflow information



Reflow profile

Table of Classification Reflow Profiles

Profile	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat and soak Min. temperature (Ts_{min}) Max. temperature (Ts_{max}) Time (ts_{min} to ts_{max}) (t_s)	 100 °C 150 °C 60 ~ 120 seconds	 150 °C 200 °C 60 ~ 120 seconds
Average ramp-up rate (Ts_{max} to T_p)	3 °C/second (Max.)	3 °C/second (Max.)
Liquid temperature (T_L) Time at liquid (t_L)	183 °C 60 ~ 150 seconds	217 °C 60 ~ 150 seconds
Peak package body temperature (T_p)*	Please refer to the classification temperature in Table 4.1 of IPC/JEDEC J-STD-020E – Classification Temperatures.	Please refer to the classification temperature in Table 4.2 of IPC/JEDEC J-STD-020E – Classification Temperatures.
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to Ts_{max})	6 °C/second (Max.)	6 °C/second (Max.)
Time to peak temperature from 25 °C	6 minutes (Max.)	8 minutes (Max.)

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g. live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e. dead-bug), T_p shall be within ±2°C of the live-bug T_p and still meet the T_c requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, please refer to JEP140 for recommended thermocouple use.
Note 2: All components in the test load shall meet the classification profile requirements.

Note 3: SMD packages classified to a given moisture sensitivity level by using Procedures of Criteria defined within any previous version of J-STD-020, JESD 22-A112 (Rescinded), IPC-SM-786 (Rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Table of IPC/JEDEC J-STD-020E: SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume (mm^3) <350	Volume (mm^3) ≧350
<2.5mm	235°C	220°C
≧2.5mm	220°C	220°C

Note 1: Previously classified SMDs should only be reclassified by the manufacture. Users should refer to the "Moisture Sensitivity" label on the bag to determine at which reflow temperature the SMD packages were classified.
Note 2: Unless labeled otherwise, level 1 SMD packages are considered to eb classified at 220℃.
Note 3: If supplier and user agree, components can be classified at temperatures other than those in Table of IPC/JEDEC J-STD-020E SnPb Eutectic Process and Pb-Free Process.

Table of IPC/JEDEC J-STD-020E: Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume (mm^3) <350	Volume (mm^3) 350~2000	Volume (mm^3) ≧350
<1.6mm	260°C	260°C	260°C
1.6mm~2.5mm	260°C	250°C	245°C
≧2.5mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak body temperature (T_p) can exceed the values specified in the Table of IPC/JEDEC J-STD-020E SnPb Eutectic Process and Pb-Free Process. the use of higher T_p does not change the classification temperature T_c.
Note 2: Package volume excludes external terminates (e.g. balls. Bumps. Lands, leads) and/or nonintegral heat heat sinks.
Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection flow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.
Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process shall be evaluated using the Pb-free classification temperatures and profiles defined in Table of IPC/JEDEC J-STD-020E - SnPb Eutectic Process and this appendix, whether or not Pb-free.
Note 5: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current version unless a change in classification level or a higher peak classification temperature is desired.

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