ACS37600K

High-Precision, Programmable Linear Hall-Effect Sensor IC

with VREF and High-Bandwidth (400 kHz) Analog Output for Core-Based Current Sensing

FEATURES AND BENEFITS

- Industry-leading noise performance
- User-programmable bandwidth (100 to 400 kHz) for easy tradeoff between speed and noise
- Very fast response time (<1.25 µs typ.)
- Wide sensing range
- Factory-programmed sensitivity and offset over temperature
- User-programmable sensitivity and offset
- User-programmable sensitivity over temperature for ferromagnetic core drift compensation
- User-programmable, bidirectional reference pin (VREF) for full control over offset levels
- Non-ratiometric output for immunity to noisy supplies
- Undervoltage and overvoltage detection
- High output drive current (15 mA)
- Low power mode for reduced I_{CC}
- VDD pin survives exposure up to 15 V
- Monolithic Hall IC for high reliability

PACKAGE: 4-pin SIP (suffix OK)

Not to scale

TYPICAL APPLICATIONS

- Current sensing modules
- Solar (MPPT, combiner box)
- Motor control
- Uninterruptible power supplies (UPS)
- Smart fuse
- Overcurrent detection
- Power supplies

DESCRIPTION

The Allegro ACS37600 is a linear sensor IC designed to be used in conjunction with a ferromagnetic core to provide a highly accurate current sensor suitable for industrial, commercial, and communications applications.

The device consists of a precise, low-offset, chopper-stabilized Hall-effect front end. Magnetic flux orthogonal to the IC package surface is sensed by the integrated Hall and converted into a proportional voltage. A very wide sensitivity range allows current sensor module makers to use this IC for a <20 A or a >1000 A module.

A selectable bandwidth from 100 kHz to >400 kHz makes the device ideal for fast switching applications and applications where low noise is required.

A user-programmable, bidirectional reference voltage pin (VREF) enables constant monitoring of the zero-current voltage and easy interfacing with 3.3 V and 5 V ADCs.

The sensitivity and offset drift over temperature are factory-programmed at Allegro to provide a highly accurate solution across the full temperature range.

The ACS37600 is customer programmable. The absolute value of sensitivity and offset can be programmed after manufacturing. Additionally, customers can program the sensitivity over temperature to compensate for ferromagnetic core drifts, enabling industry-leading current sensor accuracy.

A nonratiometric output immune to supply noise, the ability to survive up to 15 V on the supply pin, and a stellar ESD performance make the ACS37600 ideal for applications where reliability and robustness are required.

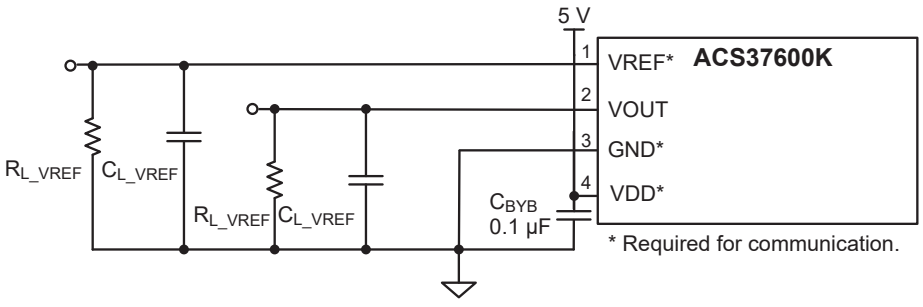


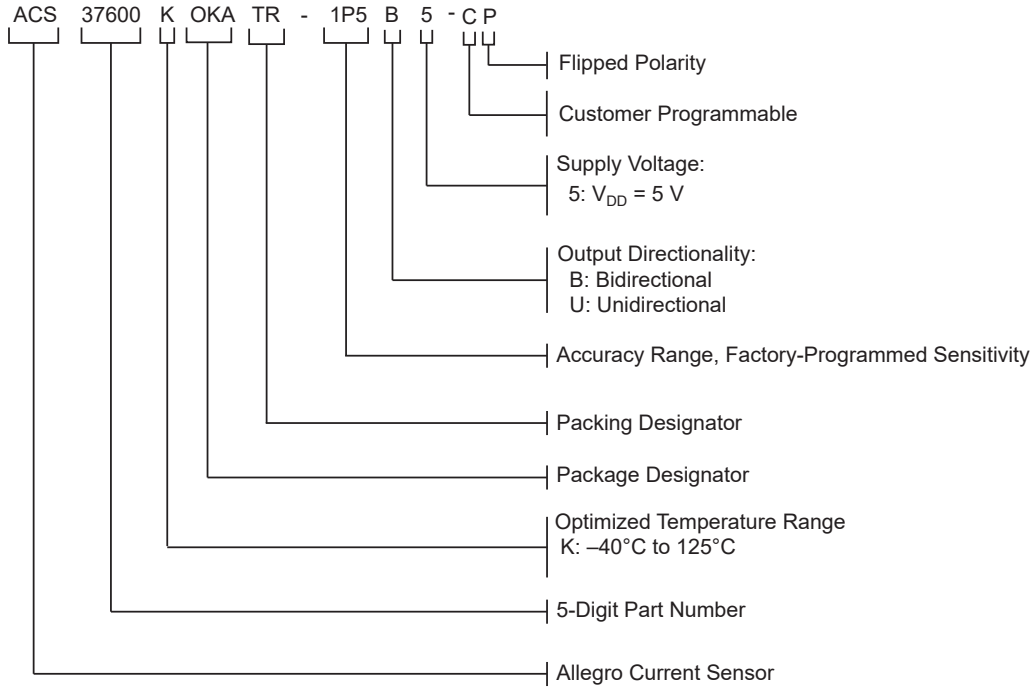
Figure 1: Typical Application Circuit for ACS37600K

SELECTION GUIDE

Part Number	Factory-Trimmed Sensitivity (mV/G)	Factory-Programmed Operating Range (G)		Programmable Sens Range (mV/G) [2]	T_A (°C)	Packing
		Bidirectional	Unidirectional [1]			
ACS37600KOKA-003B5-C	3	±667	0 to 1333	2.4 to 3.6	–40 to 125	4000 pieces per 13-inch reel
ACS37600KOKA-006B5-C	6	±333	0 to 667	4.8 to 7.2		
ACS37600KOKA-003B5-CP	–3	±667	0 to –1333	–3.6 to –2.4		
ACS37600KOKA-006B5-CP	–6	±333	0 to –667	–7.2 to –4.8		

[1] This range applies if the VREF pin is overdriven to 0.5 V.
[2] Characteristics are guaranteed within the sense programmable range of the corresponding part number.

Part Numbering Specification



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Min.	Max.	Unit
Supply Voltage	V_{DD}		–0.5	15	V
Output Voltage	V_O	Applies to V_{OUT}	–0.5	$(V_{DD} + 0.5) \le 15$	V
Reference Voltage	V_R	Applies to V_{REF}	–0.5	$(V_{DD} + 0.5) \le 6.5$	V
Operating Ambient Temperature	T_A	Range K	–40	125	°C
Storage Temperature	T_{STG}		–65	165	°C
Maximum Field Range	B	The output may still respond but linearity degrades significantly within this range	–3000	3000	G

OPERATING PARAMETERS

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Optimal Absolute Field Range	B_{OG}	Performance specifications are guaranteed at or within this limit of |B|	0	–	1650	G
Nominal Absolute Field Range	B_{NG}	Linearity degrades within this |B| range	1650	–	2000	G

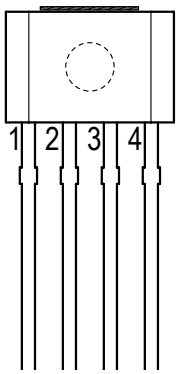

Figure 2: OK Package Pinout Diagram

(Ejector pin mark on opposite side)

Terminal List Table

Number	Name	Function
1	VREF	Zero gauss reference voltage
2	VOUT	Output signal
3	GND	Device ground terminal
4	VDD	Device power supply terminal; used for programming

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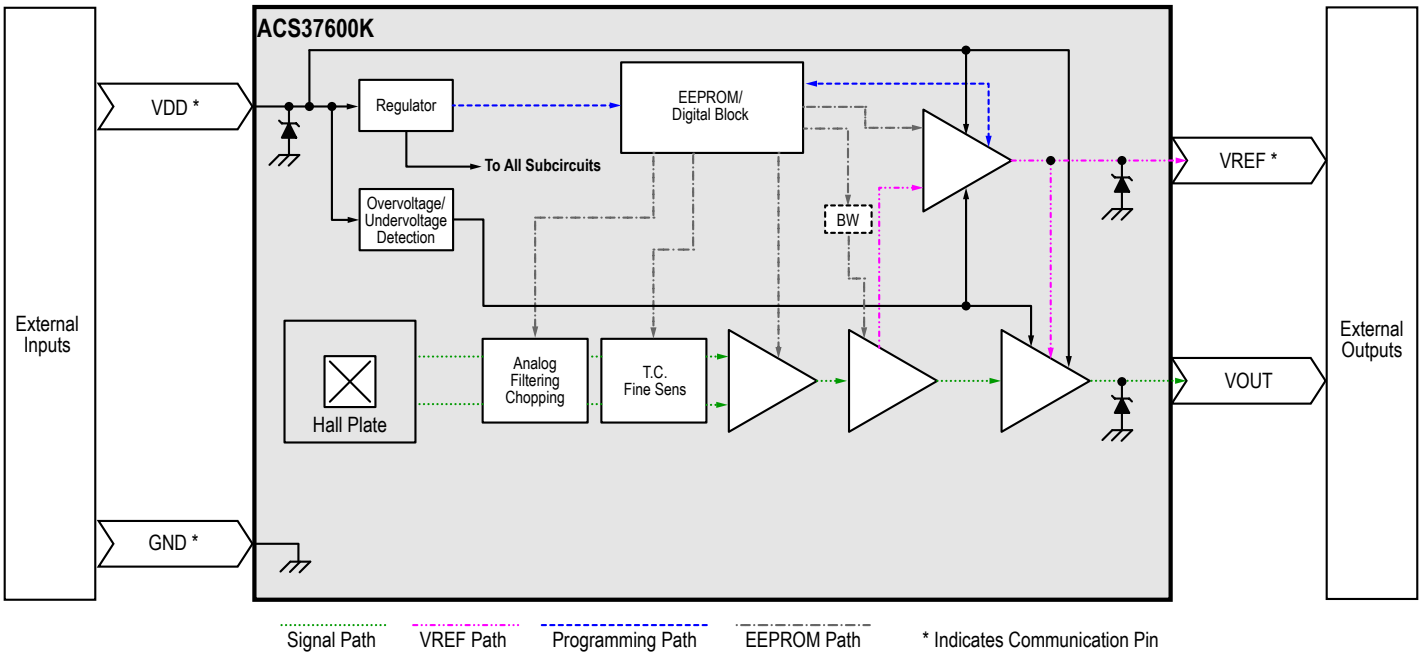
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS: Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{DD} = 5 V, ECO_MODE = 0, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		4.5	5	5.5	V
Supply Current	I_{CC}	V_{DD} = 4.5 to 5.5 V, output open, factory default	–	16	23	mA
		V_{DD} = 4.5 to 5.5 V, output open, ECO_MODE = 1	–	14	23	mA
VOUT Resistive Load	R_{L_VOUT}	VOUT to GND, VOUT to VDD	–	–	4.7	kΩ
VOUT Capacitive Load	C_{L_VOUT}	VOUT to GND	2	–	–	nF
VREF Resistive Load	R_{L_VREF}	VREF to GND	200	–	–	kΩ
VREF Capacitive Load	C_{L_VREF}	VREF in input/output mode, VREF to GND	0.5	–	47	nF
		VREF in output mode only, VREF to GND	0.5	–	4.7	nF
Supply Bypass Capacitor	C_{BYPASS}	VDD to GND	–	0.1	–	µF
Power-On Reset Release Voltage	V_{POR}	V_{DD} rising 1 V/ms	3.6	3.8	3.9	V
Power-On Reset Hysteresis	V_{POR_HYS}		250	400	560	mV
Power-On Reset Release Time [1]	t_{PORR}		–	95	–	µs
Power-On Reset Output Delay [1]	t_{POR_OUT}	C_{L_VREF} = 4.7 nF, no R_{L_VOUT}	–	8	–	µs
Power-On Reset Reference Delay [1]	t_{POR_REF}	V_{REF} in output/input or output only mode; no R_{L_VREF}, C_{L_VREF} = 4.7 nF	–	17	–	µs
Power-On Delay [1]	t_{PO}	T_A = 25°C, V_{REF} in input only mode, driven to 2.5 V; C_{L_VOUT} = 4.7 nF, no R_{L_VOUT}	–	103	–	µs
		T_A = 25°C, V_{REF} in input/output or output only mode, driving to 2.5 V; C_{L_VOUT} and C_{L_VEF} = 4.7 nF, no R_{L_VOUT} or R_{L_VREF}	–	112	–	µs
Temperature Compensation Update Rate	t_{UR}		–	8	–	ms
Undervoltage Detection Threshold	V_{UVD}	T_A = 25°C, V_{DD} falling 1 V/ms	4	–	4.4	V
Undervoltage Detection Hysteresis	V_{UVD_HYS}		–	0.4	–	V
Undervoltage Detection Time [1] [2]	t_{UVD}	$V_{DD} < V_{UVD}$	35	64	90	µs
Undervoltage Detection Release Time [1] [2]	t_{UVD_R}	$V_{DD} > (V_{UVD} + V_{UVD\_HYS})$	–	8	–	µs
Overvoltage Detection Threshold	V_{OVD}	T_A = 25°C, VDD rising 1 V/ms	7.2	7.6	8	V
Overvoltage Detection Hysteresis	V_{OVD_HYS}	T_A = 25°C	–	1	–	V
Overvoltage Detection Time [1]	t_{OVD}	$V_{DD} > V_{OVD}$	35	64	90	µs
Overvoltage Detection Release Time [1]	t_{OVD_R}	$V_{DD} < (V_{OVD} - V_{OVD\_HYS})$	–	7	–	µs

[1] Timing parameters are based off design and characterization data.
[2] Power-on release threshold is either V_{POR} if UVD_DIS = 1 or V_{UVD} if UVD_DIS = 0. Factory default setting is UVD_DIS = 0.

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ELECTRICAL CHARACTERISTICS (continued): Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{DD} = 5 V, ECO_MODE = 0, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
OUTPUT OPERATING CHARACTERISTICS (VOUT)							
Output Saturation Voltage	V_{SAT_H}	R_{L_VOUT} = 2 kΩ to GND		V_{DD} – 0.3	–	–	V
	V_{SAT_L}	R_{L_VOUT} = 2 kΩ to GND		0	–	0.4	V
DC Output Resistance	R_{OUT}			–	2	5	Ω
Output Maximum Drive Current	I_{OD}	Drive mode: Turbo		–	–	15	mA
		Drive mode: Economy		–	–	7.5	mA
Rise Time	t_R	T_A = 25°C, C_{L_VOUT} = 4.7 nF, C_{BYPASS} = 1 µF	BW = 100 kHz	–	2.4	3.5	µs
			BW = 250 kHz	–	1.65	2.5	µs
			BW = 400 kHz	–	1.2	2	µs
			BW = 450 kHz	–	1.15	–	µs
Propagation Delay	t_{PD}	T_A = 25°C, C_{L_VOUT} = 4.7 nF, C_{BYPASS} = 1 µF	BW = 100 kHz	–	0.9	1.5	µs
			BW = 250 kHz	–	0.85	1.4	µs
			BW = 400 kHz	–	0.75	1.3	µs
			BW = 450 kHz	–	0.7	–	µs
Response Time	t_{RESP}	T_A = 25°C, C_{L_VOUT} = 4.7 nF, C_{BYPASS} = 1 µF	BW = 100 kHz	–	3.5	6	µs
			BW = 250 kHz	–	2.4	3.5	µs
			BW = 400 kHz	–	1.25	2.5	µs
			BW = 450 kHz	–	1.2	–	µs
Noise Density	N_D	T_A = 25°C, at 400 kHz	T_A = 25°C	–	1.21	1.64	mG/√Hz
			T_A = 125°C	–	1.69	2.25	mG/√Hz
Noise	N	T_A = 25°C, C_{L_VOUT} = 1 nF, Sens = 3 mV/G, BW = 400 kHz	T_A = 25°C	–	2.83	–	mV_{RMS}
			T_A = 125°C	–	3.61	–	mV_{RMS}
Nonlinearity	E_{LIN}	T_A = –40°C to 125°C, |B| ≤ 1650 G		–0.5	±0.25	0.5	%
		T_A = –40°C to 125°C, 2000 G > |B| > 1650 G		–1	–	1	%
Power Supply Sensitivity Error	E_{SENS_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$		–5	±0.25	5	mV
Power Supply Offset Error	V_{OE_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$		–0.5	–	0.5	%
VOUT Short-Circuit Current	I_{SC_VOUT}	T_A = 25°C, VOUT shorted to GND		–	30	–	mA
		T_A = 25°C, VOUT shorted to VDD		–	–30	–	mA
REFERENCE OUTPUT OPERATING CHARACTERISTICS (VREF)							
VREF Noise Density	N_{D_VREF}	f > 100 Hz		–	0.5	–	µV/√Hz
DC Internal Reference Output Resistance	R_{REF_INT}	Output/Input Mode		150	200	300	Ω
		Output Mode Only		–	2	5	Ω
		Input Mode Only		–	200	–	kΩ
Reference Voltage Input Range	V_{REF_IN}	T_A = 25°C, VREF overdriven externally		0.5	–	2.65	V
VREF Short-Circuit Current	I_{SC_VREF}	T_A = 25°C, VREF shorted to GND		0.5	0.7	1	mA
		T_A = 25°C, VREF shorted to VDD			5	10	mA

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ELECTRICAL CHARACTERISTICS (continued): Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{DD} = 5 V, ECO_MODE = 0, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
PROGRAMMABLE CHARACTERISTICS: QUIESCENT VOLTAGE AND REFERENCE VOLTAGE							
Reference Voltage Coarse	$BITS_{VREF\_COARSE}$	VREF_COARSE		–	2	–	bit
Reference Voltage Fine	$BITS_{VREF\_FINE}$	VOFF_FINE		–	9	–	bit
Factory-Programmed Reference Voltage	V_{REF}			–	2.5	–	V
Average VREF Programming Step Size	$STEP_{VREF}$	T_A = 25°C		–	0.98	–	mV
Reference Voltage Temperature Compensation Step Size	$STEP_{VREF\_TC}$	Step size at each of TC point		–	$STEP_{VREF}$	–	mV
Reference Voltage Output Programming Range	V_{REF_OUT}	T_A = 25°C; VREF_FINE programming range for a given VREF_COARSE	VREF_COARSE = 11; factory default	2.35	2.5	2.65	V
			VREF_COARSE = 10	1.5	1.65	1.8	V
			VREF_COARSE = 01	1.35	1.5	1.65	V
			VREF_COARSE = 11	0.35	0.5	0.65	V
Offset Voltage Programming Bits	$BITS_{VOFF\_FINE}$	VOFF_FINE		–	9	–	bit
Factory-Programmed Quiescent Voltage Output	V_{QVO}	T_A = 25°C; 0 G		–	V_{REF}	–	V
Offset Voltage Programming Step Size	$STEP_{VOE}$	$V_{OE} = V_{QVO} - V_{REF}$		–	1.15	–	mV
Offset Voltage Temperature Compensation Step Size	$STEP_{VOE\_TC}$	Step size at each of TC point		–	$STEP_{VREF}$	–	mV
Offset Voltage Programming Range	V_{OE_PR}	$V_{OE} = V_{QVO} - V_{REF}$		–200	–	200	mV
PROGRAMMABLE CHARACTERISTICS: SENSITIVITY							
Coarse Sensitivity Programming Bits	$BITS_{SENS\_C}$	SENS_COARSE		–	2	–	bit
Sensitivity Programming Bits	$BITS_{SENS\_FINE}$	SENS_FINE		–	9	–	bit
Factory-Programmed Sensitivity	Sens	T_A = 25°C	SENS_COARSE = 10; 006B5-C/CP	–	6	–	mV/G
			SENS_COARSE = 01; 003B5-C/CP	–	3	–	mV/G
Average Sensitivity Step Size	$STEP_{SENS}$	T_A = 25°C; SENS_FINE programming step size for a given SENS_COARSE	SENS_COARSE = 10	13.14	15.11	17.78	µV/G
			SENS_COARSE = 01	6.57	7.56	8.89	µV/G
Sensitivity Temperature Compensation Step Size	$STEP_{SENS\_TC}$	Step size at each of TC point		–	$STEP_{SENS}$	–	Sens

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ELECTRICAL CHARACTERISTICS (continued): Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{DD} = 5 V, ECO_MODE = 0, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
PROGRAMMABLE CHARACTERISTICS: SENSITIVITY (CONTINUED)							
Sensitivity Programming Range	$Sens_{PR}$	T_A = 25°C; SENS_FINE programming range for a given SENS_COARSE	SENS_COARSE = 10	4.8	–	7.2	mV/G
			SENS_COARSE = 01	2.4	–	3.6	mV/G
Sensitivity Slope Over Temperature Bits	$BITS_{SENS\_SLOPE}$	GAIN_TC		–	6	–	bit
Sensitivity Slope Temperature Coefficient Step Size	$STEP_{SENS\_SLOPE}$			–	0.002	–	%/°C
Sensitivity Slope Temperature Coefficient Programming Range	$Sens_{SLOPE\_PR}$			–0.025	–	0.05	%/°C

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ACS37600KOK DEVICE PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{DD} = 5 V, ECO_MODE = 0, unless otherwise specified

Characteristics[1]	Symbol	Test Conditions	Min.[2]	Typ.[3]	Max.[2]	Unit
ERROR COMPONENTS						
Sensitivity Error	E_{SENS}	T_A = 25°C	–1.75	±0.6	1.75	%
		T_A = 25°C to 125°C, with respect to 25°C	–1.75	±0.6	1.75	%
		T_A = –40°C to 25°C, with respect to 25°C	–3.5	±1	3.5	%
Quiescent Voltage Output Error	V_{QVO_E}	B = 0 G, T_A = 25°C	–10	±2	10	mV
		B = 0 G, T_A = 25°C to 125°C, with respect to 25°C	–10	±2.5	10	mV
		B = 0 G, T_A = –40°C to 25°C, with respect to 25°C	–16	±5	16	mV
Reference Voltage Output Error	V_{REF_E}	T_A = 25°C	–10	±2	10	mV
		T_A = 25°C to 125°C, with respect to 25°C	–10	±2.2	10	mV
		T_A = –40°C to 25°C, with respect to 25°C	–10	±2	10	mV
Offset Error	V_{OE}	B = 0 G, T_A = 25°C	–10	±1	10	mV
		B = 0 G, T_A = 25°C to 125°C, with respect to 25°C	–10	±1	10	mV
		B = 0 G, T_A = –40°C to 25°C, with respect to 25°C	–14	±4	14	mV
ERROR COMPONENTS LIFETIME DRIFT[4]						
Sensitivity Error Lifetime Drift	E_{SENS_LTD}	T_A = 25°C	–	±0.6	–	%
Quiescent Voltage Output Error Lifetime Drift	V_{QVO_LTD}	B = 0 G, T_A = 25°C	–	±1.2	–	mV
Reference Voltage Output Error Lifetime Drift	V_{REF_LTD}	B = 0 G, T_A = 25°C	–	±1	–	mV
Offset Error Lifetime Drift	V_{OE_LTD}	B = 0 G, T_A = 25°C	–	±0.5	–	mV

[1] Characteristics are valid within the sense programmable range of the corresponding part number.
[2] Min. and Max. is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ± 3σ from production characterization data was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime.
[3] Typical values are |mean| +1σ based on production characterization data.
[4] Lifetime drift typical values are worst case mean values seen during AEC Q-100 qualification.

ACS37600KOK-CP DEVICE PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{DD} = 5 V, ECO_MODE = 0, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Polarity Bit	–	Flipped polarity		Enabled		–

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FUNCTIONAL DESCRIPTION

Introduction

The Power-On thresholds of the ACS37600 are based on a combination of a check on the internal regulator supplied and V_{DD}. This allows the ACS37600 to accurately report a signal, including internal stress and temperature compensation, at startup. To ensure that the device output is reporting accurately, the ACS37600 contains an overvoltage and an undervoltage detection flag. This internal flag on V_{OUT} can be used to alert the system when the supply voltage for the device is outside of the operational range by putting the output into a known high-impedance (high Z) state. If one or both are not desired, the UVD and OVD functionality can be individually toggled off.

The provided graphs in this section show V_{OUT} moving with V_{DD}. The voltage of V_{OUT} during a high Z state will be most consistent with a known load (R_{L_VOUT}, C_{L_VOUT}, R_{L_VREF}, C_{L_VREF}). Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 all use the same labeling scheme for different power thresholds. References in brackets "[ ]" are valid for each of these plots.

POWER-ON OPERATION

Note that the ACS37600 comes factory programmed with UVD enabled.

UVD Enabled

When UVD is enabled, as V_{DD} ramps up, the ACS37600 V_{OUT} and V_{REF} pins are high Z until V_{DD} reaches and passes V_{UVD} [2]. Once V_{DD} passes [2], the device takes some time without V_{DD} dropping below V_{POR} -V_{POR_HYS} [8] before the device enters normal operation.

UVD Disabled

When UVD is disabled, as V_{DD} ramps up, the ACS37600 V_{OUT} and V_{REF} pins are high Z until V_{DD} reaches and passes V_{POR} [1]. Once V_{DD} has passed V_{POR} [1], V_{OUT} enters normal operation.

POWER-OFF OPERATION

UVD Enabled

When UVD is enabled, before the device powers off, it will force V_{OUT} to GND if V_{DD} reaches below $V_{UVD} - V_{UVD\_HYS}$ [6]. When V_{POR}-V_{POR_HYS} [8] is reached, V_{OUT} and V_{REF} will go high Z.

UVD Disabled

When UVD is disabled, then V_{REF} and V_{OUT} will continue to report until V_{DD} is less than $V_{POR} - V_{POR\_HYS}$ [8], at which point,V_{OUT} and V_{REF} will enter a high Z state.

Note: since the device is entering a high Z state and not driving the output, the time it takes the output to reach a steady state will depend on the external circuitry used.

Voltage Thresholds

POWER-ON RESET RELEASE VOLTAGE(V_{POR})

If V_{DD} falls below $V_{POR} - V_{POR\_HYS}$ [8] while in operation, the digital circuitry turns off and the output will re-enter a high Z state. After V_{DD} recovers and exceeds V_{UVD} [2], the output will begin reporting again after the delay of t_{PO}.

UNDERVOLTAGE DETECTION THRESHOLD (V_{UVD})

The 5 V devices are factory-programmed with UVD enabled. It is important to note that when powering up the device for the first time after a Power-On Reset event, V_{OUT} and V_{REF} will remain high Z until V_{DD} is raised above V_{UVD} [2], at which point the V_{OUT} and V_{REF} outputs will begin to normal operation. If UVD is disabled, V_{OUT} and V_{REF} will begin normal operation after V_{DD} raises above V_{POR} [1] under the same conditions.

If V_{DD} drops below $V_{UVD} - V_{UVD\_HYS}$ [6] after normal operation, V_{OUT} will pull to GND regardless of R_{L_VOUT} configuration. The V_{OUT} will remain at GND until V_{DD} raises above V_{UVD} [7] or V_{DD} falls below $V_{POR} - V_{POR\_HYS}$ [8]. If V_{DD} rises above V_{UVD} [7] after a UVD event, the V_{OUT} and V_{REF} outputs will resume operation. If V_{DD} drops below $V_{POR} - V_{POR\_HYS}$ [8], the device will enter a POR event and reset; V_{OUT} and V_{REF} will switch to high Z if this occurs.

OVERVOLTAGE DETECTION THRESHOLD (V_{OVD})

When V_{DD} raises above V_{OVD} [4], the output of the V_{OUT} and V_{REF} pin will go high Z, V_{REF} be pulled to GND, and V_{OUT} will be pulled to either VDD or GND, depending if R_{L_VOUT} is in a pull-up or pull-down configuration.

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OVERVOLTAGE/UNDERVOLTAGE DETECTION HYSTERESIS (V_{OVD_HYS}, V_{UVD_HYS})

There is hysteresis between enable and disable thresholds to reducing nuisance flagging and clears.

Timing Thresholds

Overvoltage and Undervoltage Detection Time and Detection Release Time (t_{OVD}/t_{OVD_R}, t_{UVD}/t_{UVD_R})

The enable time for OVD, t_{OVD}, is the time from V_{OVD} [4] to OVD flag [B]. The UVD enable time, t_{UVD}, is the time from $V_{UVD} – V_{UVD\_HYS}$ [6] to the UVD flag [D]. The enable flag for both OVD and UVD have a counter to reduce transients faster than 64 µs from nuisance flags.

If V_{DD} ramps from $>V_{UVD} – V_{UVD\_HYS}$ [6] to $<V_{POR} – V_{POR\_HYS}$ [8] faster than t_{UVD} (≈64 µs), then the device will not have time to report a UVD event before power off occurs.

The detection release time for OVD, t_{OVD_R}, is the time from $V_{OVD} – V_{OVD\_HYS}$ [5] to the OVD clear to normal operation [C]. The UVD disable time, t_{UVD_R}, is the time from V_{UVD} [7] to the point that the UVD flag clears and V_{OUT} returns to nominal operation [E]. The disable time does not have a counter for either OVD or UVD to release the output and resume reporting.

Power-On Reset (POR)

If V_{DD} falls below $V_{POR} – V_{POR\_HYS}$ [8] while in operation, the output will re-enter a high Z state. After V_{DD} recovers and exceeds V_{UVD} [2], the output will begin reporting again after the delay of t_{PO}. This t_{PO} depends on t_{PORR}, t_{POR_OUT} and, t_{POR_REF}.

Power-On Reset Release Time (t_{PORR})

When V_{DD} rises above V_{UVD} [2], the Power-On Release Time counter starts. If UVD is disabled, this threshold is V_{POR} [1]. The output will only release from high Z to nominal operation after the Power-On Reset counter has reached the internal t_{PORR} value and the temperature compensation has been updated. This allows for robust and stable output reporting that is temperature compensated. If V_{DD} falls below $V_{POR} – V_{POR\_HYS}$ [8] before the counter finishes, the counter is reset and the part remains in the reset state.

Power-On Reset Output Delay (t_{POR_OUT})

The term t_{POR_OUT} is defined as the time required for the output to reach 90% of its stable state around V_{REF} after t_{PORR}. This is best measured with V_{REF} either being overdriven or externally supplied. Because V_{OUT} takes direct input and is centered at V_{REF}, the output stable state is $V_{OUT(Field)} = Sens \times Field + V_{REF}$. Refer to the next section for discussion of the implications of V_{REF} driven internally.

Power-On Reset Reference Delay (t_{POR_REF})

The term t_{POR_REF} is defined as the time required for the V_{REF} output to drive the pin to 90% V_{REF} stable state from the high-Z state. The voltage on the VREF pin is the common mode voltage for the V_{OUT} amplifier and dictates the zero for V_{OUT}.

The VREF pin is meant to be overdriven, which is achieved by limiting the drive strength of the output amplifier. This drive limitation makes the t_{POR_REF} extremely dependent on the application circuit elements R_{L_VREF} and C_{L_VREF}. This dependency should be considered when selecting the R_{L_VREF} and C_{L_VREF} values.

Power-On Delay (t_{PO})

When the supply is ramped to V_{UVD} [2], the device requires a finite time to power its internal components before the outputs are released from high Z and can respond to an input magnetic field. Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, which can be viewed as the time from [2] to [A] or [a], depending on the V_{REF} configuration. After this delay, the output quickly approaches $V_{OUT(Field)} = Sens \times Field + V_{REF}$. An externally driven V_{REF} t_{PO} is shown in Figure 7, and the internally driven V_{REF} t_{PO} is shown in Figure 8.

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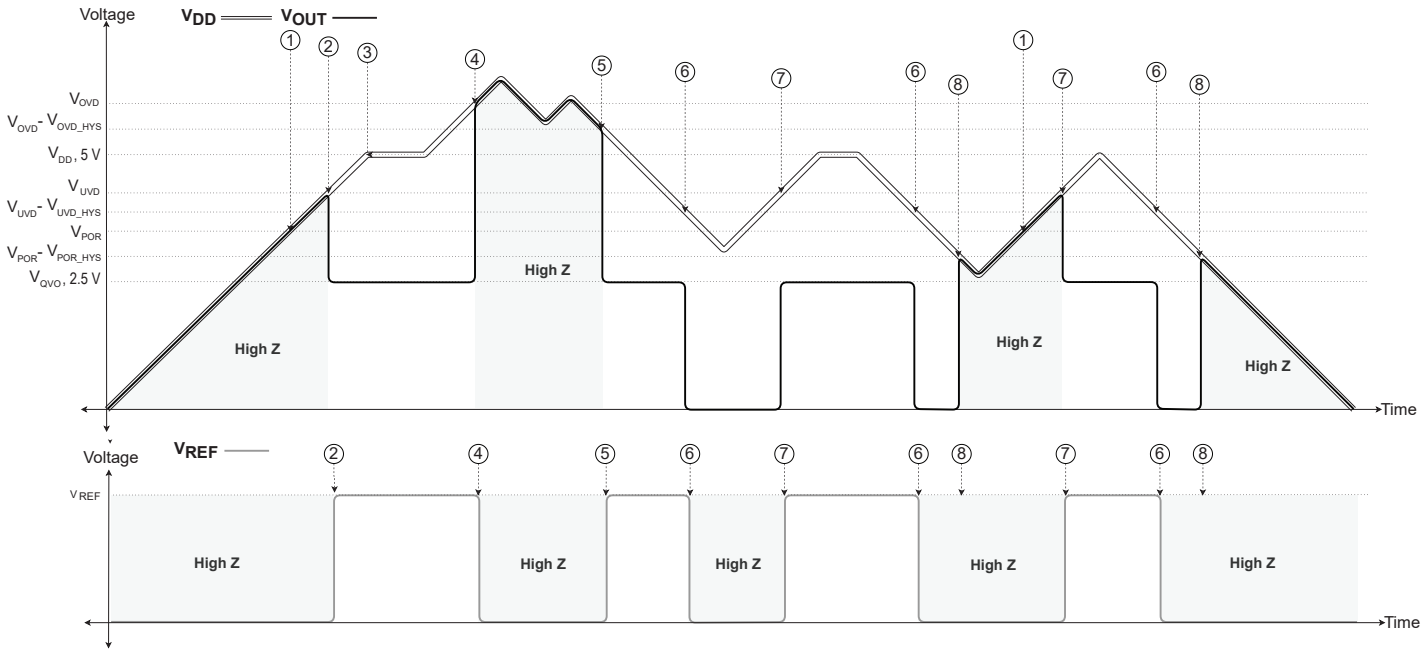

Figure 3: Power States Thresholds with VOUT and VREF Behavior, R_L = Pull Up, UVD Enabled

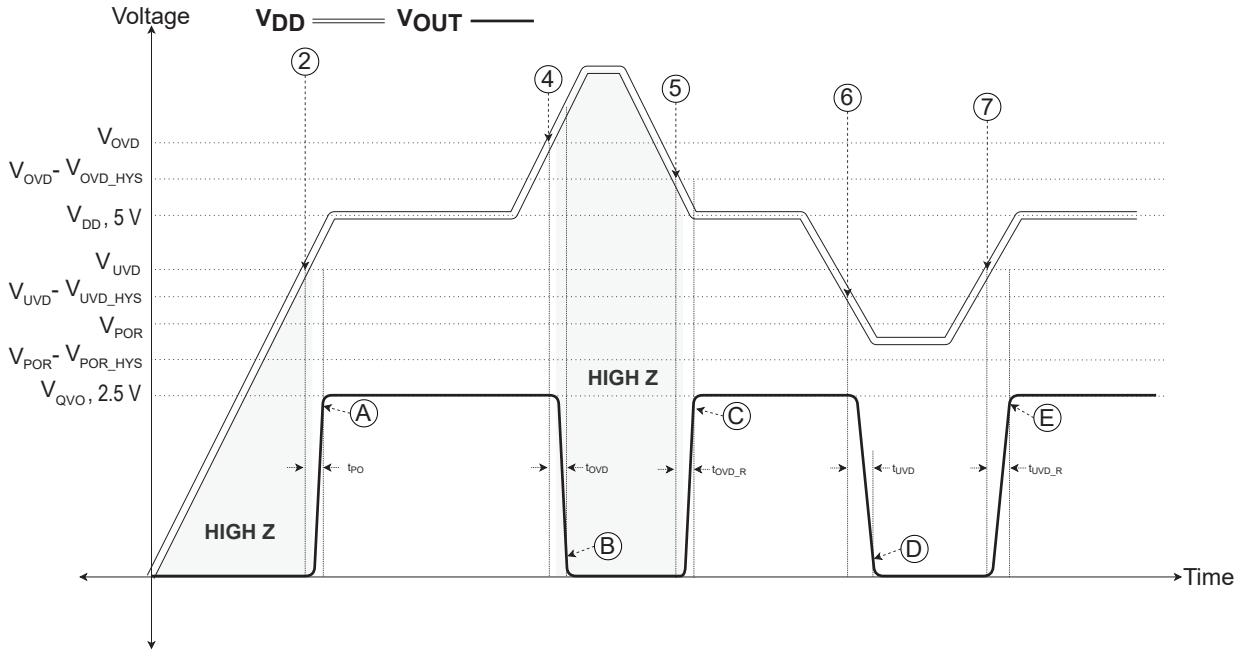

Figure 4: t_{PO}, t_{OVD}/t_{OVD_R}, and t_{UVD}/t_{UVD_R}, Behavior with Fast V_{DD} Ramping

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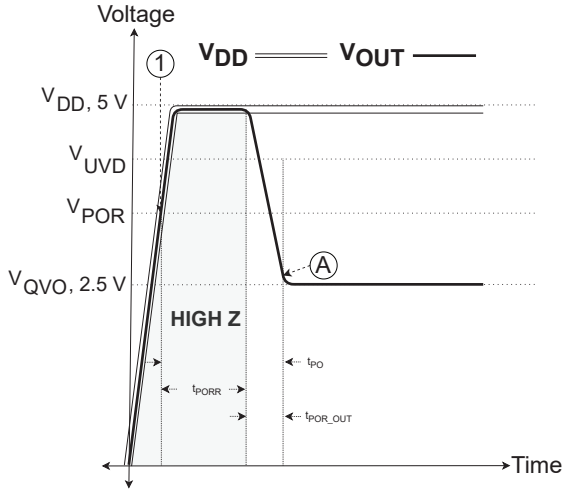

Figure 5: Power-on Reset Behavior, UVD Disabled, R_L = Pull-Up

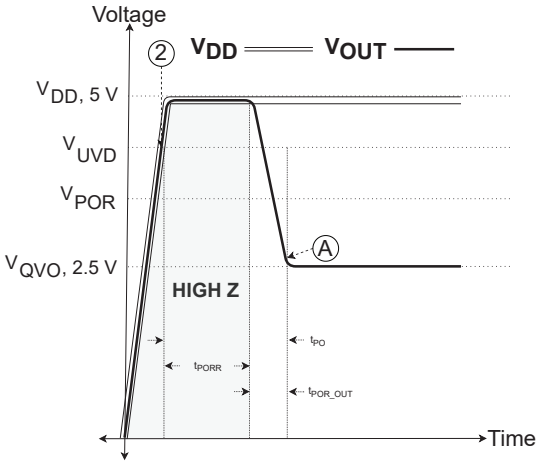

Figure 6: Power-on Reset Behavior, UVD Enabled, R_L = Pull-Up

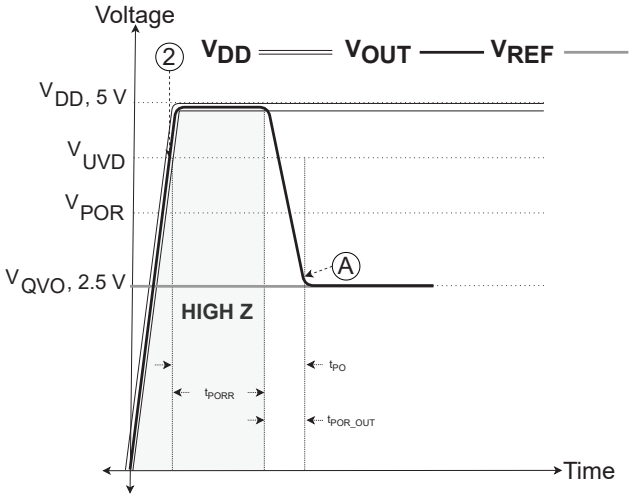

Figure 7: t_{PO} V_{OUT} Behavior with V_{REF} Externally Driven, t_{POR_OUT}, R_L = Pull-Up

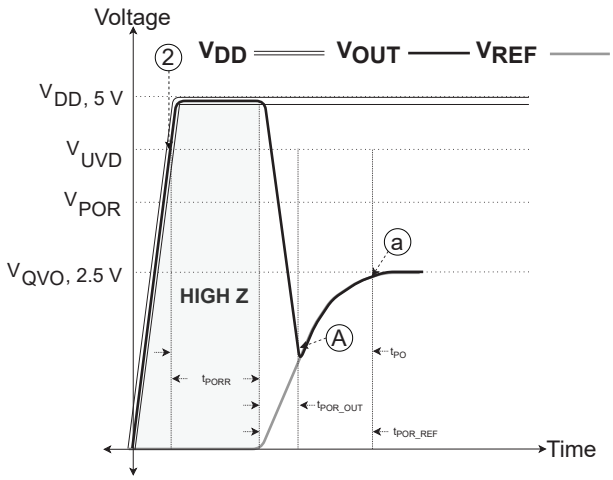

Figure 8: t_{PO} V_{OUT} Behavior with V_{REF} Internally Driven, t_{POR_REF}, R_L = Pull-Up

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DEFINITIONS OF OPERATING AND PERFORMANCE CHARACTERISTICS

Quiescent Voltage Output (V_{QVO})

The quiescent voltage output is defined as the voltage on the output VOUT when zero gauss is applied. V_{QVO} is determined by two quantities, the VREF pin voltage and the VOFF_FINE register that adjusts the output channel offset error from the VREF pin.

Quiescent Voltage Output Error(V_{QVO_E})

Quiescent Voltage Output Error, or V_{QVO_E}, is defined as the drift of V_{OUT} from room to hot or room to cold (25°C to 125°C or 25°C to –40°C, respectively). Temperature drift is compensated with the Allegro factory trim to remain within the limits across temperature; because of this, only room-trimming/programming is needed. This parameter is controlled by the VOFF_FINE register. Programming too close (<32 LSB) to the minimum and maximum values of the VOFF_FINE register will affect temperature performance. This compensation is performed in increments of $STEP_{VOE}$ over temperature.

Reference Voltage Output (V_{REF})

The reference voltage output pin (VREF) is used as the common-mode voltage reference for the output channel V_{OUT}. The voltage of the VREF pin determines the quiescent voltage, V_{OUT}, of the output amplifier, allowing the pin to be driven internally, externally, and overdriven to change the quiescent output voltage. This pin can be programmed to operate as input-only, output-only, or input/output using the IO_VREF_MODE register. The output voltage can also be adjusted with two internal VREF DACs: VREF_COARSE, which determines the coarse range that VREF_FINE can adjust, and fine tune. For further information about these registers, refer to the Defining Programming Parameters section.

- V_{REF} programmable range is 0.35 to 2.65 V
- V_{REF} can be overdriven to 0.5 to 2.65 V

Reference Voltage Temperature Drift (V_{REF_E})

Reference voltage temperature drift, V_{REF_E}, is defined as the drift of VREF from room to hot or room to cold (25°C to 125°C or 25°C to –40°C, respectively). Only room-trimming/programming is needed because temperature drift is compensated with the Allegro factory trim to remain within the limits across temperature. This parameter is controlled by the VREF_FINE register. Programming too close (<32 LSB) to the minimum and maximum values of the VREF_FINE register will affect temperature performance. This compensation is performed in increments of $STEP_{VREF}$ over temperature. V_{REF_E} is dependent on the VREF_COARSE register. If VREF_COARSE is changed from factory default, V_{REF_E} may not meet datasheet parameters.

Reference Voltage Programming Step Size ($STEP_{VREF}$)

Reference voltage programming step size is defined as the average change in VREF voltage per an LSB change in VREF_FINE register.

Offset Voltage (V_{OE})

Offset voltage, V_{OE}, is defined as $V_{QVO} - V_{REF}$. The voltage offset between the output and V_{REF} can be adjusted with the VOFF_FINE register. For best accuracy, verify actual device step size and result when trimming.

Offset Voltage Programming Step Size ($STEP_{VOE}$)

Offset voltage programming step size is defined as the average of change in $V_{QVO} - V_{REF}$ voltage per an LSB change in the VOFF_FINE register. For best accuracy, verify the actual device step size and result when trimming.

Output Saturation Voltage ($V_{SAT\_H/L}$)

Output saturation voltage, V_{SAT}, is defined as the voltage at which output no longer changes when the magnitude of the magnetic field is increased. V_{SAT_H} is the highest voltage the output can drive, while V_{SAT_L} is the lowest. Note that changing the sensitivity does not change the V_{SAT} points.

Power Supply Offset Error (V_{OE_PS})

Power supply offset error, V_{PS}, is defined as the offset error in mV between V_{DD} at 5 V to 4.5 V and 5 V to 5.5 V.

Power Supply Sensitivity Error (E_{SENS_PS})

Power supply sensitivity error, EPS, is defined as the percentage of the sensitivity error measured between V_{DD} at 5 V to 4.5 V and 5 V to 5.5 V.

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Sensitivity (Sens)

Sensitivity, or Sens, is the output swing in the presence of a magnetic field, perpendicular to and out of the top surface of the package face. This magnetic field moves the output voltage away from its V_{OUT} and toward the supply voltage rails. The magnitude and direction of the output voltage swing is proportional by Sens to the magnitude and direction of the applied magnetic field. The Sens of the device is calculated slightly differently for unidirectional application (positive or negative operating range) and bidirectional (positive and negative operating range) parts.

Bidirectional parts have sensitivity defined as:

$$Sens = \frac{V_{OUT(B_1)} - V_{OUT(B_2)}}{B_1 - B_2}$$

Parts in a unidirectional application have sensitivity defined as:

$$Sens = \frac{V_{OUT(B+)} - V_{QVO}}{B+}$$

$$Sens = \frac{V_{OUT(B-)} - V_{QVO}}{B-}$$

B+/B- are two magnetic fields with opposite polarities, and $V_{OUT(B+)}$ and $V_{OUT(B-)}$ are the output voltages at the applied fields. V_{QVO} is the actual measured offset voltage, not calculated. The fine sensitivity of the device can be programmed and controlled by the SNS_FINE register.

Sensitivity Programming Range ($Sens_{PR}$)

Sensitivity programming range, $Sens_{PR}$, is the sensitivity programming range of the device with the SNS_FINE register. The SNS_FINE register scales with the SNS_COARSE register to determine the Sens range of a given device; for specific devices, refer to the Device Performance Characteristics section. Sensitivity can be programmed from the factory value within the Sensitivity Programming Range limits. Exceeding the specified $Sens_{PR}$ limits can cause the device to operate beyond datasheet limits. For further information about these registers, refer to the Defining Programming Parameters section.

Sensitivity Error (E_{SENS})

Sensitivity error, or E_{SENS} , is defined as the drift of Sens from room to hot or room to cold (25°C to 125°C or 25°C to –40°C, respectively). Only room-trimming/programming is needed because temperature drift is compensated with the Allegro factory trim to remain within limits across temperature. This parameter is controlled by the SNS_FINE register. Programming too close (<32 LSB) to the $STEP_{SENS}$ min and max values affects temperature performance. This compensation is performed in increments of $STEP_{SENS}$ over temperature and, because $STEP_{SENS}$ is dependent on SNS_COARSE, the E_{SENS_TC} limit is only valid for factory-programmed SNS_COARSE.

Average Sensitivity Step Size ($STEP_{SENS}$)

Average sensitivity step size, $STEP_{SENS}$, is defined as the average change in the magnetic sensitivity of the device with an LSB change to the SNS_FINE register. $STEP_{SENS}$ is dependent on SNS_COARSE; as such, the device $STEP_{SENS}$ varies for different SENS_COARSE settings.

Polarity

Polarity can be changed using the GC_POL register, inverting the output response to a magnetic field. If this is changed from the factory default, then E_{SENS_TC}, V_{OFF_TC}, and V_{REF_TC} may not meet datasheet limits. The default fault polarity is a positive output swing in the presence of a magnetic field, perpendicular and out of the top surface of the package face, as shown in Figure 9.

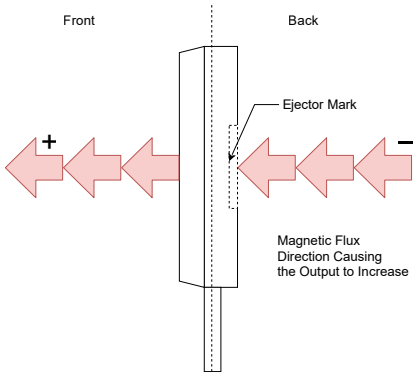

Figure 9: OK Package Flux and Output Directionality

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Nonlinearity (E_{LIN})

As the amount of field applied to the part changes, the sensitivity of the device can also change slightly. This is referred to as linearity error, or E_{LIN}. Consider two magnetic fields, B1(1/2 FS) and B2(FS). Ideally, the sensitivity of the device is the same for both fields. Linearity Error is calculated as the percent change in sensitivity from one field to another. Error is calculated separately for positive ($E_{LIN(+)}$) and negative ($E_{LIN(–)}$) magnetic fields, and the percent errors are defined as:

$$E_{LIN(\pm)} = [1 - Sens_{B2\pm} / (Sens_{B1\pm})] \times 100\%$$

where:

$$Sens_{Bx+} = (V_{OUTBx+} - QVO) / B_{x+}$$

and

$$Sens_{Bx-} = (V_{OUTBx-} - QVO) / B_{x-}$$

B_x are positive and negative magnetic fields, such that $|B_{+2}| = 2 \times |B_{+1}|$ and $|B_{-2}| = 2 \times |B_{-1}| \times E_{LIN} = \max(E_{LIN(+)}, E_{LIN(–)})$.

Assumed fields are within the response range of the device.

Temperature Compensation

To remove the effects of temperature on the performance of the ACS37600, an internal temperature sensor is integrated. This sensor, along with compensation algorithms, helps to standardize device performance over the full range of operating temperatures.

TEMPERATURE COMPENSATION UPDATE RATE (t_{UR})

After power-on delay (t_{PO}) elapses, the temperature compensation update rate, t_{UR}, is required to maintain a valid temperature-compensated output.

SENSITIVITY TEMPERATURE COEFFICIENT ($SENS_{SLOPE}$)

The Sensitivity Temperature Coefficient, $SENS_{SLOPE}$, is a parameter that allows the user to increase or decrease the sensitivity linearly over temperature. This allows for temperature compensation of other elements in the application system.

SENSITIVITY TEMPERATURE COEFFICIENT STEP SIZE ($STEP_{SENS\_SLOPE}$)

Sensitivity Temperature Coefficient Step Size, $STEP_{SENS\_SLOPE}$, is defined as the average change in % Sens/°C per LSB change in the gain_tc register.

Package Stress Compensation

Sensitivity drift due to package hysteresis is internally compensated to reduce the effects of temperature and lifetime drift error. Package stress and relaxation can cause the device sensitivity at T_A = 25°C to change during and after temperature cycling and over life stress.

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RESPONSE CHARACTERISTICS DEFINITIONS AND TYPICAL PERFORMANCE DATA

Response Time (t_{RESP})

The time interval between a) when the sensed input current reaches 90% of its final value, and b) when the sensor output reaches 90% of its full-scale value.

Propagation Delay (t_{PD})

The time interval between a) when the sensed input current reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value.

Rise Time (t_R)

The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

Output Slew Rate (SR)

The rate of change [V/µs] in the output voltage from a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

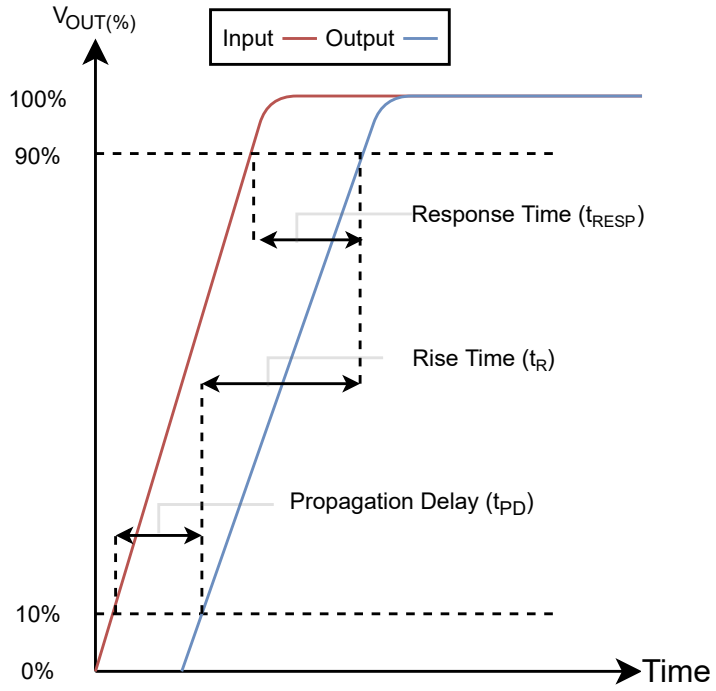

Figure 10: Dynamic Response Parameters

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APPLICATION AND THEORY

Parameter Trim Algorithm

For best results, a trim flow of sensitivity, V_{REF}, then V_{OE}/V_{QVO} is recommended, because sensitivity and V_{REF} affect V_{OE}/V_{QVO}.

SENSITIVITY (SENS):

1. Determine the actual sensitivity and target sensitivity. To calculate Sens:
   $Sens = Sens_{TARGET} - Sens_{ACTUAL}$
2. Divide the calculated Sens by $STEP_{SENS}$ to determine the number of codes to change the SNS_FINE register.
   A. If more accuracy is required or desired, the actual $STEP_{Sens}$ of the device must be measured. This measurement should be performed if an iterative process is used. Number of Sens codes = round(Sens/$STEP_{SENS}$)
3. Read the SNS_FINE register and add the number of Sens codes to the register value. Write the result in SNS_FINE.
4. Measure the new sensitivity. If it is not within $0.5 \times STEP_{SENS}$ or within the desired error, repeat steps 1 through 4; for best accuracy, be sure to measure $STEP_{Sens}$.

REFERENCE VOLTAGE OUTPUT (VREF):

5. Determine the actual V_{REF} and target V_{REF}. Calculate V_{REF} as: $V_{REF} = V_{REF\_TARGET} - V_{REF\_ACTUAL}$
6. Divide the calculated V_{REF} by $STEP_{VREF}$ to determine the number of codes to change for the VREF_FINE register.
   A. If more accuracy is required or desired, the actual $STEP_{VREF}$ of the device must be measured. This measurement should be performed if an iterative process is used. Number of VREF codes = round(V_{REF} / $STEP_{VREF}$)
7. Read the vref_fine register and add the number of V_{REF} codes to the register value. Write the result in VREF_FINE.
8. Measure the new V_{REF}. If it is not within $0.5 \times STEP_{VREF}$ or within the desired error, repeat steps 5 through 8; for best accuracy, be sure to measure $STEP_{VREF}$.

QUIESCENT VOLTAGE OUTPUT (V_{QVO}):

9. Knowing the actual V_{OE} and target V_{OE}, calculate V_{OE_STEP} as:
   $V_{OE} = V_{OE\_TARGET} - V_{OE\_ACTUAL}$.
10. Divide the calculated V_{OE} by $STEP_{VOE}$ to determine the number of codes to change for the voff_fine register.
    A. If more accuracy is required or desired, the actual $STEP_{VOE}$ of the device must be measured. This measurement should be performed if an iterative process is used. Number of V_{OE} codes = round (V_{OE} / $STEP_{VOE}$)
11. Read the VOFF_FINE register and add the number of V_{OE} codes to the REGISTER value. Write the result in VOFF_FINE.
12. Measure the new V_{OE}. If it is not within $0.5 \times STEP_{VOE}$ or within desired error, repeat steps 9 through 12; for best accuracy, be sure to measure $STEP_{VREF}$.

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Overdriving V_{REF} Introduction

The VREF pin can be overdriven while in the factory VREF_IO_MODE. This can be used to dynamically change the effective range of field to which the output is mapped, as well as overdriving the VREF pin during startup POR to reduce the t_{PO} time. To increase V_{REF} voltage, the pin must be supplied with a source that can maintain the desired higher voltage level while being capable of supplying a current greater than I_{SC_VREF}. To decrease the voltage, the pin must be supplied with a sink that can maintain the desired lower voltage while being able to sink $-I_{SC\_VREF}$.

DYNAMIC OUTPUT

Range changing can be performed by adjusting the VREF pin by overdriving the pin voltage. V_{REF} can be overdriven in the opposite direction down 2 V from 2.5 V to 0.5 V. This effectively allows for a dynamic output operation range, allowing for better accuracy during low current needs while maintaining the ability to capture signals that would otherwise be out of range of the device for the accuracy requirement.

ACCELERATED t_{PO}

When the ACS37600 powers up, the power-on time can be limited by the low internal drive strength of the VREF pin. One way to reduce this is by overdriving the VREF pin during POR to remove the VREF limited drive strength from slowing t_{PO}. This allows t_{PO} to depend on t_{POR_OUT} instead of t_{POR_REF}, which is twice as slow.

Manchester Communication and Device Features

USING THE ANALOG_LOCK BIT

The ANALOG_LOCK configuration is located in register 0x0F, bit 24, and controls whether an OVD event is required for read/write communications after the initial unlock. With this bit set to the factory default of 0, OVD is not required to send a read or write command. With this bit set to 1, OVD is required for every read/write. This bit does not change the unlock procedure, but only communication after unlock.

USING THE UNLOCK_CODE BIT

The UNLOCK_CODE register is located in register 0x0F, bit 25, and sets the requirement for and additional unlock code to unlock and communicate with the device. With this bit set to the factory default of 0, only one unlock code is required to unlock the part. With this bit set to 1, two codes must be used in succession in order to successfully unlock the part for communication. This bit does not affect communication after unlock.

HOW OVD CAN BE USED WITH PROGRAMMING

Using OVD during read/write removes the need for the MCU to overdrive the VREF pin for successful communication. Using the OVD flag to make VREF high Z during communication can be used with ANALOG_LOCK = 1 or 0, but only when OVD_DIS = 0, which is the factory default.

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DEFINING PROGRAMMING PARAMETERS

Fine Tuning Sensitivity, Reference Voltage Output, and Quiescent Voltage Output

Sensitivity and V_{OE} can be adjusted by programming the SNS_FINE and VOFF_FINE bits, as illustrated in Figure 11. Users should not program sensitivity or V_{QVO} beyond the maximum or minimum programming ranges specified in the Operating Characteristics table. Exceeding the specified limits will cause sensitivity and V_{QVO} to drift through the temperature range (V_{REF_E}, V_{OE}, and E_{SENS}) to deteriorate beyond the specified values.

Programming sensitivity might cause a small change in V_{QVO}/V_{OE}; as a result, Allegro recommends programming sensitivity first, then programming V_{QVO}/V_{OE}.

FINE SENSITIVITY (SNS_FINE)

Device sensitivity can be programmed by adjusting the SNS_FINE register. This register is a 2's complement number, meaning that the sensitivity can be programmed up or down from its nominal value at SNS_FINE = 0. As part of final testing, the SNS_FINE register is set by Allegro in the trimming process, so devices may already contain a nonzero SNS_FINE value. Programing too close (<32 LSB) to the $STEP_{SENS}$ minimum and maximum values affects temperature performance. It is recommended that the user keep the codes from 0 to 223 and 288 to 511.

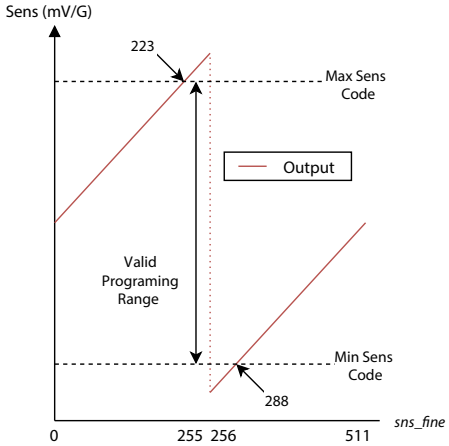

Figure 11: Sensitivity Register/DAC Transfer Curve

FINE REFERENCE VOLTAGE (VREF_FINE)

The reference voltage, V_{REF}, can be set two different ways. The value can be programmed internally, in which case the VREF_FINE and VREF_COARSE (refer to the Coarse Reference Voltage (VREF_COARSE) section) settings determine which voltage the device outputs on the VREF pin. The second method of setting the reference voltage is by externally overdriving the VREF pin to the desired voltage. In this case, the internal settings do not matter, because the reference is the physical voltage on the pin, not related to the internal settings. Programming too close (<32 LSB) to the $STEP_{SENS}$ minimum and maximum values affects temperature performance. It is recommended that the user keep the codes from 0 to 223 and 288 to 511.

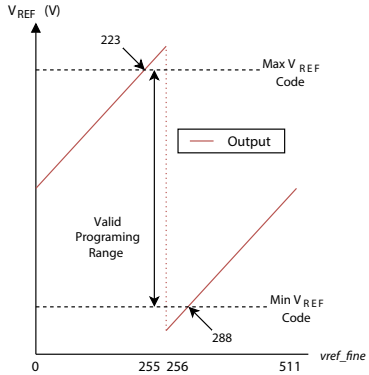

Figure 12: V_{REF} Register/DAC Transfer Curve

QUIESCENT VOLTAGE OFFSET (V_{QVO})

The quiescent voltage output, V_{QVO}, is defined as the output voltage when zero gauss is present on the device sensing element. In application, this is determined by the reference voltage (V_{REF}) and any offset voltage from the reference (V_{OE}). To eliminate this offset, VOFF_FINE can be adjusted to remove any error. This 2's complement number allows V_{QVO} to be moved up and down without affecting V_{REF} to remove V_{OE}. At final test, this value is set to trim for the chosen V_{REF} and may need to be adjusted if V_{REF} is changed or overdriven. Programming too close (<32 LSB) to the $STEP_{SENS}$ minimum and maximum values affects temperature performance. It is recommended that the user keep the codes from 0 to 223 and 288 to 511.

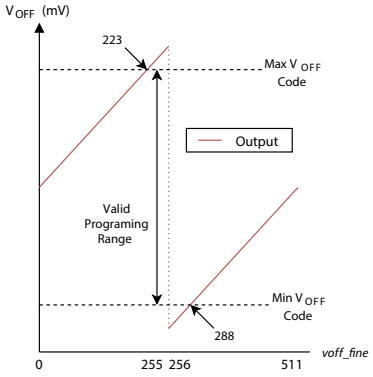

Figure 13: V_{OFF} Register/DAC Transfer Curve

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VREF INPUT/OUTPUT OPERATIONAL MODES (IO_REF_MODE)

The VREF pin has two different operational modes. The VREF pin factory default is input/output mode; this means that the output is internally driving but is configured to be overdriven. If it is desired to change this to either a dedicated input or dedicated output, the value of IO_REF_MODE can be change to the corresponding value below.

IO_REF_MODE (code)	Mode
0	Input only
1	Input only
2	Output only
3 (factory default)	Input/Output

ECONOMY MODE (VOUT_ECO_MODE)

This device has an aggressive drive strength at the cost of current consumption during normal operation. If this is not desired, the VOUT_ECO_MODE register can be set to 1. This reduces the drive strength and quiescent current, thereby reducing the overall current consumption.

VOUT_ECO_MODE (code)	Name	Max. Output Drive
0 (factor default)	Turbo	15 mA
1	Economy	7.5 mA

Additional Core / Temperature Compensation

SENSITIVITY TEMPERATURE COMPENSATION SLOPE (GAIN_TC)

This device has a user-programmable temperature sensitivity slope DAC, GAIN_TC. This 6-bit, 2's-complementary DAC linearly alters device sensitivity over temperature, allowing the user to compensate for other systemic temperature drifts like a magnetic core. The GAIN_TC register linearly changes the existing sensitivity slope over temperature centered at 25°C, as illustrated in Figure 14. To calculate the code needed to obtain the desired sensitivity slope, determine the GAIN_TC, which is the percentage of change from room sensitivity at temperature T, and follows the equation below.

$$GAIN\_TC = SENS_{SLOPE\_T} / [(T - 25) \times 2.5 \times 10^{-5}]$$

NOTE: When calculating E_{SENS}, use the expected $Sens_T$ (sensitivity value at temperature T) that can be calculated with the equations for $Sens_T$ below. The hot and cold ranges are not symmetric and the GAIN_TC for hot and cold will not match at the extreme temperatures.

$$Sens_T = Sens_{(25°C)} \times [1 + SENS_{SLOPE\_T}]$$

$$SENS_{SLOPE\_T} = (T - 25) \times gain\_tc \times 2.6 \times 10^{-5}$$

Registers Useful for Prototyping

The registers that are contained in this section are useful for prototyping and room temperature applications. Changing the values of these registers from the factory default may affect the over temperature performance.

COARSE SENSITIVITY (SNS_COARSE)

Each ACS37600 is programmed to a different coarse sensitivity setting per the Selection Guide. Devices are tested and temperature compensated for the specific coarse sensitivity setting. If the coarse sensitivity is changed, by programming the SNS_COARSE bits, Allegro cannot guarantee the specified sensitivity drift through temperature and lifetime limits.

COARSE REFERENCE VOLTAGE (VREF_COARSE)

This device has a coarse reference DAC that changes the centered voltage for the VREF_FINE DAC. To program VREF_COARSE, refer to the following table. If this register is not in the factory default setting, Allegro cannot guarantee the over temperature performance of the device.

VREF_COARSE (code)	Approx. Center Voltage (V)
0	0.5
1	1.5
2	1.65
3	2.5

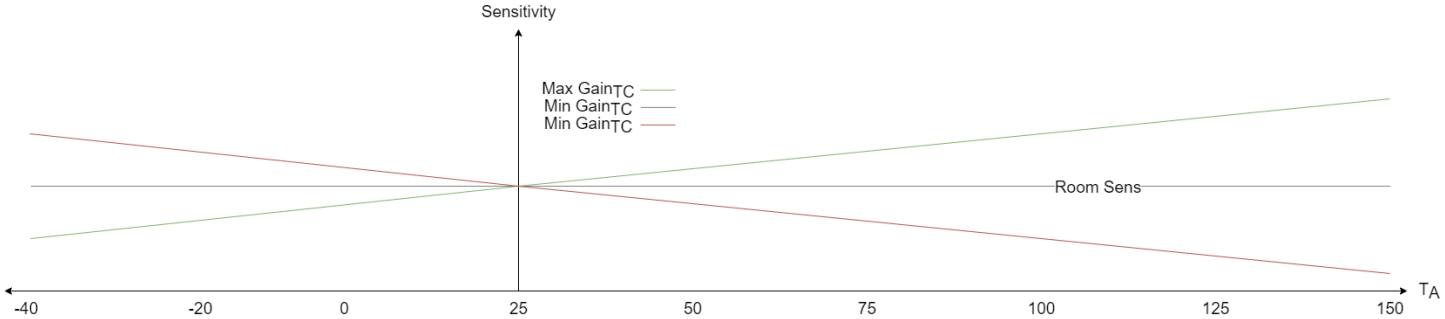

Figure 14: GAIN_TC and Sensitivity Over Temperature Performance

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OUTPUT POLARITY (GC_POL)

It is possible to change the direction of the output direction for a given field by changing the GC_POL register. The factory default setting is GC_POL = 0. If the GC_POL is changed from the factory default, Allegro cannot guarantee the over temperature performance of the device.

MEMORY LOCKING MECHANISMS

The ACS37600 is equipped with multiple memory-locking mechanisms. The purpose of these mechanisms is to allow the user to reduce the likelihood of unintended communication and programming in the future.

NOTE: Due to the nature of locking a part, some of these settings may limit the ability of the user to debug issues in the future, and in some cases, may even limit the ability of Allegro to provide assistance in these cases. Make sure that, when locking a part, the settings chosen are desired, and functionality of the part is fully understood.

CHOPPER STABILIZING TECHNIQUE

When using Hall-effect technology, a limiting factor for total accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip.

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DEVICE PROGRAMMING

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, to the device using a point-to-point command/acknowledge protocol. The device does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledging from the device. If the command is a read, the device responds by transmitting the requested data.

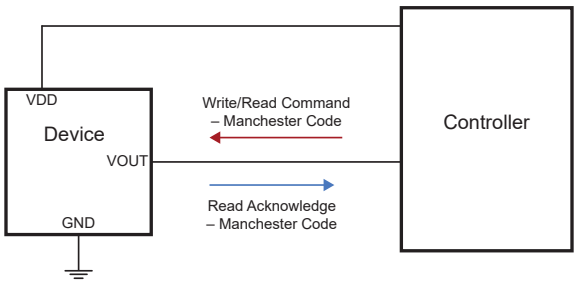

Figure 15: Programming Connections

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the device: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the device in response to a Read command.

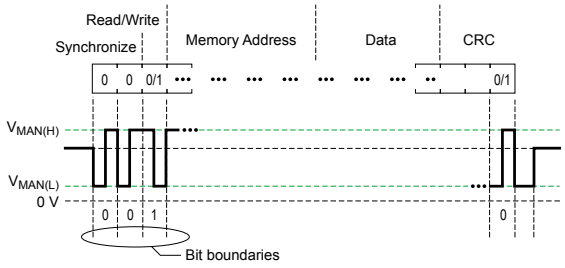

Figure 16: General Format for Serial Interface Communication

READ (CONTROLLER TO DEVICE)

The fields for the Read command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 1 for read)
- CRC (3 bits)

The sequence for a Read command is shown in Figure 17.

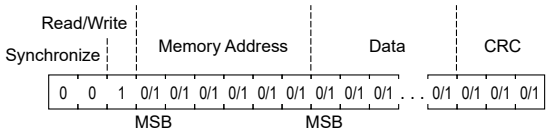

Figure 17: Read Sequence

READ ACKNOWLEDGE (DEVICE TO CONTROLLER)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (32 bits):
  - [31:28] Don't Care
  - [27:26] ECC Pass/Fail
  - [25:0] Data

The Read Acknowledge sequence is shown in Figure 18. For instructions about how to detect Read/Write Synchronize Memory Address Data (32 bits) and ECC failure, refer to the Detecting ECC Error section.

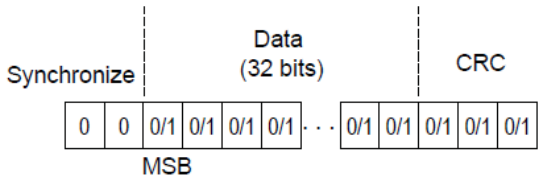

Figure 18: Read Acknowledge Sequence

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WRITE (CONTROLLER TO DEVICE)

The fields for the Write command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits):
  - □ [31:26] Don't Care
  - □ [25:0] Data
- CRC (3 bits)

The sequence for a Write command is shown in Figure 19. Bits [31:26] are Don't Care because the device automatically generates 6 ECC bits based on the content of bits [25:0]. These ECC bits will be stored in EEPROM at locations [31:26].

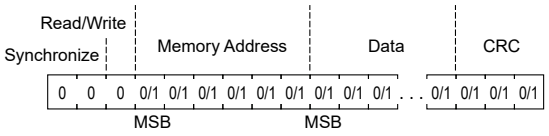

Figure 19: Write Sequence

WRITE ACCESS CODE (CONTROLLER TO DEVICE)

The fields for the Access Code command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits)
- CRC (3 bits)

The sequence for an Access Code command is shown in Figure 20.

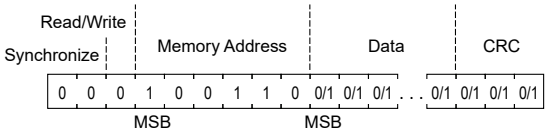

Figure 20: Write Access Code

The controller must open the serial communication with the device by sending an Access Code. It must be sent within Access Code Timeout, t_{ACC}, from power-up, or the device will be disabled for read and write access.

Name	Serial Interface Format	
Register Address	**Data (Hex)**	**(Hex)**
User Access	0x26	0x2C413736
Unlock Code	0x26	0xAFCF6C27

EEPROM ERROR CHECKING AND CORRECTION (ECC)

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up.

The device always returns 32 bits.

The message received from the controller is analyzed by the device EEPROM driver and ECC bits are added. The first six received bits from device to controller are dedicated to ECC.

DETECTING ECC ERROR

If an uncorrectable error has occurred, bits 27:26 are set to 10, the VOUT pin enters a high Z state, and the device does not respond to the applied magnetic field.

Bits	Name	Description
31:28	–	No meaning
27:26	ECC	00 = No error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	D[25:0]	EEPROM data

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
V_{DD} Programming Enable Voltage	V_{PROG}	V_{DD} pulse required when initializing first communication	8	–	–	V
Program Time Delay	t_d		–	74	–	µs
Program Write Delay	t_w		–	20	–	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VREF	4	5	V_{DD}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VREF	0	–	1	V
Bit Rate	t_{BITR}	Communication rate	1	30	100	kbps
Bit Time	t_{BIT}	Data bit pulse width at 30 kbps	–	(33)	–	µs
Access Code Timeout	t_{ACC}		–	10	–	ms

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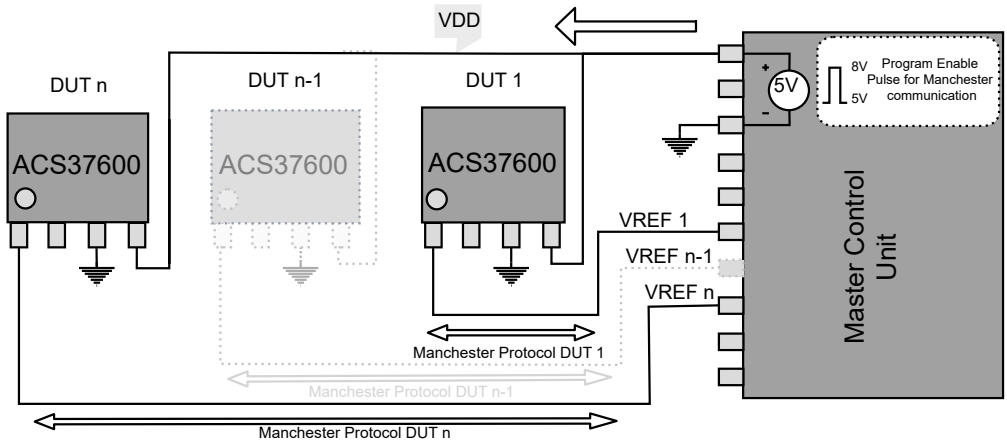
Multi-Device Communication Setup



Multi-Device Communication Setup

In this configuration, individual communication can be established with a total of n devices by asserting the program enable pulse on the shared V_{DD} line, then sending/receiving the Manchester protocol along individual VREF lines. However, when a program enable pulse is sent in this configuration, all of the devices enter a listen state, and VREF enters a high Z state. If communication with a specific device is desired without disruption to other device outputs, a dedicated V_{DD} is required for each independent device.

Error Checking

CYCLICAL REDUNDANCY CHECK (CRC)

The serial interface uses a 3-bit CRC with polynomial $g(x) = x^3 + x + 1$. The CRC is initialized at '111'. Synchronization bits are ignored during calculation of CRC. If the serial interface receives a command with a CRC error, the error is ignored, and it is up to the host controller to resend the command.

EEPROM ERROR CHECKING AND CORRECTION (ECC)

The EEPROM space includes check bits for the purpose of error checking and correction (ECC); these bits are called Hamming codes. ECC can be enabled or disabled via the ECC_DISABLE register. This register has the following effects:

- ECC_DISABLE = 0 (ECC enabled)
- ECC_DISABLE = 1 (ECC disabled)

ECC_DISABLE = 0 (ECC enabled)

Read: 26 bits are returned [25:0]

A single bit read error will be corrected and the ECC_SINGLE register will be set to 1.

A double bit read error will cause the data in EEPROM to remain unchanged and the dual bit error to be set to 1, and will force the output to its diagnostic state (high Z).

Write: 26 bits are accepted.

Hamming check bits are handled internally and written with each write to the EEPROM.

ECC_DISABLE = 1 (ECC disabled)

Read: 32 bits are returned [31:0]

Data is passed through unchecked. Check bits are passed to the serial interface, so checks can be made by the host controller.

Write: 32 bits are accepted.

Check bits can be written by the serial interface.

In the event of a single or dual bit error, the respective flag is set in register. These flags are read-only, and they reset after a read command to the register.

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Customer Memory Map

Address	Register Name	Parameter Name	Location	Description	R/W	Bits	Factory Default		
							Decimal	Binary	Effect
0x05	EEPROM_5	VREF_COARSE	0:1	Coarse setting for V_{REF}	R/W [1]	2	3	11	V_{REF} = 2.35 to 2.65 V
		SENS_COARSE	2:3	Coarse for sensitivity.	R/W [1]	2	DS	DS	Sets sens range
		BW_SEL	4:5	Internal bandwidth selection	R/W	2	2	10	400 kHz
		IO_REF_MODE	6:7	VREF input/output mode selection	R/W	2	0	00	Input/Output
		VOUT_ECO_MODE	8	Reduces operational I_{CC} and I_{OD}	R/W	1	0	0	Turbo
		OVD_DIS	9	Disables OVD flag	R/W	1	0	0	OVD enabled
		UVD_DIS	10	Disables UVD flag	R/W		0	0	UVD enabled
		SPARE_USER	11:14	No internal function. Customer scratch.	R/W	4	0	0000	N/A
		VOFF_FINE	15:23	Adjusts V_{QVO} offset from V_{REF}	R/W	9	N/A	N/A	Sets offset error
		ECC	26:31		R	6	N/A	N/A	
0x06	EEPROM_6	GC_POL	18	Changes in direction output will respond with field	R/W [1]	1	0	0	Positive field perpendicular to top face of package will cause positive increase in output
		ECC	26:31		R	6	N/A	N/A	
0x0F	EEPROM_F	VREF_FINE	0:8	Adjusts the V_{REF} output voltage within VREF_COARSE dependent range	R/W	9	DS	DS	2.5 V
		SENS_FINE	9:17	Adjusts sensitivity of the device within SENS_COARSE dependent range	R/W	9	DS	DS	Selection specific sensitivity
		GAIN_TC	18:23	Adjusts change in sensitivity over temperature up or down	R/W	6	0	000000	Flat over temperature
		ANALOG_LOCK	24		R/W	1	0	0	
		UNLOCK_CODE	25		R/W	1	0	0	
		ECC	26:31		R	6	N/A	N/A	

[1] Temperature performance is guaranteed while GC_POL, SENS_COARSE, and VREF_COARSE are in the factory default state.

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PACKAGE OUTLINE DRAWING

For Reference Only - Not for Tooling Use

(Reference DWG-0000395)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

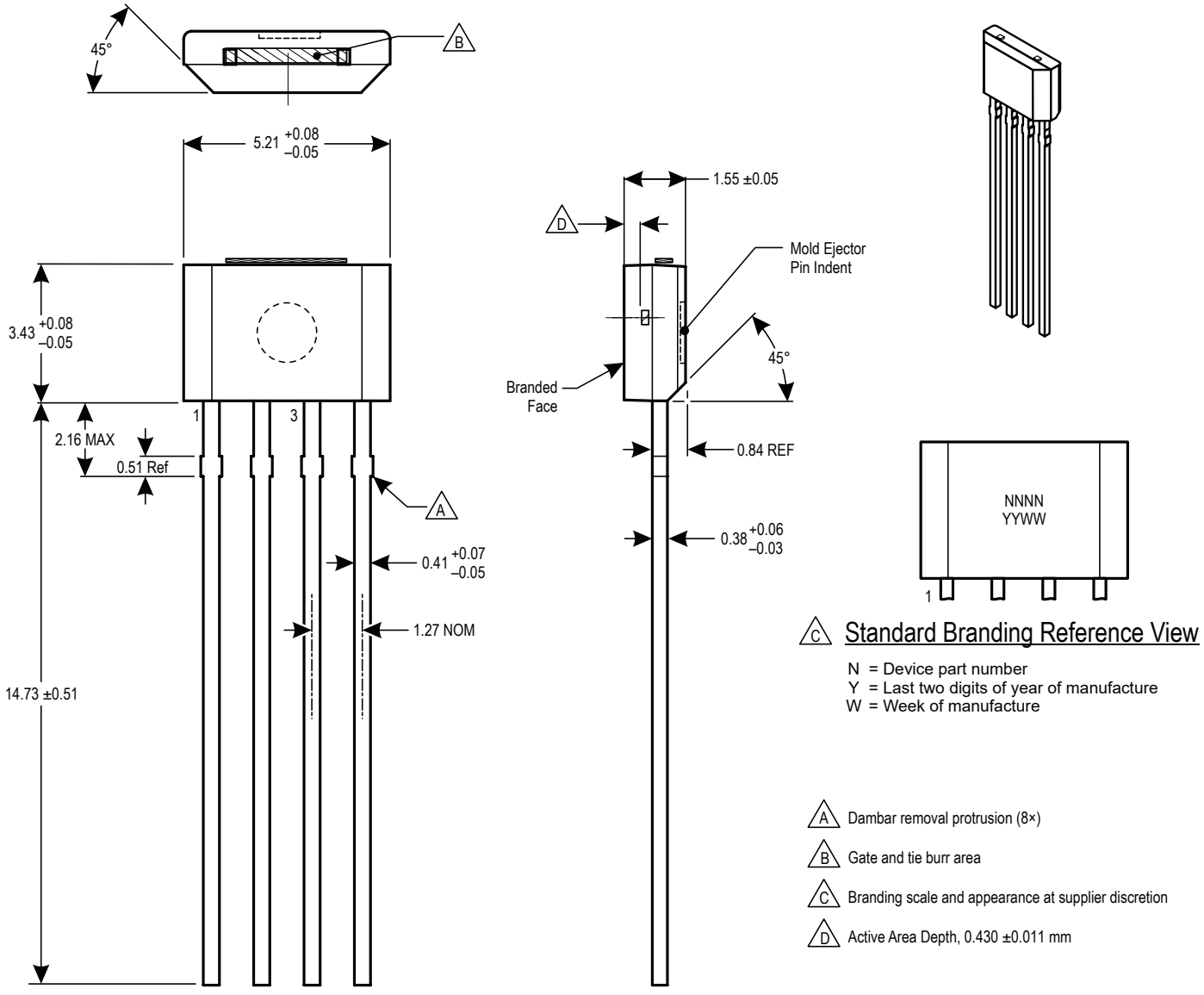

Figure 21: Package OK, 4-Pin SIP, TN Leadform

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Revision History

Number	Date	Description
–	March 22, 2023	Initial release
1	November 1, 2023	Added reversed polarity part variants, removed ACS37600KOKA-013B5-C variant, and removed all reference to SENS_COARSE code 0 and code 3 (all pages); capitalized all registers to meet current register notation standard.

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