A31316

3D Magnetic Position Sensor IC

FEATURES AND BENEFITS

- 3D magnetic sensor enables flexible mechanical integration for contactless linear and rotary position applications
- Configurable signal path processing and on-chip angle calculation for accurate 360° and short-stroke (<360°) rotary applications
- Multiple programmable linearization options for maximum measurement accuracy:
  - □ Piecewise-linear and binning modes
  - □ Up to 33-point fixed position
  - □ Up to 22-point programmable positions
- PWM and SENT (SAE J2716) output formats
- Integrated IC diagnostics for high reliability
- Developed in accordance with ISO 26262 requirements for hardware product development for use in safety-critical applications targeting ASIL B compatibility
- Broken-wire detection
- 5 V operation with undervoltage detection (UVD)
- Built-in self-test (BIST) diagnostic capability
- Wide operating temperature range: –40°C to 150°C
- In-package passives remove the need for external support circuitry.

PACKAGE

Figure 1: 3-Pin SIP (Suffix UC)

Not to scale

DESCRIPTION

The A31316 is a robust 3D Hall-effect magnetic position sensor designed for on-axis and off-axis rotary as well as linear-stroke position measurement in automotive, industrial, and consumer applications.

This sensor integrates vertical and planar Hall-effect elements with precision temperature-compensation circuitry to detect two out of three magnetic field components (X, Y, and Z). Configurable signal processing, linearization, and angle calculation allows the A31316 to accurately resolve the absolute rotary (full 360° and short stroke <360°) or linear position of a moving magnetic target.

The A31316 features PWM or SENT (SAE J2716) interface options to output the angle between the two factory-selected axes or the field of a single axis. In addition, the SENT interface provides the option to output the field measurement from both channels.

On-chip EEPROM technology, capable of supporting up to 100 write cycles, is integrated for flexible programming of configuration and calibration parameters and includes bits provided for customer device identification purposes.

The A31316 contains on-chip diagnostic features required for high-reliability automotive applications, including monitors of both internal and external fault conditions.

Developed in accordance with ISO 26262 as a hardware safety element out of context (SEooC) with ASIL B capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

SELECTION GUIDE

Part Number	Temperature Trim Range	Optimized Field Range	Channel A	Channel B	Packing
A31316LUCHTN-XZ-S-SE-10	–40°C to 150°C	300 to 1000 gauss	X	Z	4,000 pieces per 13-in reel
A31316LUCHTN-XY-S-SE-10	–40°C to 150°C	300 to 1000 gauss	X	Y	4,000 pieces per 13-in reel
A31316LUCHTN-YZ-S-SE-10	–40°C to 150°C	300 to 1000 gauss	Z	Y	4,000 pieces per 13-in reel

PART NUMBER GUIDE

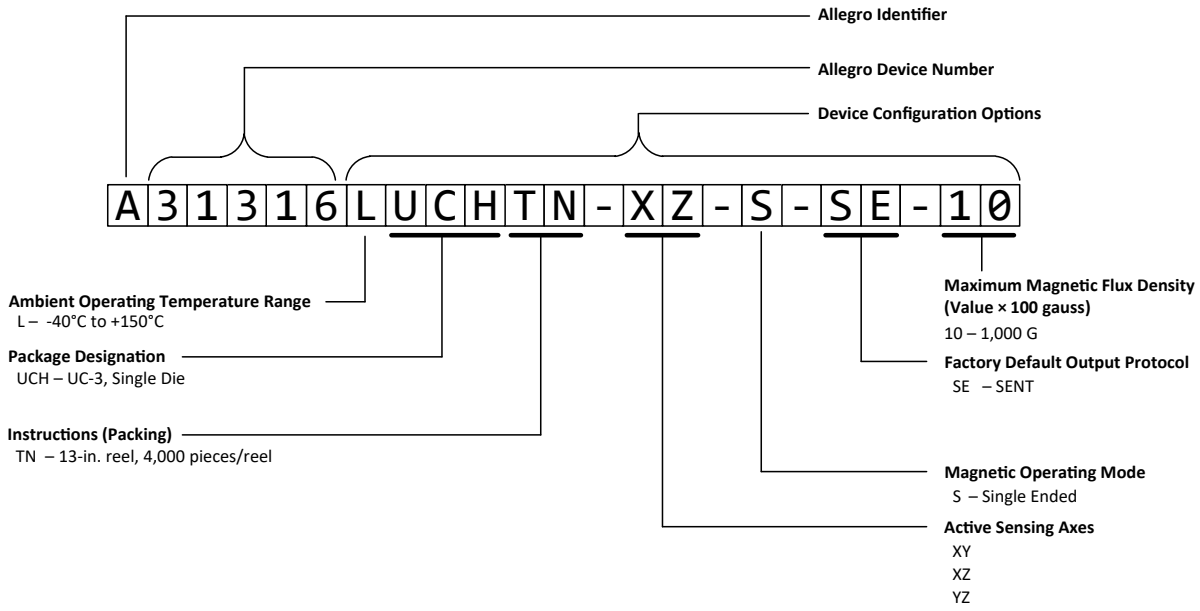

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Table of Contents

Features and Benefits ... 1
Description ... 1
Packages ... 1
Selection Guide ... 2
Absolute Maximum Ratings ... 4
Thermal Characteristics ... 4
Functional Block Diagram ... 5
Pinout Diagram Terminal and Capacitor Lists ... 6
Axis Definitions ... 6
Application Circuit ... 6
Operating Characteristics ... 7
Performance Characteristics ... 8
Interface Characteristics ... 10
Functional Description ... 13
- Typical Application Information ... 13
- Temperature Output ... 13
- Signal Path ... 15
- 1-D Signal Path ... 15
  - Factory Channel A / Channel B Input Selection ... 15
  - Factory Range Selection ... 15
  - Factory Trimming ... 15
  - Customer Controllable Data Path ... 15
- Customer Trimming ... 15
  - Low-Pass filter ... 15
  - Sensor Output During Low-Pass Filter Initialization ... 16
  - Factory Correction ... 16
  - Orthogonality Correction ... 16
  - Polarity, Offset, Sensitivity, and Temperature Calibration ... 16
  - Polarity Correction ... 17
  - Sensitivity Adjustment ... 17
  - Sensitivity Correction Over Temperature ... 17
  - Customer Offset Correction ... 17
  - Customer Offset Correction Over Temperature ... 17
  - Hysteresis Filter ... 18
  - Direct Output Register ... 18
  - ATAN Input Selection ... 18
  - Pre-gain Angle Offset Correction ... 19
  - Angle Gain Correction ... 19
  - Post Gain Angle Offset Correction ... 20
  - Angle Sign (Rotation Direction) ... 21
  - Linearization and Binning ... 21
  - Linearization / Binning Mode Selection ... 21
  - Fixed Segment Linearization (Lin_mode 0) ... 22
  - Fixed Segment Binning (lin_mode 1) ... 22
  - Variable Segment Linearization (lin_mode 2) ... 23
  - Variable Segment Binning (lin_mode 3) ... 23
  - Linearization/Binning Parameter Storage ... 23
  - Number of Linearization / Binning Points ... 25
  - Binning Mode Hysteresis ... 25
- Output Clamps ... 25
- Output Protocols ... 26
  - PWM Output Mode ... 26
  - PWM Sampling Time ... 26
  - SENT Output Mode ... 27
  - Message Structure ... 27
  - SENT Sampling Time ... 28
  - SENT Output Rate ... 28
  - Optional SENT Slow Serial Output Protocol ... 29
  - Data Nibble Format ... 30
  - SENT CRC ... 31
  - SENT Serial Message 6-Bit CRC ... 31
  - SENT Message Frame Definitions ... 33
  - Error Indicators / Specific Messages / Initialization Message in SENT Output Codes ... 34
  - SAE J2716 SENT ... 34
  - SENT Initialization Code Selection ... 34
  - Output Pin Drive Strength Options ... 35
    - Output Pin Fall Time Selection ... 35
    - Push-Pull Output Setting for SENT and PWM Rising Edge ... 36
- Programming Protocol ... 37
  - Physical Layer ... 37
  - Settings Controlling the Manchester Communication ... 37
    - Serial Interface Message Structure ... 38
    - Manchester Unlocking – SENT/PWM Mode via OVD ... 39
    - Manchester Unlocking – SENT/PWM Mode via Triggering Pulses ... 39
  - Manchester Communication CRC ... 39
  - EEPROM Lock ... 39
  - Analog Check Failure (ACF) ... 40
  - Angle Outside Clamp (AOC) ... 40
  - EEPROM Margin Checking ... 40
  - Error Flag Registers ... 40
  - Temperature Error (TSE) ... 40
  - Saturation Flag (SAT) ... 40
  - Oscillator Frequency Error (OFE) ... 41
  - Signal Processing Logic Failure (SLF) ... 41
  - Signal Radius Out of Range (SSR) ... 41
  - Power-On Reset (POR) ... 42
  - EEPROM Multiple Bit Error (EUE) and EEPROM Single Bit Error (ESE) ... 42
  - Shadow Parity Error (SPE) ... 42
  - Undervoltage Detection (UVD) ... 42
  - Overvoltage Detection (OVD) ... 43
  - SENT Output Error Reporting ... 43
  - PWM Output Error Reporting ... 43
  - Broken Wire Detection ... 44
  - Logic Built-In Self-Test (LBIST) ... 44
- Diagnostic Setting and Clearing ... 46
- Memory Access ... 46
  - Shadow Memory Read and Write Transactions ... 46
- Package Outline Drawing ... 60

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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	$V_{CC(absmax)}$	Supply is clamped with 20 V limit to GND	18	V
Reverse Supply Voltage	$V_{RCC(absmax)}$	Supply is clamped with –20 V limit to GND	–18	V
Forward V_{OUT}-V_{CC} Voltage	$V_{OUT-CC(absmax)}$	V_{OUT} is clamped with 20 V limit to V_{CC}; Note: There is no reverse V_{OUT}-V_{CC} clamp	18	V
Forward Output Voltage	$V_{OUT(absmax)}$	Output is clamped with 20 V limit to GND	18	V
Reverse Output Voltage	$V_{ROUT(absmax)}$	Output is clamped with –10 V limit to GND	–6	V
Forward Supply Current	I_{CC}		40	mA
Reverse Supply Current	I_{RCC}		–30	mA
Output Current Limit	$I_{OUT(SOURCE)}$	VOUT shorted to GND	30	mA
	$I_{OUT(SINK)}$	VCC shorted to VOUT	–30	mA
Extended Operating Ambient Temperature	$T_{A(EXT)}$	Device functions within this temperature range, but performance is not specified	–45 to 165	°C
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\Theta JA}$		270	°C/W

[1] Additional thermal information is available on the Allegro website.

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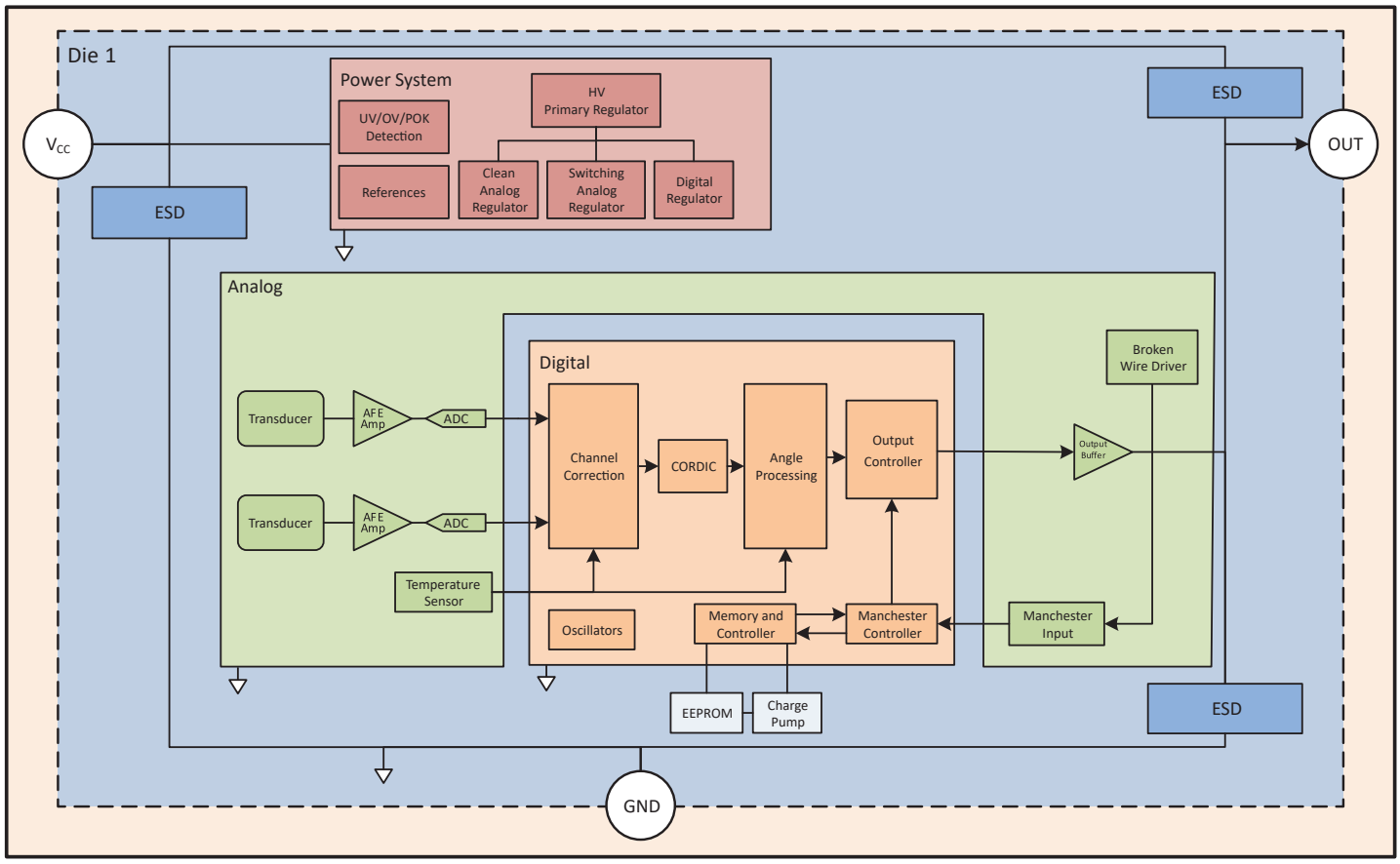

Figure 2: Functional Block Diagram

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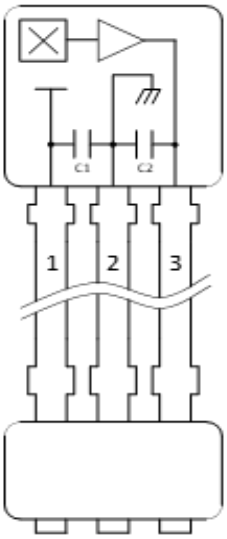
PINOUT DIAGRAM, TERMINAL, AND CAPACITOR LIST

Terminal List

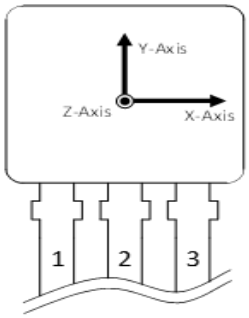
Pin	Name	Function
1	VCC	Supply voltage
2	GND	Ground
3	OUT	Device output

Capacitor List

Capacitor	Value
C1	100 nF
C2	4.7 nF



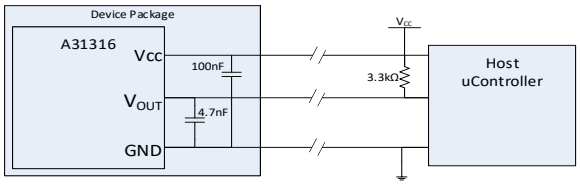
AXIS DEFINITIONS



NOTE: Arrows show the default polarity of each axis. Polarity can be changed with internal settings.

APPLICATION CIRCUIT

The A31316 contains all internal components required for use in default configurations (push-pull mode). It is still recommended to provide a pull-up resistor in the event of a line break or an error condition that causes the devices to enter a high-impedance (high-Z) state, so that there is a known output voltage.



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OPERATING CHARACTERISTICS: Valid at T_A = –40°C to 150°C, V_{CC} = 4.5 to 5.5 V, unless otherwise noted.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL REQUIREMENTS						
Supply Voltage	V_{CC}		4.5	5	6	V
Supply Buffer Capacitor	C_{SUP}	External capacitance in addition	0	–	500	nF
Supply Current	I_{CC}		5	8.5	10	mA
DEVICE REQUIREMENTS						
Ambient Operating Temperature	T_A		–40	–	150	°C
Number of EEPROM Writes [1]	N_{EEPROM}	T_A = 25°C	–	–	100	writes
MAGNETIC REQUIREMENTS [2]						
Magnetic Flux Density	$\|B_{IN}\|$	For xxx-10 parts, devices tested at $\|B_{IN}\|$ = 300 G; operation below this value is characterized, but not specified	–	±300	±1000	G

[1] EEPROM writes are not supported at temperatures above 85°C.
[2] Magnetic flux density values are based on target device sensitivity. Values here do not account for temperature or lifetime drift. To avoid saturation in application, Allegro recommends a 10% margin below the maximum field.

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PERFORMANCE CHARACTERISTICS: Valid for all electrical and device requirement ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
DEVICE SPECIFICATIONS							
Undervoltage Detection Threshold	$V_{UVD\ (LOW,\ FALL)}$	V_{CC} falling, UVD_SEL = 0		3.6	–	4.1	V
	$V_{UVD\ (LOW,\ RISE)}$	V_{CC} rising, UVD_SEL = 0		3.7	–	4.2	V
	$V_{UVD\ (HIGH,\ FALL)}$	V_{CC} falling, UVD_SEL = 1		4.1	–	4.4	V
	$V_{UVD\ (HIGH,\ RISE)}$	V_{CC} rising, UVD_SEL = 1		4.2	–	4.5	V
Overvoltage Detection Threshold	$V_{OVD\ (LOW,\ FALL)}$	V_{CC} falling, OVD_SEL = 1		5.6	–	6	V
	$V_{OVD\ (LOW,\ RISE)}$	V_{CC} rising, OVD_SEL = 1		5.65	–	6.05	V
	$V_{OVD\ (HIGH,\ FALL)}$	V_{CC} falling, OVD_SEL = 0		8.4	–	10.2	V
	$V_{OVD\ (HIGH,\ RISE)}$	V_{CC} rising, OVD_SEL = 0		8.6	–	10.4	V
Power-On Reset Voltage	$V_{POR(FALL)}$	V_{CC} falling		2.6	–	2.9	V
	$V_{POR(RISE)}$	V_{CC} rising		2.8	–	3.1	V
Power-On Time	t_{PO}	Time from $V_{CC} > V_{CC(MIN)}$ until unfiltered output is settled		–	1	1.7	ms
Oscillator Frequency	f_{OSC}			7.36	8	8.64	MHz
Output Current Limit	I_{LIMIT}	Output FET on, T_A = 25°C		19	–	30	mA
ABSOLUTE ANGLE SPECIFICATIONS							
Angle Error (XY)	$ERR_{ANG(XY)}$	T_A = 25°C [1]		–1	–	1	degrees
		–40°C ≤ T_A ≤ 150°C		–1.2	–	1.2	degrees
Angle Error (XZ)	$ERR_{ANG(XZ)}$	T_A = 25°C [1]		–1	–	1	degrees
		–40°C ≤ T_A ≤ 150°C		–1.2	–	1.2	degrees
Angle Error (YZ)	$ERR_{ANG(YZ)}$	T_A = 25°C [1]		–1	–	1	degrees
		–40°C ≤ T_A ≤ 150°C		–1.2	–	1.2	degrees
Input-Referred Angle Noise [2]	$N_{ANG(IN)}$	$\|B_{IN}\|$ = ± 300 G input field	BW_SEL = 0, 329.1 Hz	–	0.0291	–	$degree_{RMS}$
			BW_SEL = 1, 465.8 Hz	–	0.0291	–	$degree_{RMS}$
			BW_SEL = 2, 556 Hz	–	0.0326	–	$degree_{RMS}$
			BW_SEL = 3, 700 Hz	–	0.0381	–	$degree_{RMS}$
			BW_SEL = 4, 1000 Hz	–	0.0468	–	$degree_{RMS}$
			BW_SEL = 5, 1482 Hz	–	0.0575	–	$degree_{RMS}$
			BW_SEL = 6, 2024 Hz	–	0.0673	–	$degree_{RMS}$
ANGLE DRIFT SPECIFICATIONS							
Angle Drift (XY)	$DRIFT_{Ang,Temp(XY)}$	Change in angle relative to T_A = 25°C		–1.2	–	1.2	degrees
	$DRIFT_{Ang,Life(XY)}$	Change in angle relative to pre-stress conditions [3]		–0.9	±0.16	0.9	degrees
Angle Drift (XZ)	$DRIFT_{Ang,Temp(XZ)}$	Change in angle relative to T_A = 25°C		–1.2	–	1.2	degrees
	$DRIFT_{Ang,Life(XZ)}$	Change in angle relative to pre-stress conditions [3]		–1.1	±0.65	1.1	degrees
Angle Drift (YZ)	$DRIFT_{Ang,Temp(YZ)}$	Change in angle relative to T_A = 25°C		–1.2	–	1.2	degrees
	$DRIFT_{Ang,Life(YZ)}$	Change in angle relative to pre-stress conditions [3]		–1	±0.69	1	degrees

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PERFORMANCE CHARACTERISTICS (continued): Valid for all electrical and device requirement ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ABSOLUTE CHANNEL SPECIFICATIONS						
Default Channel Sensitivity	$SENS_{Target}$	Selection Guide Part Number: XXX-10	–	32.125	–	LSB/G
Channel Sensitivity Error (X,Y)	$ERR_{Sens(X,Y)}$	T_A = 25°C [1]	–1.5	–	1.5	%
		–40°C ≤ T_A ≤ 150°C	–3	–	3	%
Channel Sensitivity Error (Z)	$ERR_{Sens(Z)}$	T_A = 25°C [1]	–1.5	–	1.5	%
		–40°C ≤ T_A ≤ 150°C	–4	–	4	%
Channel Offset Error (X,Y)	$ERR_{Off(X,Y)}$	T_A = 25°C [1]	–1.5	–	1.5	G
		–40°C ≤ T_A ≤ 150°C	–4	–	4	G
Channel Offset Error (Z)	$ERR_{Off(Z)}$	T_A = 25°C [1]	–1.5	–	1.5	G
		–40°C ≤ T_A ≤ 150°C	–2.5	–	2.5	G
Channel Linearity Error [2]	ERR_{LIN}	100 G ≤ B_{IN} ≤ 1000 G	–0.3	–	0.3	%
Input-Referred Channel Noise (X,Y) [2]	$N_{CHAN(X,Y)}$	T_A = 25°C [1]	–	5.245	–	mG (RMS/√Hz)
		–40°C ≤ T_A ≤ 150°C	–	7.821	–	mG (RMS/√Hz)
Input-Referred Channel Noise (Z) [2]	$N_{CHAN(Z)}$	T_A = 25°C [1]	–	2.083	–	mG (RMS/√Hz)
		–40°C ≤ T_A ≤ 150°C	–	3.104	–	mG (RMS/√Hz)
CHANNEL DRIFT SPECIFICATIONS						
Channel Sensitivity Error Drift (X,Y)	$DRIFT_{Sens,Temp(X,Y)}$	Change in sensitivity relative to T_A = 25°C [1]	–2	–	2	%
	$DRIFT_{Sens,Life(X,Y)}$	Change in sensitivity relative to pre-stress conditions [3]	–1.4	±0.31	1.4	%
Channel Sensitivity Error Drift (Z)	$DRIFT_{Sens,Temp(Z)}$	Change in sensitivity relative to T_A = 25°C [1]	–3	–	3	%
	$DRIFT_{Sens,Life(Z)}$	Change in sensitivity relative to pre-stress conditions [3]	–4.7	±2.3	4.7	%
Channel Offset Drift (X,Y)	$DRIFT_{Off,Temp(X,Y)}$	Change in offset relative to T_A = 25°C [1]	–3.5	–	3.5	G
	$DRIFT_{Off,Life(X,Y)}$	Change in sensitivity relative to pre-stress conditions [3]	–0.97	±0.33	0.97	G
Channel Offset Drift (Z)	$DRIFT_{Off,Temp(Z)}$	Change in offset relative to T_A = 25°C [1]	–1.5	–	1.5	G
	$DRIFT_{Off,Life(Z)}$	Change in sensitivity relative to pre-stress conditions[3]	–0.6	±0.15	0.6	G

[1] 25°C measurements taken after 48 to 72-hour wait at 40% to 55% relative humidity.
[2] Parameter not measured at final test. Determined by design and characterization.
[3] Min and max values based on worst-case drift observed during Q100 qualification.

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INTERFACE CHARACTERISTICS: Valid for all electrical and device requirement ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Broken-Wire Response Time	t_{BW}	Time after V_{CC} – GND = 0.2 V; either V_{CC} or GND wire broken	–	–	500	µs
Diagnostic Voltage Ranges	$V_{SATDIAG(HIGH)}$	V_{CC} = 5 V; R_L = 3.3 kΩ	94	98	100	$\%V_{CC}$
		V_{CC} = 5 V; R_L = 5 kΩ	96	98	100	$\%V_{CC}$
		V_{CC} = 5 V; R_L = 10 kΩ	97	98	100	$\%V_{CC}$
	$V_{SATDIAG(LOW)}$	V_{CC} = 5 V; R_L = 3.3 kΩ	0	2	6	$\%V_{CC}$
		V_{CC} = 5 V; R_L = 5 kΩ	0	2	4	$\%V_{CC}$
		V_{CC} = 5 V; R_L = 10 kΩ	0	2	3	$\%V_{CC}$
High-Z Leakage	$I_{leak(Hi-Z)}$	Device in high-Z mode; output shorted to GND or VCC	–10	–	10	µA
Filter Step Response Time	t_{RESP}	BW_SEL = 5; time to 90% response to step	–	396	450	µs
Angle Update Rate	t_{UPDATE}	Valid for all bandwidth settings	14.72	16	17.28	µs
MANCHESTER INTERFACE SPECIFICATIONS						
Manchester Input Thresholds [3]	$V_{trig(H)}$	V_{OUT} rising, DIG_COMM_INPUT_HIGH = 0	1.8	1.98	2.16	V
		V_{OUT} rising, DIG_COMM_INPUT_HIGH = 1	2.185	2.365	2.54	V
	$V_{trig(L)}$	V_{OUT} falling, DIG_COMM_INPUT_LOW = 0	0.83	0.99	1.155	V
		V_{OUT} falling, DIG_COMM_INPUT_LOW = 1	1.385	1.64	1.905	V
	$V_{trig(hys)}$	DIG_COMM_INPUT_HIGH = 0, DIG_COMM_INPUT_LOW = 0	0.815	0.985	1.15	V
		DIG_COMM_INPUT_HIGH = 0, DIG_COMM_INPUT_LOW = 1	0.16	0.335	0.525	V
		DIG_COMM_INPUT_HIGH = 1, DIG_COMM_INPUT_LOW = 0	1.155	1.38	1.605	V
		DIG_COMM_INPUT_HIGH = 1, DIG_COMM_INPUT_LOW = 1	0.495	0.725	0.995	V
Manchester Communication Speed [3]	f_{MAN}	Manchester input bit rate (from host to sensor)	4	–	100	kbps
		Manchester output bit rate with 100 nF load (device responds at the input bit rate)	4	–	8 [1]	kbps
SENT INTERFACE SPECIFICATIONS						
SENT Tick Time	t_{TICK}	Valid for all SENT modes, DIG_OUT_DATA_RATE = 0	2.76	3	3.24	µs
		Valid for all SENT modes, range of selectable tick times [2]	0.25	–	10	µs
SENT Tick Time Tolerance	TOL_{TICK}	Valid for all selectable tick times	–8	–	8	%
SENT Output Resolution		Based on SENT_DATA_SEL	12	–	16	bits
SENT Output Saturation Voltage	$V_{SAT(LOW)}$	Output current = –4.7 mA, V_{CC} = 5 V, output FET on	–	–	0.55	V
SENT Output Load Capacitance	C_L		0	–	1	nF
SENT Output Load Resistance	$R_{L(PULLUP)}$	Output current ≥ –10 mA	3.3	–	–	kΩ
SENT Output Low Voltage [3]	V_{OL}	Low-state voltage with 0.52 mA DC load current	–	–	0.5	V
SENT Output High Voltage [3]	V_{OH}	High-state voltage with 0.1 mA DC load current	4.1	–	–	V

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SENT Ground Current [3]	I_{GND}	Average current through (signal) ground line over one message	–	–	50	mA
SENT Supply Ripple Current [3]	$I_{SUP-RIPPLE}$	Peak-to-peak variation in supply current consumption over one message at frequencies up to f_C = 30 kHz measured as described for I_{GND}	–	–	9	mA
SENT Fall Time [3]	t_{FALL}	From V_{OUT} = 3.8 V to V_{OUT} = 1.1 V, $I_{GND} \leq 20$ mA, 3 µs tick time	–	–	6.5	µs
		From V_{OUT} = 3.8 V to V_{OUT} = 1.1 V, 20 mA ≤ I_{GND} ≤ 50 mA, 3 µs tick time	–	–	5	µs
SENT Rise Time [3]	t_{RISE}	From V_{OUT} = 1.1 V to V_{OUT} = 3.8 V, 3 µs tick time	–	–	18	µs
SENT Edge Jitter [3]	Δt_{FALL}	Edge-to-edge jitter with static environment for any pulse prior; 3 µs tick time	–	–	0.1	µs
SENT Nibble Jitter [3]	Δt_{NIBBLE}	Variation of maximum nibble time compared to the expected time derived from the calibration pulse; 3 µs tick time	–	–	0.3	µs
PWM INTERFACE SPECIFICATION						
PWM Carrier Frequency	f_{PWM}	See Table 10	125	–	160000	Hz
PWM Carrier Frequency Tolerance	$TOL(f_{PWM})$		–8	–	8	%
PWM Resolution	res_{PWM}	Based on f_{PWM}	8	–	15	bit
Output Jitter, PWM	PWM_{JIT}	$f_{PWM} \geq 2$ kHz; see Table 3 for LSB definition	–1	–	1	LSB
		$f_{PWM} < 2$ kHz; see Table 3 for LSB definition	–3	–	3	LSB
PWM Duty Cycle	D_{PWM}		2	–	98	%
PWM Output Saturation Voltage	$V_{SAT(LOW)}$	$R_{PULLUP} \geq 1.2$ kΩ	–	–	0.4	V
PWM Output Load Resistance	$R_{L(PULLUP)}$		3.3	–	–	kΩ

[1] Based on receiver design.
[2] Tick times less than 0.5 µs are available, but not guaranteed.
[3] Parameter not measured at final test. Determined by design and characterization.

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POWER-UP AND POWER-DOWN SEQUENCES

A. As long as the supply voltage is less than $V_{POR(RISE)}$, the sensor is held in reset; V_{OUT} is between GND and VCC.

B. As the supply passes $V_{POR(RISE)}$, the sensor leaves the reset state and copies EEPROM values to the shadow registers.

C. After the power-on reset (POR) procedure is complete, the sensor enters typical operation.

D. At that point:

- If the supply is still below $V_{UVD(RISE)}$, the sensor reports undervoltage on the output, as per the error diagnostic configuration.
- If there is no error to be reported, the sensor outputs data on the output pin.

E. After t_{PO} elapses, the first unfiltered data are available.

For the $V_{UVD(RISE)}$ and $V_{UVD(FALL)}$ settings and the $V_{OVD(RISE)}$ and $V_{OVD(FALL)}$ options, see the Interface Characteristics table.

NOTE: Depending on the region, the output high or low level is determined by R_L, *OUT_ERR_RESP_SEL(OV/UV)*. These three levels can be defined independently of each other.

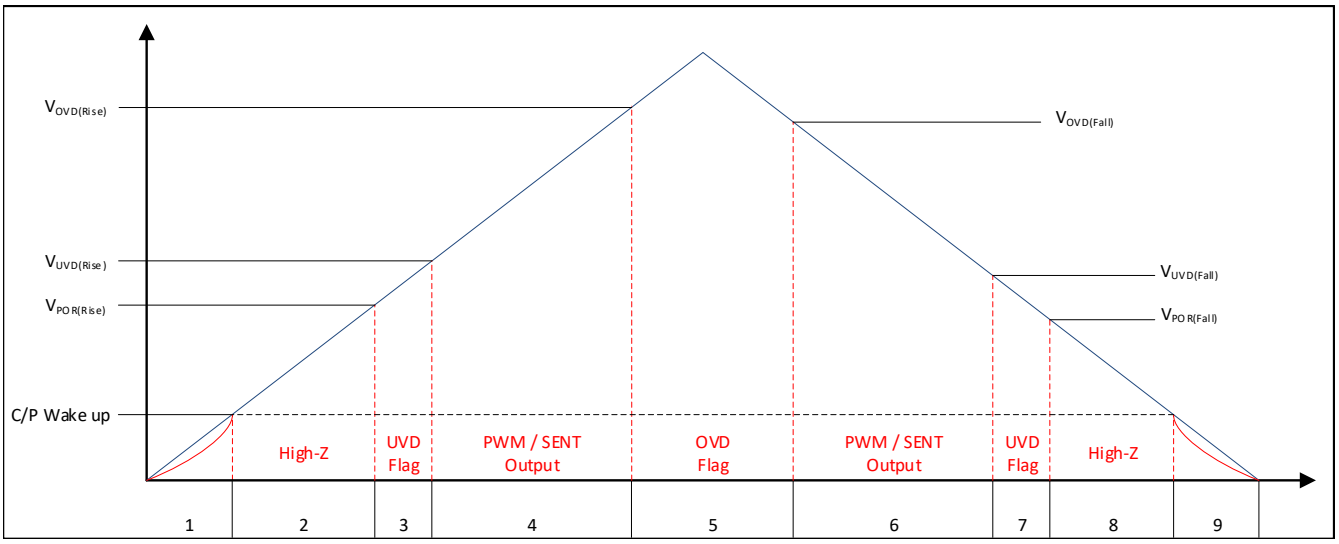

Figure 3

Power-Up Time Specifications

1, 9	Device is off. Output is determined by output stage and load circuit.
2, 8	Device is in the high-Z state. Output voltage is based on load circuit.
3, 7	Device is in UVD. Output voltage is based on UVD error reporting settings.
4, 6	Device is active and in typical operation.
5	Device is in OVD. Output is based on OVD error reporting settings.

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FUNCTIONAL DESCRIPTION

The A31316 contains two independent signal paths: One path is dedicated to alternate between the two sensing dimensions for the angle calculation; and the other path is a complete copy of the time-shared signal path to provide a diagnostic check of the sensing channels to ensure accuracy for safety-critical applications. Each channel has dedicated polarity, sensitivity, and offset correction that is available to the customer for end-of-line calibration. This allows the A31316 to be used in both rotary and linear position applications in any mounting orientation relative to the sensing magnet and to provide high accuracy and matching as the device and magnetic system changes over temperature.

The A31316 features an internal CORDIC calculation of angle from factory-selected pairs of detection axes (X, Y, and Z). The CORDIC calculation effective accuracy is 16 bits.

Equation 1:

$$\theta = \text{atan2}(\sin(\theta), \cos(\theta))$$

The output angle value is available in both SENT and PWM options. Alternatively, the two factory-selected channels of the X, Y, and Z channels are available to output in SENT. Along with the magnetic data, the SENT option provides access to additional device data, such as temperature, error flag data, and customer identification register data. End-of-line angle-calibration options are available in customer space to allow the device to be used in a wide number of contactless sensing applications.

Typical Application Information

The A31316 has a high level of customer programmability to be used in a number of applications for either on- or off-axis rotary-angle or linear-position sensing. For on-axis rotary sensing, the on-chip ATAN2 provides an angle output that, combined with the configurable update rate, allows magnetic angular sensing at a wide range of system bandwidth requirements. To help account for errors associated with off-axis mounting of the sensor, the individual Channel A and Channel B sensitivity and offset correction can be used to match the amplitude of the signals input to the ATAN2.

The A31316 can be used for slide-by applications, in which a one-dimensional position change of a target is to be measured. The angle output from the A31316 is related to the linear position of the magnetic target. With the available linearization on the A31316, stroke lengths greater than the length of the magnet can be realized.

Temperature Output

The A31316 temperature sensor output that is used for temperature compensation within the device can be read from primary register TEMPERATURE_16B [11:0] or, in SENT, from the extended data nibbles or status and communication nibble (SCN) serial message.

Table 1: Temperature Output Options

Temperature Reporting Method	Code Range	Temperature Range	Step Size	Conversion
Read of Register (TEMPERATURE_16B)	–32,768 … 32,767	–231.0°C … 281.0°C	1/8°C	$T_A\,[°C] = \frac{\text{signed 16-bit temperature code}}{128} + 25$
SENT Serial or Extended Nibble	1 … 4088	–230.9°C … 280.0 °C	1/8°C	$T_A\,[°C] = \frac{\text{unsigned 12-bit temperature code} - 2048}{8} + 25$
SENT 8-BIT Temperature Data	1 … 255	–229.0°C … 279.0 °C	2°C	$T_A\,[°C] = (\text{unsigned 8-bit temperature code} - 128) \times 2 + 25$

SENT temperature sensor output corresponds to SAEJ2716 APRIL2016, chapter E.2.2.3, with the following function representation:

SENT Serial or Extended Nibble:
X_1 = –230.875°C = 42.275 K
Y_1 = 1

X_2 = 280°C = 553.15 K
Y_2 = 4088

SENT 8-Bit Data:
X_1 = –229°C = 44.15 K
Y_1 = 1

X_2 = 279°C = 552.15 K
Y_2 = 255

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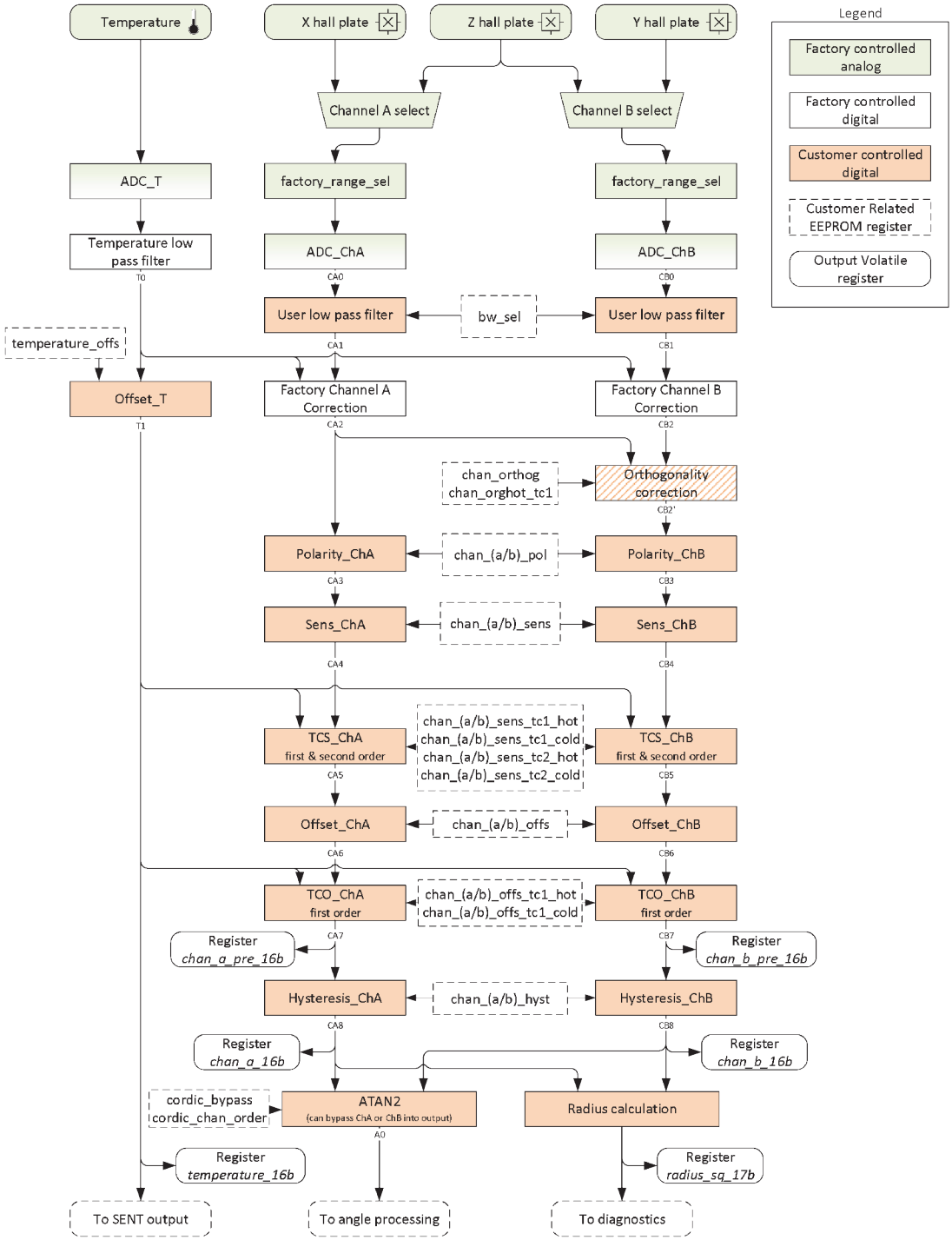

Figure 4: 1D Signal Path Processing Flow

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Signal Path

The A31316 signal path contains two min sections. The first is two 1D signal paths, each reflecting the magnetic field in one direction, as specified in the selection guide. The second section uses a CORDIC calculation to determine an angle from the 1D signals. Both sections provide customer-accessible trim registers for end-of-line calibrations.

1D Signal Path

FACTORY CHANNEL A/CHANNEL B INPUT SELECTION

Selects the input to Channel A and Channel B. This is programmed at factory level. To determine which axes are used, refer to the selection guide.

FACTORY RANGE SELECTION

Factory range selection sets the analog pre-amplifier. The A31316 front-end settings are configured for a limited field range. To determine the field range, consult the selection guide.

CUSTOMER-CONTROLLABLE DATA PATH

The data path is further processed as per the equations provided in the Customer Trimming section.

NOTE: If the segment processor correction components are changed by the customer, temperature performance may deviate from specification. The customer must take care in changing these components and assumes liability for temperature performance deviations that come about from the changes applied.

Customer Trimming

LOW-PASS FILTER

The user-selectable low-pass filter (see Figure 5 and Table 2) allows a noise reduction without data update rate change using a combination of a cascaded-integrator-comb (CIC) filter and an infinite-impulse-response (IIR) filter. The IIR filter is a third-order low-pass filter.

Equation 2:

$$CA_1 = LPF(CA_0)$$
$$CB_1 = LPF(CB_0)$$

$$H(z) = \frac{1}{2^{k+1}} \cdot \frac{1 + z^{-1}}{1 - (1 - 2^{-k})z^{-1}}$$

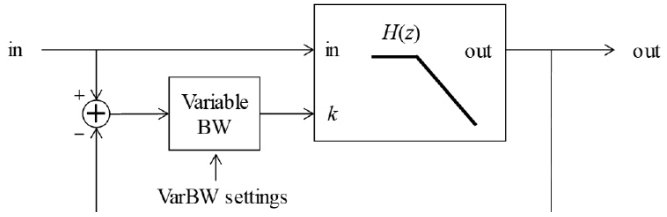

Figure 5: Low-Pass Filter

The adaptive filter has a selectable minimum and maximum bandwidth for increased customization. The minimum and maximum bandwidths are selected via the *BW_ADAP_MIN* and *BW_ADAP_MAX* registers, respectively. The corresponding bandwidths for each register are shown in Table 3. By default, *BW_ADAP_MIN* is set to code 0 and *BW_ADAP_MAX* is set to code 7. The overall filter response is shown in Figure 6.

Table 2: Selection of Customer Low-Pass Filter, EEPROM Parameter *BW_SEL*

BW_SEL	3 dB Frequency (Hz)	90% Settling (ms)
0	329.1	1.666
1	465.8	1.172
2	556	0.9925
3	700	0.763
4	1000	0.554
5	1482	0.396
6	2024	0.249
7	Adaptive	0.135

Table 3: BW_ADAPT_(MIN/MAX) Frequencies

BW_ADAPT_(MIN/MAX) (LSB)	Frequency (Hz)
0	38.9
1	77.8
2	156.3
3	314.8
4	638.7
5	1308.6
6	2672.1
7	4734.2

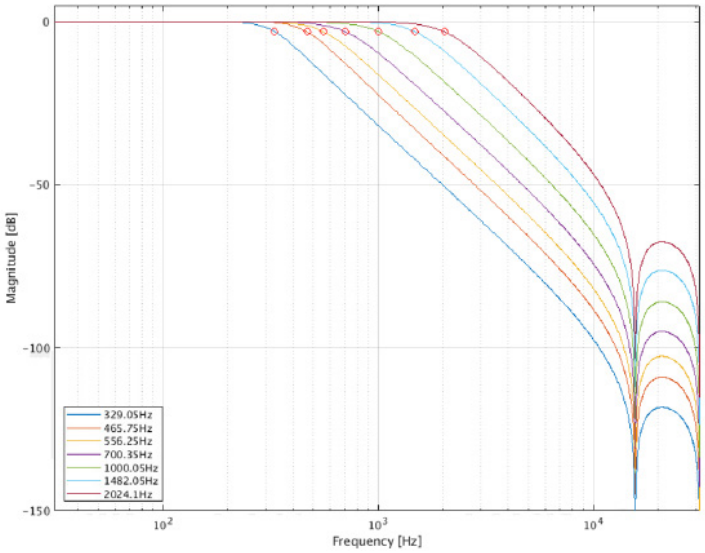

Figure 6: Overall IIR Filter Response Depending on the Selected Bandwidth

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SENSOR OUTPUT DURING LOW-PASS FILTER INITIALIZATION

After startup, the low-pass filter takes some time to settle. It may be undesirable for the output values to show this settling behavior. For this reason, the parameter *POWER_ON_DELAY* allows suppressing the sensor output for a configurable amount of time. If desired, the time that the output is suppressed should be set to a value compatible with the filter settling time. It is the user's responsibility to do this. The value is not automatically chosen by the sensor to be compatible with the filter bandwidth setting.

For SENT output:

- If *SENT_ENCODING_SEL* = 1 and *SENT_DATA_SEL* = 0, 4, 7, or 15, an initialization code selected by parameter *SENT_INIT_SEL* is transferred for the configured amount of time.
- In other cases, the data is sent out with SCN[0] = 1 for the configured filter initialization time.

For PWM output, the POR error code is sent out for the time selected by *POWER_ON_DELAY*. This error code is represented by the values shown in Table 32. The error may be superseded by errors of higher priority as per Table 32.

The *POWER_ON_DELAY* options are shown in Table 4.

Table 4: Selection of output during low-pass filter startup, EEPROM Parameter *POR_ON_DELAY*

POR_ON_DELAY (code)	SENT Additional Init Code Time (ms) / Additional POR Error Time (ms)	PWM POR state duration (ms)
0	0.5	0.5
1	1.0	1.0
2	1.5	1.5
3	2.0	2.0
4	2.5	2.5
5	3.0	3.0
6	4.0	4.0
7	none	0.25

FACTORY CORRECTION

The A31316 devices are factory-trimmed for the channels and field ranges noted in the selection guide. The trim provides a flat temperature compensation (TC) to all parameters and accuracy to the datasheet specifications for channel and angle.

$$CA_2 = Factory_{Correction}\ (CA_1)$$

$$CB_2 = Factory_{Correction}\ (CB_1)$$

ORTHOGONALITY CORRECTION

A factory-trimmed orthogonality correction is implemented. This works by modeling the orthogonality error as a cross-sensitivity from Channel A into Channel B prior to CORDIC calculation.

Equation 3:

$$CB_2' = CB_2 + (Phase_{Corr} \times CA_2)$$

For information about how to adapt the orthogonality correction, contact Allegro MicroSystems.

POLARITY, OFFSET, TCO, SENSITIVITY, TCS CALIBRATION

Polarity bits are provided for each channel to invert the direction of sensitivity of either or both axes. Polarity change is the first operation performed in the customer trim path. Because of this, it should be set first to ensure the offset is programmed properly.

The offset and sensitivity parameters can be used to help provide a linear output when using the device in any off-axis orientation. The angle output is linear for well-matched input sensing vectors. When mounting off axis, one dimension often has offset and amplitude variation relative to the other. Using the *CHAN_(A/B)_OFFS* and *CHAN_(A/B)_SENS* parameters can correct this system-level mismatch, effectively providing a simple two-parameter linearization method.

The offset and sensitivity parameters can be used to stabilize the sensor output over temperature. First- and second-order corrections, separated per channel and separated for temperature above and below 25°C, are provided for post-mounting offset and gain calibration.

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POLARITY CORRECTION

Equation 4:

$$CA_3 = \begin{cases} CA_2 & \text{for} \quad CHAN\_A\_POL = 0 \\ -CA_2 & \text{for} \quad CHAN\_A\_POL = 1 \end{cases}$$
$$CB_3 = \begin{cases} CB_2 & \text{for} \quad CHAN\_B\_POL = 0 \\ -CB_2 & \text{for} \quad CHAN\_B\_POL = 1 \end{cases}$$

SENSITIVITY ADJUSTMENT

Equation 5:

$$CA_4 = CA_3 \times S_{CHAN\_A\_SENS}$$
$$CB_4 = CB_3 \times S_{CHAN\_B\_SENS}$$

where $S_{CHAN\_(A/B)\_SENS}$ is the sensitivity of the *CHAN_(A/B)_SENS* register. The range of $S_{CHAN\_(A/B)\_SENS}$ is [0 … 7.9995], with a resolution of 2^{-11} = 4.88e-04. The default value is 2048, resulting in a gain of 1.

SENSITIVITY CORRECTION OVER TEMPERATURE

Equation 6:

$$CA_5 = \begin{cases} CA_4 \times (1 + S_{CHAN\_A\_SENS\_TC1\_COLD} \times (T_0 - 25°C) + S_{CHAN\_A\_SENS\_TC2\_COLD} \times (T_0 - 25°C)^2) & \text{Temperature} < 25°C \\ CA_4 \times (1 + S_{CHAN\_A\_SENS\_TC1\_HOT} \times (T_0 - 25°C) + S_{CHAN\_A\_SENS\_TC2\_HOT} \times (T_0 - 25°C)^2) & \text{Temperature} \geq 25°C \end{cases}$$
$$CB_5 = \begin{cases} CB_4 \times (1 + S_{CHAN\_B\_SENS\_TC1\_COLD} \times (T_0 - 25°C) + S_{CHAN\_B\_SENS\_TC2\_COLD} \times (T_0 - 25°C)^2) & \text{Temperature} < 25°C \\ CB_4 \times (1 + S_{CHAN\_B\_SENS\_TC1\_HOT} \times (T_0 - 25°C) + S_{CHAN\_B\_SENS\_TC2\_HOT} \times (T_0 - 25°C)^2) & \text{Temperature} \geq 25°C \end{cases}$$

The range for $S_{CHAN\_X\_SENS\_TC1\_COLD}$ is [-2^{-7} … ($2^{-7} - 2^{-17}$)] = –0.0078 … +0.0078 with a resolution of 2^{-17} = 7.63e–06[1/K].
The range for $S_{CHAN\_X\_SENS\_TC1\_HOT}$ is [-2^{-8} … ($2^{-8} - 2^{-18}$)] = –0.0039 … +0.0039 with a resolution of 2^{-18} = 3.81e–06[1/K].
The range for $S_{CHAN\_X\_SENS\_TC2\_COLD}$ is [-2^{-14} … ($2^{-14} - 2^{-23}$)] = –6.10e–05 … +6.09e–05 with a resolution of 2^{-23} = 1.19e–07[1/K^2].
The range for $S_{CHAN\_X\_SENS\_TC2\_HOT}$ is [-2^{-16} … ($2^{-16} - 2^{-25}$)] = –1.53e–05 … +1.52e–05 with a resolution of 2^{-25} = 2.98e–08[1/K^2].

CUSTOMER OFFSET CORRECTION

Equation 7:

$$CA_6 = CA_5 + O_{CHAN\_A\_OFFS}$$
$$CB_6 = CB_5 + O_{CHAN\_B\_OFFS}$$

where $O_{CHAN\_B\_OFFS}$ is the offset of the *CHAN_B_OFFS* register. The range for $O_{CHAN\_B\_OFFS}$ is –32768 … +32764 with a resolution of 4 LSB.

CUSTOMER OFFSET CORRECTION OVER TEMPERATURE

Equation 8:

$$CA_7 = \begin{cases} CA_6 + O_{CHAN\_A\_OFFS\_TC1\_COLD} \times (T_0 - 25°C) & \text{Temperature} < 25°C \\ CA_6 + O_{CHAN\_A\_OFFS\_TC1\_HOT} \times (T_0 - 25°C) & \text{Temperature} \geq 25°C \end{cases}$$
$$CB_7 = \begin{cases} CB_6 + O_{CHAN\_B\_OFFS\_TC1\_COLD} \times (T_0 - 25°C) & \text{Temperature} < 25°C \\ CB_6 + O_{CHAN\_B\_OFFS\_TC1\_HOT} \times (T_0 - 25°C) & \text{Temperature} \geq 25°C \end{cases}$$

The range for $O_{CHAN\_X\_OFFS\_TC1\_COLD}$ is [–128 … +127.9375] LSB/K with a resolution of 2^{-4} = 0.0625 LSB/K.
The range for $O_{CHAN\_X\_OFFS\_TC1\_HOT}$ is [–256 … +255.875] LSB/K with a resolution of 2^{-3} = 0.125 LSB/K.

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HYSTERESIS FILTER

Equation 9:

$$CA_8 = FLT_{HYSTERESIS\_FILTER(CA7)}$$
$$CB_8 = FLT_{HYSTERESIS\_FILTER(CB7)}$$

where FLT is the filter.

The hysteresis block limits change in the sensor output to remove noise from the channels. The hysteresis block can be disabled by setting the hysteresis window width to zero. The hysteresis block input as measured by the sensor is at the head of the hysteresis window. As long as the hysteresis input (CA_7/CB_7) advances in the same direction of rotation, the hysteresis output (CA_8/CB_8) is unchanged, minimizing latency. If the hysteresis input (CA_7/CB_7) reverses direction, the hysteresis output is held static until the input data exit the hysteresis window in either direction. If the exit is in the opposite direction of movement as to where the head was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. On sensor reset, the first value change is accepted as initial direction. The behavior of the hysteresis block is shown in Figure 6.

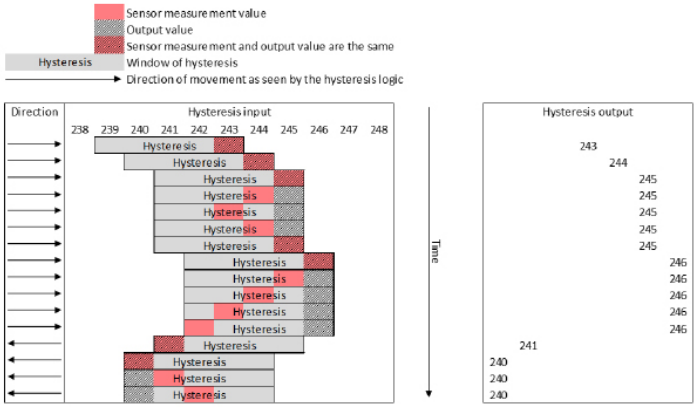

Figure 7: Input and Output Example of Hysteresis Block

The range for $H_{CHAN\_(A/B)\_HYST}$ is [0 … 1023] LSB with a resolution of 1 LSB.

DIRECT OUTPUT REGISTER

The Channel A and Channel B data can be read directly through the digital interface for customer trimming and in-application debugging purposes.

Equation 10:

$$CHAN\_A\_16B[15:0] = CA_8$$
$$CHAN\_B\_16B[15:0] = CB_8$$

ATAN INPUT SELECTION

To provide the angle output from the 3D Hall elements, the two-input function atan2 is used. It is internally implemented using the CORDIC algorithm. The sine and cosine inputs to the ATAN2 are user-selectable based on the EEPROM parameter CORDIC_CHAN_ORDER. The CORDIC algorithm calculates the arctangent to provide the angle between the two input vectors. This angle is related to the linear position in slide-by long-stroke applications. A bypass option is provided to route the CA or CB data directly to the next processing steps. This allows for use of the A31316 as a 1D sensor. When bypassing the ATAN2 calculation, the most negative 1D value (–32768) becomes an angle of 0° (value 0), a zero value of the 1D channel becomes 180° (value 32768), and the most positive value of the 1D channel becomes 359.99° (value 65535).

Equation 11:

$$A_0 = \begin{cases} \text{atan2}(B_8, C_8) & CORDIC\_BYPASS = 0,\ CORDIC\_CHAN\_ORDER = 0 \\ \text{atan2}(C_8, B_8) & CORDIC\_BYPASS = 0,\ CORDIC\_CHAN\_ORDER = 1 \\ B_8 + 32768 & CORDIC\_BYPASS = 1,\ CORDIC\_CHAN\_ORDER = 0 \\ C_8 + 32768 & CORDIC\_BYPASS = 1,\ CORDIC\_CHAN\_ORDER = 1 \end{cases}$$

NOTE: In Equation 11, atan2(0,1) = 0°, atan2(1,0) = +90°, atan2(0,–1) = +180°, and atan2(–1,0) = +270°. This follows from the function definition of θ = atan2(sin(θ),cos(θ)) as it is implemented in MATLAB. Microsoft Excel provides the input arguments in the opposite sequence.

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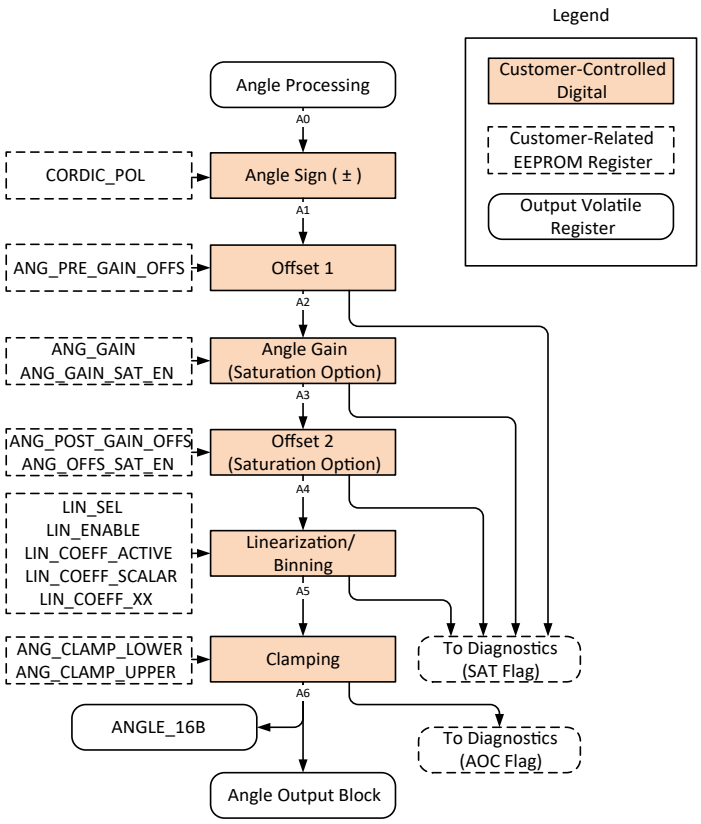

Figure 8: Angle Signal Path Processing Flow

PRE-GAIN ANGLE OFFSET CORRECTION

A31316 contains a programmable zero-angle point allowing the electrical zero angle to be adjusted from the magnetic angle to match mechanical orientations. This is provided in the form of an angle offset correction at the output of the angle-averaging filter. This offset is a full-scale offset with a range of 0 to 360 degrees following Equation 12.

Equation 12:

$$A_1 = mod(A_0 + \theta_{ANG\_PRE\_GAIN\_OFFS}, 360°)$$

The output of the pre-gain offset-correction block, A_2, is always allowed to roll over from the maximum output to the minimum output as needed. It is possible to compare the output angle of this block to programmed limits using the parameters $\theta_{ANG\_THRESH\_LOW}$ and $\theta_{ANG\_THRESH\_HIGH}$, if $ANG\_THRESH\_EN = 1$. These limits do not saturate the A_2 angle, but can be used to cause a saturation flag.

The range for $\theta_{ANG\_PRE\_GAIN\_OFFS}$ is [0 … 359.989013671875]° with a resolution of $360/2^{15} = 0.010986328125$.

The range for $\theta_{ANG\_THRESH\_LOW}$ is [0 … 358.59375]° with a resolution of $360/2^8 = 1.40625°$.

The range for $\theta_{ANG\_THRESH\_HIGH}$ is [0 … 358.59375]° with a resolution of $360/2^8 = 1.40625°$.

For possible diagnostics for this block, see the Saturation Flag (SAT) section.

ANGLE GAIN CORRECTION

Following the initial angle offset correction, there is an angle gain block. This gain correction, defined by the EEPROM parameter *ANG_GAIN*, allows inputs to be scaled to any desired output range. This can be to increase inputs, such as in short-stroke rotary applications or slide-by linear applications to provide the desired output range, or to reduce the inputs if a reduced range is desired for a full output range.

The range, G_{ANG_GAIN}, is [0 … 63.9990234375] with a resolution of $2^{-10} = 0.0009765625$. Setting the gain to zero results in a zero output of the block and has no practical use.

If the gain is set to a value larger than 1.0x, some input values result in an output angle larger than 360°. In this case, the output of the angle gain block, A_3, can either saturate to the maximum code or roll over, depending on the preference set by the EEPROM parameter *ANG_GAIN_SAT_EN*.

If $ANG\_GAIN\_SAT\_EN = 0$, the output rolls over from 360° to restart from 0°.

If $ANG\_GAIN\_SAT\_EN = 1$ (saturation after gain enabled), and gain is set to >1, the output saturates to 360° instead of rolling over. After that, there is a point where the sensor output jumps from 360° to 0°. This point, measured in pre-gain angle A_2, is user configurable using the parameter *ANG_SAT_ROLLOVER*. This is displayed in Figure 8.

The range, $\theta_{ANG\_SAT\_ROLLOVER}$ is [0 … 358.59375]° with a step size of $360°/2^8 \approx 1.40625°$.

In most applications, it is safest to put the output discontinuity of the chip as far away as possible from the range that is being gained up. This is achieved by setting:

$$\theta_{ANG\_SAT\_ROLLOVER} = 180° + (180°)/M_{ANG\_GAIN},$$

where M_{ANG_GAIN} is the gain of the *ANG_GAIN* register.

For example, with M_{ANG_GAIN} set to 4×, the recommended value in degrees for $\theta_{ANG\_SAT\_ROLLOVER}$ is 225°. This is equal to a register value of $\theta_{ANG\_SAT\_ROLLOVER}$=round($2^8 \cdot (225°)/(360°)$)=160. The value for $\theta_{ANG\_SAT\_ROLLOVER}$ must be larger than $360°/M_{ANG\_GAIN}$.

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The behavior is summarized by the following equations:

Equation 13:

If $ANG\_GAIN\_SAT\_EN = 0$:

$$A_2 = mod(A_1 \times M_{ANG\_GAIN}, 360)$$

Equation 14:

If $ANG\_GAIN\_SAT\_EN = 1$:

$$A_1 = \begin{cases} M_{ANG\_GAIN} \times A_1 & \text{for } A_1 \le \left(\frac{360°}{M_{ANG\_GAIN}}\right) \\ 359.9945° & \text{for } \left(\frac{360°}{M_{ANG\_GAIN}}\right) < A_1 \le \theta_{ANG\_SAT\_ROLLOVER} \\ 0° & \text{for } A_1 > \theta_{ANG\_SAT\_ROLLOVER} \end{cases}$$

As an example, the output function for a setting of $M_{ANG\_GAIN} = 4$, $ANG\_GAIN\_SAT\_EN = 1$, and $\theta_{ANG\_SAT\_ROLLOVER} = 225°$ is given in Figure 9.

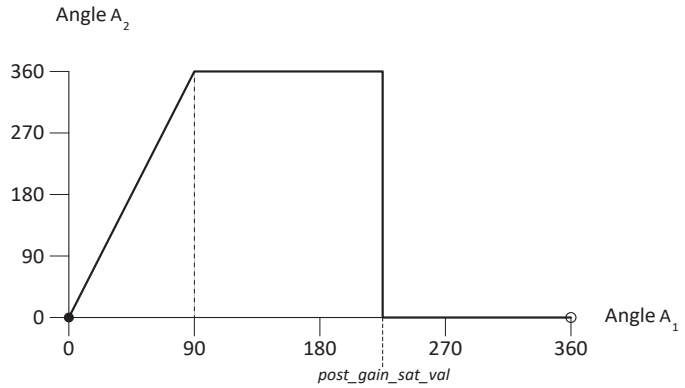

Figure 9: Angle gain behavior over full rotation with gain = 4 and output clamping enabled

As a second example, the output function for a setting of $ANG\_GAIN = 3$ and $ANG\_GAIN\_SAT\_EN = 0$ is given in Figure 10.

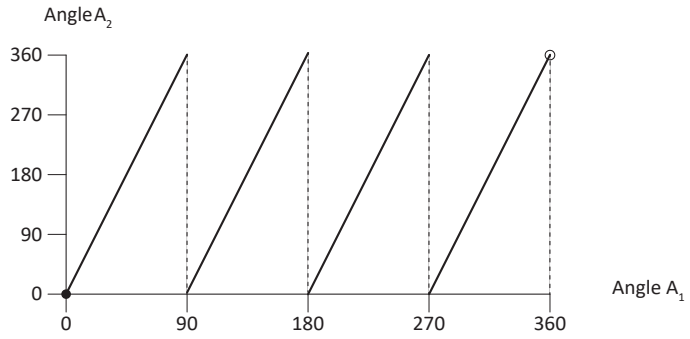

Figure 10: Angle gain behavior over full rotation with gain = 3 and ANG_GAIN_SAT_EN = 0

For information regarding the possible diagnostics for this block, see the Saturation Flag (SAT) section.

POST-GAIN ANGLE OFFSET CORRECTION

After the gain block, there is an additional offset-correction block to allow full flexibility of angle programming. The user can optionally saturate the output of the post-gain angle offset block or allow the output to rollover using the EEPROM parameter *ANG_OFFS_SAT_EN*.

Equation 15:

$$A_3 = \begin{cases} \text{mod}(A_2 + \theta_{ANG\_POST\_GAIN\_OFFS}, 360) & \text{for } ANG\_OFFS\_SAT\_EN = 0 \\ \text{min}(\text{max}(A_2 + \theta_{ANG\_POST\_GAIN\_OFFS}, 0), 359.9945) & \text{for } ANG\_OFFS\_SAT\_EN = 1 \end{cases}$$

The range for *ANG_POST_GAIN_OFFS* is [–360 … 359.9890137]° with a step size of 720° / 2^{16} ≈ 0.010986328125°.

For information regarding the possible diagnostics for this block, see the Saturation Flag (SAT) section.

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ANGLE SIGN (ROTATION DIRECTION)

The A31316 has a bit in EEPROM, *CORDIC_POL,* designating the polarity of the angle reading of the device, determined by whether the output is increasing for clockwise or counterclockwise rotation. Because each channel can be inverted individually in the channel path, this setting must be combined with the channel polarity bits to determine which direction of rotation is considered positive.

Equation 16:

$$A_4 = \begin{cases} A_3 & \text{for} \quad CORDIC\_POL = 0 \\ 360° - A_3 & \text{for} \quad CORDIC\_POL = 1 \end{cases}$$

LINEARIZATION AND BINNING

The A31316 contains two different means of producing an output based on any sensed angle waveform. These options are in the form of a segmented linearization and a discretized output option referred to as binning mode. Each option allows either use of up to 33 fixed points to quantize the angle output or the ability to apply the segment end points at configurable sensed angle locations.

For information regarding the possible diagnostics for this block, see the Saturation Flag (SAT) section.

LINEARIZATION/BINNING MODE SELECTION

The preferred mode is selected by the EEPROM parameter *LIN_MODE*, as shown in Table 5 and depicted in Figure 11.

Table 5: Linearization/Binning Mode Selection

LIN_MODE Code	Output Transfer Function Option
0	Fixed Segment Linearization
1	Fixed Segment Binning Mode
2	Variable Segment Linearization Mode
3	Variable Segment Binning Mode

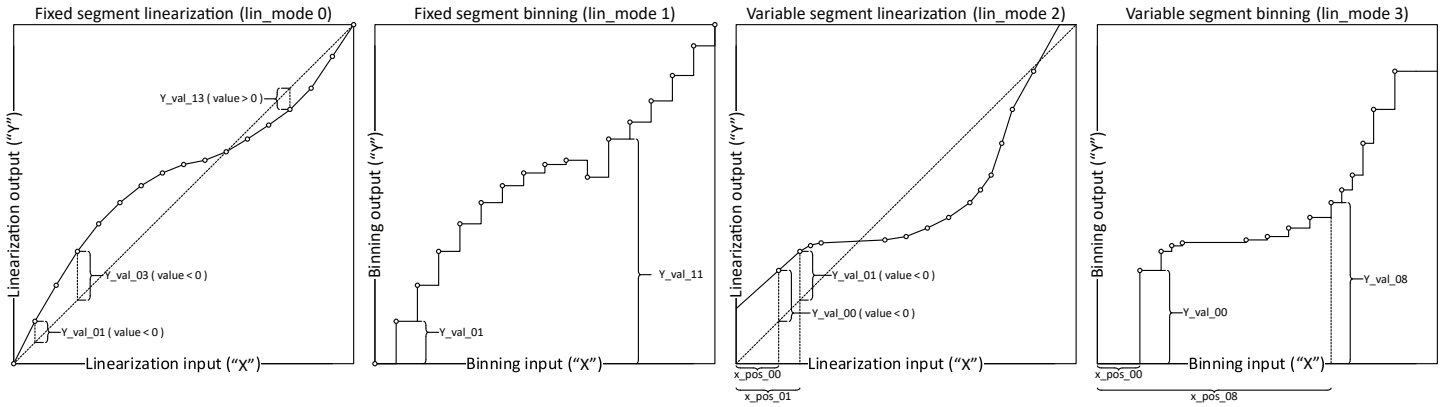

Figure 11: Linearization and Binning Modes

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FIXED-SEGMENT LINEARIZATION (LIN_MODE 0)

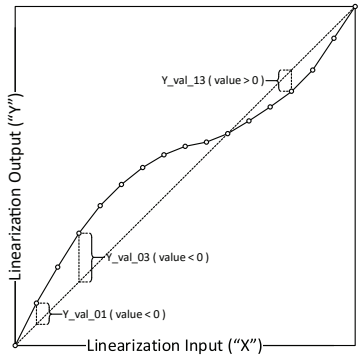

Figure 12: Fixed-Segment Linearization

In fixed-segment linearization mode, between 2 and 33 output correction points are equidistantly positioned between 0° and 360° input. The correction codes *Y_VAL_XX* are in signed 13-bit format and represent a correction using the format in Table 6:

Table 6: *Y_VAL_XX* Range Depending on *LIN_COEFF_SCALAR* Setting

LIN_COEFF_SCALAR	Range (°)	Value for code –4096 (°)	Value for code +4095 (°)	Step size (°)
0	±45	+45	–44.99	$90/2^{13} \approx 0.011$
1	±90	+90	–89.98	$180/2^{13} \approx 0.022$
2	±180	+180	–179.96	$360/2^{13} \approx 0.044$
3	±360	+360	–359.91	$720/2^{13} \approx 0.088$

Most applications have monotonically rising outputs. However, the sensor can support rising and falling outputs if needed.

If the result of the linearization is outside the 0–360° range, the value is clipped to 0° or 360°. Overflow does not occur in the linearization block. This means that, for rotary applications, the 0° correction value and the 360° correction value must both be set to 0.

FIXED-SEGMENT BINNING (LIN_MODE 1)

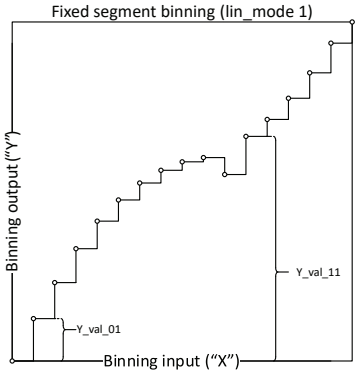

Figure 13: Fixed-Segment Binning

In fixed-segment binning mode, between 2 and 33 bins are equidistantly positioned between 0° and 360° input. The binning output codes *Y_VAL_XX* are in unsigned 13-bit format and represent an output value of 0° (*Y_VAL_XX* = 0) and 359.96° (*Y_VAL_XX* = 8191). Any value is mapped to the bin with a lower value than the input. The parameter *LIN_COEFF_SCALAR* has no meaning in binning mode. The order of the *Y_VAL_XX* values is not relevant.

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VARIABLE-SEGMENT LINEARIZATION (LIN_MODE 2)

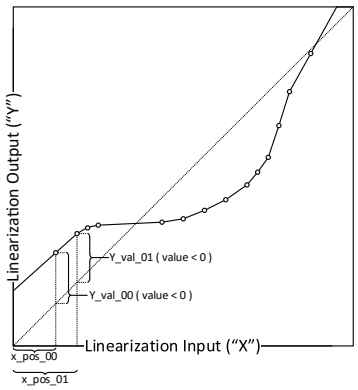

Figure 14: Variable-Segment Linearization

In variable-segment linearization mode, between 2 and 22 output correction points are positioned at user-selected positions. The correction codes *Y_VAL_XX* are in signed 13-bit format and represent a correction using the format in Table 7.

Table 7: Y_VAL_XX Range Depending on LIN_COEFF_ SCALAR Setting

LIN_COEFF_ SCALAR	Range (°)	Value for code –4096 (°)	Value for code +4095 (°)	Step size (°)
0	±45	+45	–44.99	$90/2^{13} \approx 0.011$
1	±90	+90	–89.98	$180/2^{13} \approx 0.022$
2	±180	+180	–179.96	$360/2^{13} \approx 0.044$
3	±360	+360	–359.91	$720/2^{13} \approx 0.088$

Most applications have monotonically rising outputs. However, the sensor can support rising and falling outputs if needed.

The position codes *X_POS_XX* are in unsigned 6-bit format and represent positions of 0° (*X_POS_XX* = 0) to 354.375° (*X_POS_XX* = 63). The X values must be placed in a rising manner, so that the value of $X\_POS(n+1) \geq X\_POS(n)$.

If the result of the linearization is outside the 0–360° range, the value is clipped to 0° or 360°. Overflow does not occur in the linearization block. This means that, for rotary applications, the 0° correction value and the 360° correction value must both be set to 0.

For input values below the angle defined by the *X_POS_00* value, the linearization function extrapolates the slope set by the first two defined points. For input angles above the angle defined by the last *X_POS_XX* value, the linearization function extrapolates the slope set by the last two defined points. For input angles between 354.375° and 360°, this always occurs, and there is no other way to control the behavior in this area than by making use of the extrapolation of the two previous points. The extrapolating behavior is shown in Figure 14 for both low-input and high-input values

VARIABLE-SEGMENT BINNING (LIN_MODE 3)

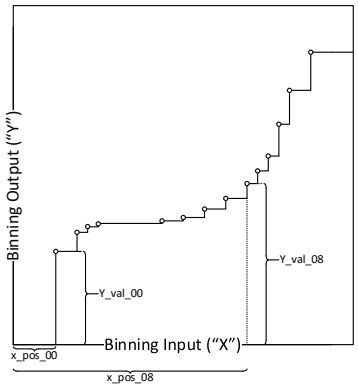

Figure 15: Variable-Segment Binning

In variable-segment binning mode, between 2 and 21 bins are equidistantly positioned between 0° and 360° input. The binning output codes *Y_VAL_XX* are in unsigned 13-bit format and represent an output value of 0° (*Y_VAL_XX* = 0) and 359.96° (*Y_VAL_XX* = 8191). Any value is mapped to the bin as an input angle below that of the input; i.e., the bin that the output ends up in is the bin whose X value is to the left of the measured angle. The parameter *LIN_COEFF_SCALAR* has no meaning in binning mode.

The position codes *X_POS_XX* are in unsigned 6-bit format and represent positions between 0° (*X_POS_XX* = 0) and 354.375° (*X_POS_XX* = 63). The X values must be placed in a rising manner, so that the value of $X\_POS\_(n+1) \geq X\_POS\_(n)$.

If *X_POS_00* does not define a bin at position 0°, a bin with *X_POS* = 0°, *Y_VAL* = 0° is automatically assumed.

LINEARIZATION/BINNING PARAMETER STORAGE

The individual linearization/binning parameters are stored in the EEPROM parameters *LIN_COEFF_00 ... LIN_COEFF_32*. Depending on the linearization/binning configuration, the contents of these memory locations have different meanings. All modes and EEPROM field contents are listed in Table 8. Parameters that are not used for linearization may be used otherwise. The parameters *LIN_COEFF_17 … LIN_COEFF_31* can be sent out through the SENT enhanced serial message for certain constants (see Table 20). If they are used in this manner, the parameter *COEFF_ACTIVE* must be set in such a way that these two usages do not interfere (see Table 9).

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Table 8: Linearization/Binning Parameter Storage

EEPROM Coefficient	Fixed position linearization (LIN_MODE 0)	Fixed position binning (LIN_MODE 1)	Variable segment linearization (LIN_MODE 2)	Variable segment binning (LIN_MODE 3)	SENT EMSG
	12 11 10 9 8 7 6 5 4 3 2 1 0	12 11 10 9 8 7 6 5 4 3 2 1 0	12 11 10 9 8 7 6 5 4 3 2 1 0	12 11 10 9 8 7 6 5 4 3 2 1 0	
LIN_COEFF_00	Y_VAL_00 (signed 13 bit)	Y_VAL_00 (unsigned 13 bit)	X_POS_01 (uns. 6 bit) X_POS_00 (uns. 6 bit)	X_POS_01 (uns. 6 bit) X_POS_00 (uns. 6 bit)	
LIN_COEFF_01	Y_VAL_01 (signed 13 bit)	Y_VAL_01 (unsigned 13 bit)	X_POS_03 (uns. 6 bit) X_POS_02 (uns. 6 bit)	X_POS_03 (uns. 6 bit) X_POS_02 (uns. 6 bit)	
LIN_COEFF_02	Y_VAL_02 (signed 13 bit)	Y_VAL_02 (unsigned 13 bit)	X_POS_05 (uns. 6 bit) X_POS_04 (uns. 6 bit)	X_POS_05 (uns. 6 bit) X_POS_04 (uns. 6 bit)	
LIN_COEFF_03	Y_VAL_03 (signed 13 bit)	Y_VAL_03 (unsigned 13 bit)	X_POS_07 (uns. 6 bit) X_POS_06 (uns. 6 bit)	X_POS_07 (uns. 6 bit) X_POS_06 (uns. 6 bit)	
LIN_COEFF_04	Y_VAL_04 (signed 13 bit)	Y_VAL_04 (unsigned 13 bit)	X_POS_09 (uns. 6 bit) X_POS_08 (uns. 6 bit)	X_POS_09 (uns. 6 bit) X_POS_08 (uns. 6 bit)	
LIN_COEFF_05	Y_VAL_05 (signed 13 bit)	Y_VAL_05 (unsigned 13 bit)	X_POS_11 (uns. 6 bit) X_POS_10 (uns. 6 bit)	X_POS_11 (uns. 6 bit) X_POS_10 (uns. 6 bit)	
LIN_COEFF_06	Y_VAL_06 (signed 13 bit)	Y_VAL_06 (unsigned 13 bit)	X_POS_13 (uns. 6 bit) X_POS_12 (uns. 6 bit)	X_POS_13 (uns. 6 bit) X_POS_12 (uns. 6 bit)	
LIN_COEFF_07	Y_VAL_07 (signed 13 bit)	Y_VAL_07 (unsigned 13 bit)	X_POS_15 (uns. 6 bit) X_POS_14 (uns. 6 bit)	X_POS_15 (uns. 6 bit) X_POS_14 (uns. 6 bit)	
LIN_COEFF_08	Y_VAL_08 (signed 13 bit)	Y_VAL_08 (unsigned 13 bit)	X_POS_17 (uns. 6 bit) X_POS_16 (uns. 6 bit)	X_POS_17 (uns. 6 bit) X_POS_16 (uns. 6 bit)	
LIN_COEFF_09	Y_VAL_09 (signed 13 bit)	Y_VAL_09 (unsigned 13 bit)	X_POS_19 (uns. 6 bit) X_POS_18 (uns. 6 bit)	X_POS_19 (uns. 6 bit) X_POS_18 (uns. 6 bit)	
LIN_COEFF_10	Y_VAL_10 (signed 13 bit)	Y_VAL_10 (unsigned 13 bit)	X_POS_21 (uns. 6 bit) X_POS_20 (uns. 6 bit)	X_POS_20 (uns. 6 bit)	
LIN_COEFF_11	Y_VAL_11 (signed 13 bit)	Y_VAL_11 (unsigned 13 bit)	Y_VAL_00 (signed 13 bit)	Y_VAL_00 (unsigned 13 bit)	
LIN_COEFF_12	Y_VAL_12 (signed 13 bit)	Y_VAL_12 (unsigned 13 bit)	Y_VAL_01 (signed 13 bit)	Y_VAL_01 (unsigned 13 bit)	
LIN_COEFF_13	Y_VAL_13 (signed 13 bit)	Y_VAL_13 (unsigned 13 bit)	Y_VAL_02 (signed 13 bit)	Y_VAL_02 (unsigned 13 bit)	
LIN_COEFF_14	Y_VAL_14 (signed 13 bit)	Y_VAL_14 (unsigned 13 bit)	Y_VAL_03 (signed 13 bit)	Y_VAL_03 (unsigned 13 bit)	
LIN_COEFF_15	Y_VAL_15 (signed 13 bit)	Y_VAL_15 (unsigned 13 bit)	Y_VAL_04 (signed 13 bit)	Y_VAL_04 (unsigned 13 bit)	
LIN_COEFF_16	Y_VAL_16 (signed 13 bit)	Y_VAL_16 (unsigned 13 bit)	Y_VAL_05 (signed 13 bit)	Y_VAL_05 (unsigned 13 bit)	
LIN_COEFF_17	Y_VAL_17 (signed 13 bit)	Y_VAL_17 (unsigned 13 bit)	Y_VAL_06 (signed 13 bit)	Y_VAL_06 (unsigned 13 bit)	$03
LIN_COEFF_18	Y_VAL_18 (signed 13 bit)	Y_VAL_18 (unsigned 13 bit)	Y_VAL_07 (signed 13 bit)	Y_VAL_07 (unsigned 13 bit)	$05
LIN_COEFF_19	Y_VAL_19 (signed 13 bit)	Y_VAL_19 (unsigned 13 bit)	Y_VAL_08 (signed 13 bit)	Y_VAL_08 (unsigned 13 bit)	$06
LIN_COEFF_20	Y_VAL_20 (signed 13 bit)	Y_VAL_20 (unsigned 13 bit)	Y_VAL_09 (signed 13 bit)	Y_VAL_09 (unsigned 13 bit)	$07
LIN_COEFF_21	Y_VAL_21 (signed 13 bit)	Y_VAL_21 (unsigned 13 bit)	Y_VAL_10 (signed 13 bit)	Y_VAL_10 (unsigned 13 bit)	$08
LIN_COEFF_22	Y_VAL_22 (signed 13 bit)	Y_VAL_22 (unsigned 13 bit)	Y_VAL_11 (signed 13 bit)	Y_VAL_11 (unsigned 13 bit)	$09
LIN_COEFF_23	Y_VAL_23 (signed 13 bit)	Y_VAL_23 (unsigned 13 bit)	Y_VAL_12 (signed 13 bit)	Y_VAL_12 (unsigned 13 bit)	$0A
LIN_COEFF_24	Y_VAL_24 (signed 13 bit)	Y_VAL_24 (unsigned 13 bit)	Y_VAL_13 (signed 13 bit)	Y_VAL_13 (unsigned 13 bit)	$90
LIN_COEFF_25	Y_VAL_25 (signed 13 bit)	Y_VAL_25 (unsigned 13 bit)	Y_VAL_14 (signed 13 bit)	Y_VAL_14 (unsigned 13 bit)	$91
LIN_COEFF_26	Y_VAL_26 (signed 13 bit)	Y_VAL_26 (unsigned 13 bit)	Y_VAL_15 (signed 13 bit)	Y_VAL_15 (unsigned 13 bit)	$92
LIN_COEFF_27	Y_VAL_27 (signed 13 bit)	Y_VAL_27 (unsigned 13 bit)	Y_VAL_16 (signed 13 bit)	Y_VAL_16 (unsigned 13 bit)	$93
LIN_COEFF_28	Y_VAL_28 (signed 13 bit)	Y_VAL_28 (unsigned 13 bit)	Y_VAL_17 (signed 13 bit)	Y_VAL_17 (unsigned 13 bit)	$94
LIN_COEFF_29	Y_VAL_29 (signed 13 bit)	Y_VAL_29 (unsigned 13 bit)	Y_VAL_18 (signed 13 bit)	Y_VAL_18 (unsigned 13 bit)	$95
LIN_COEFF_30	Y_VAL_30 (signed 13 bit)	Y_VAL_30 (unsigned 13 bit)	Y_VAL_19 (signed 13 bit)	Y_VAL_19 (unsigned 13 bit)	$96
LIN_COEFF_31	Y_VAL_31 (signed 13 bit)	Y_VAL_31 (unsigned 13 bit)	Y_VAL_20 (signed 13 bit)	Y_VAL_20 (unsigned 13 bit)	$97
LIN_COEFF_32	Y_VAL_32 (signed 13 bit)	Y_VAL_32 (unsigned 13 bit)	Y_VAL_21 (signed 13 bit)		

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NUMBER OF LINEARIZATION/BINNING POINTS

All modes have a configurable number of activated linearization/binning points. The number of active points is selected with the parameter *COEFF_ACTIVE* (see Table 9).

Table 9: Linearization/Binning Mode Parameters Used Depending on *COEFF_ACTIVE*

COEFF_ACTIVE Setting	Number of Active Coefficients			
	LIN_SEL 0 Fixed-Segment Linearization	*LIN_SEL* 1 Fixed -Segment Binning	*LIN_SEL* 2 Variable-Segment Linearization	*LIN_SEL* 3 Variable-Segment Binning [2]
0	33	32	2	1 [1]
1	17	16	2	2
2	9	8	3	3
3	5	4	4	4
4	3	2	5	5
5	2	1 [1]	6	6
6	2	1 [1]	7	7
7	2	1 [1]	8	8
8	2	1 [1]	9	9
9	2	1 [1]	10	10
10	2	1 [1]	11	11
11	2	1 [1]	12	12
12	2	1 [1]	13	13
13	2	1 [1]	14	14
14	2	1 [1]	15	15
15	2	1 [1]	16	16
16	2	1 [1]	17	17
17	2	1 [1]	18	18
18	2	1 [1]	19	19
19	2	1 [1]	20	20
20	2	1 [1]	21	21
21...31	2	1 [1]	22	21

[1] Single coefficient settings for binning mode serve no practical purpose. The output is always equal to the set value.
[2] In LIN_SEL = 3, if X_POS_00 does not define a bin at position 0°, a bin with X_POS = 0°, Y_VAL = 0° is automatically assumed.

BINNING MODE HYSTERESIS

To prevent chattering around the transition threshold between the bins, the A31316 contains internal hysteresis control in binning mode. The *BIN_HYST* parameter establishes the hysteresis in codes below the threshold that the input into the binning block must pass before changing to the lower bin. This prevents expected noise and drift from changing the desired output bin for the designated output range. The binning hysteresis is controlled using the parameter *BIN_HYST*. The default value of *BIN_HYST* = 0 results in no hysteresis being applied.

The range for H_{BIN_HYST} is [0… 11.162109375]° with a step size of 11.25° / 2^7 = 0.087890625°.

Output Clamps

The A31316 contains a digital clamp feature that can clamp the digital output range of the device. These high and low clamps are both programmable to the entire output range of the device. If the input to the clamp block exceeds the upper clamp value, the output is set to the upper clamp value. Similarly, if the input to the clamp block is less than the lower clamp value, the output is set to the lower clamp value. If high and low clamp values are equal, the output equals the clamp value. This can be practical for testing purposes. If the low clamp value is set to a higher value than the high clamp value, the output equals the low clamp number. This configuration has no practical use.

Equation 17:

$$A_6 = \max[\theta_{ANG\_CLAMP\_LOWER}, \min(\theta_{ANG\_CLAMP\_UPPER}, A_5)]$$

The range for $\theta_{ANG\_CLAMP\_UPPER}$ is [0 … 65535] LSB with a step size of 1 LSB.

The range for $\theta_{ANG\_CLAMP\_LOWER}$ is [0 … 65535] LSB with a step size of 1 LSB.

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OUTPUT PROTOCOLS

PWM Output Mode

PWM involves converting the output value to a series of constant-frequency binary pulses, with the percentage of the high portion of the pulse varied in direct proportion to the digital angle.

The PWM output mode (*DIG_OUT_SEL* = 0) is configured by setting the carrier frequency and diagnostic reporting options in EEPROM. The slew rate of the edges may be adjusted using the EEPROM parameters *DIG_OUT_PULL_LIM* and *DIG_OUT_DRIVE_SEL*. For more information, refer to the digital output pin drive strength options.

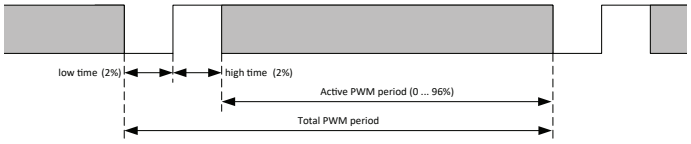

Figure 16: PWM Frame Format

Table 10: PWM Carrier Frequency, EEPROM Parameter DIG_OUT_DATA_RATE

EEPROM Code	PWM Frequency (Hz)	Output Resolution (bit)
0 or 16 (X0000)	125	15
1 or 17 (X0001)	167	15
2 or 18 (X0010)	250	14
3 or 19 (X0011)	333	14
4 or 20 (X0100)	500	13
5 or 21 (X0101)	667	13
6 or 22 (X0110)	800	13
7 or 23 (X0111)	1000	12
8 or 24 (X1000)	1333	12
9 or 25 (X1001)	1600	12
10 or 26 (X1010)	2000	11
11 or 27 (X1011)	2667	11
12 or 28 (X1100)	4000	10
13 or 29 (X1101)	5333	10
14 or 30 (X1110)	8000	9
15 or 31 (X1111)	16000	8

PWM Sampling Time

The data for the PWM output is sampled at the beginning of each frame, as shown in Figure 17. In the figure, Data 0, 1, 3, 5, 7, and 8 are transmitted. Data 2, 4, 6, and 9 are discarded.

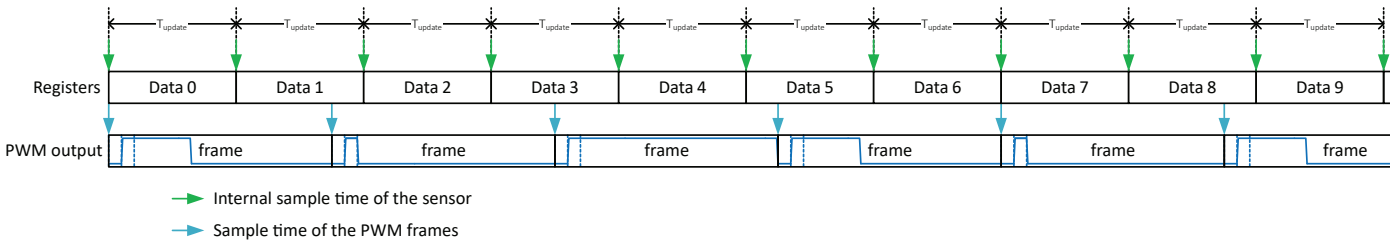

Figure 17: PWM Frame Sampling Timing

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SENT Output Mode

The Single Edge Nibble Transmission (SENT) output mode converts the calculated angle to a binary value mapped to the full-scale output, FSO, range of 0 to 4095, as shown in Figure 18 (for a 12 bit output). This data is inserted into a binary pulse message, referred to as a frame that conforms to the SENT data transmission specification (SAEJ2716 APRIL2016). Certain parameters for configuration of the SENT messages can be set in EEPROM.

The SENT output mode is configured by setting the following parameters in EEPROM:

- SAE J2716 SENT with enhancement options [*DIG_OUT_SEL* = 1 (no pause pulse), *DIG_OUT_SEL* = 2 (pause pulse)].
- Additional configuration parameters in EEPROM.

Message Structure

A SENT message is a series of nibbles. Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval. The low interval is defined as 5 SENT ticks. The high interval contains data and is variable in duration to indicate the data payload of the nibble. The duration of a nibble is denominated in ticks. The period of a tick is set by the *DIG_OUT_DATA_RATE* parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval. The slew rate of the falling edge may be adjusted using the EEPROM parameter *DIG_OUT_PULL_LIM*.

The nibbles of a SENT message are arranged in the following required sequence (see Figure 18):

1. Synchronization and Calibration: Flags the start of the SENT message.
2. Status and Communication (SCN): Provides A31316 status.
3. Data: Magnetic field and optional data.
4. Cyclical Redundancy Check (CRC): Error checking.
5. Pause Pulse: Sets timing relative to a constant message frame length. For settings, refer to the SENT Output Rate section.

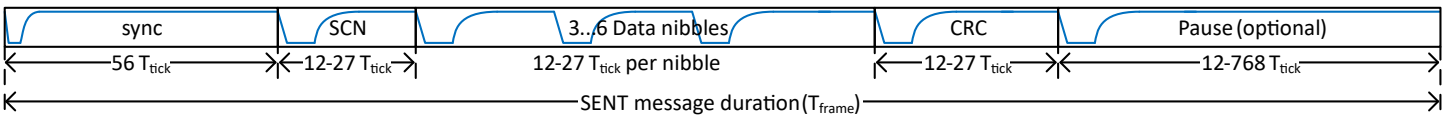

Figure 18: General Format for SENT Message

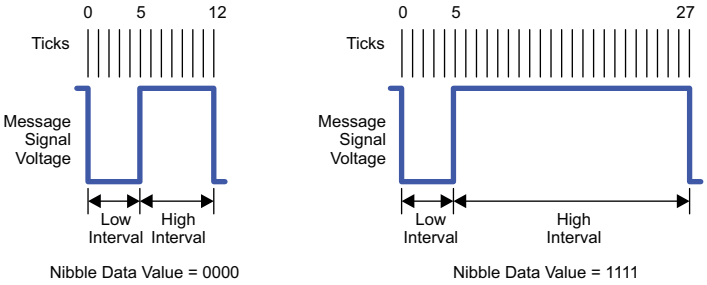

Figure 19: General SENT Nibble Composition

Table 11: SENT Nibble Composition and Value

Quantity of Ticks			Binary (4-bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0010	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15

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SENT Sampling Time

The SENT output data is sampled 33 ticks prior to the start of the SCN nibble. If beginning a new serial message, it is also composed at this time. This is detailed in Figure 20. In the figure, Data 1 and Data 5 are transmitted. Others are discarded.

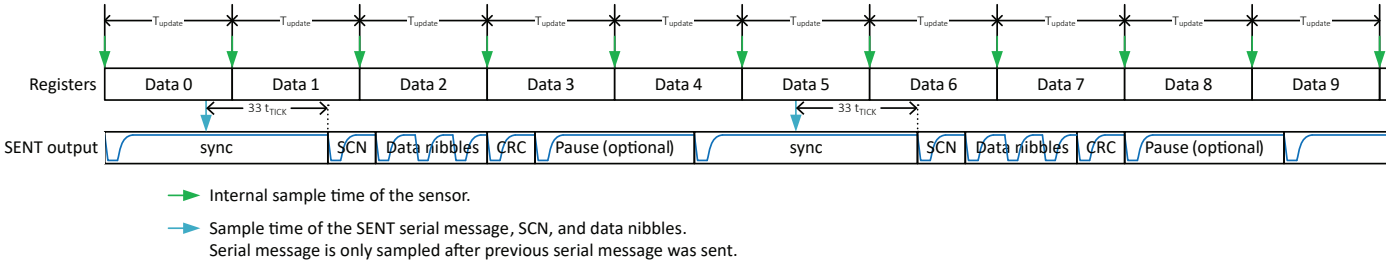

Figure 20: SENT Frame Sample Timing

SENT Output Rate

The SENT output rate depends on the SENT mode. In regular SENT, the frame length is defined by the frame contents. Using SENT-Pause, the frame length is constant. The length of the frames can be selected. There are four options for the frame-length settings. Using *SENT_FRAME_RATE* = 0, the shortest possible pause-pulse that can achieve a fixed frame duration is used, with the calculation shown in Table 12. Using the options *SENT_FRAME_RATE* = 1, 2 or 3, a fixed frame rate, measured in ms rather than ticks, can be selected. Settings are detailed in Table 12.

Table 12: SENT Frame Duration, Depending on *SENT_FRAME_RATE*

SENT_FRAME_RATE	Frame rate including pause pulse
0	3 data nibbles: frame length 210 t_{tick} 4 data nibbles: frame length 228 t_{tick} 6 data nibbles: frame length 282 t_{tick}
1	0.5 ms
2	1 ms
3	2 ms

The output behavior for correct frame rate configurations is shown in Figure 21.

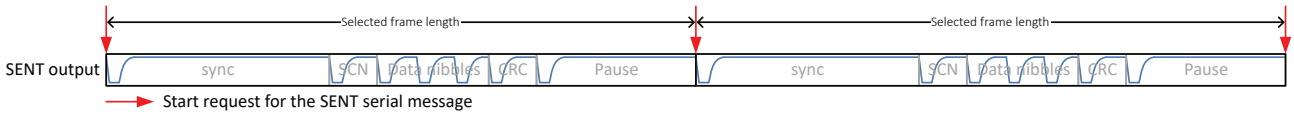

Figure 21: SENT Frame Start Depending on Selected Frame Rate

If the frame rate is configured to be so high that a message is not finished before the intended start of the next one, the start request is discarded. Such a setting is shown in Figure 22.

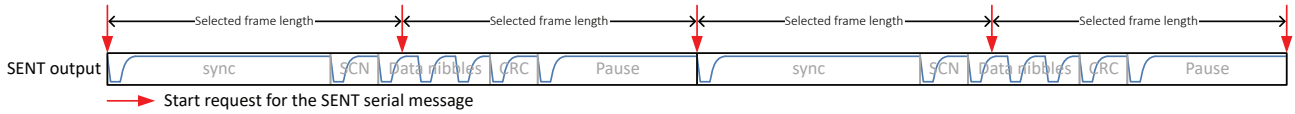

Figure 22: SENT Frame Start Depending on Selected Frame Rate, with *SENT_FRAME_RATE* Defining an Excessively Fast Frame-Rate Setting

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Optional SENT Slow Serial Output Protocol

SENT output supports an optional mode to transmit additional data. The slow serial mode enables transmission of additional data by encoding information in the Status and Communication (SCN) nibbles. The encoded data is captured over several transmissions and is then decoded to indicate additional serial message data. For more details on the serial message, refer to the SENT SAE J2716 APRIL2016 specification.

The slow serial mode is enabled when the EEPROM parameter *SENT_EMSG_DIS* = 0. Following a reset, the first message transmitted is 0, following in order of the message ID until message 7, and then repeating. The data sent with each message ID is identified in Table 13 and Table 14. The CRC for the serial message is derived from the message ID and data.

Table 13: SCN [3:2] Configuration Control

SENT_EMSG_DIS	SCN Nibble bits [3:2] Contents
0	Serial Message
1	All Zeros

The data in the serial message follows Table 14.

Table 14: Serial Message Format in SENT Status and Communication Nibble

Received SCN Nibble #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
SCN[3]	1	1	1	1	1	1	0	0	8-bit ID[7:4]				0	8-bit ID[3:0]				0
SCN[2]	6-bit CRC						12-bit data field											

There are a number of codes available to be sent out in serial mode.

Some codes are based on sensor data, such as the following:

- $01: Error and status codes
- $23: Supplementary data channel #4,1 (temperature data)

Other codes only send out constants, such as:

- $03: Channel 1/2 sensor type
- $05: Manufacturer code
- $06: Protocol standard revision
- $07-0A: Fast channel 1 characteristic X1, X2, Y1, Y2
- $29~2C: Sensor ID #1~4
- $90~97: ASCII character OEM codes MESSAGE_ID

Due to EEPROM sharing, the constant values are not compatible with all linearization modes. The constant values are factory-programmed to EEPROM locations that are shared with *LIN_COEFF_17* through *LIN_COEFF_31*. If using linearization in parallel with these constants, only *LIN_COEFF_00* through *LIN_COEFF_16* should be used. This means fixed-position linearization and binning can be used with up to 17 points, and variable-segment linearization and binning can be used with up to 6 points. For reference, see Table 8. For selecting how many coefficients are used, see Table 9 for the desired COEFF_ACTIVE setting.

If the *LIN_COEFF_XX* value that is assigned to a constant is changed, the new value is output instead of the desired constant. For that reason, it is important to take caution when programming linearization coefficients, to ensure desired constant values are not overwritten.

Each message can be activated or deactivated using the *SENT_EMSG_SEL* EEPROM bits. In this way, if the first constant(s) is(are) not required, their corresponding *LIN_COEFF_XX* value(s) can be used for linearization. The lowest $xx value used determines how many extra linearization coefficients can be used. If $03 is used, even if no other constants are reported, only 17 or 6 coefficients can be used for fixed or movable point respectively (e.g., if constants $03 and $05 are not reported, up to 19 fixed-point coefficients or 8 movable-point coefficients can be used).

Using the EEPROM setting *SENT_SERIAL_REPEAT_1* = 1, the message-ID $01 is repeated between any other messages. That means that, if messages $01, $07, $08, $09, $0A are activated, the transmission is $01-$07-$01-$08-$01-$09-$01-$0A-$01-$07-$01-$08-….

The serial output message numbers, enable bits, data source, and byte contents are provided in Table 15 and Table 16.

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Table 15: SENT Serial Output Message ID Contents for Data Registers

SENT Serial Message ID	Enable	Data Source	Contents
$01	SENT_EMSG_SEL[0]	error register 0xA3[11:0]	Error and Status Codes
$23	SENT_EMSG_SEL[1]	TEMPERATURE_16B[15:4]	Supplementary data channel #4,1 (Temperature data)

Table 16: SENT Serial Output Message ID Contents for Constants

SENT Serial Message ID	Enable	Data Source	Contents
$03	SENT_EMSG_SEL[2]	LIN_COEFF_17[11:0]	Channel 1/2 sensor type
$05	SENT_EMSG_SEL[3]	LIN_COEFF_18[11:0]	Manufacturer code
$06	SENT_EMSG_SEL[4]	LIN_COEFF_19[11:0]	Protocol standard revision
$07	SENT_EMSG_SEL[5]	LIN_COEFF_20[11:0]	Fast channel 1 characteristic X1
$08	SENT_EMSG_SEL[6]	LIN_COEFF_21[11:0]	Fast channel 1 characteristic X2
$09	SENT_EMSG_SEL[7]	LIN_COEFF_22[11:0]	Fast channel 1 characteristic Y1
$0A	SENT_EMSG_SEL[8]	LIN_COEFF_23[11:0]	Fast channel 1 characteristic Y2
$29	SENT_EMSG_SEL[9]	0x0 & WAFER_ID[15:8]	Sensor ID #1
$2A	SENT_EMSG_SEL[10]	0x0 & WAFER_ID[7:0]	Sensor ID #2
$2B	SENT_EMSG_SEL[11]	0x0 & WAFER_YPOS[7:0]	Sensor ID #3
$2C	SENT_EMSG_SEL[12]	0x0 & WAFER_XPOS[7:0]	Sensor ID #4
$90	SENT_EMSG_SEL[13]	LIN_COEFF_24[11:0]	ASCII character OEM codes [1]
$91	SENT_EMSG_SEL[14]	LIN_COEFF_25[11:0]	ASCII character OEM codes [1]
$92	SENT_EMSG_SEL[15]	LIN_COEFF_26[11:0]	ASCII character OEM codes [1]
$93	SENT_EMSG_SEL[16]	LIN_COEFF_27[11:0]	ASCII character OEM codes [1]
$94	SENT_EMSG_SEL[17]	LIN_COEFF_28[11:0]	ASCII character OEM codes [1]
$95	SENT_EMSG_SEL[18]	LIN_COEFF_29[11:0]	ASCII character OEM codes [1]
$96	SENT_EMSG_SEL[19]	LIN_COEFF_30[11:0]	ASCII character OEM codes [1]
$97	SENT_EMSG_SEL[20]	LIN_COEFF_31[11:0]	ASCII character OEM codes [1]

[1] Can be used to send two 6-bit ASCII characters in representation according to SAE J2716, APR2016, Table D.9-1.

Data Nibble Format

When transmitting typical operation data, information about the measurement data is embedded in the first three or four data nibbles. Each data nibble consists of 4 bits with values ranging from 0 to 15. An output with the resolution of 12 or 16 bits requires 3 or 4 data nibbles. The data nibble containing the MSB of the whole data section is sent first.

Three additional optional data nibbles can be associated with other parameters, by setting the EEPROM parameter *SENT_DATA_SEL,* as shown in Table 17.

- Counter—Each message frame has a serial number in each counter nibble.
- Temperature—Temperature data from the A31316 internal temperature sensor.
- Diagnostics—Diagnostic flags can be sent as described in Table 32.
- Inverted nibble 1—Nibble 1 contents (data MSB) can be sent in one's complement.

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SENT CRC

The SENT message contains a 4-bit CRC for data validity checks. The CRC polynomial is shown in Equation 18 with an initial seed of 0×5. By default, the CRC only includes the data nibbles of the SENT message; the synchronization and SCN nibbles are ignored. When EEPROM parameter *SENT_CRC_SCN* = 1, the SCN nibble is included in the CRC calculation.

Equation 18:

$$g(x) = x^4 + x^3 + x^2 + 1$$

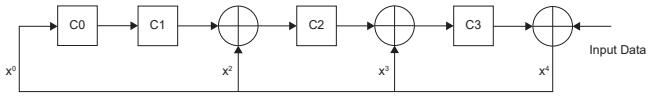

Figure 23: SENT CRC Calculation

SENT Serial Message 6-Bit CRC

The SENT serial message contains a 6-bit CRC, based on the polynomial $x^6 + x^4 + x^3 + 1$.

The CRC checksum can be implemented via a bitwise exclusive OR with a 64-array lookup. The checksum is determined by reading 6-bit groups of the 24-bit message data in sequence, then calculating the checksum with an extra zero value (augmentation by six zero bits).

Table 17: SENT Options Bit Contents EEPROM Parameter: *SENT_DATA_SEL*

SENT Frame	*SENT_DATA_SEL*	Nibble 1				Nibble 2				Nibble 3				Nibble 4				Nibble 5				Nibble 6			
		3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
H2	0	12 Bit Angle [11:0] [1]												Not Used											
	1	12 Bit Angle [11:0]												8-bit Temperature								4-Bit Message Counter			
	2	12 Bit Angle [11:0]												8-bit diag_byte (see SENT Output Error Reporting section)								4-Bit Message Counter			
	3	12 Bit Angle [11:0]												12-Bit Message Counter											
H4	4	12 Bit Angle [11:0] [1]												8-bit Message Counter								Inverted Nibble 1			
	5	12 Bit Angle [11:0]												Ones Complement 12 Bit Angle ~[11:0]											
	6	16-Bit Angle [15:0]																Not Used							
H7	7	16-Bit Angle [15:0] [1]																8-bit Temp[3:0] [1]				8-bit Temp[7:4] [1]			
	8	16-Bit Angle [15:0]																8-bit diag_byte (see Table 32)							
	9	16-Bit Angle [15:0]																8-bit Message Counter							
	10	12bit ChA data												12bit ChB data											
	11	ChA	ChB	14-bit ChA, ChB (rotates each message)														Not Used							
	12	ChA	ChB	14-bit ChA, ChB (rotates each message)														8-bit Temperature							
	13	ChA	ChB	14-bit ChA, ChB (rotates each message)														8-bit diag_byte (see SENT Output Error Reporting section)							
	14	ChA	ChB	14-bit ChA, ChB (rotates each message)														8-Bit Message Counter							
H1	15	12-Bit Angle [11:0] [1]												12-Bit Temp[3:0] [1]				12-Bit Temp[7:4] [1]				12-Bit Temp[11:8] [1]			

[1] This value is subject to modification as per Table 20 based on setting *SENT_ENCODING_SEL*.

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Table 18: SENT Tick Times, EEPROM Parameter DIG_OUT_DATA_RATE

EEPROM Code	SENT Tick Time (µs)
0 (00000)	3
1 (00001)	0.25
2 (00010)	0.375
3 (00011)	0.5
4 (00100)	0.625
5 (00101)	0.75
6 (00110)	0.875
7 (00111)	1
8 (01000)	1.125
9 (01001)	1.25
10 (01010)	1.375
11 (01011)	1.5
12 (01100)	1.625
13 (01101)	1.75
14 (01110)	1.875
15 (01111)	2
16 (10000)	2.125
17 (10001)	2.25
18 (10010)	2.375
19 (10011)	2.5
20 (10100)	2.625
21 (10101)	2.75
22(10110)	2.875
23 (10111)	3
24 (11000)	3.5
25 (11001)	4
26 (11010)	4.5
27 (11011)	5
28 (11100)	5.5
29 (11101)	6
30 (11110)	7
31 (11111)	10

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Table 19: SENT Message Frame Definitions

Section	Description
Synchronization and Calibration	
Function	Provides the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section for ease of distinction by the external controller.
Syntax	Nibbles: 1 Quantity of ticks: 56 Quantity of bits: 1
Status and Communication	
Function	Provides the external controller with the status of the A31316 and indicates the format and contents of the data section.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 Quantity of bits: 4 1:0 Device status 3:2 Message serial data protocol
Data	
Function	Provides the external controller with data selected by the *SENT_DATA_SEL* parameter.
Syntax	Nibbles: 3 to 6 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4 (each nibble)
CRC	
Function	Provides the external controller with cyclic redundancy check (CRC) data for certain error-detection routines applied to the data nibbles and to the status information.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4
Pause Pulse	
Function	Additional time can be added at the end of a SENT message frame to ensure all message frames are of appropriate length and correlate to the internal update rate of the device.
Syntax	Nibbles: N/A Quantity of ticks: Varies Quantity of bits: N/A.

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Error Indicators/Specific Messages/ Initialization Message in SENT Output Codes

If SENT_DATA_SEL is set to code 0, 4, 7, or 15, it is possible to output specific status data to the SENT data code by EEPROM setting SENT_ENCODING_SEL.

Table 20: SENT Error Indicators/Initialization Message, If SENT_ENCODING_SEL = 1 and (SENT_DATA_SEL = 0, 4 , 7 or 15)

n-Bit Data Value	12-Bit Data Value	SENT Definition	Sensor Mapping
Output is High Impedance, or High, or Low, depending on *ERR_RESP_SEL*			Sensor is in UVD mode (undervoltage detected)
Selectable (see SENT Initialization Code Selection section)	Selectable (see SENT Initialization Code Selection section)	Initialization	Sensor is not in UVD mode, AND Sensor is initializing, no final data available yet
2^n–5	4091	Sensor error indication	Sensor is not in UVD mode, AND Sensor is not initializing, AND any of the errors (UVD | OVD | SAT | AOC) are set
2^n–6	4090	Sensor functionality and processing error indication	Sensor is not in UVD mode, AND Sensor is not initializing, AND none of (OVD | SAT | AOC) are set, AND any of the errors (SLF | SRR | ACF | TSE | POR) are set

SAE J2716 SENT

When configured for free-running mode (SENT), *DIG_OUT_SEL* = 1, the SENT output transmits continuously, while in typical operating conditions with no extended pause pulse. When in *DIG_OUT_SEL* = 2, the SENT message frame rate is extended with a variable pause pulse to ensure a constant output rate. The pause pulse is limited to 768 tick times, as defined by the SAEJ2716 APRIL2016 SENT standard.

SENT Initialization Code Selection

According to the SAEJ2716, the output for initialization status must be 0. However, the A31316 permits the user to select other messages instead, which is adjuvant for standard compliance eschewal. The parameter *SENT_INIT_SEL* controls which code is used for initialization, if *SENT_ENCODING_SEL* = 1 and *SENT_DATA_SEL* is set to code 0, 4, 7, or 15.

Table 21: SENT Initialization Code Mapping Selection When SENT_ENCODING_SEL = 1

SENT_INIT_SEL	n-bit Data Output for Initialization	8-Bit Data Output for Initialization	12-Bit Data Output for Initialization	16-Bit Data Output for Initialization
0	0	0	0	0
1	$2^n - 7$	249	4089	65529
2	$2^n - 4$	252	4092	65532
3	$2^n - 3$	253	4093	65533
4	$2^n - 2$	254	4094	65534
5	$2^n - 1$	255	4095	65535
6	0	0	0	0
7	0	0	0	0

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Output Pin Drive Strength Options

The A31316 provides configurable output drive strength. This can be used in open-drain and in push-pull mode.

OUTPUT PIN FALL TIME SELECTION

The A31316 allows the user to change the fall time of the open-drain output digital SENT or PWM signal using the EEPROM parameter *DIG_OUT_PULL_LIM*. This control is viewed as a discrete gradient from faster to slower, with intermediate steps to provide the desired pulse shaping to improve electromagnetic-compatibility (EMC) emissions performance. The resulting fall time is heavily dependent on load capacitance. As reference, fall times for certain capacitance values are shown in Table 22.

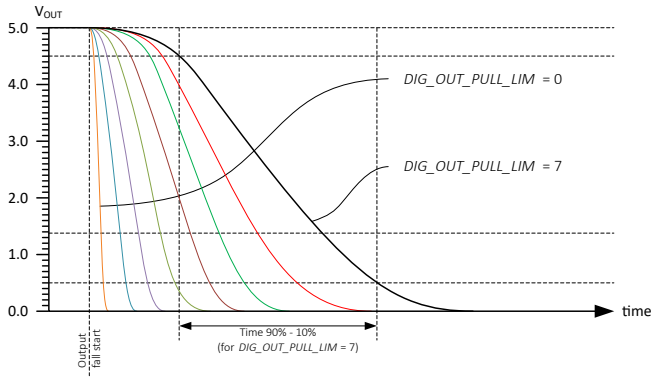

Figure 24: Definition of Output Fall Times and Output Delay (Exemplary Plot)

Table 22: Typical Output Fall Time for Each DIG_OUT_PULL_LIM

DIG_OUT_PULL_LIM	Time 90% to 10% (µs) C_L = 4.7 nF Pullup R_L = 55 kΩ
0	1.15
1	1.18
2	1.2
3	1.33
4	2
5	2.87
6	4.37
7	5.68

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PUSH-PULL OUTPUT SETTING FOR SENT AND PWM RISING EDGE

To decrease the rise time for digital outputs, it is possible to enable a push-pull output. This is accomplished by setting *DIG_OUT_DRIVE_SEL* = 0. In such a configuration, a pull-up resistor is not necessary but is still recommended. The digital output rise times depending on the capacitive load are shown in Table 23.

Table 23: Typical Output Rise Time If DIG_OUT_DRIVE_SEL = 0

Time 10% to 90% (µs) C_{load} = 4.7 nF Pullup R_L = 55 kΩ
0.38

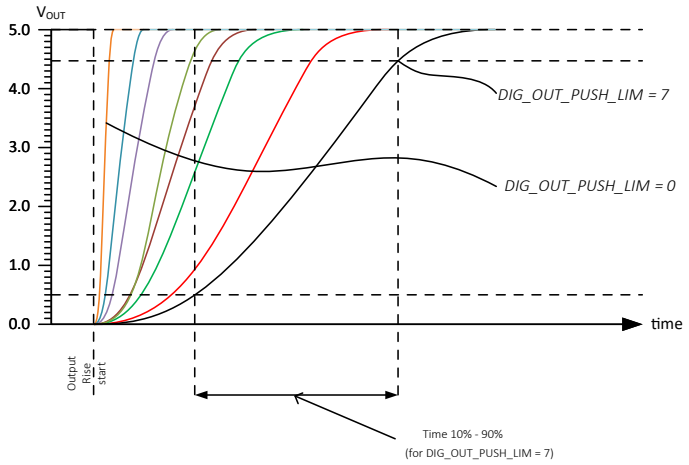

Figure 25: Definition of Output Rise Times and Output Delay (Exemplary Plot)

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PROGRAMMING PROTOCOL

The A31316 device generally uses a three-wire programming interface where V_{CC} can control the program-enable signal, data is transmitted on the output pin, and all signals are referenced to ground. This three-wire interface makes it possible to use multiple devices with shared V_{CC} and ground lines. If V_{CC} can be controlled by the host, this is the preferred method of communication. If V_{CC} cannot be controlled by the host, initiating Manchester communication can be accomplished through the output pin as well. For more information, see the Physical Layer section.

When performing a write to EEPROM transaction, the A31316 requires a delay of t_w to store the data into the EEPROM. The device responds with a low-to-high transition on the output pin to indicate the write to EEPROM sequence is complete.

Physical Layer

The serial interface allows an external controller to read and write registers, including EEPROM, in the A31316 using a point-to-point command/acknowledge protocol when using any of the output protocols. The A31316 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is an acknowledge pulse from the A31316 in the form of a low pulse following a successful write. If the command is a read, the A31316 responds by transmitting the requested data in a read acknowledge frame. It is the responsibility of the external controller to avoid sending a command frame that overlaps a read acknowledge frame.

The serial interface uses a Manchester encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the A31316: write access code, write to volatile memory, write to nonvolatile memory (EEPROM), and read. One frame type, read acknowledge, is sent by the A31316 in response to a read command.

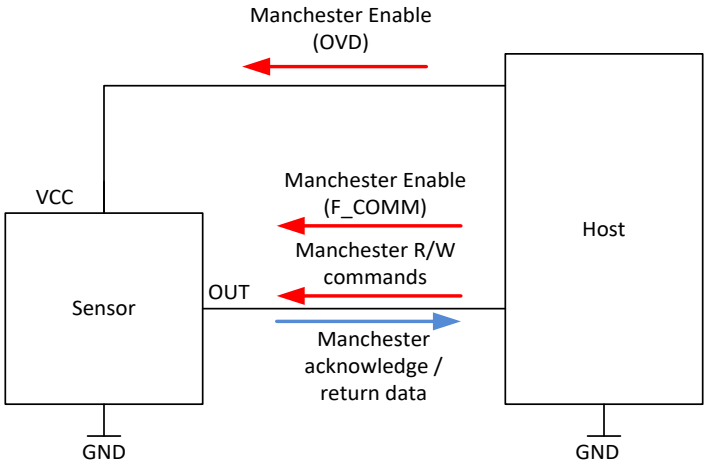

Figure 26: Manchester Communication Block Diagram

Settings Controlling the Manchester Communication

It is possible to limit access to the device by programming certain options detailed in Table 24.

Table 24: MANCH_ACCESS_SEL Behavior

MANCH_ ACCESS_SEL	Overvoltage Detection	Trigger	Description
00 (default)	Enabled	Enabled	Communication is enabled by either option.
01	Enabled	Disabled	Communication is enabled only by overvoltage detection.
10	Disabled	Enabled	Communication is enabled only by external trigger on output line.
11	Disabled	Disabled	Communication is locked.

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SERIAL INTERFACE MESSAGE STRUCTURE

The general format of a command message frame is shown in Figure 27. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary. The time period for the bit boundary is determined by the baud rate initiated by the external controller. The A31316 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 25.

- For a write access command frame, the data consists of 16 bits.
- For a read request frame, the data bits are omitted.
- For a read acknowledge or write frame, the data bits are defined as shown in Figure 27, where bit 0 is the LSB.

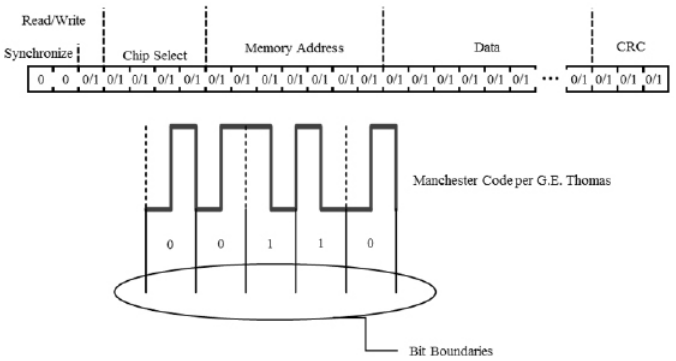

Figure 27: Manchester Bit-Stream Definition

Table 25: Manchester Bit Definition (host commands)

Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a Manchester command and communication bit time
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
2	Chip Select	–	Chip select for up to two dies connected in parallel:
		01	[As required] Device communication address 0
		10	[As required] Device communication address 1
		00/11	[As required] Broadcast 00 can be used as default if only one device is connected
8	Address	Any	Register address for read or write
32 (write command) 0 (read command)	Data	Any	32 data bits (write command) 0 bits (read command)
3	CRC	Any	Bits to check the validity of frame

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During a read command, the device determines the baud rate from the sync bits and responds with a read response frame using the same baud rate detected. The baud rate during a write command is also automatically detected, but is only used for decoding, because the A31316 does not respond to write commands.

Table 26: Manchester Bit Definition (Device Response)

Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to announce the beginning of a Manchester interface response
32	Data	Any	Read data
3	CRC	Any	Bits to check the validity of frame.

The device memory contains nonvolatile (EEPROM) and volatile registers, which are accessible via the serial interface through Manchester communication modes. The memory address space is divided into factory and customer areas.

MANCHESTER UNLOCKING—VIA OVD

1. At any time after POR, create an OVD condition. This sets the OUT in a high-impedance (high-Z)state because the PWM/SENT output is turned off.
2. Send the correct access code.
3. Device is unlocked.
4. If *MANCH_EN* bit was set low, the OVD condition can be removed and the device returned to PWM/SENT mode, with the device unlocked. OVD is needed for every Manchester read/write command.
5. If *MANCH_EN* bit was set high, the OVD condition can be removed, but the device remains in communication mode. OVD is not needed for Manchester transactions until the *MANCH_EN* bit is set low through a write command. This action locks the device.

MANCHESTER UNLOCKING—VIA TRIGGERING PULSE

1. At any time after POR, create the trigger condition by driving the output low for a specific amount of time depending on the PWM (minimum of two full PWM messages) or SENT mode (minimum of 30 t_{tick}). Then release the line or drive it high to create a 0→1 condition.
2. The device is in communication mode and a 300 µs timeout starts.
3. Write the correct access code before the 300 µs expires. Timing requirements stop once the first sync bit is detected.
   - If the code is wrong or aborted, or if the code is an incorrect transaction, the part goes back to PWM/SENT mode. Retrying by starting at step 1 is possible.
   - If the code is correct, the device is unlocked and MANCH_EN bit is set to 1. The output is disabled, and the device remains unlocked until *MANCH_EN* is written to 0 through a manchester write.

Table 27: Unlock Code and Customer Access Codes

Command	Write Address	Write Data
Customer access code (Read access to factory) *MANCH_EN* = 1	0x86	0xC2D8E67B
Customer access code (Read access to factory) *MANCH_EN* = 0	0x86	0xC2D8E67A

Manchester Communication CRC

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check). The CRC algorithm is based on the polynomial shown in Equation 19, and the calculation is represented graphically in Figure 28. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.

Equation 19:

$$g(x) = x^3 + x + 1$$

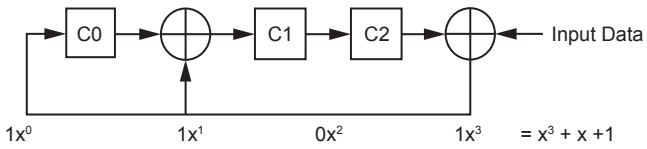

Figure 28: Manchester CRC Implementation

EEPROM Lock

There are three different lock modes available in the A31316: EELOCK, WRLOCK, and FLOCK. Each mode is separate from access lock, which requires a customer unlock code to control. EELOCK locks the EEPROM from external write access, while still allowing writes to shadow and volatile registers. The entirety of memory can still be read in this mode, allowing for a level of customer lock while maintaining debug support. WRLOCK prevents any write to EEPROM and volatile registers. Factory read support is maintained. This is not recommended for any

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output mode. The FLOCK mode locks out both reads and writes to EEPROM and all registers. This prevents any access by either customer or factory, removing available support options from the factory.

NOTE: When any of the EEPROM lock options are set, non-destructive factory debug support is limited.

Table 28: Serial Communication Lockout Modes

MEM_LOCK_SEL[3:0]	Lock Mode	Description
4'b0011	EELOCK	EEPROM Lock: Prevents writes to EEPROM but all volatile registers including shadow can be written. All registers and EEPROM can be read as typical.
4'b0110	WRLOCK	Write Lock: Prevents writing anything to either EEPROM or registers. Factory debug support is still available
4'b1100	FLOCK	Full Lock: Prevents writing and reading to any register in the device.

EEPROM Margin Checking

The A31316 contains a test mode, EEPROM margining, to check the logic levels of the EEPROM bits. The EEPROM margining is accessible with customer access. The EEPROM margining is selectable to check all logic 1, logic 0, or both. The results of the test are reported in EEPROM registers.

NOTE: A fail of the margin test does not force the output to a diagnostic state.

Error Flag Registers

The different error flags available in the A31316 are stored in the primary memory space of register 0xA4. If the error conditions are removed, all noncritical error flags are cleared on a read of this register or after being sent out through the output protocols. The register contents are provided in Table 29.

Table 29: Error Registers

Address	NAME	Access	Bit													
			31…13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xA3	ERROR	RO	0	OFE	SPE	EUE	OVD	UVD	ESE	POR	SRR	SLF	SAT	TSE	AOC	ACF

Analog Check Failure (ACF)

To ensure proper operation of the internal regulators, a voltage check is performed for the different reference sources for the analog and digital circuitry as well as for the Hall-element drivers. If any of these voltages deviate such that the accuracy of the part is in question, the ACF flag becomes set and the device enters a state as defined in Table 32. If the voltages are detected to recover, a read of the device register or reporting through the output modes clears the error flag so typical operation can resume. The ACF flag can be disabled by setting *ACF_MASK* bit in EEPROM.

Angle Outside Clamp (AOC)

If the upper and lower clamps are set within the operating range of the device, the AOC flag can be set as shown in Table 32 to indicate the signal reaching this clamp value. If the signal moves back within the range defined by *ANG_CLAMP_HIGH* and *ANG_CLAMP_LOW* as described in the Output Clamps section, the AOC flag can be removed by a read of the device register or through reporting in the applicable output protocol. If the flag is not desired, the EEPROM bit *AOC_MASK* can be set. The AOC error is updated with every angle update. However, the error may be suppressed for up to 16 t_{update} based on the *FAULT_FILT* EEPROM setting.

Temperature Error (TSE)

The TSE flag is set if the temperature sensor output saturates high, which indicates the ambient temperature is greater than 175.138°C or if the measured temperature is less than −54.963°C. If any of these conditions occur, the TSE flag becomes set, and the device enters a state as defined in Table 32. If the temperature is detected to recover, a read of the device register or reporting through the output modes clears the error flag so typical operation can resume. The TSE flag can be disabled by setting *TSE_MASK* bit in EEPROM. The TSE error is detected every nominal 1.5 ms and reaches the output after 1.62 ms.

Saturation Flag (SAT)

The saturation flag is provided to warn the user if the magnetic signal is outside of the detectable range of the signal path. A saturation can occur:

- In the ADC and filters, which indicates a front-end gain that is too large for the detected field, or
- A digital signal path saturation, which indicates that a gain setting is too large.

If either of these conditions occur, the SAT flag becomes set as defined in Table 32. If the saturation condition is removed,

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the error flag can be cleared by a read of the device register or through reporting in the applicable output protocol.

Overall, the SAT flag is constructed as follows:

- SAT can be caused by saturation at multiple points of the signal path. Each point is lumped in with a sub-flag that can be individually masked to customize the saturation detection flag. Provided in order of the signal path, the individual sub-flags are: SAT_FILT, SAT_CHAN, SAT_COR, and SAT_LIN. Alternatively, if saturation detection is not required, the entire SAT error can be masked by the setting *SAT_MASK* = 1.
  - □ SAT_FILT is set when saturation occurs in the ACD or low-pass filter. This sub-flag can be disabled by the setting *SAT_FILT_MASK* = 1. Possible causes are:
    - ◦ Excessively high input field on the device.
    - ◦ Digital or analog error in the ADC or filter circuitry.
  - □ SAT_CHAN is saturation caused by the one-dimensional (1D) offset/gain corrections of channel A/B. This sub-flag can be disabled by the setting *SAT_CHAN_MASK* = 1. Possible causes are:
    - ◦ Excessively high input field on the device.
    - ◦ Digital error in the factory or customer 1D trims.
    - ◦ Customer 1D trim is set incorrectly for the input field used.
  - □ SAT_COR is set when saturation would otherwise occur within the angle offset and gain corrections. This sub-flag can be disabled by the setting *SAT_COR_MASK* = 1. Possible causes are:
    - ◦ Output value of pre-gain offset is outside of the *ANG_THRESH_LOW/ANG_THRESH_HIGH* limits. This check is only performed if the *ANG_THRESH_EN* bit is set.
    - ◦ Output value of angle gain is outside of the signal-path range. This check is only performed if *ANG_GAIN_SAT_EN* is set. Otherwise, the output rolls over to a valid output.
    - ◦ Output value of the post-gain offset is outside of the signal-path range. This check is only performed if the *ANG_OFFS_SAT_EN* bit is set.
  - □ SAT_LIN is set when the output of linearization would otherwise cause saturation. This sub-flag can be disabled by S*AT_LIN_MASK* = 1. Possible causes are:
    - ◦ Linearization correction applies a correction that results in a value beyond the range.

The SAT error is updated with every angle update. However, the error can be suppressed for up to 16 t_{update} based on the *FAULT_FILT* EEPROM setting.

Oscillator Frequency Error (OFE)

The A31316 contains a low-frequency oscillator to act as a watchdog of the main oscillator. If these two oscillators deviate beyond the comparison threshold (20%), the device enters a state as defined in Table 32. This error is considered critical and cannot be cleared by any action other than a device reset (POR). To mask OFE errors, the *OFE_MASK* bit can be set. It is not recommended to set this bit for typical operation; this bit is provided for debugging purposes. The OFE error detection starts every 10 t_{update}.

Signal Processing Logic Failure (SLF)

To help check the main signal-path logic in the device during operation, a set of known inputs is run periodically through key parts of the data path and compared to known outputs. This allows the user to have confidence in the accuracy of the digital signal path without the need to run the LBIST, which would interrupt device operation. Additionally, a watchdog checks that the output angle is updated at the expected delay after the input signals are available. If test outputs show unexpected results or if there is a missed watchdog timer, the SLF flag becomes set, as shown in Table 32. If the error condition is removed, the error flag can be cleared by a read of the device register or by reporting through the output modes so typical operation can resume. The SLF error is determined every 10 t_{update}.

Signal Radius Out of Range (SRR)

The A31316 has an internal check of the two dimensions that are used to calculate angle (called sine and cosine) by calculating the radius and comparing it to user-defined diagnostic boundaries. These boundaries are set by the *MAGNETIC_THRESH_MIN* and *MAGNETIC_THRESH_MAX* EEPROM parameters. The condition for no error is calculated by:

Equation 20:

$$MAGNETIC\_THRESH\_MIN^2 < RADIUS\_SQ\_17B < MAGNETIC\_THRESH\_MAX^2,$$

where:

$$RADIUS\_SQ\_17B = ([CHAN\_A\_16B/128])^2 + ([CHAN\_B\_16B/128])^2$$

The brackets [*x*] denote the floor function, which rounds x down to the nearest integer. The current value of *RADIUS_OUT_SQ_17B* can be read directly from the appropriate register.

The SRR check helps ensure the accuracy of the ATAN2 by the assumption that the magnitude of the two dimensions remains constant over the complete rotation. This is only true in rotary applications. If the magnetic field is outside of the threshold boundaries *MAGNETIC_THRESH_MIN* and *MAGNETIC_*

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THRESH_MAX, the SRR flag becomes set, as shown in Table 32. If the error condition is removed, the error flag can be cleared by a read of the device register or reporting through the output modes so typical operation can resume. The SRR flag can be disabled by setting the *SRR_MASK* bit in EEPROM. The SRR error is updated with every angle update. However, the error can be suppressed for up to 16 t_{update} based on the *FAULT_FILT* EEPROM setting.

Power-On Reset (POR)

To indicate a power-on reset event occurred, the POR error flag becomes set on startup. In the event of a reset, the filters and signal path require time to settle, and this error flag becomes set to help indicate this state in the event the reset was unintentional. This flag is reported as shown in Table 32. Once the first angle update is available, a read of the device register, or reporting through the output modes clears the POR flag so typical operation can resume. The POR flag can be disabled by setting the *POR_MASK* bit in EEPROM.

The first output message (SENT) or first output cycle (PWM) reports the POR error, unless POR is masked.

POR error may be prolonged in PWM mode to suppress filter initialization from showing on the output. For more information, refer to the Sensor Output During Low-Pass Filter Initialization section

EEPROM Multiple-Bit Error (EUE) and EEPROM Single-Bit Error (ESE)

The A31316 contains EEPROM with error checking and correction codes, ECC, that provide correction of any single EEPROM bit error without effecting device performance. The ECC also detects multiple-bit EEPROM errors and triggers an internal fault signal, at which point the device enters a state as defined in Table 32. An EEPROM multi-bit error is considered critical and cannot be cleared by any action other than a device reset (POR). The EEPROM error indication bits containing the single-bit error is cleared after a read. A single-bit error does not affect the device output because it is corrected; however, it may indicate deteriorating performance of the EEPROM and should be monitored. The ESE flag can be disabled by setting the *ESE_MASK* bit in EEPROM. The EUE flag cannot be disabled. The EUE and ESE flags can only be set on EEPROM read, which occurs only at POR.

Shadow Parity Error (SPE)

Upon power up of the A31316, the EEPROM parameters are loaded into fast-access shadow registers for use in operation. These registers have a simple parity structure to ensure proper loading of the EEPROM parameters. If a parity error is detected, the SPE error flag is set and the device enters a state as defined in Table 32. This error is considered critical and cannot be cleared by any action other than a device reset (POR). The SPE flag can be disabled by setting the *SPE_MASK* bit in EEPROM. The parity error is detected every 10 t_{update}.

Undervoltage Detection (UVD)

The A31316 contains circuitry to detect a condition when the supply voltage drops below the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{UVD(RISE)} - V_{UVD(FALL)}$. As an example, initially V_{CC} and OUT are within the typical operating range. If V_{CC} reduces below $V_{UVD(FALL)}$, OUT is forced to a state as defined in Table 32. When V_{CC} returns above $V_{UVD(RISE)}$, OUT returns to its typical operating state after a read of the device register or once the error is reported through the output mode. If V_{CC} reduces below the internal reset level, $V_{POR(FALL)}$, the output is forced to a high-impedance state. When V_{CC} returns above the rising reset level, $V_{POR(RISE)}$, the output responds with the POR flag if enabled.

Undervoltage detection is set to one of two configurable thresholds based on the EEPROM parameter *UVD_SEL* as shown in Table 30 and Figure 29.

Table 30: UVD_SEL Settings for V_{UVD}

UVD_SEL	$V_{UVD(RISE)}$	$V_{UVD(FALL)}$
0	$V_{UVD(LOW, RISE)}$	$V_{UVD(LOW, FALL)}$
1	$V_{UVD(HIGH, RISE)}$	$V_{UVD(HIGH, FALL)}$

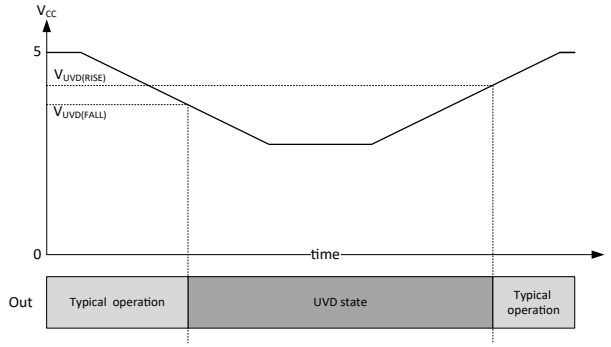

Figure 29: V_{CC} Low Threshold Levels

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Overvoltage Detection (OVD)

The A31316 contains circuitry to detect a condition when the supply voltage rises above the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{OVD(RISE)} - V_{OVD(FALL)}$. As an example, Initially, V_{CC} and OUT are within the typical operating range. If V_{CC} rises above $V_{OVD(RISE)}$, OUT is forced to a state as defined in Table 32. When V_{CC} returns below $V_{OVD(FALL)}$, OUT returns to its typical operating state after a read of the device register or reporting through the output mode. If the device is in SENT/PWM or analog output modes, and the EEPROM lock options are not set, the device enters programming mode and the output is always forced to a high-impedance state when V_{CC} increases above $V_{OVD(RISE)}$. The overvoltage detection is only enabled if the EEPROM lock options are set; otherwise, the device is in programming mode (Manchester communication on the OUT pin).

Overvoltage detection is set to one of two configurable thresholds based on the EEPROM parameter OVD_SEL as shown in Figure 30 and Table 31.

Table 31: OVD_SEL Settings for V_{OVD}

OVD_SEL	$V_{OVD(RISE)}$	$V_{UVD(FALL)}$
0	$V_{OVD(HIGH, RISE)}$	$V_{OVD(HIGH, FALL)}$
1	$V_{OVD(LOW, RISE)}$	$V_{OVD(LOW, FALL)}$

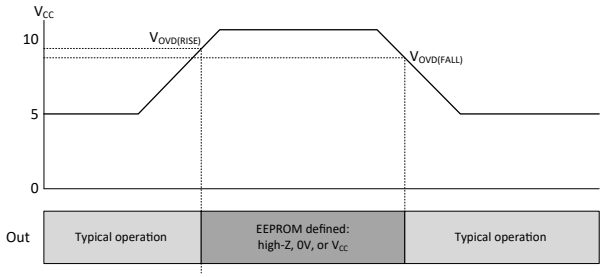

Figure 30: OVD Threshold Levels

SENT Output Error Reporting

In SENT mode, there are four ways to report error flags: 1) the SCN status bits [1:0]; 2) the slow serial message; and the extended data options that include 3) a rotating reporting of error registers or 4) entering a high-impedance output state when an error condition occurs. The SCN status bits [1:0] are broken up based on the likelihood that the cause of the error is internal or external. When any error flag is set, these status bits become set until a clear condition occurs. The clear condition can be a read of the ERR register or the inclusion of a SENT message with the SCN bit-set. The SENT message clears the error flag from the ERR register. If either of the SCN status bits are set, an error condition occurred some time after the previous SENT message was received; therefore, the data should not be trusted. The bits are constructed as follows:

SCN[0] = SLF | SRR | ACF | TSE | POR (For information about POR bit-setting during filter initialization, see the Sensor Output During Low-Pass Filter Initialization section.)

SCN[1] = UVD | OVD | SAT | AOC

The serial message requires successive SENT messages to be received. The error flags that are sent in this method are taken from an internal register that is not cleared during typical conditions to allow typical operation for other interfaces. After the error bits are sent out from the slow serial message, the register is cleared.

The third reporting method is through the optional extended diagnostic nibbles in *SENT_DATA_SEL* options 2, 8, or 13. This method sends the *DIAG_BYTE* error flags in every SENT message. The error flags for this method are taken from an internal copy of the error registers to allow the error register to be cleared separately. The bits are sent out as shown in Table 32.

NOTE: Overvoltage and undervoltage are reported through the same bit.

If transmission of a specific error flag is not desired, the EEPROM parameter *DIG_OUT_ERR_RESP_SEL* can be set to put the output in a high-impedance state when an error condition occurs. If the error condition is removed, the output returns to typical operation. This option prevents the device from transmitting any data through the SENT mode; however, Manchester communication remains possible.

PWM Output Error Reporting

When in PWM output mode, the error flags are reported by sending out a specific diagnostic message format. The format consists of setting the carrier frequency to half of the configured setting and sending a specific duty cycle as defined in Table 32. In the event of more than one error occurring, the higher-priority message is sent. If two error conditions occur and clear at the same time, only one error flag is shown. Table 32 is listed in descending order in terms of priority.

If transmission of a specific error flag is not desired, the EEPROM parameter *DIG_OUT_ERR_RESP_SEL* can be set to put the output in a high-impedance state when an error condition occurs. If the error condition is removed, the output returns to typical operation. This option prevents the device from transmitting any data through the PWM mode; however, Manchester communication remains possible. If using half-frequency error reporting with the trigger-pulse Manchester method, the trigger must cover two full periods of the new frequency.

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Broken-Wire Detection

The A31316 contains circuitry to detect a condition when the ground or supply connection is disconnected. If the GND connection is broken, the output is at $V_{SAT(DIAG, HIGH)}$. If the V_{CC} connection is broken, the output is at $V_{SAT(DIAG, LOW)}$.

Logic Built-In Self-Test (LBIST)

It is possible to test the logic of the sensor using a built-in self-test. This self-test runs quasi-random signals though a scan chain connection of the digital logic. A checksum is calculated by the sensor and compared to the value of a known-good checksum.

The user can start the self-test by unlocking the part (see the Programming Protocol section) and writing 1 to the *BIST_START*. The self-test typically takes 200 ms to complete. While LBIST is running, communication is not possible.

After LBIST is complete:

- *LBIST_STATUS* is set to 1, regardless of the test result.
- *LBIST_RESULT* is set to 1 if the test was successful.
- The checksum can be read out be reading *LBIST_RESULT_SIGNATURE*. This is not necessary to judge the test result. The correct checksum is 0x556E4F7D.

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Table 32: Device Error Flag Responses

Error Flag	ERR Register (Bit)	Meaning	Analog / PWM Error Priority	SENT Response ERR_RESP_SEL = 0	PWM Response ERR_RESP_SEL = 0	SENT/PWM Response ERR_RESP_SEL = 1
OFE	ERR[12]	Oscillator Frequency Error	1 (highest)	High Impedance	High Impedance	High Impedance
EUE	ERR[10]	EEPROM Multiple-Bit Error	2	High Impedance	High Impedance	High Impedance
SPE	ERR[11]	Shadow Parity Error	3	High Impedance	High Impedance	High Impedance
SLF	ERR[4]	Signal Processing Logic Failure	5	SCN[0] = 1 DIAG_BYTE[0] = 1	½ Frequency 10% Duty Cycle	High Impedance [*4]
SRR	ERR[5]	Signal Radius Out of Range	6	SCN[0] = 1 DIAG_BYTE[1] = 1	½ Frequency 20% Duty Cycle	High Impedance [*4]
ACF	ERR[0]	Voltage Check Failure	7	SCN[0] = 1 DIAG_BYTE[2] = 1	½ Frequency 30% Duty Cycle	High Impedance [*4]
TSE	ERR[2]	Temperature Error	8	SCN[0] = 1 DIAG_BYTE[3] = 1	½ Frequency 40% Duty Cycle	High Impedance [*4]
POR	ERR[6]	Power-On Reset	9	SCN[0] = 1 [*6] DIAG_BYTE[4] = 1	½ Frequency 50% Duty Cycle [*6]	High Impedance [*4]
UVD	ERR[8]	Undervoltage Detection	10	High Impedance, or High, or Low, depending on ERR_RESP_SEL_UV and SENT reset [*2] and SCN[1] = 1 [*3] and DIAG_BYTE[5] = 1 [*5]	High Impedance, or High, or Low, depending on ERR_RESP_SEL_UV and ½ Frequency 60% Duty Cycle [*3]	Same as with ERR_RESP_SEL = 0
OVD [*1]	ERR[9]	Overvoltage Detection	11	SCN[1] = 1 DIAG_BYTE[5] = 1	½ Frequency 70% Duty Cycle	High Impedance [*4]
SAT	ERR[3]	Saturation Flag	12	SCN[1] = 1 DIAG_BYTE[6] = 1	½ Frequency 80% Duty Cycle	High Impedance [*4]
AOC	ERR[1]	Angle Outside Clamp	13	SCN[1] = 1 DIAG_BYTE[7] = 1	½ Frequency 90% Duty Cycle	High Impedance [*4]
ESE	ERR[7]	EEPROM Single-Bit Error	14 (lowest)	None	None	High Impedance [*4]

[*1] OVD causes the device to enter high impedance if *MANCH_ACCESS_SEL* = 2'b0X.
[*2] SENT interface restarts after coming out of the UVD reporting, starting with message counter = 0 (if enabled) and the first serial message (if enabled).
[*3] At the first frame and potentially further frames transmitted after UVD condition is released, depending on *ERR_MIN* setting.
[*4] The error is included in the next enhanced message to start after the current enhanced message finishes
[*5] At the first frame after UVD condition is released.
[*6] POR status on PWM output, and SCN[0] = 1 status can also be caused by filter initialization reporting. See the Sensor Output During Low-Pass Filter Initialization section.

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DIAGNOSTIC SETTING AND CLEARING

Diagnostic bits are set internally as soon as an error is detected and are sent out whenever the protocol allows it. In PWM, this is at the start of the next PWM cycle. In SENT, this is at the creation of the next SENT frame. For SENT serial messages, this is at the creation of the next serial message.

In both SENT and PWM mode, most errors are cleared when they no longer occur. A few errors that are considered critical do not clear themselves; these errors require a POR event before the device returns to typical operation. These errors are: OFE, EUE, and SPE.

All errors are guaranteed to output at least once. This means that, if an error condition occurs but is cleared before the next output reporting, the error flag is still be reported. For example, if the angle exceeds the clamp value in the middle of a PWM period or SENT message but returns to a valid angle before the start of the next PWM period or SENT message, that next period or message still reports the AOC error, even though the angle is not currently outside of the clamp. This ensures that an error condition is not lost during the operation.

MEMORY ACCESS

The A31316 utilizes a primary-only memory structure to allow fast communication. The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing a write to the shadow addresses, or by reprogramming the corresponding EEPROM fields and power cycling the IC. Use of shadow memory is substantially faster than accessing EEPROM. In situations where many parameters need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register and return 0 when read. Shadow registers do not contain the ECC bits. All EEPROM and shadow locations may be read after customer unlock.

The device does not answer Manchester read commands from registers that do not exist or registers that only contain “write-only” bits.

Shadow Memory Read and Write Transactions

Shadow memory read and write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM addresses, one must address to the shadow addresses, which are located at an offset of 0x40 above the EEPROM.

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Table 33: Register Description—Volatile

Volatile Address (hex)	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Volatile Address (hex)
0x83																			EE_MARGIN_LOOP	EE_MARGIN_TEST_ADDR						EE_MARGIN_TEST_ADDR_EN	EE_MARGIN_RESULT	EE_MARGIN_STATUS		EE_MARGIN_MIN_DIS	EE_MARGIN_MAX_DIS	EE_MARGIN_START	0x83
0x85																											LBIST_RESULT	LBIST_STATUS					0x85
0x86																															MEMORY_ACCESS		0x86
0xA0																									MANCH_EN							LBIST_START	0xA0
0xA1	LBIST_RESULT_SIGNATURE																																0xA1
0xA2																																SOFTWARE_RESET	0xA2
0xA3																				OFE	SPE	EUE	OVD	UVD	ESE	POR	SRR	SLF	SAT	TSE	AOC	ACF	0xA3
0xA7	TEMPERATURE_16B																ANGLE_16B																0xA7
0xA8	CHAN_B_16B																CHAN_A_16B																0xA8
0xA9	CHAN_B_PRE_16B																CHAN_A_PRE_16B																0xA9
0xAA																RADIUS_SQ_17B																	0xAA

The locations of all useful volatile registers are shown in Table 33. Most volatile registers are read-only and are meant to provide data about the internal functions of the device.

Other unmarked registers may contain data used for internal purposes; only registers useful for external interfacing are shown. When writing to volatile registers, all unlabeled bits should be set to 0.

Volatile 0x83

EE_MARGIN_LOOP (BITS 13) R/W (READ AND WRITE)

If set, the margin testing continuously tests the register in *EE_MARGIN_TEST_ADDR*.

EE_MARGIN_TEST_ADDR (BITS 12:7) R/W

If the margin testing fails, this register contains the address of the register that failed. If multiple registers fail, this contains the address of the most recent failed register (highest register). If *EE_MARGIN_TEST_ADDR_EN* is set to 1, this address can be written to and used as the starting address for margin testing.

EE_MARGIN_TEST_ADDR_EN (BIT 6) R/W

Determines if a custom starting address is used or if the default starting address is used.

- If *EE_MARGIN_TEST_ADDR_EN* = 0
  Margin testing begins at address 0
- If *EE_MARGIN_TEST_ADDR_EN* = 1
  Margin testing begins at the address contained in *EE_MARGIN_TEST_ADDR*

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EE_MARGIN_RESULT (BIT 5) RO (READ ONLY)

Indicates which limit the margin failed. When the margin testing fails, this bit is set based on the fail condition.

- If *EE_MARGIN_RESULT* = 0: Lower margin failed
- If *EE_MARGIN_RESULT* = 1: Upper margin failed

EE_MARGIN_STATUS (BITS 4:3) RO

Indicates the current status of margin testing.

- If *EE_MARGIN_STATUS* = 00: Test has not been run
- If *EE_MARGIN_STATUS* = 01: Test passed
- If *EE_MARGIN_STATUS* = 10: Test failed
- If *EE_MARGIN_STATUS* = 11: Test is currently running

EE_MARGIN_MIN_DIS (BIT 2) R/W

Determines if the low-margin testing is performed or skipped.

- If *EE_MARGIN_MIN_DIS* = 0: Lower-margin testing is performed when margin testing is run
- If *EE_MARGIN_MIN_DIS* = 1: Lower-margin testing is not performed when margin testing is run

EE_MARGIN_MAX_DIS (BIT 1) R/W

Determines if the high-margin testing is performed or skipped.

- If *EE_MARGIN_MAX_DIS* = 0: Upper-margin testing is performed when margin testing is run
- If *EE_MARGIN_MAX_DIS* = 1: Upper-margin testing is not performed when margin testing is run

EE_MARGIN_START (BIT 0) R/W

Write to 1 to begin the margin testing. This bit self-clears when the margin testing finishes. If cleared during testing, the test ends prematurely.

Volatile 0x85

LBIST_RESULT (BIT 5) RO

Indicates whether LBIST passed or failed.

- If *LBIST_RESULT* = 0: LBIST test failed
- If *LBIST_RESULT* = 1: LBIST test passed

LBIST_STATUS (BIT 4) RO

Indicates when BIST test is finished.

- If *LBIST_STATUS* = 0: BIST is not finished or not started
- If *LBIST_STATUS* = 1: BIST has finished and LBIST_RESULT contains valid results

Volatile 0x86

MEMORY_ACCESS (BIT 1) RO

Set to 1 when access code is successfully sent.

Volatile 0xA0

MANCH_EN (BIT 7) R/W

Disables the current device output and forces Manchester interface to be active.

- If *MANCH_EN* = 0: Device is in typical operation mode and outputs data based on EEPROM settings
- If *MANCH_EN* = 1: Device output is in the high-Z mode, and Manchester is active and waiting for commands

Volatile 0xA1

LBIST_START (BITS 32:0) RO

Contains the calculated LBIST signature. This is internally compared to the expected value to determine if there are any internal logic failures.

Volatile 0xA3

OFE (BIT: 12) RO

Indicates when the oscillator frequency error has occurred. This bit is NOT asserted if the flag is masked.

SPE (BIT: 11) RO

Indicates when the shadow parity error has occurred. This bit is NOT asserted if the flag is masked.

EUE (BIT: 10) RO

Indicates when the EEPROM uncorrectable error has occurred. This bit is NOT asserted if the flag is masked.

OVCC (BIT: 9) RO

Indicates when the OVD error has occurred. This bit is NOT asserted if the flag is masked.

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UVCC (BIT: 8) RO

Indicates when the UVD error has occurred. This bit is NOT asserted if the flag is masked.

ESE (BIT: 7) RO

Indicates when the EEPROM single-bit error has occurred. This bit is NOT asserted if the flag is masked.

POR (BIT: 6) RO

Indicates when a power-on reset has occurred. This bit is NOT asserted if the flag is masked.

SRR (BIT: 5) RO

Indicates when the signal radius is out of range. This bit is NOT asserted if the flag is masked.

SLF (BIT: 4) RO

Indicates when an error is detected in the signal-path logic. This bit is NOT asserted if the flag is masked.

SAT (BIT: 3) RO

Indicates when saturation occurs within the signal path. This bit is NOT asserted if the flag is masked.

TSE (BIT: 2) RO

Indicates when the temperature sensor is either in error or out of range. This bit is NOT asserted if the flag is masked.

AOC (BIT: 1) RO

Indicates when the angle is outside of the clamped region. This bit is NOT asserted if the flag is masked.

ACF (BIT: 0) RO

Indicates when a failure has occurred on the internal analog checks. This bit is NOT asserted if the flag is masked.

Volatile 0xA7

TEMPERATURE_16B (BITS: 31:16) RO

Contains the digital readout of the temperature sensor. This value is provided in 2's complement. Conversion to degrees can be performed using:

$$Temperature\ [°C] = (TEMPERATURE\_16B) / 128 + 25°$$

ANGLE_16B (BITS: 15:0) RO

The calculated angle after all trimming and compensation. Conversion to degrees can be performed using:

$$Angle\ [Deg] = ANGLE\_16B \times (360°)/2^{16}$$

Volatile 0xA8

CHAN_B_16B (BITS: 31:16) RO

Final output of channel B after customer-trimmed compensation. This value is directly input to the CORDIC calculation.

CHAN_A_16B (BITS: 15:0) RO

Final output of channel A after customer-trimmed compensation. This value is directly input to the CORDIC calculation.

Volatile 0xA9

CHAN_B_PRE_16B (BITS: 31:16) RO

Customer-trimmed output of channel B before the hysteresis filter.

CHAN_A_PRE_16B (BITS: 15:0) RO

Customer-trimmed output of channel A before the hysteresis filter.

Volatile 0xAA

RADIUS_SQ_17B (BITS: 16:0) RO

The squared radius as calculated internally. This value is used to determine if the signal radius is out of range for the SSR flag.

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Table 34: Register Description—EEPROM and Shadow

EEPROM Address (hex)	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	EEPROM Address (hex)	Shadow Address (hex)
0x05	ECC			DIG_OUT_DRIVE_SEL	CHAN_B_HYSTERESIS										CHAN_A_HYSTERESIS													0x05	0x45
0x15	ECC											SPARE_0X15			CHAN_ORTHOG											CHAN_B_DIS	CHAN_A_DIS	0x15	0x55
0x16	ECC										ANG_THRESH_HIGH				ANG_THRESH_LOW												ANG_THRESH_EN	0x16	0x56
0x17	ECC												CHAN_A_POL	CHAN_A_OFFS														0x17	0x57
0x18	ECC			CHAN_A_OFFS_TC1_HOT												CHAN_A_OFFS_TC1_COLD												0x18	0x58
0x19	ECC													CHAN_A_SENS														0x19	0x59
0x1A	ECC					CHAN_A_SENS_TC1_HOT										CHAN_A_SENS_TC1_COLD													0x1A	0x5A
0x1B	ECC							CHAN_A_SENS_TC2_HOT										CHAN_A_SENS_TC2_COLD										0x1B	0x5B
0x1C	ECC												CHAN_B_POL	CHAN_B_OFFS														0x1C	0x5C
0x1D	ECC			CHAN_B_OFFS_TC1_HOT												CHAN_B_OFFS_TC1_COLD												0x1D	0x5D
0x1E	ECC													CHAN_B_SENS														0x1E	0x5E
0x1F	ECC					CHAN_B_SENS_TC1_HOT										CHAN_B_OFFS_TC1_HOT													0x1F	0x5F
0x20	ECC		TEMPERATURE_OFFS					CHAN_B_SENS_TC2_HOT										CHAN_B_SENS_TC2_COLD										0x20	0x60
0x21	ECC			LIN_COEFF_0											SPARE_0X21	LIN_COEFF_ACTIVE							LIN_COEFF_SCALAR		LIN_SEL		LIN_ENABLE	0x21	0x61
–	ECC			–											–													–	–
0x31	ECC			LIN_COEFF_32											LIN_COEFF_31													0x31	0x71
0x32	ECC										ANG_PRE_GAIN_OFFS														CORDIC_BYPASS	CORDIC_CHAN_ORDER	CORDIC_POL	0x32	0x72
0x33	ECC				BIN_HYST							ANG_GAIN																0x33	0x73
0x34	ECC			ANG_SAT_ROLLOVER						ANG_GAIN_SAT_EN	ANG_POST_GAIN_OFFS																	ANG_OFFS_SAT_EN	0x34	0x74
0x35	ECC										MAGNETIC_THRESH_MAX							MAGNETIC_THRESH_MAX_EN	MAGNETIC_THRESH_MIN								MAGNETIC_THRESH_MIN_EN	0x35	0x75
0x36	ECC											ANG_CLAMP_LOWER																0x36	0x76
0x37	ECC		BW_ADAPT_MAX			BW_ADAPT_MIN				BW_SEL		ANG_CLAMP_UPPER																0x37	0x77

Continued on next page...

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Table 34: Register Description—EEPROM and Shadow (continued)

EEPROM Address (hex)	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	EEPROM Address (hex)	Shadow Address (hex)
0x38	ECC						POWER_ON_DELAY			BW_ADAPT_DELAY										BW_ADAPT_EXP				BW_ADAPT_FRAC				0x38	0x78
0x39	ECC			SENT_FRAME_RATE		SENT_INIT_SEL				SENT_ENCODING_SEL	SENT_CRC_SEL	SENT_EMSG_DIS	DIG_OUT_PULL_LIM_DIS	DIG_OUT_PULL_LIM		DIG_OUT_DATA_RATE				SENT_DATA_SEL				DIG_COMM_ID	DIG_OUT_SEL		0x39	0x79
0x3A	ECC					SENT_EMSG_ERR_REPEAT	SENT_EMSG_SEL																					0x3A	0x7A
0x3B	ECC	ENHANCED_SETTINGS_UNLOCK		DIG_OUT_PUSH_LIM		DIG_OUT_PUSH_LIM_SEL	SAT_CHAN_MASK		SAT_FILT_MASK	SAT_COR_MASK	SAT_LIN_MASK	ACF_FAULT_FILT	FAULT_FILT			OVD_MASK	UVD_MASK	SPE_MASK	ESE_MASK	POR_MASK	SRR_MASK	SLF_MASK	OFE_MASK	SAT_MASK	TSE_MASK	AOC_MASK	ACF_MASK	0x3B	0x7B
0x3C	ECC		MEM_LOCK_SEL				MANCH_ACCESS_SEL		TEST_MODE_DIS	OVD_SEL	UVD_SEL	SPARE_0X3C				ERR_RESP_SEL_OV		ERR_RESP_SEL		ERR_RESP_SEL_UV		ERR_HOLD_SEL				DIG_COMM_INPUT_HIGH	DIG_COMM_INPUT_LOW	0x3C	0x7C
0x3D	ECC	SPARE_0X3D																										0x3D	0x7D
0x3E	ECC	SPARE_0X3E																										0x3E	0x7E
0x3F	ECC	SPARE_0X3F																										0x3F	0x7F

The locations of all customer-accessible EEPROM registers are shown in Table 34. Additionally, shadow registers are mirrored in volatile space to allow quick access to the values during operation. All shadow registers are located at an address 0x40 higher than the EEPROM register of which it is a copy. The shadow registers are written with copies of the data from EEPROM at power-up and when an EEPROM write is performed. Values that are manually written to shadow take effect immediately and persist until they are reset either by changing the shadow register itself, changing the EEPROM register, or power-cycling the device. This allows quick testing of parameters with no risk of permanently changing the device performance. It also reduces the number of EEPROM write transactions required during testing, which can improve test time because EEPROM write transactions take longer than shadow write transactions.

For all EEPROM and shadow registers, the first 6 most significant bits [31:26] are dedicated to ECC bits. These are used for internal testing to allow the device to correct single-bit disturbances and detect double-bit disturbances when copying EEPROM into shadow. When performing an EEPROM/shadow write transaction, there is no need to manually calculate the ECC bits. The ECC bits are ignored and replaced with the internally calculated values. During an EEPROM/shadow read transaction, the ECC bits are transmitted along with the rest of the register data and may be ignored.

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EEPROM 0x05/Shadow 0x45

DIG_OUT_DRIVE_SEL (BIT 23)

Selects the digital output driver mode.

- If *DIG_OUT_DRIVE_SEL* = 0, the digital output driver functions as a push-pull output.
- If *DIG_OUT_DRIVE_SEL* = 1, the digital output driver functions as an open-drain output.

CHAN_B_HYST (BITS 22:13)

Selects the amount of hysteresis present on channel B of the 1D signal path. This value directly selects the number of LSBs of hysteresis applied to each channel at a 1:1 ratio.

CHAN_A_HYST (BITS 12:3)

Selects the amount of hysteresis present on channel A of the 1D signal path. This value directly selects the number of LSBs of hysteresis applied to each channel at a 1:1 ratio.

EEPROM 0x15/Shadow 0x55

EEPROM 0x15 can be factory- or customer-accessible, based on the bit *ENHANCED_SETTINGS_UNLOCK*. When *ENHANCED_SETTINGS_UNLOCK* = 0, EEPROM 0x15 is considered factory space and cannot be written to at customer level. This can be used to prevent accidental changes to this value.

SPARE_0X15 (BITS 15:11)

Spare bits that can be used as nonvolatile storage within the device. This register has no effect on device performance.

CHAN_ORTHOG (BITS 10:2)

CHAN_ORTHOG determines the phase correction that is applied to channel B for the purposes of removing orthogonality error.

CHAN_B_DIS (BIT 1)

Disables channel B when set.

- If *CHAN_B_DIS* = 0, channel B operates normally.
- If *CHAN_B_DIS* = 1, channel B is disabled.

CHAN_A_DIS (BIT 0)

Disabled channel A when set.

- If *CHAN_A_DIS* = 0, channel A operates normally.
- If *CHAN_A_DIS* = 1, channel A is disabled.

EEPROM 0x16/Shadow 0x56

ANG_THRESH_HIGH (BITS 16:9)

Sets a high angle-saturation point before gain is applied to the channel. A diagnostic flag triggers if the angle recorded exceeds the programmed value. $\theta_{ANG\_THRESH\_HIGH}$ can be set between 0 and 360 degrees with 1.41-degree steps. Because the value into the comparison is rolled over to 0–360, an *ANG_THRESH_HIGH* value of 0 always results in an error flag, and an *ANG_THRESH_HIGH* value of 255 never results in an error flag.

ANG_THRESH_LOW (BITS 8:1)

Sets a low angle-saturation point before gain is applied to the channel. A diagnostic flag triggers if the angle recorded is less than the programmed value. $\theta_{ANG\_THRESH\_LOW}$ can be set between 0 and 360 degrees with 1.41 degree steps. Because the value into the comparison is rolled over to 0–360, an *ANG_THRESH_LOW* value of 0 never results in an error flag, and an *ANG_THRESH_LOW* value of 255 always results in an error flag.

ANG_THRESH_LOW/HIGH	Degrees
0	0
x	x × 1.41
255	359.55

ANG_THRESH_EN (BIT 0)

Enables the pre-gain saturation check.

- If *ANG_THRESH_EN* = 0, angle saturation check is disabled.
- If *ANG_THRESH_EN* = 1, angle value prior to gain block is compared to the programmed thresholds *ANG_THRESH_(LOW/HIGH)* to set the saturation diagnostic flag.

EEPROM 0x17/Shadow 0x57

CHAN_A_POL (BIT 14)

Changes the polarity of channel A when set.

- If *CHAN_A_POL* = 0, channel A follows axis definition.
- If *CHAN_A_POL* = 1, channel A polarity is inverted.

CHAN_A_OFFS (BITS 13:0)

Customer offset trim at room temperature for channel A.

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EEPROM 0x18/Shadow 0x58

CHAN_A_OFFS_TC1_HOT (BITS 23:12)

Customer first-order offset trim for room-to-hot slope of channel A.

CHAN_A_OFFS_TC1_COLD (BITS 11:0)

Customer first-order offset trim for room-to-cold slope of channel A.

EEPROM 0x19/Shadow 0x59

CHAN_A_SENS (BITS 13:0)

Customer sensitivity trim at room temperature for channel A.

EEPROM 0x1A/Shadow 0x5A

CHAN_A_SENS_TC1_HOT (BITS 21:11)

Customer first-order sensitivity trim for room-to-hot slope of channel A.

CHAN_A_SENS_TC1_COLD (BITS 10:0)

Customer first-order sensitivity trim for room-to-cold slope of channel A.

EEPROM 0x1B/Shadow 0x5B

CHAN_A_SENS_TC2_HOT (BITS 19:10)

Customer second-order sensitivity trim for room-to-hot slope of channel A.

CHAN_A_SENS_TC2_COLD (BITS 9:0)

Customer second-order sensitivity trim for room-to-cold slope of channel A.

EEPROM 0x1C/Shadow 0x5C

CHAN_B_POL (BIT 14)

Changes the polarity of channel B when set.

- If *CHAN_B_POL* = 0, channel B follows axis definition.
- If *CHAN_B_POL* = 1, channel B polarity is inverted.

CHAN_B_OFFS (BITS 13:0)

Customer offset trim at room temperature for channel B.

EEPROM 0x1D/Shadow 0x5D

CHAN_B_OFFS_TC1_HOT (BITS 23:12)

Customer first-order offset trim for room-to-hot slope of channel B.

CHAN_B_OFFS_TC1_COLD (BITS 11:0)

Customer first-order offset trim for room-to-cold slope of channel B.

EEPROM 0x1E/Shadow 0x5E

CHAN_B_SENS (BITS 13:0)

Customer sensitivity trim at room temperature for channel B.

EEPROM 0x1F/Shadow 0x5F

CHAN_B_SENS_TC1_HOT (BITS 21:11)

Customer first-order sensitivity trim for room-to-hot slope of channel B.

CHAN_B_SENS_TC1_COLD (BITS 10:0)

Customer first-order sensitivity trim for room-to-cold slope of channel B.

EEPROM 0x20/Shadow 0x60

TEMPERATURE_OFFS (BITS 24:20)

Customer temperature offset trim. Value is added to the temperature reported, represented in 2's complement format, step size is 0.5°C/LSB.

CHAN_B_SENS_TC2_HOT (BITS 21:11)

Customer second-order sensitivity trim for room-to-hot slope of channel B.

CHAN_B_SENS_TC2_COLD (BITS 10:0)

Customer second-order sensitivity trim for room-to-cold slope of channel B.

EEPROM 0x21/Shadow 0x61

LIN_COEFF_0 (BITS 25:13)

Linearization coefficient number 0. Functionality is based on linearization mode and scalar. For details, see the Linearization and Binning section.

SPARE_0X21 (BITS 12:10)

Spare bits that can be used as nonvolatile storage within the device. This register does not effect device performance.

LIN_COEFF_ACTIVE (BITS 9:5)

Determines the number of active linearization coefficients. For details, see the Linearization and Binning section.

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LIN_COEFF_SCALAR (BITS 4:3)

Determines what scalar quantity is applied to the *LIN_COEFF_X* values. For details, see the Linearization and Binning section.

LIN_SEL (BITS 2:1)

Determines what function the linearization block performs on the signal path.

LIN_ENABLE (BIT 0)

Enables the linearization block when set.

- If *LIN_ENABLE* = 0, linearization is disabled and all related registers have no effect on device operation.
- If *LIN_ENABLE* = 1, linearization is enabled and the device functions based on the linearization settings.

EEPROM 0x22/Shadow 0x62

LIN_COEFF_2 (BITS 25:13)

Linearization coefficient number 2. Functionality is based on linearization mode and scalar. For details, see the Linearization and Binning section..

LIN_COEFF_1 (BITS 12:0)

Linearization coefficient number 1. Functionality is based on linearization mode and scalar. For details, see the Linearization and Binning section.

EEPROM 0x23:0x31/Shadow 0x63:0x71

LIN_COEFF_XX (BITS 25:13 AND BITS 12:0)

The remaining linearization coefficients are stored in EEPROM registers 0x23 through 0x31. They follow the same pattern as EEPROM 0x22, with the higher coefficient value stored in bits 25:13 of the register and the lower coefficient value stored in bits 12:0.

EEPROM 0x32/Shadow 0x72

ANG_PRE_GAIN_OFFS (BITS 17:3)

The 2's complement value that is added to the digital angle prior to the gain stage of the short-stroke block.

CORDIC_BYPASS (BIT 2)

Bypasses the CORDIC angle calculation when set. The value that is passed through is based on the *CORDIC_CHAN_ORDER* bit.

- If *CORDIC_BYPASS* = 0, device performs CORDIC angle calculation based on channel A and channel B data.
- If *CORDIC_BYPASS* = 1, CORDIC calculation is not performed, and the device passes through channel A or B, directly through the rest of the signal path.

CORDIC_CHAN_ORDER (BIT 1)

Determines the order of inputs to the CORDIC calculation or determines which channel to pass when *CORDIC_BYPASS* = 1.

CORDIC_BYPASS	CORDIC_CHAN_ORDER	Output of CORDIC
0	0	atan2(chanA, chanB)
0	1	atan2(chanB, chanA)
1	0	chanA+32768
1	1	chanB+32768

CORDIC_POL (BIT 0)

Inverts the polarity of the output of the CORDIC when set.

EEPROM 0x33/Shadow 0x73

BIN_HYST (BITS 22:16)

Determines the amount of hysteresis for each bin when using binning mode of linearization.

ANG_GAIN (BITS 15:0)

Determines the amount of that is applied to the signal within the short-stroke block.

EEPROM 0x34/Shadow 0x74

ANG_SAT_ROLLOVER (BITS 25:18)

Determines the saturation rollover point for the post-gain signal value.

ANG_GAIN_SAT_EN (BIT 17)

Determines the signal functionality in cases where the digital value exceeds the value set by the *ANG_SAT_ROLLOVER*.

- If *ANG_GAIN_SAT_EN* = 0, the angle rolls over back to 0.
- If *ANG_GAIN_SAT_EN* = 1, the angle saturates high or low based on the pre-gain angle and *ANG_SAT_ROLLOVER*.

ANG_POST_GAIN_OFFS (BITS 16:1)

Offset value added to the digital signal after the gain of the short-stroke block.

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ANG_OFFS_SAT_EN (BIT 0)

Enables the post-gain saturation feature when set.

- If *ANG_OFFS_SAT_EN* = 0, the device outputs the value after gain and offset, ignoring A*NG_SAT_ROLLOVER*.
- If *ANG_OFFS_SAT_EN* = 1, the device either rolls over or saturates the signal at the *ANG_SAT_ROLLOVER* based on the *ANG_GAIN_SAT_EN* bit.

EEPROM 0x35/Shadow 0x75

MAGNETIC_THRESH_MAX (BITS 17:10)

Sets the maximum magnetic magnitude threshold. All values exceeding this set value trigger an error flag.

MAGNETIC_THRESH_MAX_EN (BIT 9)

Enables the maximum magnetic threshold checking when enabled.

- If *MAGNETIC_THRESH_MAX_EN* = 0, *MAGNETIC_THRESH_MAX* is ignored.
- If *MAGNETIC_THRESH_MAX_EN* = 1, magnetic magnitude is compared to *MAGNETIC_THRESH_MAX* and triggers a flag if the condition fails.

MAGNETIC_THRESH_MIN (BITS 8:1)

Sets the minimum magnetic magnitude threshold. All values below this set value trigger an error flag.

MAGNETIC_THRESH_MIN_EN (BIT 0)

Enables the minimum magnetic threshold checking when enabled.

- If *MAGNETIC_THRESH_MIN_EN* = 0, MAGNETIC_THRESH_MIN is ignored.
- If *MAGNETIC_THRESH_MIN_EN* = 1, magnetic magnitude is compared to *MAGNETIC_THRESH_MIN* and triggers a flag if condition fails.

EEPROM 0x36/Shadow 0x76

CLAMP_LOWER (BITS 15:0)

Sets the low clamp value for the output of the digital signal path. All signals below this value are limited to this value.

EEPROM 0x37/Shadow 0x77

BW_ADAPT_MAX (BITS 24:22)

Sets the maximum bandwidth of the adaptive filter.

BW_ADAPT_MIN (BITS 21:19)

Sets the minimum bandwidth of the adaptive filter.

BW_SEL (BITS 18:16)

Determines which bandwidth settings to use for internal filtering.

BW_SEL	Bandwidth (Hz)
0	329.1
1	465.8
2	556
3	700
4	1000
5	1482
6	2024
7	Adaptive

CLAMP_UPPER (BITS 15:0)

Sets the upper clamp value for the output of the digital signal path. All signals above this value are limited to this value.

EEPROM 0x38/Shadow 0x78

POWER_ON_DELAY (BITS 20:18)

Selects the length of time for which the device outputs the POR condition before beginning to transmit data. For more details, see the Sensor Output During Low-Pass Filter Initialization section.

POWER_ON_DELAY	Additional Delay (ms)
0	0.5
1	1.0
2	1.5
3	2.0
4	2.5
5	3.0
6	4.0
7	0.0

BW_ADAPT_DELAY (BITS 17:8)

Number of clock cycles at 8 MHz delay before the adaptive filter bandwidth decreases.

BW_ADAPT_EXP (BITS 7:4)

Exponential gain of the feed-forward adaptive filter loop.

BW_ADAPT_FRACT (BITS3:0)

Fractional gain of the feed-forward adaptive filter loop.

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EEPROM 0x39/Shadow 0x79

SENT_FRAME_RATE (BITS 23:22)

Sets the frame rate when using paused SENT.

SENT_FRAME_RATE	Frame Rate including pause pulse
0	3 data nibbles: frame length 210 t_{tick} 4 data nibbles: frame length 228 t_{tick} 6 data nibbles: frame length 282 t_{tick}
1	0.5 ms
2	1 ms
3	2 ms

SENT_INIT_SEL (BITS 21:19)

Selects which data the SENT interface transmits during the initialization time. If an initialization time is not selected, this register does nothing.

SENT_INIT_SEL	n-bit data Output
0	0
1	$2^n - 7$
2	$2^n - 4$
3	$2^n - 3$
4	$2^n - 2$
5	$2^n - 1$
6	0
7	0

SENT_ENCODING_SEL (BIT 18)

Selects SENT data mapping for SENT configurations 0, 4, 7, and 15.

- If *SENT_ENCODING_SEL* = 0, mapping is disabled, SENT outputs the data as it appears in the registers.
- If *SENT_ENCODING_SEL* = 1, output SENT data is remapped per the table below.

DATA Value	SENT Output
0	1
1 through 2^{n-8}	Unchanged
>=2^{n-8}	2^{n-8}
SCN 1 Error Flag	2^{n-5}
SCN 2 Error Flag	2^{n-6}
Not Valid	0

* n is the number of bits in the data of the SENT packet.

** Not valid refers to the period of time after power up before the SENT interface receives the first valid update from the signal path.

SENT_CRC_SEL (BIT 17)

Includes the SCN nibble in the CRC calculations when set.

SENT_EMSG_DIS (BIT 16)

Disables SENT serial message when set.

DIG_OUT_PULL_LIM_DIS (BIT 15)

Disables slew rate control when set.

DIG_OUT_PULL_LIM (BITS 14:12)

Selects the slew rate control for digital drivers.

DIG_OUT_DATA_RATE (BITS 11:7)

Selects the tick time if using SENT interface, or the period when using the PWM interface.

SENT_DATA_SEL (BITS 6:3)

Selects the SENT data configuration.

DIG_COMM_ID (BIT 2)

Sets the device ID for Manchester communication protocol.

DIG_OUT_SEL (1:0)

Selects the output mode for digital interface devices.

DIG_OUT_SEL	Output Protocol
0	PWM
1	SENT
2	SENT with Pause Pulse
3	PWM

EEPROM 0x3A/Shadow 0x7A

SENT_EMSG_ERR_REPEAT (BIT 21)

Enables SENT message repeat when set.

SENT_EMSG_SEL (BITS 20:0)

Selects which EMSG messages are sent.

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EEPROM 0x3B/Shadow 7B

ENHANCED_SETTINGS_UNLOCK (BIT 25)

Enables write access to register 0x16 when set.

SPARE_0X3B (BITS 24:23)

Spare bits that can be used as nonvolatile storage within the device. This register does not effect device performance.

DIG_OUT_PUSH_LIM (BITS 24:22)

Selects the digital output push driver current limit. Approximate current limits are provided below:

DIG_OUT_PUSH_LIM	Current Limit (mA)
0	10
1	8.75
2	7.5
3	6.25
4	5
5	3.75
6	2.5
7	1.25

DIG_OUT_PUSH_LIM_SEL (BIT 21)

Disables the digital push driver current limit.

- If *DIG_OUT_PUSH_LIM_DIS* = 0, current limit is set by the *DIG_OUT_PUSH_LIM* register.
- If *DIG_OUT_PUSH_LIM_DIS* = 1, current limit is ~20 mA

SAT_COR_MASK (BIT 20)

Disables the channel level saturation sub-flag when set. This mask only affects the error flag reporting ability and does not change the effects of saturation on the signal-path data.

SAT_FILT_MASK (BIT 19)

Disables the filter-level saturation sub-flag when set. This mask only affects the error flag reporting ability and does not change the effects of saturation on the signal-path data.

SAT_COR_MASK (BIT 18)

Disables the saturation correction error flag when set. This mask only affects the error flag reporting ability. It does not change the effect of the saturation on the signal-path data.

SAT_LIN_MASK (BIT 17)

Disables the saturation linearization error flag when set. This mask only affects the error flag reporting ability. It does not change the effect of the saturation on the signal-path data.

ACF_FAULT_FILT (BITS 16:15)

Filters the ACF fault condition. The error condition must be present for the number of cycles shown below before a fault flag is tripped.

ACF_FAULT_FILT	Cycles
0	0
1	2
2	4
3	8

FAULT_FILT (BITS 14:12)

Filters the SAT, AOC, and SRR flags; each error condition must be present for the number of cycles shown below before their respective flag is tripped. Additionally, also sets the number of temperature updates for which the temperature sensor must be in error before a TSE flag is set

FAULT_FILT	SAT, AOC, SSR [Cycles]	TSE [Temperature Updates]
0	0	1
1	2	2
2	4	4
3	8	8
4	16	16
5	32	2
6	64	4
7	128	8

OVD_MASK (BIT 11)

Disables the overvoltage-detection error flag when set.

UVD_MASK (BIT 10)

Disables the undervoltage-detection error flag when set.

SPE_MASK (BIT 9)

Disables the signal-path error flag when set.

ESE_MASK (BIT 8)

Disables the EEPROM single-bit error flag when set.

POR_MASK (BIT 7)

Disables the power-on reset error flag when set.

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SRR_MASK (BIT 6)

Disables the signal radius out of range error flag when set.

SLF_MASK (BIT 5)

Disables the signal-processing-logic failure error flag when set.

OFE_MASK (BIT 4)

Disables the oscillator frequency error flag when set.

SAT_MASK (BIT 3)

Disables the saturation error flag when set.

TSE_MASK (BIT 2)

Disables the temperature-sensor error flag when set.

AOC_MASK (BIT 1)

Disables the angle outside of clamp error flag when set.

ACF_MASK (BIT 0)

Disables the analog-check failure error flag when set.

EEPROM 0x3C/Shadow 0x7C

MEM_LOCK_SEL (BITS 24:21)

Prevents writes to EEPROM memory when set.

MANCH_ACCESS_SEL (BITS 20:19)

Disables Manchester entry triggers.

MANCH_ACCESS_SEL	Manchester Entry Method
00	Manchester enabled by OVD or function pulses
01	Manchester enabled by OVD only
10	Manchester enabled by function pulses only
11	Manchester cannot be enabled

NOTE: The setting *MANCH_ACCESS_SEL* = 11 prevents all further communication.

TEST_MODE_DIS (BIT 18)

Disables internal test modes that effect the device output (margin testing). To perform margin testing with this bit active, it must first be cleared in shadow. This is provided to prevent a single-bit error in volatile space from causing an invalid output.

OVD_SEL (BIT 17)

Selects which overvoltage value to use when determining if an overvoltage error occurred.

UVD_SEL (BIT 16)

Selects which undervoltage value to use when determining if an undervoltage error occurred.

SPARE_0X3C (BITS 15:12)

Spare bits that can be used as nonvolatile storage within the device. This register does not effect device performance.

ERR_RESP_SEL_OV (BITS 11:10)

Selects how the device responds to overvoltage conditions when MANCH_ACCESS_SEL = 2'b1X.

ERR_RESP_SEL_OV	*MANCH_ACCESS_SEL*	Output Response
XX	0X	High-Z
00	1X	Based on output prorotocol
01	1X	High-Z
10	1X	High*
11	1X	LOW**

ERR_RESP_SEL (BITS 9:8)

Selects how the device responds to error flags.

ERR_RESP_SEL	Output Response
00	Based on output protocol
01	High-Z
10	HIGH*
11	RESERVED

ERR_RESP_SEL_UV (BITS 7:6)

ERR_RESP_SEL_UV	Output Response
00	High-Z
01	HIGH*
10	LOW**
11	High-Z

* Device can only drive HIGH if *DIG_OUT_DRIVE_SEL* = 0; otherwise, the output is high-Z

** If MANCH_ACCESS_SEL = 2'bX0, recovery from an error reported as LOW may be delayed by an additional Manchester code timeout length (300 µs)

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ERR_HOLD_SEL (BITS 5:3)

Selects the number of updates for which the SENT and PWM interface report a UVD error condition after returning to normal V_{CC} levels.

ERR_HOLD_SEL	Digital UVD Reports
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

DIG_COMM_INPUT_HIGH (BIT 1)

Sets the threshold for the rising edge when determining Manchester data input.

DIG_COMM_INPUT_LOW (BIT 0)

Sets the threshold for the falling edge when determining Manchester data input. Also determines the low threshold for overdriving the output to initiate Manchester interface when in digital modes.

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PACKAGE OUTLINE DRAWING

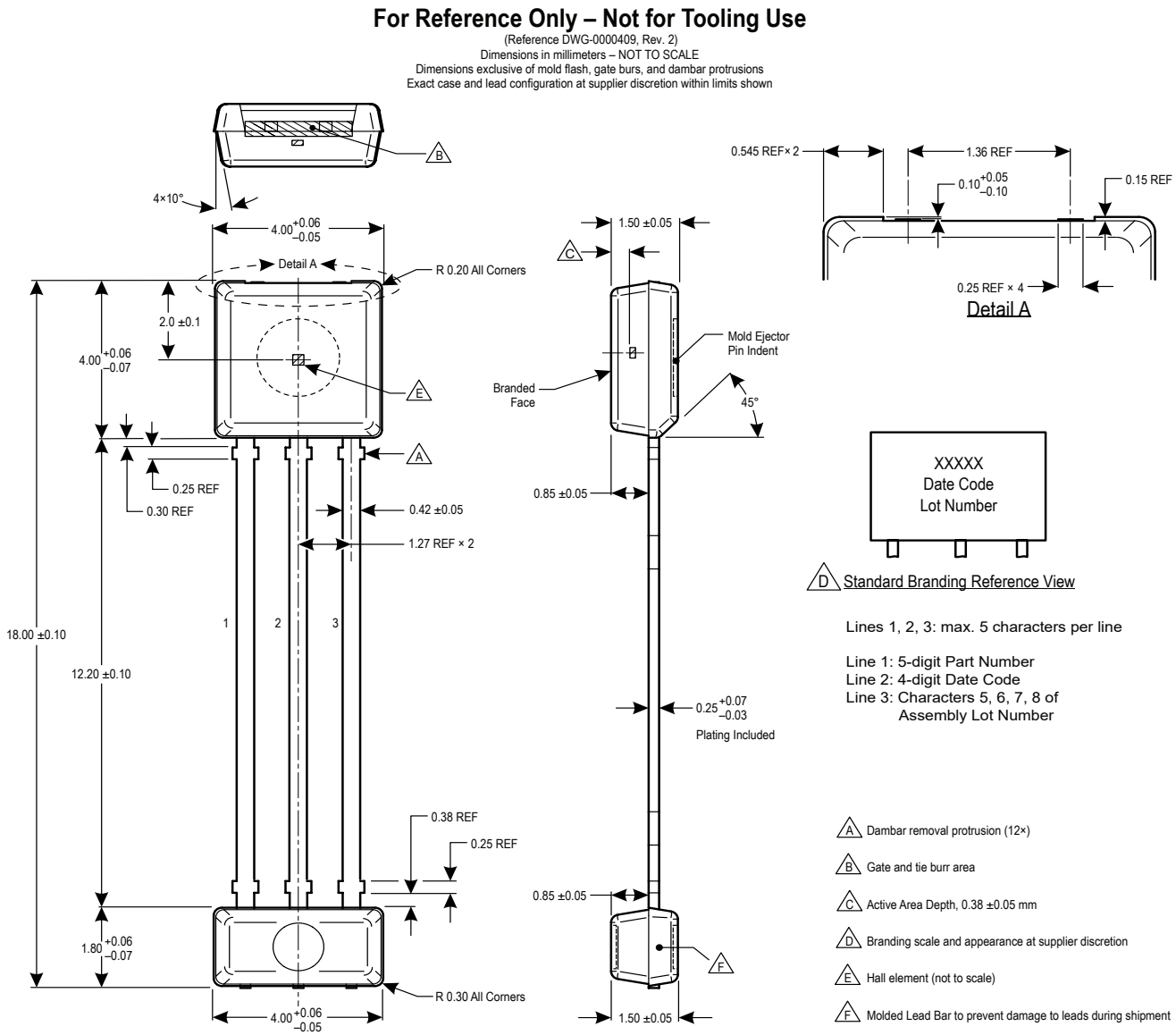

Figure 31: 3-Pin SIP (Suffix UC)

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Revision History

Number	Date	Description
–	September 14, 2022	Initial release
1	November 3, 2022	Updated Angle Drift TBD values (page 8) and Channel Drift values (page 9); removed TBD Angle Error rows (page 9)
2	November 29, 2022	Updated Figure 8 (page 19), and Table 32 (page 45, error flag UVD SENT and PWM Response)
3	March 18, 2024	Removed “pending assessment” from ASIL compatibility statement (page 1), added magnetic requirements notes (page 7), and made minor editorial corrections throughout (all pages), including: changed the future tense to the present tense, updated register names to standard (uppercase) and minimized use of capitalization elsewhere, added clarifications that distinguish between register value and real value of register setting, and added missing hyperlinks and corrected hyperlinks for cross-references

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