A31102

Low-Noise, Programmable Linear Hall IC with Advanced Diagnostics

FEATURES AND BENEFITS

- Industry-leading noise performance reduces audible noise impact of torque ripple in EPS applications
  - High speed, low noise 16-bit ADC
  - Increased number of user-selectable bandwidth options to better optimize tradeoff between noise and response time
  - Advanced adaptive filter option for further noise improvements
- Flexible programming interface
  - Standard 3-wire serial programming interface
  - Optional 2-wire serial programming interface, eliminates need for increased supply voltage when connected to other sensitive components
- Developed in accordance with ISO 26262 requirements for hardware product development for use in safety-critical applications
  - A31102LLUBTR-DD (dual die) designed to meet ASIL D requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A31102 Safety Manual
  - A31102LLUATR (single die) designed to meet ASIL B requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A31102 Safety Manual

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PACKAGE:

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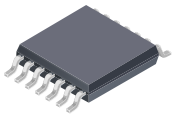

14-pin TSSOP (suffix LU)

DESCRIPTION

The A31102 is available in two package options: one includes a single monolithic integrated circuit (IC), and the second includes two electrically isolated ICs. Each IC consists of a high-precision programmable Hall-effect linear sensor with an open-drain output, which can be configured for either pulse-width-modulated (PWM) or Single Edge Nibble Transmission (SENT) output protocols. Each IC within the A31102 package includes fully independent power and ground connections. The A31102 is an especially configurable and robust solution for the most demanding linear magnetic field sensing applications, including torque sensing in electronic power steering (EPS).

Two key features of the A31102 are the low noise output and capability to provide a highly linear device output even with nonlinear input magnetic fields. To achieve this, each BiCMOS monolithic integrated circuit includes the following: a Hall sensing element, an ultra-low noise front end amplifier, proprietary dynamic offset cancellation circuits, on-chip stress compensation circuitry, a 16-bit analog-to-digital converter (ADC), and a highly flexible digital signal path that includes precision temperature compensating circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element, advanced output linearization circuitry and advanced diagnostic detection features. It also includes on-chip EEPROM for storing all necessary factory- and customer-programmable parameters to correctly configure each device.

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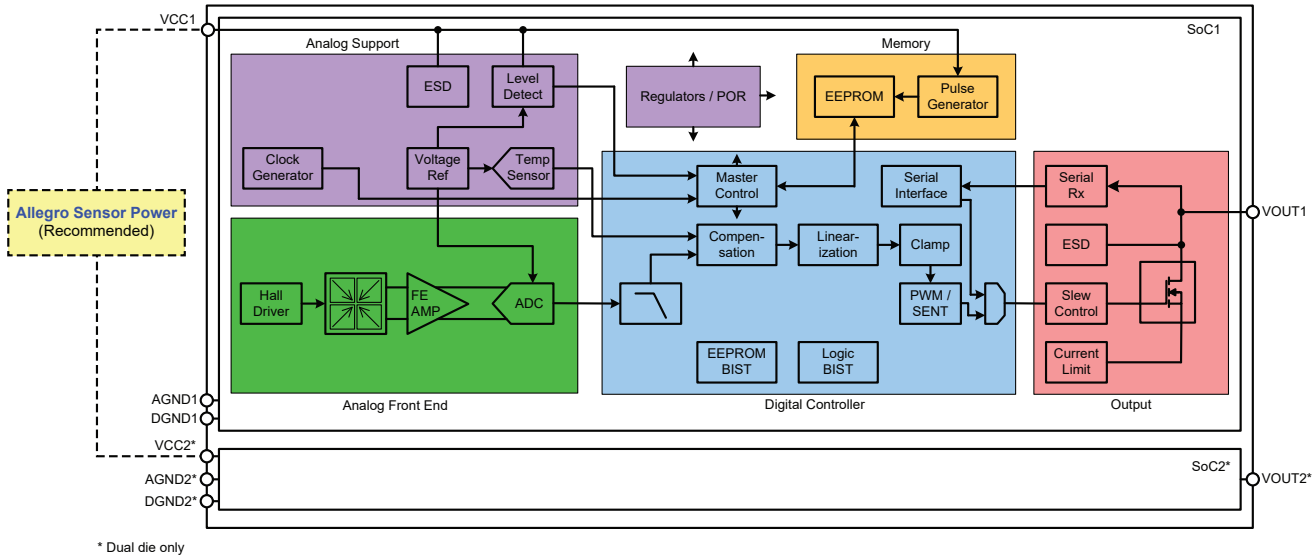

Functional Block Diagram

FEATURES AND BENEFITS (continued)

- Multiple on-chip diagnostics provide high level of fault coverage for on-chip and environmental faults
  - Overvoltage and undervoltage detection
  - Overtemperature
  - Magnetic field out-of-range detection
  - Broken wire detection
  - Signal path monitoring
- AEC-Q100 Grade 0
  - Dual die version Q104 qualified
- Exceptional stability throughout lifetime and across temperature changes
  - Factory-programmed to have flat sensitivity over full operating temperature range
  - Customer programmable 1st and 2nd order sensitivity and 1st order offset compensation across temperature range for pairing A31102 with wide variety of magnet types
  - Active stress compensation circuitry helps minimize lifetime sensitivity drift
- Integrated linearization allows for flexible output waveform translation and compensation for nonlinear magnetic inputs
- Flexible output protocols with up to 16-bit resolution and configurable error notifications
  - Digital open-drain output allows for flexible output voltage levels
  - PWM (pulse-width-modulated) output with diagnostic output mode to identify fault conditions
  - Configurable SENT output with 12- or 16-bit magnetic data
  - SENT (Single Edge Nibble Transmission) compliant output with configurable reporting of error conditions and other diagnostic information
  - Proprietary Fast SENT provides increased data rates to support high-bandwidth applications
  - Allegro proprietary shared SENT protocols, SSENT (Sequential SENT) and ASENT (Addressable SENT), allow users to connect up to 4 devices on the same output line to reduce wiring harness needs
  - Enhanced EMC tuning through programmable fall-time configurability
- On-chip EEPROM for storing factory- and customer-programmable parameters
  - Integrated charge pump reduces requirements for high-voltage pulses to program EEPROM
  - Single bit Error Correction and Double bit Error Detection (SECDED) capability
  - Unique lot and date code information stored in EEPROM to provide full traceability of each IC
  - Includes customer-reserved “scratchpad” EEPROM space

DESCRIPTION (continued)

The A31102 was developed in accordance with Allegro’s third-party certified ISO 26262 compliant development processes, and as such is ideal for safety-critical applications like EPS torque sensing. The A31102 dual die option (DD) was designed to meet ASIL D requirements and the A31102 single die option was design to meet ASIL B requirements, when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A31102 Safety Manuals. Contact your local Allegro sales representative for more detailed functional safety-related documentation, like the Safety Manual.

The A31102 contains two proprietary SENT protocols in addition to SAEJ2716—SSENT and ASENT. Both protocols enable the user to attach up to four devices on one SENT line to reduce system costs. SSENT allows sequential access to the sensors connected to the same line. SSENT provides a very low overhead method to maximize the sensor bandwidth on this single SENT line, minimizing impact on system performance. ASENT allows direct addressable access to all the sensors on the common SENT line. Both protocols allow individual sensors on the same line to enter diagnostic mode while the other sensors continue to respond to queries, allowing for the highest diagnostic coverage while maintaining 100% availability of the sensor solution.

The A31102 is available in a surface-mount, lead (Pb) free 14-pin TSSOP package (LU suffix), with 100% matte-tin leadframe plating.

The A31102 complies with the requirements of EU Directive 2002/95/EC (RoHS) and 2011/65/ EU (RoHS II), amended by 2015/863/EU, on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment.

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SELECTION GUIDE

Part Number	Input Field Range (G)	Dual Die	Package	Packing [1]
A31102LLUBTR-DD750	±750	Yes	14-pin TSSOP	4000 pieces per 13-inch reel
A31102LLUBTR-DDLN500 [2]	±500			
A31102LLUATR-750	±750	No	14-pin TSSOP	4000 pieces per 13-inch reel
A31102LLUATR-LN500 [2]	±500			

[1] Contact Allegro™ for additional packing options.
[2] Recommend use of Allegro LDOs and other DC/DC regulators for highly accurate supply voltage. See Allegro's Sensor Bias Solutions page at: https://www.allegromicro.com/en/insights-and-innovations/technical-documents/Sensor-Bias-Solutions.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		20	V
Reverse Supply Voltage	V_{RCC}		–16	V
Forward Supply Current	I_{CC}		30	mA
Reverse Supply Current	I_{RCC}		–30	mA
Forward Output Voltage	V_{OUT}		20	V
Reverse Output Voltage	V_{ROUT}		–0.7	V
Output Short-Circuit Current	$I_{OUTSC(SINK)}$	V_{CC} to V_{OUT}, 4.5 V < V_{CC} < 5.5 V	–20	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard JESD51-7	174	°C/W

*Additional thermal information available on the Allegro website.

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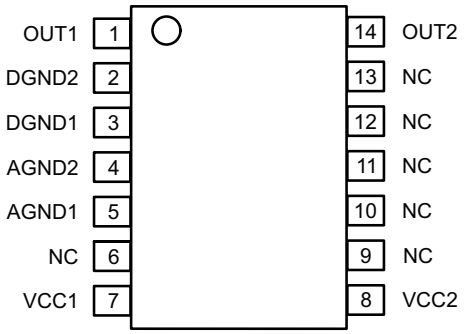
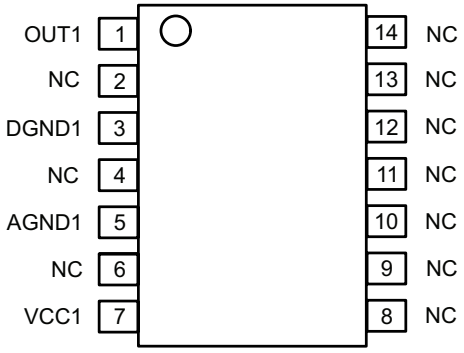
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LUB-DD, 14-Pin TSSOP Pinout Diagram (Dual Die)

Dual Die Terminal List Table

Number	Name	Function
1	OUT1	Output signal, die 1
2	DGND2	Ground, die 2, must be connected to pin 4
3	DGND1	Ground, die 1, must be connected to pin 5
4	AGND2	Ground, die 2, must be connected to pin 2
5	AGND1	Ground, die 1, must be connected to pin 3
6, 9, 10, 11, 12, 13	NC	No connection; recommend connecting to GND for best EMC performance
7	VCC1	Input power supply, die 1
8	VCC2	Input power supply, die 2
14	OUT2	Output signal, die 2



Package LUA, 14-Pin TSSOP Pinout Diagram (Single Die)

Single Die Terminal List Table

Number	Name	Function
1	OUT1	Output signal, die 1
2	NC	No connection; recommend connecting to GND for best EMC performance
3	DGND1	Ground, die 1, must be connected to pin 5
4	NC	No connection; recommend connecting to GND for best EMC performance
5	AGND1	Ground, die 1, must be connected to pin 3
6	NC	No connection; recommend connecting to GND for best EMC performance
7	VCC1	Input power supply, die 1
8-14	NC	No connection; recommend connecting to GND for best EMC performance

Allegro offers sensor bias solutions such as LDOs and regulated linear output supply voltage rails off multiple output regulators, well-suited for providing tightly regulated supply voltage to sensor ICs. For available devices, see Allegro's Sensor Bias Solutions page at: https://www.allegromicro.com/en/insights-and-innovations/technical-documents/Sensor-Bias-Solutions.

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OPERATING CHARACTERISTICS: Valid T_A and V_{CC}, unless otherwise specified (specifications relate to one die in the package)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1]	V_{CC}	A31102LLUATR-750, A31102LLUBTR-DD750	4.5	5.0	5.5	V
		A31102LLUATR-LN500, A31102LLUBTR-DDLN500	4.8	5.0	5.5	V
Supply Current	I_{CC}	A31102LLUATR-750, A31102LLUBTR-DD750	–	–	11	mA
		A31102LLUATR-LN500, A31102LLUBTR-DDLN500	–	–	12	mA
Reverse Supply Current	I_{RCC}	V_{CC} = –16 V, T_A = 25°C	–3	–	–	mA
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	I_{CC} = 14 mA, compensation coil off, T_A = 25°C	20	–	–	V
Oscillator Frequency	f_{OSC}		7200	8000	8800	kHz
Undervoltage Detection Threshold [2]	$V_{CC(UV)}$	A31102LLUATR-750, A31102LLUBTR-DD750	–	–	4.5	V
		A31102LLUATR-LN500, A31102LLUBTR-DDLN500	–	–	4.8	V
Power-On-Reset Threshold	$V_{CC(POR)LOW}$	V_{CC} falling, see Figure 1	3.4	–	3.6	V
	$V_{CC(POR)HIGH}$	V_{CC} rising, see Figure 1	3.6	–	3.8	V
Overvoltage Detection Threshold [3]	$V_{CC(OV)LOW}$	V_{CC} falling, see Figure 1	6.6	–	7.4	V
	$V_{CC(OV)HIGH}$	V_{CC} rising, see Figure 1	6.7	–	7.6	V
High-Voltage Threshold	$V_{CC(HV)LOW}$	V_{CC} falling, see Figure 1	15	–	–	V
	$V_{CC(HV)HIGH}$	V_{CC} rising, see Figure 1	–	–	17	V
OUTPUT CHARACTERISTICS						
Output Leakage Current	I_{OUT}	Output voltage ≤ 5.5 V, output FET off	–	1.0	100	µA
Output Load Resistance	$R_{L(PULLUP)}$	Output current ≥ –10 mA	1.2	–	–	kΩ
Output Saturation Voltage	$V_{OUT(Sat)LOW}$	Output current = –4.7 mA, V_{CC} = 5 V, output FET on	–	–	0.35	V
Output Current Limit	I_{LIMIT}	Output FET on, T_A = 25°C	20	30	50	mA
Output Zener Clamp Voltage	V_{ZOUT}	T_A = 25°C, I_{OUT} = –3 mA	20	–	–	V
External Load Capacitor	C_{LX}		–	–	4.7	nF
Output Response Time [4]	t_{resp}	BW_SEL = 0 (8500 Hz)	–	0.16	–	ms
		BW_SEL = 1 (6660 Hz)	–	0.17	–	ms
		BW_SEL = 2 (3330 Hz)	–	0.25	–	ms
		BW_SEL = 3 (1520 Hz)	–	0.43	–	ms
		BW_SEL = 4 (733 Hz)	–	0.75	–	ms
		BW_SEL = 5 (360 Hz)	–	1.42	–	ms
		BW_SEL = 6 (179 Hz)	–	2.75	–	ms
		BW_SEL = 7 (89 Hz)	–	5.39	–	ms

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OPERATING CHARACTERISTICS (continued): Valid T_A and V_{CC}, unless otherwise specified (specifications relate to one die in the package)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power-On Time [4]	t_{PO}	BW_SEL = 0 (8500 Hz)	–	0.61	–	ms
		BW_SEL = 1 (6660 Hz)	–	0.62	–	ms
		BW_SEL = 2 (3330 Hz)	–	0.7	–	ms
		BW_SEL = 3 (1520 Hz)	–	0.88	–	ms
		BW_SEL = 4 (733 Hz)	–	1.2	–	ms
		BW_SEL = 5 (360 Hz)	–	1.9	–	ms
		BW_SEL = 6 (179 Hz)	–	3.3	–	ms
		BW_SEL = 7 (89 Hz)	–	6	–	ms
Output, Integral Nonlinearity	INL	OUTMSG_MODE = 0		±0.5		%FSO
Maximum Output Resolution [5]	OUT_{RES}	T_A = 25°C, OUTMSG_MODE = 0			16	bit
		T_A = 25°C, OUTMSG_MODE = 1-7, SENT_DATA_CFG = 0-3			12	bit
		T_A = 25°C, OUTMSG_MODE = 1-7, SENT_DATA_CFG = 4-7			16	bit

[1] Recommended operation between the specified limits for V_{CC}. The full operating range by design is between $V_{CC(UV)}$ and $V_{CC(OV)}$.
[2] Undervoltage Detection asserts between $V_{CC(POR)}$ and $V_{CC(MIN)}$. The Undervoltage flag indicates when the supply voltage is below operating specification and may result in degraded output accuracy.
[3] Overvoltage Detection asserts between $V_{CC(MAX)}$ and $V_{CC(OV)MAX}$. The Overvoltage flag indicates when the supply voltage is above operating specification and may result in degraded output accuracy.
[4] Defined as time before magnetic data is 90% of the settled value.
[5] When OUTMSG_MODE = 0, PWM output mode, the output resolution is calculated using the following formula with a maximum 16 bit, $OUT_{RES} = Log(0.96 \times f_{osc} / f_{PWM}) / Log(2)$

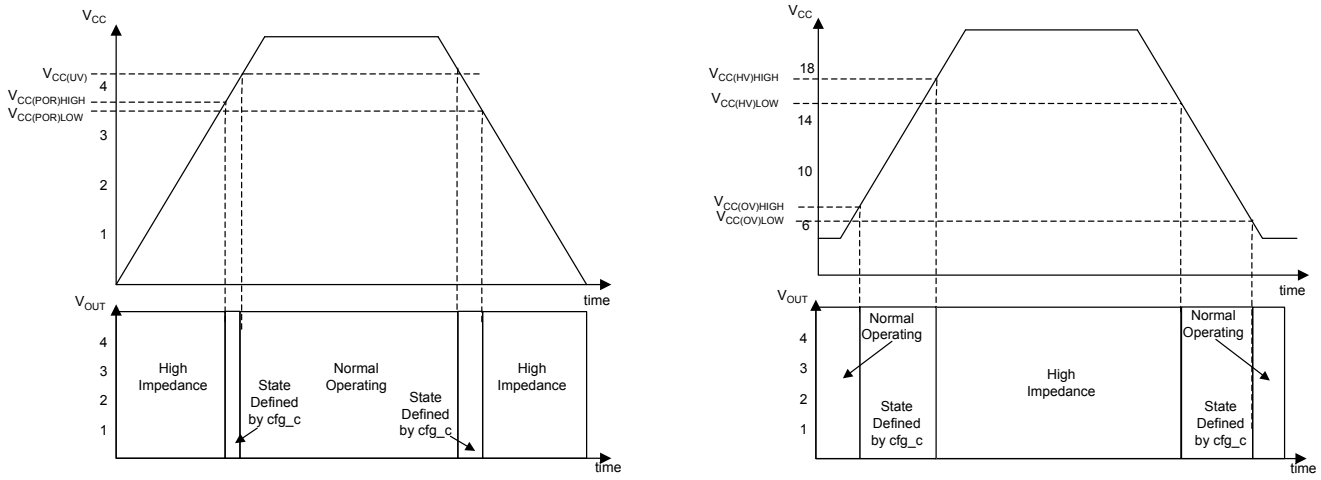

Figure 1: V_{CC} Thresholds and Resultant Output States

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A31102LLUATR-750, A31102LLUBTR-DD750 NOISE CHARACTERISTICS: Valid at T_A and V_{CC}, unless otherwise specified (specifications relate to one die in the package)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Noise (Peak-to-Peak) [1]	$B_{OUTN(PK)}$	BW_SEL = 0 (8500 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	1.19	–	G
		BW_SEL = 1 (6660 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	1.05	–	G
		BW_SEL = 2 (3330 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.75	–	G
		BW_SEL = 3 (1520 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.5	–	G
		BW_SEL = 4 (733 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.35	–	G
		BW_SEL = 5 (360 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.25	–	G
		BW_SEL = 6 (179 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.17	–	G
		BW_SEL = 7 (89 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.13	–	G

[1] Noise (Peak-to-Peak) calculated as 6 sigma (6 standard deviations) from characterization of a small sample of devices with a 0.01 µF bypass capacitor. Measurements were made at Sensitivity ≈ $SENS_{INIT}$. Conversion of noise from gauss to LSB can be done by: Noise (G) × Sensitivity (LSB/G) = Noise (LSB).

A31102LLUATR-LN500, A31102LLUBTR-DDLN500 NOISE CHARACTERISTICS: Valid at T_A and V_{CC}, unless otherwise specified (specifications relate to one die in the package)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Noise (Peak-to-Peak) [1]	$B_{OUTN(PK)}$	BW_SEL = 0 (8500 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	1.05	–	G
		BW_SEL = 1 (6660 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.92	–	G
		BW_SEL = 2 (3330 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.66	–	G
		BW_SEL = 3 (1520 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.44	–	G
		BW_SEL = 4 (733 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.31	–	G
		BW_SEL = 5 (360 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.22	–	G
		BW_SEL = 6 (179 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.15	–	G
		BW_SEL = 7 (89 Hz), T_A = 25°C –500 G < B_{IN} < 500 G	–	0.12	–	G

[1] Noise (Peak-to-Peak) calculated as 6 sigma (6 standard deviations) from characterization of a small sample of devices with a 0.01 µF bypass capacitor. Measurements were made at Sensitivity ≈ $SENS_{INIT}$. Conversion of noise from gauss to LSB can be done by: Noise (G) × Sensitivity (LSB/G) = Noise (LSB).

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MAGNETIC CHARACTERISTICS: Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1][2]
Input Field Range	B_{IN}	A31102LLUATR-750, A31102LLUBTR-DD750	–750	–	750	G
		A31102LLUATR-LN500, A31102LLUBTR-DDLN500	–500	–	500	G
Initial Sensitivity	$SENS_{INIT}$	A31102LLUATR-750, A31102LLUBTR-DD750	–	0.0667	–	%FSO/G
		A31102LLUATR-LN500, A31102LLUBTR-DDLN500	–	0.1	–	%FSO/G
Initial Quiescent Output	QO_{INIT}		–	50	–	%FSO
Initial Output Clamp	$OUT_{CLP(L)INIT}$	CLAMP_LOW = 0, OUTMSG_MODE > 0	–	0	–	LSB
		CLAMP_LOW = 0, OUTMSG_MODE = 0	–	2	–	%D
	$OUT_{CLP(H)INIT}$	CLAMP_HIGH = 0, OUTMSG_MODE > 0	–	65535	–	LSB
		CLAMP_HIGH = 0, OUTMSG_MODE = 0	–	98	–	%D
Initial Sensitivity Drift [3]	$\Delta SENS_{INIT}$	–40°C ≤ T_A ≤ 150°C	–	±0.01	–	%/°C
Initial QVO Drift [3]	ΔQVO_{INIT}	–40°C ≤ T_A ≤ 150°C	–	±1.5	–	G

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] FSO means Full Scale Output.
[3] Does not include drift over lifetime.

ACCURACY CHARACTERISTICS: Valid at T_A and V_{CC}, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
Sensitivity Drift Over Temperature	ΔSENS	25°C < T_A ≤ 150°C	–1.5	–	1.5	%
		–40°C ≤ T_A < 25°C	–3	–	3	%
Lifetime Sensitivity Drift	$\Delta SENS_{LIFE}$	Variation on final programmed Sensitivity value; measured at T_A = 25°C after AEC-Q100 grade 0 qualification	–2.2	–	2.2	%
Package Hysteresis	$\Delta SENS_{PKG}$	Variation on final programmed Sensitivity value; measured at T_A = 25°C after temperature cycling from 25°C	–	<±0.5	–	%
Lifetime Quiescent Output Drift [2]	ΔQVO		–1	–	1	G
PWM Frequency Drift [3]	Δf_{PWM}		–10	–	10	%

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Quiescent Output Drift scales with Sensitivity.
[3] PWM Carrier Frequency Drift is % of the programming target. See programmable parameter reference for PWM carrier frequency programming options.

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PROGRAMMABLE CHARACTERISTICS: Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
SENSITIVITY						
Bits Customer Sensitivity Trim, Coarse	Bit ($SENS_{COARSE}$)		–	3	–	bits
Customer Sensitivity Coarse Trim Range [2]	$SENS_{COARSE}$		1	–	32	–
Bits Sensitivity Trim, Fine	Bit ($SENS_C$)		–	11	–	bits
Sensitivity Fine Trim Range [3]	$SENS_C$		0.5	–	1.5	–
OFFSET (QUIESCENT OUTPUT)						
Bits Quiescent Output Trim, Fine	Bit (QO_C)		–	18	–	bits
Quiescent Output Fine Trim Range	QO_C		–262144	–	262142	LSB
CLAMPS (HIGH AND LOW OUTPUT CLAMPS)						
Bits Output Low Clamp	Bit ($OUT_{CLP(LOW)}$)		–	12	–	bits
Output Low Clamp Range	$OUT_{CLP(LOW)}$		0	–	65520	LSB
Bits Output High Clamp	Bit ($OUT_{CLP(HIGH)}$)		–	12	–	bits
Output High Clamp Range	$OUT_{CLP(HIGH)}$		16	–	65535	LSB
TEMPERATURE COMPENSATION						
Bits 1st Order Sensitivity Temperature Compensation	Bit ($SENS_{CTC1}$)	SENSTC1_HOT_C, SENSTC1_CLD_C	–	11	–	bits
1st Order Sensitivity Temperature Compensation Range	$SENS_{CTC1}$	25°C < T_A ≤ 150°C	–0.391	–	0.391	% / °C
		–40°C ≤ T_A < 25°C	–0.781	–	0.781	% / °C
Bits 2nd Order Sensitivity Temperature Compensation	Bit ($SENS_{CTC2}$)	SENSTC2_HOT_C, SENSTC2_CLD_C	–	10	–	bits
2nd Order Sensitivity Temperature Compensation Range	$SENS_{CTC2}$	25°C < T_A ≤ 150°C	–1.5	–	1.5	m% / °C^2
		–40°C ≤ T_A < 25°C	–6	–	6	m% / °C^2
Bits 1st Order Offset Temperature Compensation	Bit (QO_{CTC1})	QOTC_HOT_C, QOTC_CLD_C	–	12	–	bits
1st Order Offset Temperature Compensation Range	QO_{CTC1}	25°C < T_A ≤ 150°C	–128	–	127.9	LSB / °C
		–40°C ≤ T_A < 25°C	–256	–	255.9	LSB / °C

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PROGRAMMABLE CHARACTERISTICS (continued): Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
LINEARIZATION						
Linearization Positions	–		–	17	–	data points
Bits Linearization Coefficients	Bits (LIN_{COEF})		–	13	–	bits
Bits Post Linearization Sensitivity Trim	Bits ($PLIN_{SENS}$)		–	13	–	bits
Post Linearization Sensitivity Trim Range	$PLIN_{SENS}$ (Range)		–1	–	1	–
Bits Post Linearization Offset Trim	Bits ($PLIN_{QDC}$)		–	12	–	bits
Post Linearization Offset Trim Range	$PLIN_{QDC}$ (Range)		–32768	–	32752	LSB
Bit Output Polarity	Bits (POL_{OUT})		–	1	–	bit
Bit Linearization Input Polarity	Bits (POL_{IN})		–	1	–	bit

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Sensitivity Coarse Trim is a multiplier to the initial Sensitivity with step sizes defined by the sensm parameter. Refer to the Programmable Parameter Reference section for more information.
[3] Sensitivity Fine Trim is a multiplier applied to the initial Sensitivity after the Sensitivity Coarse Trim with step sizes defined by the SENS_C parameter. Refer to the Programmable Parameter Reference section for more information.

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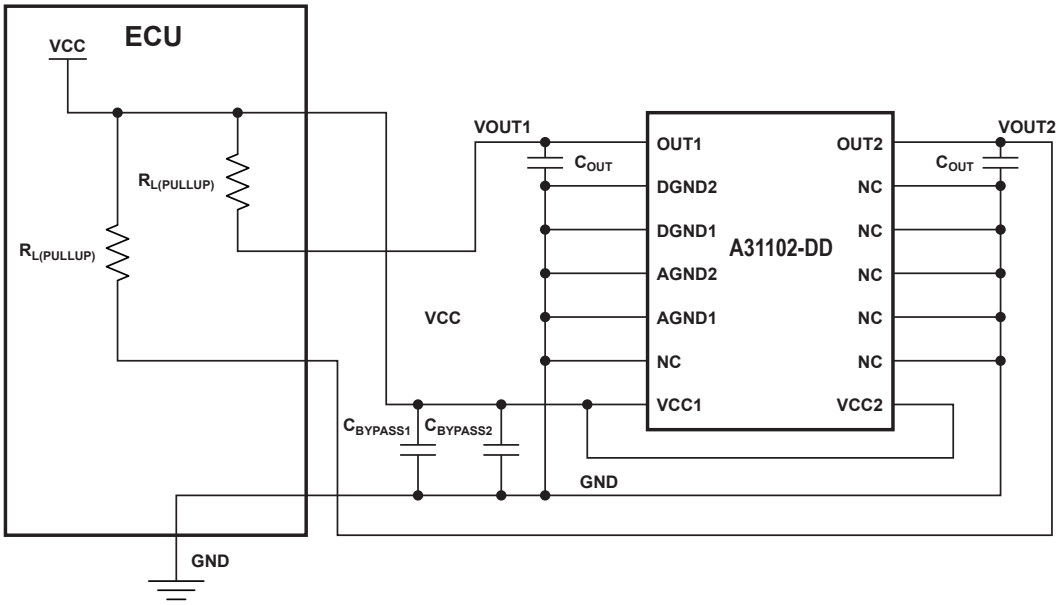

Figure 2: Dual Die Typical Application Circuit

Typical $C_{BYPASS1}$ = 1 nF and $C_{BYPASS2}$ = 10 nF.
For recommendations on C_{OUT} and EMC,
contact Allegro MicroSystems.

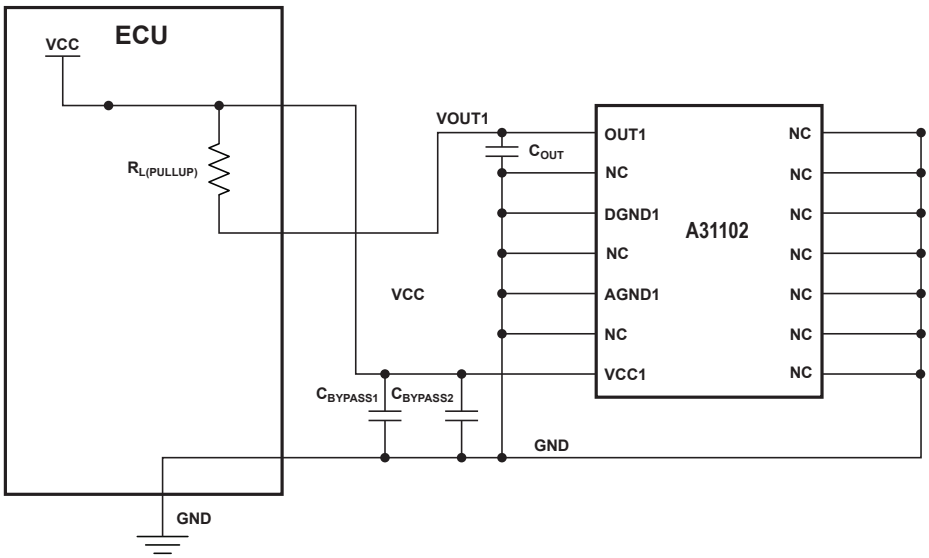

Figure 3: Single Die Typical Application Circuit

Typical $C_{BYPASS1}$ = 1 nF and $C_{BYPASS2}$ = 10 nF.
For recommendations on C_{OUT} and EMC,
contact Allegro MicroSystems.

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APPLICATION INFORMATION

ASIL Diagnostic Conditions

DIAGNOSTIC MODES

Each die in the A31102 contains features specifically designed to reduce nondetectable fault conditions and improve system-level ASIL (Automotive Safety Integrity Level) performance. The diagnostic features provide the ability to diagnose errors of the main signal path, including the analog signal path, the ADC, and the digital processing. The A31102 also contains features to diagnose broken wire or open circuit conditions. Descriptions of the broken wire fault conditions are listed in Table 1 (Broken Wire Detection Conditions).

DIAGNOSTIC CONFIGURATION

Each die in the A31102 contains EEPROM parameters to configure the diagnostic modes and output behavior. The EEPROM register, CFG_C, contains configurable parameters to enable or disable the Overvoltage Detection, Undervoltage Detection, Signal Out of Range, Signal Path Monitor, and Temperature Out of Range. In addition, the output behavior in response to the error conditions is configurable. By default, the device outputs a diagnostic error signal that is decoded by either the PWM or SENT message. Alternatively, the output behavior in response to the error conditions can be set to a high-impedance state.

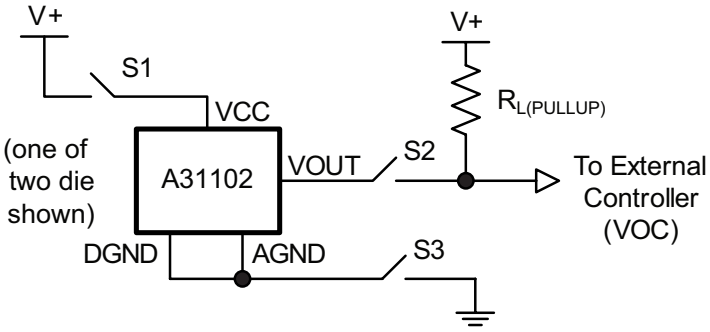

Figure 4: Diagnostic Application Circuit

ANALOG SIGNAL PATH

Each die in the A31102 contains features to monitor portions of the analog signal path. When enabled, the Signal Path monitor circuitry injects a reference signal at the output of the Hall element. The reference signal is processed through the front-end amplification circuits and the ADC. If the processed reference signal drifts beyond an internal threshold, an error is detected and the output responds according to the settings in the EEPROM register, CFG_C, and Table 2 (Diagnostic Summary Table). The Signal Path monitor reference signal is time-shared with the magnetic signal. The sample ratio is adjustable using the parameter SPDIAG_RATE. The Signal Path monitor also contains additional diagnostic circuitry to check portions of the digital signal processing. The analog and digital Signal Path monitor diagnostics are configurable to enable or disable independently. The recommended default configuration enables the digital checking and disables the analog reference signal.

SIGNAL OUT OF RANGE

Included in each of the A31102 die is a diagnostic feature, Signal Out of Range, to detect erroneous clamping of digital signal path as a result of external magnetic input signals. This feature also checks that the magnetic input does not exceed internal ADC range. The output responds to a Signal Out of Range diagnostic according to the settings in the EEPROM register, CFG_C, and Table 2 (Diagnostic Summary Table).

Table 1: Broken Wire Detection Conditions

Description	Circuit	S1	S2	S3	VOUT	VOC
Broken VCC	See Figure 4	OPEN	CLOSED	CLOSED	High Impedance	V_{CC}
Broken VOUT		CLOSED	OPEN	CLOSED	Operating	V_{CC}
Broken Ground [1]		CLOSED	CLOSED	OPEN	High Impedance	V_{CC}

[1] See Broken Ground Detection section for more information.

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UNDERVOLTAGE DETECTION AND RESET

Each A31102 die contains circuitry to detect a condition when the supply voltage, V_{CC}, drops below the required operating value. The Undervoltage Detection, UVD, monitors internal circuitry to determine if the supply voltage is sufficient for the die to operate within specification. An Undervoltage Detection error may occur when the supply voltage is within a region between the internal reset level, V_{POR}, and the minimum operating voltage, $V_{CC(min)}$. As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} drops to a level within the UVD range and an UVD error is detected, V_{OUT} is forced to a state defined by the EEPROM register, CFG_C. When V_{CC} increases to a sufficient level, the UVD error clears and V_{OUT} returns to its normal operating state. If V_{CC} drops below the internal reset level, $V_{POR(LOW)}$, the output is forced to a high-impedance state. When V_{CC} returns above the rising reset level, $V_{POR(HIGH)}$, the output responds according the UVD status. The output will not respond with normal data until a delay of t_{PO} after a reset event.

The parameter, POR_DIAG_MODE, configures the output response after a UVD event when the supply voltage returns to normal operating conditions. If POR_DIAG_MODE is set to a value of zero, the output is active immediately and settles after the response time, t_{resp}. If POR_DIAG_MODE is set to a value of 1, the UVD error condition is held for approximately 8 ms before it is cleared to allow time for the signal path to settle.

OVERVOLTAGE DETECTION

The A31102 contains circuitry to detect a condition when the supply voltage rises above the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{CC(OV)HIGH} - V_{CC(OV)LOW}$. As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} rises above $V_{CC(OV)HIGH}$, V_{OUT} is forced to a state defined by the EEPROM register, cfg_c. When V_{CC} returns below $V_{CC(OV)LOW}$, V_{OUT} returns to its normal operating state. The overvoltage detection is only enabled when the EEPROM lock bit is set. If the EEPROM lock bit is not set, and V_{CC} increases above $V_{CC(OV)HIGH}$, the device will enter programming mode and the output is forced to a high-impedance state. If V_{CC} rises above the high-voltage threshold, $V_{CC(HV)HIGH}$, the output is forced to a high-impedance state.

TEMPERATURE OUT OF RANGE

The A31102 contains circuitry to detect a condition when the ambient temperature exceeds the operating region. When the temperature sensor output is greater than 160°C or less than –55°C, the output responds according to the settings in the EEPROM register, CFG_C, and Table 2 (Diagnostic Summary Table).

BROKEN GROUND DETECTION

The A31102 contains circuitry to detect a condition when the ground connection is disconnected. The Analog Ground pin, AGND, and Digital Ground pin, DGND, for a single die, are connected internally. When the connections to both AGND and DGND are severed, the digital output driver turns off, forcing the output to a high-impedance state. See Table 1 (Broken Wire Detection Conditions) for more information.

EEPROM DIAGNOSTICS

The A31102 contains EEPROM with error checking and correction, ECC. The ECC corrects for a single EEPROM bit error without affecting device performance. The ECC also detects a dual bit EEPROM error, triggers an internal fault signal, and forces the output to a high-impedance state. Upon a read of EEPROM with no errors, bits 0 through 25 will return the requested EEPROM contents and bits 26 through 31, the six MSBs of the EEPROM register, will return as all zeros. When a corrected single bit error is detected, bit 28 of the read response data bits will return high, indicating the single bit error. When a dual bit error is detected, a read of EEPROM will have bit 29 of the data bits set high, indicating the dual bit error.

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Table 2: Diagnostic Summary Table

Diagnostic Detection	Conditions	V_{OUT} (PWM) DIAG_MODE = 0	V_{OUT} (SENT) DIAG_MODE = 0	V_{OUT} (PWM) DIAG_MODE = 1	diag_reg_c (binary, MSB – LSB)	SENT Data (binary, DIAG[7:4] DIAG[3:0])
Overvoltage Condition [1]	Overvoltage detection is enabled, device lock is set, OVD_DIS = 0, MEM_LOCK = 6 or 12.	½ carrier frequency 40.4% DC	See SENT, SCN nibble bit 1 = 1	High impedance	XXX1 XXXX	XXX1 XXXX
Undervoltage Condition	Undervoltage detection is enabled, INTREF_DIS = 0.	½ carrier frequency 11.6% DC	See SENT, SCN nibble bit 1 = 1	High impedance	XXXX 1XXX	XXXX 1XXX
Signal Path Monitor	Signal Path monitor is enabled, SPERR_CFG = 0,1, or 2. (SPERR_CFG = 2 recommended.)	½ carrier frequency 30.8% DC	See SENT, SCN nibble bit 0 = 1	High impedance	XXXX X1XX	XXXX X1XX
Temperature Condition	Temperature error detection is enabled, TMP_DIS = 0, overtemperature error	½ carrier frequency 50% DC	See SENT, SCN nibble bit 1 = 1	High impedance	XX1X XXXX	XX1X XXXX
	Temperature error detection is enabled, TMP_DIS = 0, low temperature error	½ carrier frequency 59.6% DC				
Signal Out of Range, Low	Signal Out of Range detection is enabled, and diagnostic output is set for advanced output flag, OOR_DIS = 0.	½ carrier frequency 69.2% DC	See SENT, SCN nibble bit 1 = 1	High impedance	X1XX XXXX	X1XX XXXX
Signal Out of Range, High	Signal Out of Range detection is enabled, and diagnostic output is set for advanced output flag, OOR_DIS = 0.	½ carrier frequency 78.8% DC	See SENT, SCN nibble bit 1 = 1	High impedance	1XXX XXXX	1XXX XXXX
EEPROM Fault (2-bit error detection)		High impedance	High impedance	High impedance	XXXX XXX1	High impedance

[1] An Overvoltage Condition will cause the device to enter Programming Mode which will result in the output being in a high-impedance state when mem_lock is not set to a value of 12.

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Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switch point accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 64 kHz high frequency clock. For demodulation process, a sample-and-hold technique is used, where the sampling is performed at twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

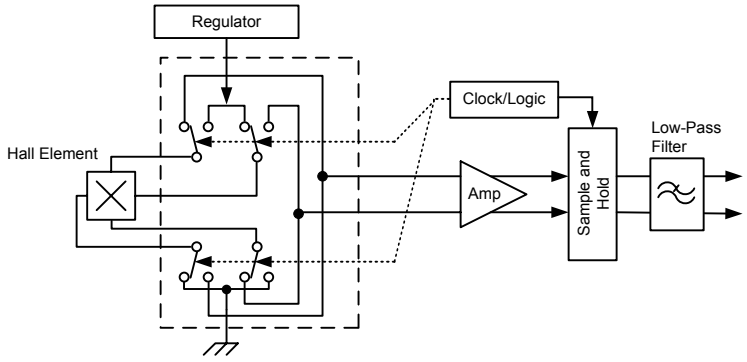

Figure 5: Model of Chopper Stabilization Technique

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Signal Path

Each die in the A31102 contains a Hall-effect transducer that produces a signal proportional to the magnetic flux density perpendicular to the face of the package, referred as the applied magnetic flux density. The output of the Hall transducer is then amplified and digitized. The resulting signal is a signed digital value that can be scaled, offset, and compensated to achieve a desired output. The advanced digital parameters allow for a large range of input signals to be adjusted for the application. This results in the A31102 being highly flexible and accurate for applications with challenging sensing requirements. The following sections give an overview of digital signal path blocks and the corresponding transfer functions.

FILTER BLOCK

Each die in the A31102 contains a configurable low-pass IIR filter. The filter response is adjustable using the EEPROM parameter BW_SEL. The filter incorporates an additional adaptive control feature. When enabled, the adaptive control adjusts the bandwidth based on the input signal. This allows the filter to potentially perform with faster response and lower steady-state noise performance. The adaptive control is tuned using EEPROM parameters. The parameter BW_SEL_MIN sets the maximum bandwidth (minimum code), parameter BW_SEL sets the minimum bandwidth (maximum code), and FILT_ADA_GAIN sets the sensitivity of the adaptive bandwidth adjustment. Higher values of FILT_ADA_GAIN result in faster response times but are less effective in reducing noise. Lower values for FILT_ADA_GAIN result in slower response times but are more effective in reducing noise. Setting FILT_ADA_GAIN to a value of zero disables the adaptive control and the filter responds as a typical low pass IIR with the 3 dB frequency set by BW_SEL.

COMPENSATION BLOCK

The compensation block contains adjustments to the Sensitivity and Offset. This includes compensation for input signal changes over the operating temperature range. First, the Sensitivity Trim Block multiplies the signal by a temperature-dependent gain (or attenuation) factor. The correction is segmented into two regions: hot and cold, where hot indicates ambient temperatures greater or equal to 25°C, and cold indicates ambient temperatures lesser or equal to 25°C. Each segmented region also contains 1st and 2nd order Sensitivity temperature compensation.

Note: The hot Sensitivity temperature compensation is independent of the cold region.

Equation 1 and Equation 2 show the transfer function of the Sensitivity Trim Block.

Included in the transfer functions shown in Equation 1 and Equation 2 is the conversion from the applied magnetic input to a digital value, $B_{IN} \times SENS_{INIT}$.

The output of the Sensitivity Trim Block, Y_1, is a 16-bit signed integer.

The Offset Trim Block adds a temperature-dependent factor to the input signal. The offset factor is segmented into two regions: hot and cold, as defined in the Sensitivity Trim Block. Each segment contains 1st order Offset temperature compensation. Equation 3 and Equation 4 show the transfer functions of the Offset Trim Block. The output, Y_2, is a 16-bit signed integer and is the value passed out of the Compensation Block.

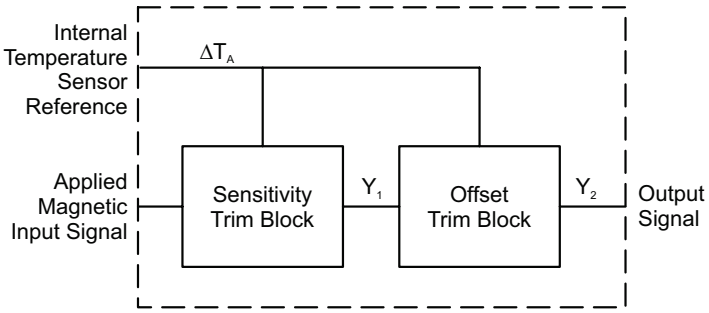

Figure 6: Compensation Block

Equation 1, Output from the sensitivity trim block. $T_A \geq 25°C$.

$$Y_1 = B_{IN} \times SENS_{INIT} \times POL_C \times SENS_{MC} \times SENS_C \times [1 + (SENS_{TC2\_HOT\_C} / 1000 \times \Delta T_A + SENS_{TC1\_HOT\_C}) \times \Delta T_A / 100]$$

Equation 2, Output from the sensitivity trim block. $T_A \leq 25°C$.

$$Y_1 = B_{IN} \times SENS_{INIT} \times POL_C \times SENS_{M\_C} \times SENS_C \times [1 + (SENS_{TC2\_CLD\_C} / 1000 \times \Delta T_A + SENS_{TC1\_CLD\_C}) \times \Delta T_A / 100]$$

Equation 3, Output from the offset trim block. $T_A \geq 25°C$.

$$Y_2 = Y_1 + QO_C + QO_{TC\_HOT\_C} \times \Delta T_A$$

Equation 4, Output from the offset trim block. $T_A \leq 25°C$.

$$Y_2 = Y_1 + QO_C + QO_{TC\_CLD\_C} \times \Delta T_A$$

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Table 3: Compensation Block Parameters

Variable	Description	Programmable Parameter (Memory Location)	Units
POL_C	Determines the sensitivity polarity. The default polarity is increasing with output with increasing applied south magnetic flux density.	POL_C (Register SENS_TRIM_C 0x3 [15])	NA
$SENS_{M\_C}$	Coarse Sensitivity multiplier	SENSM_C (Register SENS_TRIM_C 0x3 [14:12])	NA
$SENS_C$	Fine Sensitivity multiplier	SENS_C (Register SENS_TRIM_C 0x3 [10:0])	NA
$SENS_{TC2\_HOT\_C}$	2nd order Sensitivity temperature compensation for $T_A \geq 25°C$	SENSTC2_HOT_C (Register SENSTC2_C 0x5 [9:0])	m%/°C²
$SENS_{TC1\_HOT\_C}$	1st order Sensitivity temperature compensation for $T_A \geq 25°C$	SENSTC1_HOT_C (Register SENSTC1_C 0x4 [10:0])	%/°C
$SENS_{TC2\_CLD\_C}$	2nd order Sensitivity temperature compensation for $T_A \leq 25°C$	SENSTC2_CLD_C (Register SENSTC2_C 0x5 [21:12])	m%/°C²
$SENS_{TC1\_CLD\_C}$	1st order Sensitivity temperature compensation for $T_A \leq 25°C$	SENSTC1_CLD_C (Register SENSTC1_C 0x4 [22:12])	%/°C
ΔT_A	Change in ambient temperature in relation to room temperature (25°C)	n/a	°C
QO_C	Fine quiescent output adjustment	QO_C (Register QO_TRIM_C 0x6 [17:0])	LSB
$QO_{TC\_HOT\_C}$	1st order quiescent output temperature drift compensation for $T_A \geq 25°C$.	QOTC_HOT_C (Register QOTC_C 0x7 [11:0])	LSB/°C
$QO_{TC\_CLD\_C}$	1st order quiescent output temperature drift compensation for $T_A \leq 25°C$.	QOTC_CLD_C (Register QOTC_C 0x7 [23:12])	LSB/°C
$SENS_{INIT}$	Initial Sensitivity	n/a	LSB/G
B_{IN}	Applied magnetic flux density	n/a	G

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LINEARIZATION

The A31102 includes features to compensate for nonlinear inputs. The Linearization block passes the output from the Compensation block through a piecewise-linear transfer function of up to 16 line segments. The individual segments are defined by points set by the linearization coefficients. Each coefficient represents a delta output value. These coefficients are programmable and are stored as 13-bit signed words in EEPROM, register group LIN_C. Values between the points defined by the linearization coefficients are linearly interpolated.

The linearization feature operates in one of two possible modes: Lin and Bin mode. Lin mode is a fixed-point mode, where a set number of points, 17, are distributed evenly among the output range 0-100%. The linearization coefficients LINT00-LINT016 are calculated at each point. Bin mode is defined by variable segments, where the linearization table entries are divided in half. Entries LINT00-LINT07 are the linearization coefficients, and entries LINT08-LINT15 are input locations. The location values are stored as 13-bit unsigned integer values representative of a fractional amount of the input span; see Equation 5. The linearization coefficients for either Lin or Bin mode are 13-bit values represented by Equation 6. Note that the input to the Linearization block must be monotonically increasing. In Lin mode, the range of the linearization coefficients is ±25% of the full output range. It is possible to increase the range to ±50% by using the parameter lin_scalar. The linearization table entries are shown in Table 4.

Equation 5: $$Loc_x = Y_{2x} \times 2^{-3} + 2^{12}$$

where Y_{2x} is a signed integer value of the input to the linearization block at location x, and Loc_x is an unsigned integer with a range of 0 to $2^{13} - 1$.

Equation 6:

If LINT_BIN_E = 0 (Lin mode)

$$YLin_x = k_x \times 2^{-2}$$

where k_x is a signed integer of the delta output, or error, at the input location x, and $YLin_x$ is a signed integer with a range of -2^{12} to $2^{12} - 1$.

If LINT_BIN_E = 1 (Bin mode)

$$YLin_x = Y_{3x} \times 2^{-3} + 2^{12}$$

where Y_{3x} is a signed integer of the desired linearization block output at the input location x, and $YLin_x$ is an unsigned integer with a range of 0 to $2^{13} - 1$.

Table 4: LIN_COEFF Map for Fixed Point (Left) and Movable Point (Right) Modes

Linearization Parameter	Linearization Table Entry		Register Location
	Lin Mode	Bin Mode	
LINT00	$YLin_{(0)}$	$Loc_{(0)}$	LIN0_C 0x0A [12:0]
LINT01	$YLin_{(1)}$	$Loc_{(1)}$	LIN0_C 0x0A [25:13]
…	…	…	…
LINT07	$YLin_{(7)}$	$Loc_{(7)}$	LIN3_C 0x0D [25:13]
LINT08	$YLin_{(8)}$	$YLin_{(0)}$	LIN4_C 0x0E [12:0]
LINT09	$YLin_{(9)}$	$YLin_{(1)}$	LIN4_C 0x0E [25:13]
…	…	..	…
LINT15	$YLin_{(15)}$	$YLin_{(7)}$	LIN7_C 0x11 [25:13]
LINT16	$YLin_{(16)}$	$YLin_{(8)}$	LIN0_C 0x12 [12:0]

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Linearization Mode (Lin Mode)

Figure 7 shows the standard transfer function for a monotonically increasing input. The blue line represents the nonlinearized raw input to the linearization block. The points on the x-axis, B_{IN}, are at equally spaced intervals based on the number of linearization coefficients, 17. The coefficients at the points $B_{IN(x)}$ are calculated using the delta output between the input function and the desired output function. The coefficients are stored in the corresponding memory location shown in Table 4.

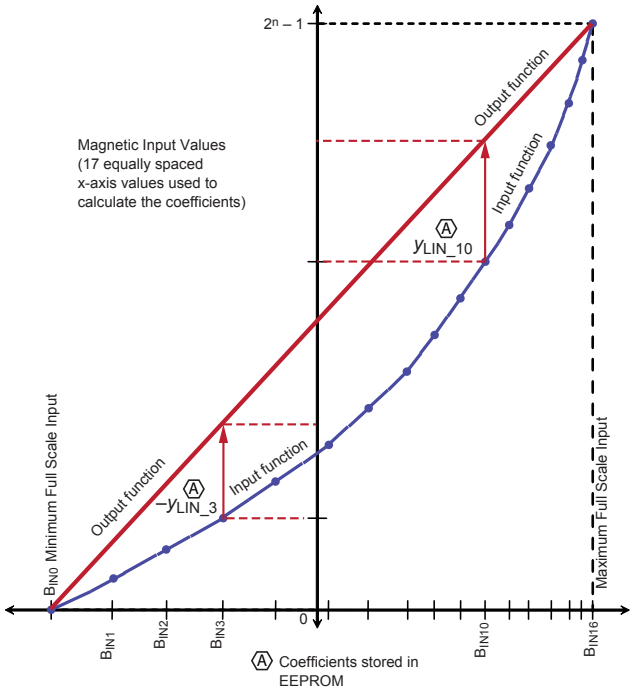

Figure 7: Linearization Example (Lin Mode)

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Linearization Binning Mode (Bin Mode)

When binning mode is selected, the output is no longer interpolated between the linearization coefficients. In the case of Bin Mode, the coefficients ($Ylin_x$) determine a discrete output level for the bin range at the locations defined by the corresponding LOC_x. The discrete output values are determined by a step function shown in Equation 7. It is possible to add hysteresis by setting the parameter LINT_BIN_HYST. The hysteresis is only applied when the output is decreasing.

Equation 7:

$$Y3 = \left\{ \begin{array}{c} -2^{15}, \ \ if\ Y2 < (8 \times (\mathrm{Loc}_0 - 2^{12}) - \mathrm{lint\_bin\_hyst} \times 2\ )\ and\ Loc_{(0)} \neq 0 \\ YLin_x, \ if\ (8 \times (\mathrm{Loc}_x - 2^{12}) - \mathrm{lint\_bin\_hyst} \times 2) < Y2 \leq 8 \times (Loc_{(x+1)} - 2^{12}) \\ YLin_{(7)}, \ \ if\ Y2 > 8 \times (\mathrm{Loc}_7 - 2^{12}) \end{array} \right\}$$

*If signal is increasing then lint_bin_hyst = 0

Figure 8 shows the simulated output of a device setup with evenly spaced output levels and bin values. The hysteresis, specified by LINT_BIN_HYST, is applied when the digital value is decreasing to prevent bouncing between linearization bin values.

The Linearization coefficients and corresponding parameters are stored in Table 5.

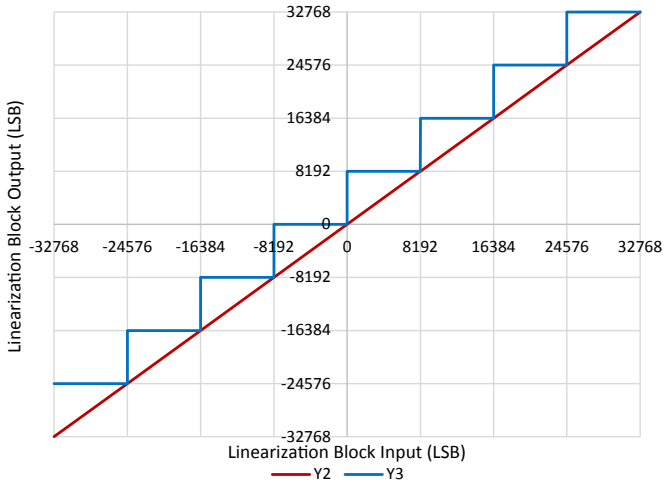

Figure 8: Linearization Output Example (Bin Mode)

Table 5: Linearization Algorithm Block Parameters

Parameter	Description	Memory Location	Units
LINT00, LINT02…LINT14, LINT16	Even Linearization Coefficients.	LIN0_C … LIN8_C	LSB
LINT01, LINT03…LINT13, LINT15	Odd Linearization Coefficients.	LINT0_C … LIN7_C	LSB
LINT_E	Set to logic 1 to enable the Linearization table.	LIN8_C 0x12 [13]	NA
LINT_BIN_E	Set to logic 1 to enable linearization binning mode.	LIN8_C 0x12 [14]	NA
LINT_OUT_INV	Set to logic 1 to Invert output of linearization block.	LIN8_C 0x12 [15]	NA
LINT_IN_INV	Set to logic 1 to Invert input of linearization block.	LIN8_C 0x12 [16]	NA
LINT_BIN_HYST	Hysteresis setting for linearization binning mode.	LIN8_C 0x12 [24:17]	LSB
LIN_SCALAR	Adjusts the range of the linearization coefficients. When set to logic 1 the linearization coefficients are multiplied by a factor of 2.	LIN8_C 0x12 [25]	NA

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POST-LINEARIZATION TRIM

An additional gain and offset trim stage is available in the linearization block. This can be used to attenuate or gain the signal. Using Post-Linearization with signal attenuation may be useful to extend the input to the linearization block to all 17 linearization points when the final output range is not full-scale. Equation 8 shows the transfer function for the Post Linearization. The output of the Post Linearization Block, Y_4, is a 16-bit signed integer.

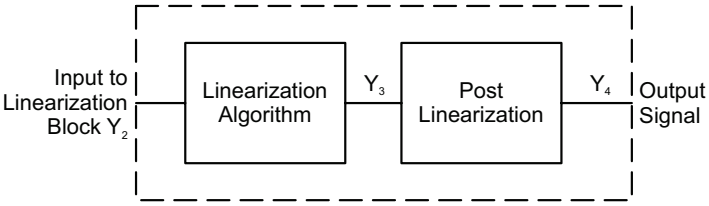

Figure 9: Linearization Block

Equation 8:

$$Y_4 = Y_3 \times (1 + PLIN_{SENS}) + PLIN_{QVO}$$

CLAMP

The clamp block limits the output to a programmable range set by the parameters CLAMPH and CLAMPL, register CLAMP_C 0x8. Clamps are programmable throughout the full output range. If the input to the clamp block is greater than the value set by CLAMPH, the output is limited to the upper clamp value. Similarly, if the input to the clamp block is less than the value set by CLAMPL, the output is limited to the lower clamp value. If the lower clamp exceeds the upper clamp, the output is undefined. Note that the input to the clamp block is a 16-bit signed value and is changed to a 16-bit unsigned value before comparing to the upper and lower clamp values. Equation 9 and Equation 10 show the transfer functions for the clamp block. The output of the Clamp Comparison is a 16-bit unsigned integer and is passed to the output block.

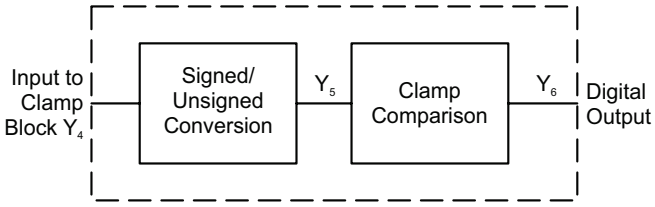

Figure 10: Clamp Block

Equation 9:

$$Y_5 = Y_4 + 2^{15} \text{ (conversion from signed to unsigned)}$$

Equation 10:

$$\text{if } (Y_5 > CLAMP_H), \text{ then } Y_6 = CLAMP_H$$
$$\text{else if } (Y_5 < CLAMP_L), Y_6 = CLAMP_L$$
$$\text{else } Y_6 = Y_5$$

Table 6: Post-Linearization Trim Memory Parameters

Variable	Step Size	Min.	Max.	Description	Parameter (Memory Location)	Units
$PLIN_{SENS}$	2^{-11}	−1	+1	Customer post-linearization sensitivity adjustment	PLIN_SENS, (POST_LIN_C 0x13 [11:0])	NA
$PLIN_{QVO}$	2^4	−32768	+32752	Customer post-linearization offset adjustment	PLIN_QVO, (POST_LIN_C 0x13 [23:12])	LSB

Table 7: Clamp Block Parameters

Variable	Step Size	Min.	Max.	Description	Programmable Parameter (Memory Location)	Units
$CLAMP_H$	2^4	16	65535	Determines the upper clamp value	CLAMPH (register CLAMP_C 0x8[11:0])	LSB
$CLAMP_L$	2^4	0	65520	Determines the lower clamp value	CLAMPL (register CLAMP_C 0x8[23:12])	LSB

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Linear Output Protocols

The A31102 operating output is a digital voltage signal that transfers information proportionally to the applied magnetic input signal. Two customer-selectable options are provided for output signal formatting: pulse-width modulated (PWM) and single edge nibble transmission encoding scheme (SENT, SAEJ2716).

Note: The device response to the applied magnetic field is on the OUT pin. The pin also functions as a transmit and receive data pin in response to serial programming commands, during which the normal output operation is suppressed. Refer to the Programming Serial Interface section for more information. The EEPROM is described in the EEPROM Structure section.

The output falling edge slew rate is adjustable using the OUT-DRV_SEL parameter. Adjusting this can improve EMC performance by reducing high-frequency currents. This parameter can also increase the output fall time and result in longer minimum pulse durations for serial communication or SENT transmission.

PWM OUTPUT MODE

PWM output mode modulates the output voltage to a series of constant-frequency binary pulses, with the percentage of the high portion of the pulse varied in direct proportion to the Digital Output (value at the output of the Clamp Block).

- OUTMSG_MODE (register OUT_CFG_C 0x14 bits [2:0]) set to 0 to select the PWM option (for programming parameters, see EEPROM Structure section)
- SENT_PWM_RATE (register OUT_CFG_C 0x14 bits [6:3]) sets the PWM carrier frequency

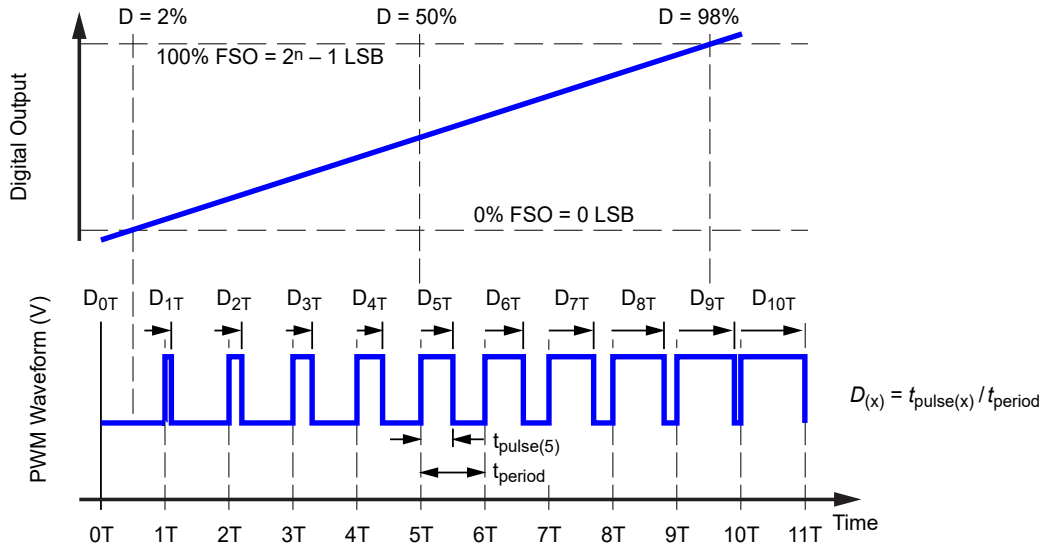

Figure 11: PWM mode outputs a duty cycle-based waveform that can be read by the external controller as a cumulatively changing continuous voltage; n = 16

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SENT OUTPUT MODES

The SENT output mode converts the Digital Output (value at the output of the Clamp Block) to a series of digital pulses with data encoded as falling to falling edge periods, shown in Figure 12. The data, along with additional information, is communicated in a message, referred to as a frame, that conforms to the SENT transmission specification (SAEJ2716 JAN2010). The A31102 contains features for enhanced SENT modes beyond the industry standard. The enhanced modes offer greater flexibility for application use. Certain parameters for configuration of the SENT messages are adjustable in EEPROM.

The SENT output modes are selected by setting the following parameters in EEPROM:

- SAE J2716 SENT with enhancement options (OUTMSG_MODE = 1).
- Triggered SENT; TSENT (OUTMSG_MODE = 2,6,7); user defines sampling and data retrieving.
- Sequential SENT; SSENT; user requests data from multiple devices on the SENT line in sequential order (OUTMSG_MODE = 4 for SHORT_TRIGGER and OUTMSG_MODE = 3 for LONG_TRIGGER). Short and long trigger modes can be differentiated on the length and number of host function/request pulses.
- Addressable SENT; ASENT; user requests data from any device on the SENT line in any order. (OUTMSG_MODE = 5).
- Additional configuration parameters in register 0x14, OUT_CFG_C.

MESSAGE STRUCTURE

A SENT message is a series of nibbles with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.
- The low interval, SENT_FIXED, is defined as 5 SENT ticks. The high interval contains information and is variable in duration to indicate the data payload of the nibble.

The duration of a nibble is denominated in clock ticks. The period of a tick is set by SENT_PWM_RATE parameter as in Table 15. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The nibbles of a SENT message are arranged in the following required sequence (see Figure 12):

1. Synchronization and Calibration: flags the start of the SENT message
2. Status and Communication: provides A31102 status and the format of the data
3. Data: magnetic and optional data
4. CRC: error checking
5. Pause Pulse: sets timing relative to A31102 updates

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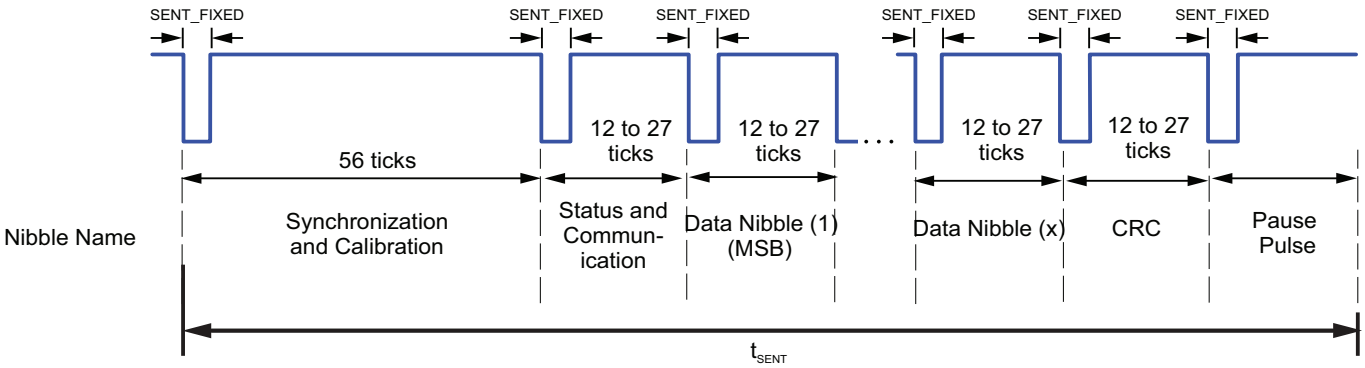

Figure 12: General Format for SENT Message Frame

Table 8: SENT Trigger Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
SENT Output Trigger Signal	$V_{SENTtrig(L)}$	SENT_HYST_CFG = 0 , 2	1.38	–	1.89	V
		SENT_HYST_CFG = 1 , 3	0.87	–	1.28	V
	$V_{SENTtrig(H)}$	SENT_HYST_CFG = 0 , 1	2.07	–	2.58	V
		SENT_HYST_CFG = 2 , 3	1.84	–	2.22	V
SENT Output Trigger Signal	$V_{SENTtrig(HYST)}$	SENT_HYST_CFG = 0	0.51	–	0.87	V
		SENT_HYST_CFG = 1	1	–	1.5	V
		SENT_HYST_CFG = 2	0.21	–	0.6	V
		SENT_HYST_CFG = 3	0.74	–	1.19	V
SENT Output Trigger Edge Filter	$V_{SENTtrig(f)}$		–	0.35	–	µs

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OPTIONAL SHORT SERIAL MESSAGE

The A31102 SENT output supports an optional mode to transmit additional data. The slow serial mode, enables transmission of additional data by encoding information in the Status and Communication (SCN) nibbles. The encoded data is captured over several transmissions and is then decoded to indicate additional short serial message data. For more details on the short serial message, refer to the SENT SAEJ2716 specification. The slow serial mode is enabled when the EEPROM parameter SENT_SCN_CFG = 0 or 3. Following a reset, the first message transmitted is 0, following in order of the message ID, and then repeating. Table 10 identifies the data sent with each message ID. The CRC for the Short Serial Message is derived for the Message ID and data, and is the same checksum algorithm used for the SENT CRC.

Table 9: Short Serial Message Format in SENT Status and Communication Nibble

SCN Bit when SENT_SCN_CFG = 0 or 3	Nibble #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Bit 3 (Start Bit)	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 2 (Serial Data)	Message ID				Data								CRC			
Bit 1 (Soft Error Diagnostic Bit)	See Table 2: Diagnostic Summary Table															
Bit 0 (Hard Error Diagnostic Bit)	See Table 2: Diagnostic Summary Table															

Table 10: SENT Slow Serial Data

Message ID	Data
0	8-bit temperature value from internal temperature sensor. Ambient temperature (°C) = 8-bit signed temperature value + 25°C.
1	Error status from the parameter DIAG_REG_C located in register ERR_STATUS_C, 0x45 bits [23:16].
2	ID_C[7:0] (Customer ID, EEPROM 0x2)
3	ID_C[15:8] (Customer ID, EEPROM 0x2)
4	ID_C[21:16] (Customer ID, EEPROM 0x2)
5-15	Unused

The SCN bits 2 and 3 are also selectable to indicate the die address of the sensor on the shared SENT line (SENT_SCN_CFG = 2), or all zeros (SENT_SCN_CFG = 1). The available configuration options for the SCN nibble are shown in Table 11.

Table 11: SCN Nibble Configuration Options

Parameter SENT_SCN_CFG	SCN Bit #3	SCN Bit #2	SCN Bit #1	SCN Bit #0
0	Short Serial Message	Short Serial Message	Diagnostic Bit, See Table 2	Diagnostic Bit, See Table 2
1	0	0		
2	DIE_ADDR_1	DIE_ADDR_0		
3	Short Serial Message	Short Serial Message		

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DATA NIBBLE FORMAT

The A31102 SENT output supports options for the message data nibble format. The data nibble format is determined by the EEPROM parameter SENT_DATA_CFG. The options for either a minimum 3 or maximum 6 nibbles of data is defined in Table 12. Where:

- MAG_OUT: [15:4] 12-bit, [15:0] 16-bit, magnetic digital output data (value at the output of the Clamp Block).
- COUNT: [11:0] 12-bit, [7:0] 8-bit, [3:0] 4-bit SENT frame count. The counter increments once for every frame that is sent up to the maximum count. At the next count, after the maximum, the counter starts again at 0.
- TEMP_OUT: [11:0] 12-bit, [11:4] 8-bit signed output from the internal temperature sensor. Ambient temperature (°C) = 12-bit signed temperature value / 8 (LSB / °C) + 25.
- DIAG: [7:0] 8 Diagnostic flags = DIAG_REG_C [7:0].

Table 12: SENT Data

SENT_DATA_CFG	Data Nibble #1	Data Nibble #2	Data Nibble #3	Data Nibble #4	Data Nibble #5	Data Nibble #6	# of Nibbles
0	MAG_OUT [15:12]	MAG_OUT [11:8]	MAG_OUT [7:4]	–	–	–	3
1	MAG_OUT [15:12]	MAG_OUT [11:8]	MAG_OUT [7:4]	DIAG[7:4]	DIAG[3:0]	COUNT[3:0]	6
2	MAG_OUT [15:12]	MAG_OUT [11:8]	MAG_OUT [7:4]	COUNT[11:8]	COUNT[7:4]	COUNT[3:0]	6
3	MAG_OUT [15:12]	MAG_OUT [11:8]	MAG_OUT [7:4]	TEMP_OUT[11:8]	TEMP_OUT[7:4]	TEMP_OUT[3:0]	6
4	MAG_OUT [15:12]	MAG_OUT [11:8]	MAG_OUT [7:4]	MAG_OUT [3:0]	–	–	4
5	MAG_OUT [15:12]	MAG_OUT [11:8]	MAG_OUT [7:4]	MAG_OUT [3:0]	DIAG[7:4]	DIAG[3:0]	6
6	MAG_OUT [15:12]	MAG_OUT [11:8]	MAG_OUT [7:4]	MAG_OUT [3:0]	COUNT[7:4]	COUNT[3:0]	6
7	MAG_OUT [15:12]	MAG_OUT [11:8]	MAG_OUT [7:4]	MAG_OUT [3:0]	TEMP_OUT[11:8]	TEMP_OUT[7:4]	6

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CHECKSUM (CRC) NIBBLE

The CRC consists of 4 bits derived from the data nibbles only. The CRC is calculated using the polynomial $x^4 + x^3 + x^2 + 1$ with a seed of 4'b0101. There is an option that SCN is included into the CRC nibble (SEN_CRC_CFG = 1, includes SCN into CRC).

OUTPUT DRIVER FALL TIME SELECTION

The fall time of the output digital signal is adjustable using the EEPROM parameter OUTDRV_SEL. See Table 13.

Table 13: Code vs C_{OUT} for OUTDRV_SEL

Function	Output Signal Configuration. Sets configuration of the output signal slew-rate control. Sets the ramp rate on the gate of the output driver, thereby changing slew rate at the output.		
Syntax	Field width: 3 bits		
Related Commands	–		
Values	Code	Fall Time (Typical) (µs)	
		C_{OUT} = 100 pF	C_{OUT} = 1 nF
	0 (Default)	0.04	0.12
	1	0.10	0.17
	2	0.18	0.25
	3	0.26	0.33
	4	0.67	0.70
	5	1.35	1.29
	6	2.80	2.58
	7	4.02	3.73
Options	Values calculated from a small number of samples with a capacitor from output to ground to simulate load capacitance. $R_{L(PULLUP)}$ = 1.2 kΩ was used.		
Examples	–		

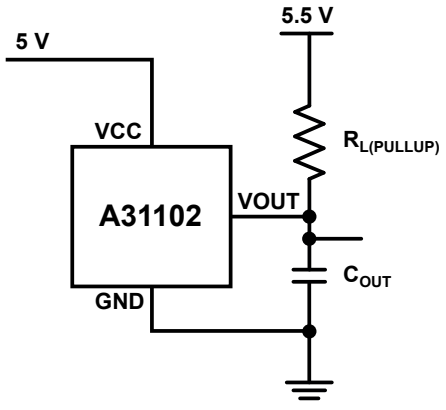

Figure 13: Fall Time Test Circuit

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Table 14: Message Frame Section Definitions

Section	Description
SYNCHRONIZATION AND CALIBRATION	
Function	Provide the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section, for ease of distinction by the external controller.
Syntax	Nibbles: 1 Quantity of ticks: 56 Quantity of bits: 1
STATUS AND COMMUNICATION	
Function	Provides the external controller with the status of the A31102 and indicates the format and contents of the Data section.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 Quantity of bits: 4 1:0 Device status (see Table 2) 3:2 Message serial data protocol (SENT_SCN_CFG)
DATA	
Function	Provides the external controller with data selected by the SENT_DATA_CFG parameter.
Syntax	Nibbles: 3 to 6 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4 (each nibble)
CRC	
Function	Provides the external controller with cyclic redundancy check (CRC) data for certain error detection routines applied to the Data nibbles and to the Status information.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4
PAUSE PULSE	
Function	Additional time is added at the end of a SENT message frame to ensure all message frames are of appropriate length and correlate to the internal update rate of the device.
Syntax	Nibbles: NA Quantity of ticks: Quantity of bits: NA
TRIGGER PULSE	
Function	(Optional) Allow the external controller to determine when to transmit data.
Syntax	Nibbles: NA Minimum Trigger length is determine by the TRIGGER_CFG parameter for TSENT and F_OUTPUT for ASENT and SSENT.

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SAEJ2716 SENT AND TSENT

The A31102 SENT output is configurable for four transmission modes: Internal Synchronous (SENT) Mode, Trigger (TSENT) Mode, Sequential (SSENT) Mode, or Addressable (ASENT) Mode. The transmission modes are configured by setting the parameter OUTMSG_MODE.

When configured for Internal Synchronous Mode, OUTMSG_MODE = 1, the SENT output transmits continuously while in normal operating conditions. The pause pulse has a minimum length of twelve ticks and is extended to correlate with the internal update rate at the start of the Synchronization pulse; see Figure 14.

When configured for External Trigger Mode, OUTMSG_MODE = 2, 6 or 7, the SENT output transmits when requested by the external controller. The pause pulse is extended until the next trigger pulse; see Figure 15 and Figure 16.

The external controller initiates a trigger pulse by holding the output pin low. The minimum width of the trigger pulse is set by the parameter TRIGGER_CFG. The SENT frame is transmitted when the external controller releases the output, the rising edge of the trigger pulse. After the rising edge of the trigger pulse, the output remains high for a minimum of seven SENT tick times before going low to initiate the start of the SENT synchronization pulse.

For TSENT Synchronous Mode, OUTMSG_MODE = 6 or 7, the data sample is latched at the falling edge of the trigger pulse; see Figure 16. For TSENT Asynchronous Mode, OUTMSG_MODE = 2, the data sample is latched at end of the SCN nibble; see Figure 15.

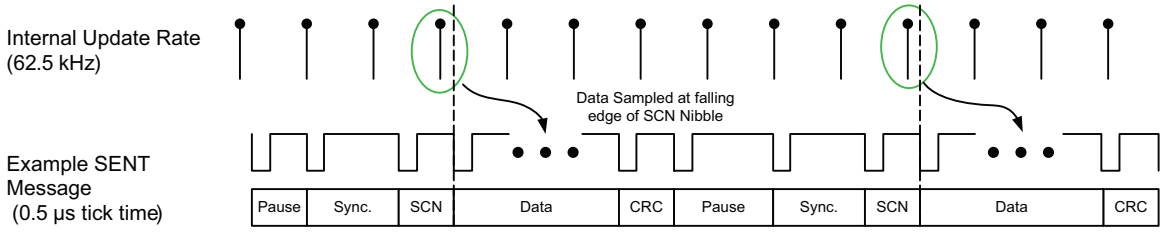

Figure 14: SENT Data Synchronization with Output Data and Internal Synchronous Mode (Figure not drawn to scale)

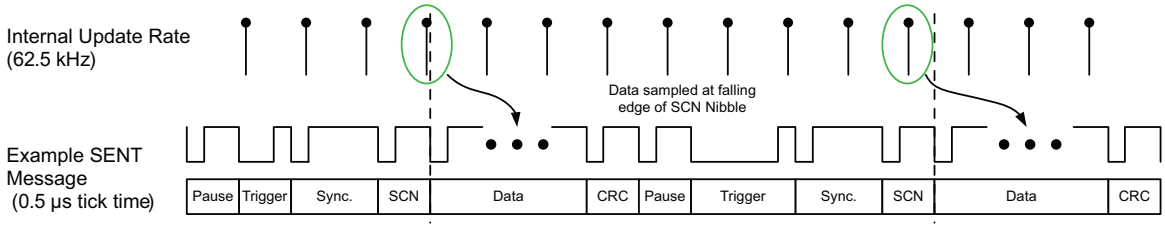

Figure 15: SENT Data Synchronization with Output Data and External Trigger Asynchronous Mode (Figure not drawn to scale)

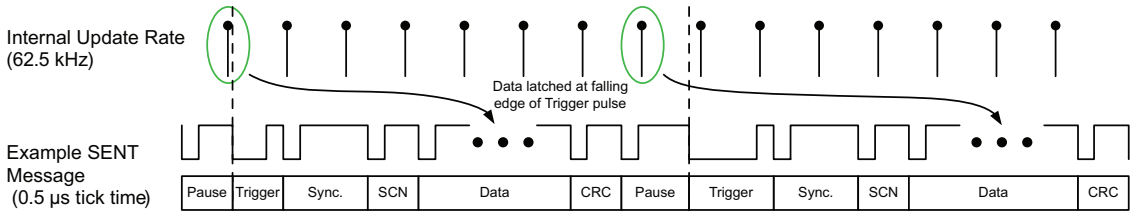

Figure 16: SENT Data Synchronization with Output Data and External Trigger Synchronous Mode (Figure not drawn to scale)

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Table 15: PWM Frequency/SENT Tick Times

PWM/SENT Code	SENT / TSENT / ASENT / SSENT	PWM
	Tick Time (µs) [1]	f_{PWM} (Hz)
0	1	125
1	0.25 (not supported)	167
2	0.375 (not supported)	250
3	0.5	333
4	0.625	500
5	0.75	667
6	0.875	800
7	1.0	1000
8	1.125	1333
9	1.25	1600
10	1.375	2000
11	1.5	2667
12	1.625	4000
13	1.75	5333
14	1.875	8000
15	2.0	16000
16	2.125	–
17	2.25	–
18	2.375	–
19	2.5	–
20	2.625	–
21	2.75	–
22	2.875	–
23	3.0	–
24	3.5	–
25	4.0	–
26	4.5	–
27	5.0	–
28	5.5	–
29	6.0	–
30	7.0	–
31	10.0	–

[1] Tick Time less than 0.5 µs are not supported.

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SSENT ADDRESSING PROTOCOL

The SSENT protocol requires sensors on the bus to be polled in sequential order, meaning increasing, consecutive, and rotating order by SensorID starting with SensorID 0. The slot for a sensor is the time at which that sensor is expected to respond to an AddressingPulse and other sensors are expected not to respond.

Each sensor independently maintains a SlotCounter that is incremented each time the sensor detects an AddressingPulse of either an F_OUTPUT or F_SAMPLE pulse. This SlotCounter becomes the SlotNumber, which is used by the sensor to decide which sensor is being polled by the host. The SlotCounter is compared to the SensorID, and if they match, that sensor will respond if it is a FrameReqPulse such as an F_OUTPUT or addressed F_SAMPLE pulse with the SENT Frame, and all other sensors do not respond, although they increment their own SlotCounter. If the SlotCounter is incremented past the total number of sensors on the bus (CFG_MAX_SENSOR (0x14 [17:16])), the SlotCounter is returned to 0. Each sensor must be programmed consistently with the total number of sensors so they all roll over to 0 at the same count. Sensors do not increment their SlotCounter on a BroadcastPulse.

The SSENT protocol relies on each sensor maintaining the exact same SlotNumber by counting the AddressingPulses. In order to synchronize all sensors to the same SlotNumber, the SSENT protocol has a broadcast F_SYNC pulse that is used by the host to force all sensors to reset their SlotCounter to 0.

To reduce the burden on the host, and also to improve detection and recovery from BusContention or system errors affecting the SENT bus, the SSENT protocol has the following Configuration options that can be selected.

- When the SENT configuration parameter slot marking is enabled, CFG_SLOT_MARKING (0x14 [23] = 1), each sensor will wait a different length of time following an AddressingPulse, based on their SensorID. This leaves the SENT bus in a high state for a varying duration before the sensor pulls the line low to begin the SENT Frame. All sensors on the bus (including the addressed sensor) measure this time to interpret the SensorID of the transmitting sensor. By comparing this to the SlotCounter, each sensor can recognize if an unexpected sensor responded to the AddressingPulse. By default, the sensor would then drop offline, since it cannot be known which sensor is out of sync. This option increases the overhead on the bus and therefore reduces the maximum rate at which sensors can be polled. SlotMarking increases the polling time of a sensor by the SlotMarking time for that sensor. All sensors on a bus must be configured with the same choice for this option.

Table 16: Slot Marking Delay Times for SSENT

SensorID	Delay Time Ticks (Nominal)
0	7
1	18
2	36
3	62

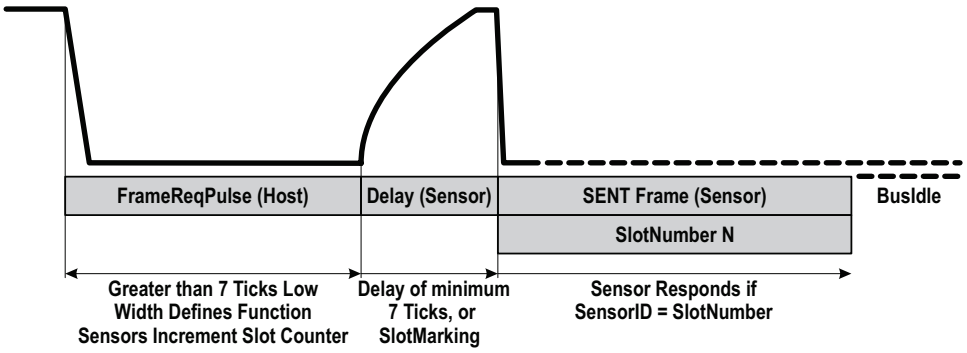

Figure 17: SSENT Sensor Addressing

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- When the SENT configuration parameter slot synchronization is enabled, CFG_SLOT_SYNC, (0x14 [24]) = 1, in conjunction with slot marking, CFG_SLOT_MARKING (0x14 [23]), a sensor that is in BusSync for a reason other than BusContention will load its SlotCounter with the measured SlotNumber from the first AddressingPulse that does not have a timeout. A sensor would normally be offline as a result of powering up, reset, or diagnostics. As long as any sensor is online and responding, this allows all other sensors that are offline to automatically synchronize their SlotCounter and begin responding correctly to future AddressingPulses targeting that sensor. If all sensors are offline, though, the host must detect that no sensor responds, and issue the F_SYNC function.
- SENT Bus Idle Configuration: When the SENT configuration parameter, CFG_SLOT_SYNC (0x14 [21]), is enabled, a sensor will monitor the bus for a long high (BusIdle) period greater than 510 ticks and reset its SlotCounter to 0. This option could be used if sensor polling is expected to always be periodic and continuous, such that the only extended BusIdle time would be after power-up.
- SENT Bus Offline Configuration: When the SENT configuration parameter CFG_POR_OFFLINE (0x14 [22]) is enabled, a sensor will stay offline until the host issues F_SYNC, or one of the other synchronization options takes effect (CFG_SLOT_SYNC 0x14 [24] or CFG_IDLE_SYNC (0x14 [21]). If disabled, a sensor will power-up with its SlotCounter set to 0, and will go directly online. This allows the sensors to initialize without any host interaction. However, if a sensor experiences a reset event after the bus is in operation, its counter may be out of sync with other sensors, and this could result in bus contention.

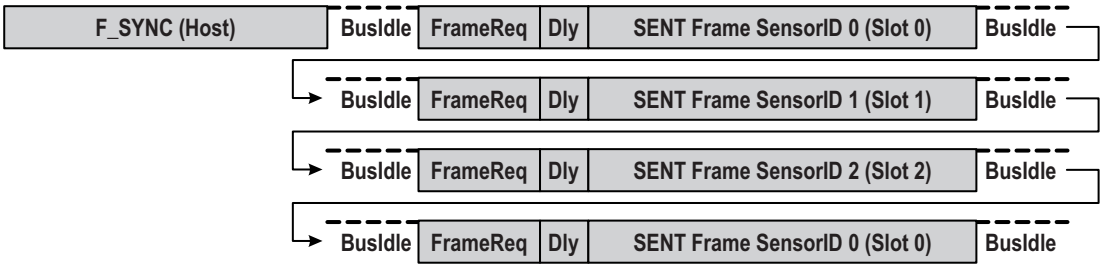

Figure 18: SSENT Sensor Addressing – No Slot Marking (3 Sensors on Bus)

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SSENT FUNCTION PULSES

SSENT has a set of function pulses where the host controller must hold the output low. The duration of the low pulse provided by the host controller defines the function, as described in Table 17 and Table 18. Following the low pulse, if the part is addressed to respond and the slot number matches the device slot counter, the device delays the output SENT frame with a minimum of 7-ticks high period to differentiate between the host trigger and the device response. For the fast tick times, the 7-tick high period may be extended to preserve a minimum time of 70.4 µs from the rising edge of the function pulse to the end of the sync pulse required for internal processing. Whether the device responds to a function pulse is defined by the purpose of each pulse.

- F_OUTPUT: Addressed sensor will return a SENT frame with sampled magnetic data. If there is data from a sample-and-hold operation available (F_SAMPLE or via CFG_ZERO_SAMPLE (0x14 [25]) = 1, then that data is returned, otherwise current data is sampled and returned. A Sensor configured with CFG_ZERO_SAMPLE (0x14 [25]) = 1 will sample-and-hold on the rising edge of the F_OUTPUT pulse for Slot 0. A Sensor configured with CFG_NO_SAMPLE (0x14 [19]) = 1 and CFG_ZERO_SAMPLE (0x14 [25]) = 0 will never sample-and-hold, thus always returns current data in response to F_OUTPUT.
- CFG_NO_SAMPLE (0x14 [19]) = 1 will sample and hold their data at the rising edge of the pulse. If CFG_FSAMPLE_ADR (0x14 [20]) = 0, this is a BroadcastPulse to a Sensor, and that Sensor will not respond. If CFG_FSAMPLE_ADR (0x14 [20] = 1, this is also an AddressingPulse to a Sensor, and the addressed sensor will return a SENT frame with either the sampled or current data. It is recommended, but not required, that all Sensors on the bus be configured the same.
- F_SYNC: All Sensors will synchronize their SlotNumbers by setting their SlotCounters such that the next AddressingPulse is for Slot 0.

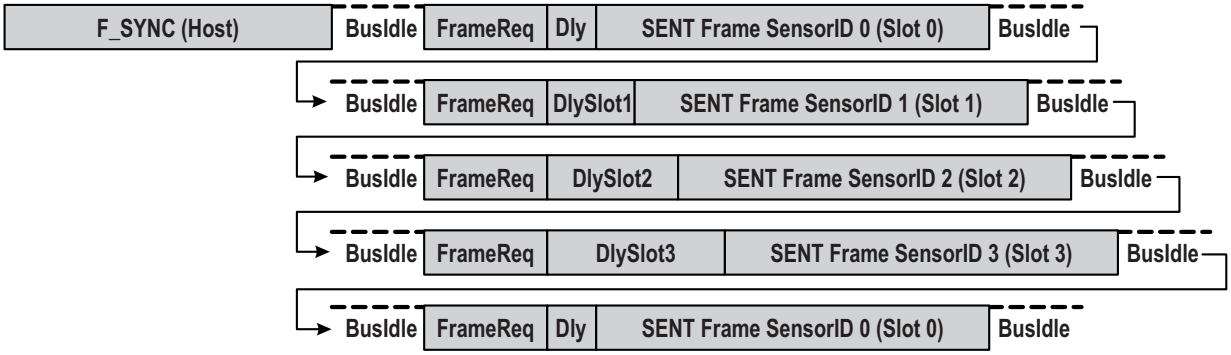

Figure 19: SSENT Sensor Addressing – with Slot Marking (4 Sensors on Bus)

Table 17: SSENT Function Pulses in SHORT_TRIGGER Mode, OUTMSG_MODE = 4

Function	Type	Min. Tick	Nom. Tick	Max. Tick
F_OUTPUT	Addressing	15	17	19
F_SAMPLE	Addressing/Broadcast	31	35	39
F_SYNC	Broadcast	93	104	115

Table 18: SSENT Function Pulses in LONG_TRIGGER Mode, OUTMSG_MODE = 3

Function	Type	Min. Tick	Nom. Tick	Max. Tick
F_OUTPUT	Addressing	9	–	81
F_SYNC	Broadcast	105	140	171

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ASENT ADDRESSING PROTOCOL

The ASENT protocol allows Sensors to be polled in an arbitrary order. The SensorID is transmitted by the Host following any AddressingPulse as a series of 0, 1, 2, or 3 IncAdrPulses. After this sequence, the SENT line is left in a high state, and each sensor will recognize after a time period of about 18 nominal ticks that there are no more IncAdrPulses coming. The sensor whose ID matches the number of IncAdrPulses received will respond.

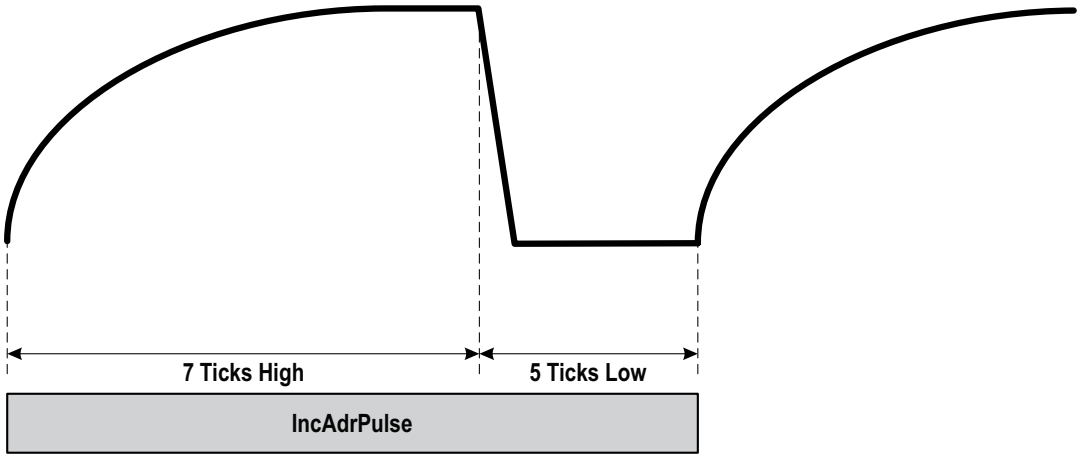

Figure 20: ASENT IncAdrPulse (output by Host)

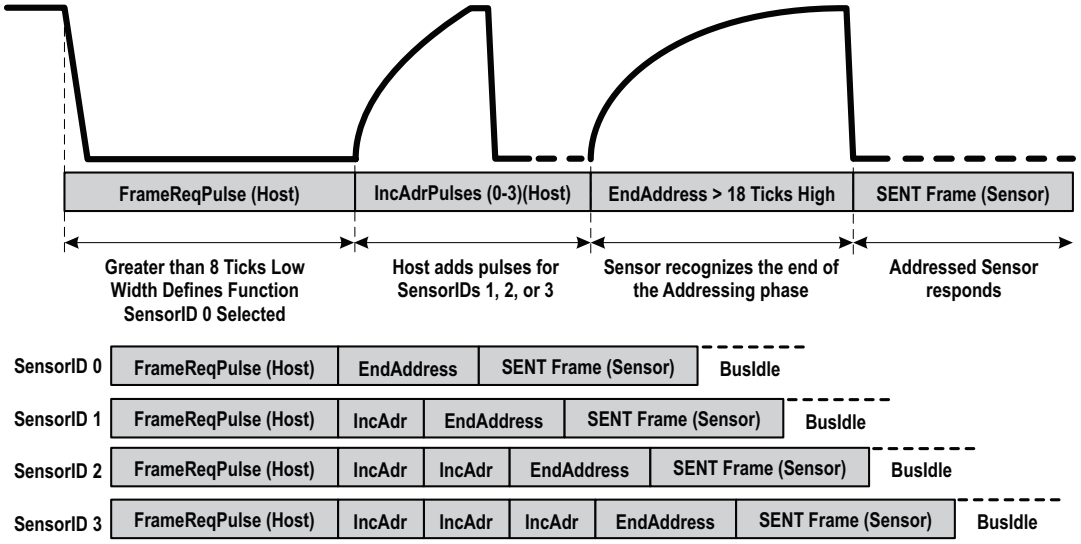

Figure 21: ASENT Sensor Addressing

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ASENT FUNCTION PULSES

- F_OUTPUT: Addressed sensor will return a SENT frame with sampled magnetic data. If there is data available from a sample-and-hold operation (F_SAMPLE), then that data is returned, otherwise current data is sampled and returned. A Sensor configured with CFG_NO_SAMPLE (0x14 [19]) = 1 will not sample-and-hold, so will always return current data in response to F_OUTPUT.
- F_SAMPLE: All sensors except those configured for CFG_NO_SAMPLE (0x14 [19]) = 1 will sample and hold their data at the rising edge of the pulse. If CFG_FSAMPLE_ADR (0x14 [20] = 0, this is a BroadcastPulse to a Sensor, and that Sensor will not respond. If CFG_FSAMPLE_ADR (0x14 [20] = 1, this is also an AddressingPulse to a Sensor, and the addressed sensor will return a SENT frame with either the sampled or current data. It is recommended, but not required, that all Sensors on the bus be configured the same.

Table 19: ASENT Function Pulses

Function	Type	Min. Tick	Nom. Tick	Max. Tick
F_OUTPUT	Addressing	15	17	19
F_SAMPLE	Addressing/Broadcast	31	35	39

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, in the A31102 using a point-to- point command/acknowledge protocol. The A31102 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no message transmitted from the A31102. If the command is a read, the A31102 responds by transmitting the requested data.

NOTE:
It is the external controller's responsibility to avoid sending a Command Frame which overlaps a Read Acknowledge frame.

The serial interface uses a Manchester encoding based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the A31102: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the A31102 in response to a Read command.

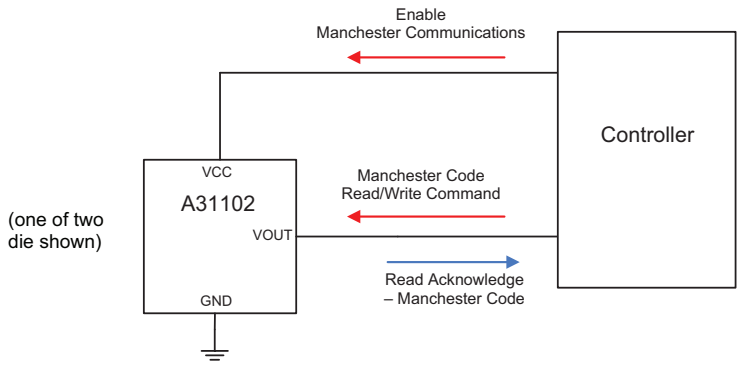

Figure 22: Top-Level Programming Interface

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PROGRAMMING INFORMATION

The A31102 device features two methods for establishing serial communications. One is a three-wire programming interface, where the input signal on VCC controls the program enable signal, data is transmitted on VOUT, and all signals are referenced to ground. The second method is a two-wire interface, where the output is interrupted using the Manchester auxiliary command, data is transmitted on VOUT, and signals are referenced to ground. Both methods support multiple devices with shared VCC and ground lines and up to four die on a single shared output line.

Serial communication with the A31102 involves four basic transactions—write access, write to EEPROM, write to volatile memory, and read. The three-wire transaction are shown in Figure 26 to Figure 29. To initialize communication using the three-wire interface, V_{CC} increases to a level above V_{PRGH}(min). At this time, VOUT is disabled and acts as input. After program enable is asserted, the external controller must drive the output low for a minimum of two Manchester bit periods before sending the message frame. Once the command is complete, V_{CC} is reduced below V_{PRGL}(max) back to its normal operating level, the output is enabled and responds to magnetic input.

Table 20: Programming Characteristics

Parameter	Symbol	Description		Min.	Typ.	Max.	Unit
Program Enable Voltage (High)	V_{PRGH}	MEM_LOCK = 0, 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 13, 14, and 15		$V_{CC(OV)HIGH}$(max)	–	19	V
		MEM_LOCK = 6		$V_{CC(HV)HIGH}$(max)	–	19	V
Program Enable Voltage (Low)	V_{PRGL}	MEM_LOCK = 0, 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 13, 14, and 15		–	–	$V_{CC(OV)LOW}$(min)	V
		MEM_LOCK = 6		–	–	$V_{CC(HV)LOW}$(min)	V
Manchester Start Delay	t_m	Minimum delay before first edge of the Manchester signal.		200	–	–	µs
Output Enable Delay	t_e			–	25	–	µs
Program Time Delay	t_d			–	–	50	µs
Program Write Delay	t_w			–	20	–	ms
Bit Time Delay	t_b			–	2	–	t_{bit} [1]
Access Code Timeout	t_{acc}			500	–	–	ms
Bit Rate		Communication Rate		4	–	100	kbps
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT		2.8	–	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT		0	–	1.2	V
Hold Time	t_{HOLD}	SSENT – Short	F_AUX	50	–	83	Ticks
		SSENT – Long	F_AUX	196	–	297	Ticks
		ASENT	F_AUX	50	–	80	Ticks
		SENT	Aux. Interrupt	30	–	–	Ticks
		TSENT	Aux. Interrupt	30	–	–	Ticks
		PWM	Aux. Interrupt	2 × PWM period [2]	–	–	µs
Edge Detection Time	t_{GATE}			0.7	–	–	µs
Access Code Timeout	t_{msgRX}			1.4	–	300	µs

[1] The unit t_{bit}, is the period for single bit defined by the Manchester encoding bit boundaries and is determined by the communication rate.
[2] The minimum hold time for the Auxiliary interrupt, when the output is set for PWM, is double the PWM frequency. Note if the PWM frequency changes as a result of a diagnostic condition, the minimum hold time is double the PWM period at the diagnostic frequency.

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Manchester Auxiliary Command for PWM Output Mode

To initialize communication using the Manchester Auxiliary command when the A31102 is configured with PWM output, the auxiliary interrupt pulse can be applied at any time. The auxiliary pulse must have a minimum width of t_{HOLD}, after which the pulse is released for t_{GATE} plus the rise time to allow the line to pull high and the device to register a rising edge. After this, the controller must pull low for t_{GATE} + ½ tbit before beginning to send the Manchester Access Code. The device must recognize the first rising edge of the Manchester access code before t_{msgRX} after the hold time or the device will timeout, aborting Manchester initialization and returning to PWM functionality. The Manchester Auxiliary command for PWM output is shown Figure 23.

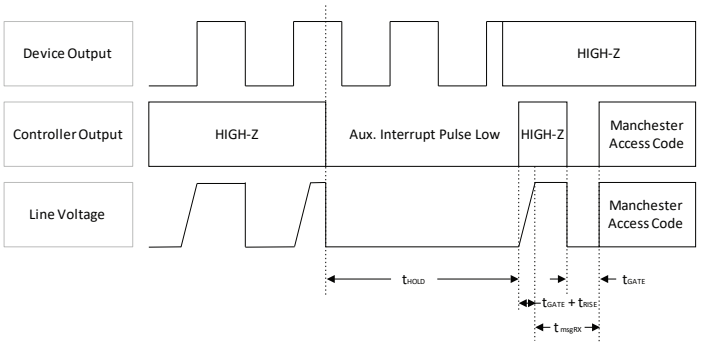

Figure 23: Auxiliary Interrupt Pulse Waveform

Manchester Auxiliary Command for SENT and TSENT Output Mode

To initialize communication using the Manchester Auxiliary command when the A31102 is configured with SENT or TSENT output, the auxiliary interrupt pulse can be applied at any time between the start of the Sync pulse and the end of the last data nibble pulse. The pulse must have a minimum width of t_{HOLD}, after which the pulse must be released for t_{GATE} plus the rise time to allow the line to pull high, followed by a low period of t_{GATE} before sending the Manchester access code. Again, if the first rising edge of the Manchester access code is not seen before t_{msgRX}, the device will timeout, Manchester initialization is aborted, and the device will return to normal functionality. The Manchester Auxiliary command for SENT and TSENT output is shown in Figure 24.

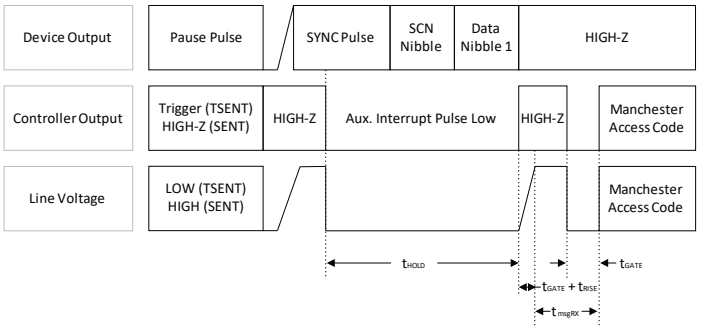

Figure 24: Interrupt waveform for SENT and TSENT output

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Manchester Auxiliary Command for SSENT and ASENT Output Mode

To initialize communication using the Manchester Auxiliary command when the A31102 is configured with SSENT or ASENT output, the auxiliary function pulse, F_AUX, is applied as the frame request pulse. The auxiliary pulse must have a minimum width of t_{HOLD}. After the pulse is released, the output line is required to go HIGH-Z for t_{GATE} plus the rise time. The controller must then pull the output line low for t_{GATE} before sending the Manchester access code. If the first rising edge of the access code is not recognized before t_{msgRX}, a timeout will occur, the Manchester initialization is aborted, and the output will return to normal functionality.

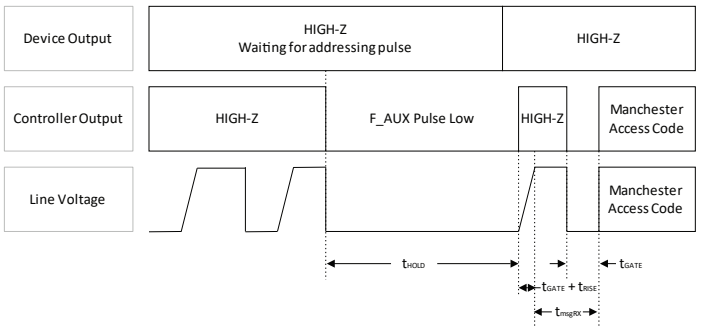

Figure 25: Interrupt waveform for SSENT and ASENT output

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When performing a write to EEPROM transaction, the A31102 requires a delay of t_w to store the data into the EEPROM. The device will respond with a high-to-low transition on VOUT to indicate the write to EEPROM sequence is complete

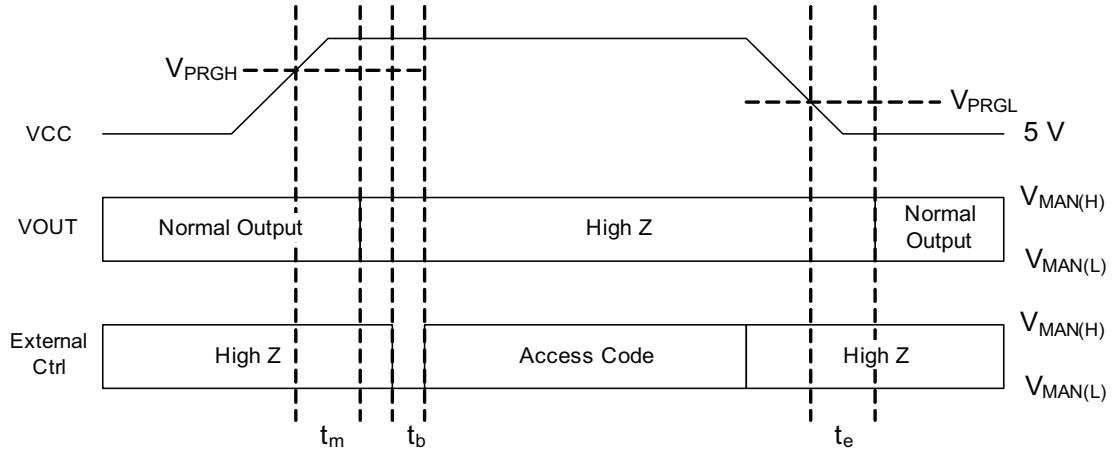

Figure 26: Write Access Code

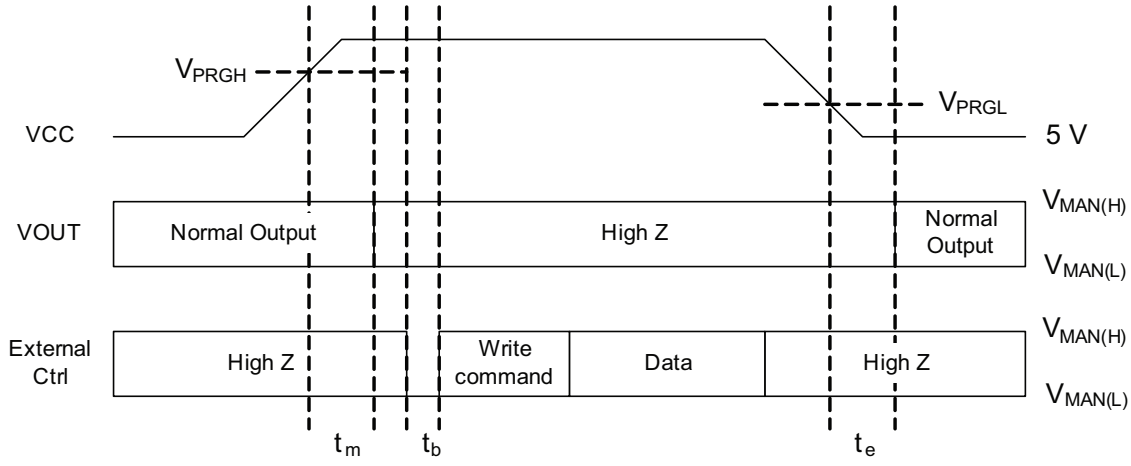

Figure 27: Write to Volatile Memory

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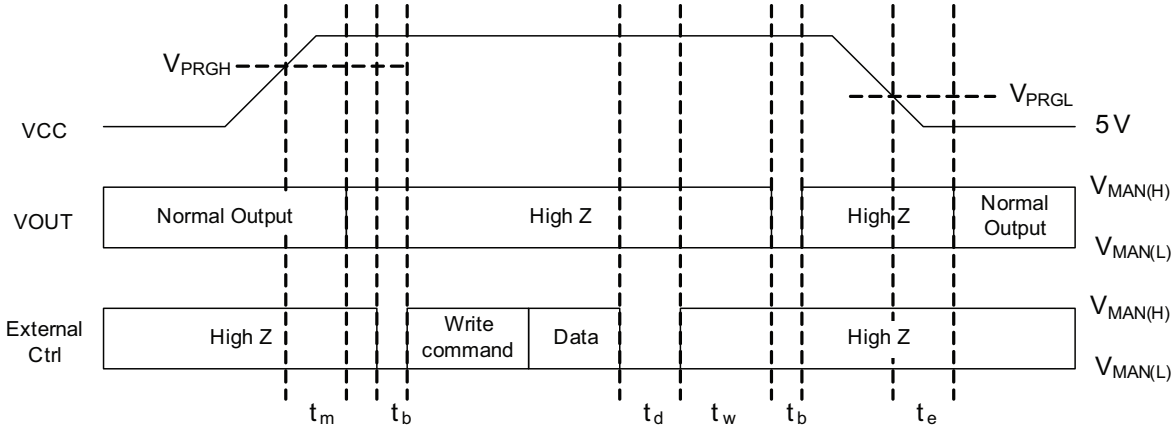

Figure 28: Write to Non-Volatile Memory (EEPROM)

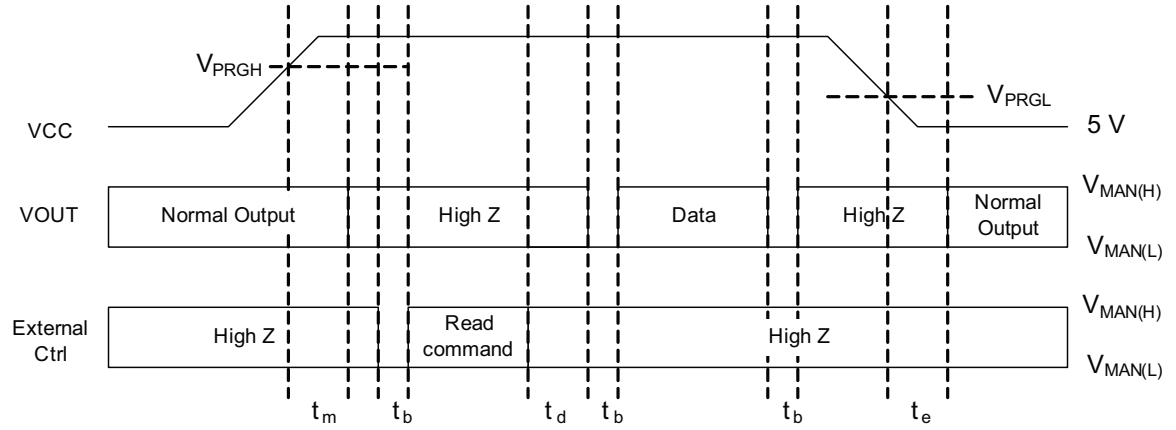

Figure 29: Read Request

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Serial Interface Message Structure

The general format of a command message frame is shown in Figure 30. Serial binary data is encoded using a Manchester encoding scheme, where a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary. The time period for the bit boundary is determined by the baud rate initiated by the external controller. The A31102 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 21.

For a Write Access command frame, the data consists of 32 bits. For a Read Request frame, the data bits are omitted. For a Read Acknowledge or Write frame the data bits are defined as shown in Figure 30, where bit 0 is the LSB.

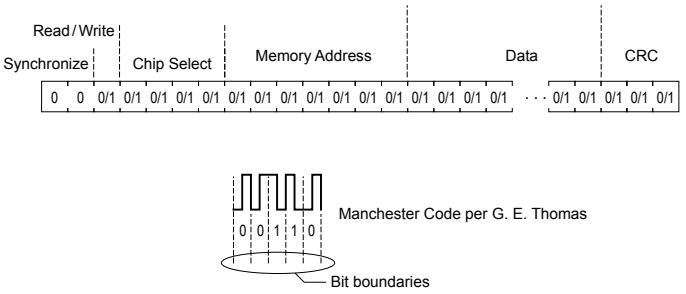

Figure 30: General Format for Serial Interface Commands

Table 21: Serial Interface Command General Format

Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command and communication bit time
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
4	Chip Select	0-15	Chip select for up to 4 die connected in parallel: XXX1 = device communication address 0 XX1X = device communication address 1 X1XX = device communication address 2 1XXX = device communication address 3 0000, 1111 = Broadcast
7	Address		[Read/Write] Register address EEPROM: 0x00-0x1F Shadow Memory: 0x20-0x3F Volatile Memory: 0x40-0x7F
32	Data		[Write] 26 data bits and 6 ECC bits
3	CRC		Bits to check the validity of the frame

Table 22: Serial Interface Read Acknowledge Format

Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command and communication bit time
32	Data		26 data bits and 6 bits EEPROM diagnostics
3	CRC		Bits to check the validity of the frame

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CRC

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check). The CRC algorithm is based on the following polynomial, and the calculation is represented graphically in Figure 31.

$$g(x) = x^3 + x + 1 \ ,$$

The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111 (see Figure 31).

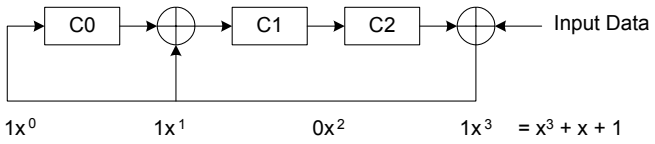

Figure 31: CRC Calculation

Customer/Factory Access Modes

The internal memory is accessible via the serial interface. The memory address space is divided into two areas: Factory and Customer.

Access is controlled by a specific code. The customer access codes, listed in Table 23, are constants. When using the three-wire interface, the access codes must be transmitted within 500 milliseconds of power-on. The two available customer access codes differ by the LSB. The LSB sets the COMM_EN parameter. When this bit is set to a logic value of one, the output is disabled until the COMM_EN bit is set to zero. It is recommended to use the access code with COMM_EN equal to one when using the Manchester auxiliary command.

For software convenience, the table gives an 8-bit "address" and 32-bit "data" field, similar to a normal Write command format (the address and data fields concatenated yield the full access code). The Customer registers may be written only if a valid Customer Access code is received. With no valid access code, customer and factory registers are addressable, but are read only. The status of the access code is indicated by bit 0 in register 0x44, where a 1 indicates customer access is enabled.

Customer Memory Lock

The A31102 contains lock features to prevent access to the device memory. The EEPROM parameter, MEM_LOCK bits [3:0] in register CFG_C, configure the lock mode. When MEM_LOCK is set to 3 (decimal), write access to the EEPROM is disabled, write access to the volatile memory is enabled, and read access to the entire memory is enabled. When MEM_LOCK is set to 6 (decimal), write access to the device is disabled and read access to the entire memory is enabled. When MEM_LOCK is set to 12 (decimal), all write and read access to the device is disabled. The remaining MEM_LOCK settings allow full read and write access to the device memory.

EEPROM Margin Checking

The A31102 contains a test mode, EEPROM Margining, to check the logic levels of the EEPROM bits. The EEPROM margining is accessible with customer access. The EEPROM margining is selectable to check all logic 1, logic 0, or both. The results of the test are reported back in EEPROM registers 0x41, 0x42, and 0x43. Note that a fail of the margin test does not force the output to a diagnostic state.

Table 23: Customer Access Code

Name	Conditions	Format	
		Address (Hex)	Data (Hex)
Customer	COMM_EN = 0	0x44	0xC41797E0
	COMM_EN = 1	0x44	0xC41797E1

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EEPROM MEMORY MAP (NONVOLATILE)

Table 24: EEPROM Memory Map (nonvolatile)

Type[1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
EEPROM (continued on the next page)	ID_CFG	WLOT_F	0x00	FACTORY_LOT	Factory Lot Number	ro	16	15	0
				FACTORY_WAFER	Factory Wafer Number	ro	6	21	16
				unused		ro	4	25	22
		ID_F	0x01	X_DIE_LOC	8-bit X die location	ro	8	7	0
				Y_DIE_LOC	8-bit Y die location	ro	8	15	8
				unused		ro	10	25	16
		ID_C	0x02	CUST_ID	Bits reserved for customer ID	rw	22	21	0
				DIE_ADDR_0	Die address for Manchester communication and Shared SENT	rw	1		22
				DIE_ADDR_1	Die address for Manchester communication and Shared SENT	rw	1		23
				unused		rw	2	25	24
	SENS_C	SENS_TRIM_C	0x03	SENS_C	Customer Sensitivity trim (fine)	rw	11	10	0
				unused		rw	1		11
				SENSM_C	Customer Sensitivity trim (coarse) multiplier: 0: 1× 1: 2× 2: 4× 3: 8× 4: 16× 5: 32× 6: 32× 7: 32×	rw	3	14	12
				POL_C	Magnetic sensitivity polarity (0 = + south pole, 1 = – south pole)	rw	1		15
				unused		rw	10	25	16
		SENSTC1_C	0x04	SENSTC1_HOT_C	1st order customer sensitivity temperature compensation, room to hot	rw	11	10	0
				unused		rw	1		11
				SENSTC1_CLD_C	1st order customer sensitivity temperature compensation, room to cold	rw	11	22	12
				unused		rw	3	25	23
		SENSTC2_C	0x05	SENSTC2_HOT_C	2nd order customer sensitivity temperature compensation, room to hot	rw	10	9	0
				unused		rw	2	11	10
				SENSTC2_CLD_C	2nd order customer sensitivity temperature compensation, room to cold	rw	10	21	12
				unused		rw	10	31	22
	QOUT_C	QO_TRIM_C	0x06	QO_C	Customer Quiescent Output (QO) adjustment (fine)	rw	18	17	0
				unused		rw	8	25	18
		QOTC_C	0x07	QOTC_HOT_C	1st order QO temperature compensation, room to hot	rw	12	11	0
				QOTC_CLD_C	1st order QO temperature compensation, room to cold	rw	12	23	12
				unused		rw	2	25	24
		CLAMP_C	0x08	CLAMPH	High Clamp	rw	12	11	0
				CLAMPL	Low Clamp	rw	12	23	12
				unused		rw	2	25	24

Continued on the next page…

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Table 24: Memory Address Map (continued)

Type[1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
EEPROM (continued)		CFG_C	0x09	MEM_LOCK	0, 1, 2, 4, 5, 7, 8, 9, 10, 11, 13, 14, and 15 - Write and read access permitted. 3 - EEPROM Lock: Prevents writes to EEPROM but all volatile registers including shadow can be written. All registers and EEPROM can be read. 6 - Write Lock: Prevents writing anything to either EEPROM or registers. All registers and EEPROM can still be read. 12 - Full Lock: Prevents all access to the device.	rw	4	3	0
				OUTDRV_SEL	Adjustment for the output fall time.	rw	3	6	4
				SENT_HYST_CFG	Adjustment for the SENT trigger thresholds.	rw	2	8	7
				POR_DIAG_MODE	Output response after UVD detection 0: Output active immediately. 1: UVD error is latched until signal path is 97% settled.	rw	1		9
				CFG_SPCMIN_ADJ	Determines minimum low time for detecting an SSENT, Long Trigger Mode, F_OUTPUT command. 0: 7 ticks 1: 8 ticks 2: 9 ticks 3: 10 ticks	rw	2	11	10
				SPDIAG_EN	Enables Signal Path Diagnostic monitoring.	rw	1		12
				SPDIAG_RATE	Internal Sampling Ratio for the Signal Path Diagnostic signal. 0: 2:1 1: 4:1 2: 8:1 3: 16:1 (recommended)	rw	2	14	13
				SPERR_CFG	Configure the signal path error reporting 0: Default. signal path error reporting is on 1: Prevent internal digital monitor from reporting errors 2: Prevent diagnostic signal path monitor from reporting errors (recommended) 3: Prevent both internal digital and diagnostic signal path from reporting errors	rw	2	16	15
				DIAG_MODE	0: Default outputs a message in PWM / SENT 1: Outputs is high Z for all diagnostic errors. Only supported when VOUT is configured for PWM, outmsg_mode=0.	rw	1		17
				Reserved		rw	1		18
				BLOCK_VOLATILE_OUTPUT	Disables volatile register outputs during normal operation	rw	1		19
				UVD_DIS	0: Undervoltage errors will be reported 1: Prevent undervoltage detection from reporting errors at the output	rw	1		20
				OVD_DIS	0: Overvoltage errors will be reported 1: Prevent overvoltage detection from reporting errors at the output	rw	1		21
				OTMP_DIS	0: Overtemperature errors will be reported 1: Prevent overtemperature monitor from reporting errors at the output	rw	1		22
				OOR_DIS	0: Magnetic signal out-of-range errors will be reported 1: Prevent out-of-range monitor from reporting errors at the output	rw	1		23
				unused		rw	2	25	24
	LIN_C (continued on next page)	LIN0_C	0x0A	LINT00	Linearization Table entry 0	rw	13	12	0
				LINT01	Linearization Table entry 1	rw	13	25	13
		LIN1_C	0x0B	LINT02	Linearization Table entry 2	rw	13	12	0
				LINT03	Linearization Table entry 3	rw	13	25	13
		LIN2_C	0x0C	LINT04	Linearization Table entry 4	rw	13	12	0
				LINT05	Linearization Table entry 5	rw	13	25	13

Continued on the next page…

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Table 24: Memory Address Map (continued)

Type[1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
EEPROM (continued)	LIN_C	LIN3_C	0x0D	LINT06	Linearization Table entry 6	rw	13	12	0
				LINT07	Linearization Table entry 7	rw	13	25	13
		LIN4_C	0x0E	LINT08	Linearization Table entry 8	rw	13	12	0
				LINT09	Linearization Table entry 9	rw	13	25	13
		LIN5_C	0x0F	LINT10	Linearization Table entry 10	rw	13	12	0
				LINT11	Linearization Table entry 11	rw	13	25	13
		LIN6_C	0x10	LINT12	Linearization Table entry 12	rw	13	12	0
				LINT13	Linearization Table entry 13	rw	13	25	13
		LIN7_C	0x11	LINT14	Linearization Table entry 14	rw	13	12	0
				LINT15	Linearization Table entry 15	rw	13	25	13
		LIN8_C	0x12	LINT16	Linearization Table entry 16	rw	13	12	0
				LINT_E	0: Bypass linearization table 1: Enable valid linearization table	rw	1		13
				LINT_BIN_E	0: Linearization mode functions normally if enabled by LINT_E 1: Enable bin mode for linearization table	rw	1		14
				LINT_OUT_INV	0: Normal output of linearization table 1: Invert output of linearization table	rw	1		15
				LINT_IN_INV	0: Normal input to linearization table 1: Invert input of linearization table	rw	1		16
				LINT_BIN_HYST	Hysteresis for linearization bin mode	rw	8	24	17
				LIN_SCALAR	Increase error range for Linearization Table entries	rw	1		25
		POST_LIN_C	0x13	PLIN_SENS	Post Linearization sensitivity adjustment	rw	12	11	0
				PLIN_QVO	Post Linearization offset adjustment	rw	12	23	12
				unused		rw	2	25	24
		OUT_CFG_C (continued on next page)	0x14 (cont. next page)	OUTMSG_MODE	0: PWM 1: SENT, Internal Synchronous Mode 2: TSENT, External Asynchronous Mode 3: SSENT, Long Trigger Mode 4: SSENT, Short Trigger Mode 5: ASENT 6-7: TSENT, External Synchronous Mode	rw	3	2	0
				SENT_PWM_RATE	Specifies the frequency of the SENT or PWM message. This is shown in Table 15.	rw	5	7	3
				TRIGGER_CFG	Adjust the minimum trigger length 0: 2.5 µs 1: 5 µs 2: 10 µs 3: 0.5 µs	rw	2	9	8
				SEN_CRC_CFG	Determines if the SCN is included in the SENT CRC 0: SCN is not included CRD 1: SCN included in CRC	rw	1		10
				SENT_DATA_CFG	Only valid for SENT modes. Number and format of data nibbles in SENT frame. see Table 12 SENT Data	rw	3	13	11
				SENT_SCN_CFG	Selects bits for SCN[3:2], Only valid for SENT output mode. 0: Enables the slow serial message stream. 1: Disables the slow serial message stream. SCN bits [3:2] = 0 2: Disables the slow serial message stream. SCN bits [3:2] = [DIE_ADDR_1:DIE_ADDR_0] 3: Enables the slow serial message stream.	rw	2	15	14

Continued on the next page…

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Table 24: Memory Address Map (continued)

Type [1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
EEPROM (continued)		OUT_CFG_C (continued)	0x14 (cont.)	CFG_MAX_SENSOR	Highest sensor number on the bus for SSENT	rw	2	17	16
				AUX_CMD_DIS	Disables 2-wire Manchester communication.	rw	1		18
				CFG_NO_SAMPLE	0: F_SAMPLE will cause the sensor to sample and hold magnetic data 1: F_SAMPLE will not create a sample and hold of the magnetic data	rw	1		19
				CFG_FSAMPLE_ADR	0: F_SAMPLE will not address the sensor 1: F_SAMPLE will be an addressing (frame request) as well as a sample and hold request	rw	1		20
				CFG_IDLE_SYNC	0: A bus idle will not resynchronize the sensors 1: For SSENT Short or Long, a bus idle time of > 510 ticks will act as an F_SYNC pulse	rw	1		21
				CFG_POR_OFFLINE	0: The sensor will come online after a power-on reset 1: the sensor will be in OFFLINE mode following a power-on reset (but not a reset that is not also power-on) and will require an F_SYNC pulse to come online	rw	1		22
				CFG_SLOT_MARKING	0: SSENT will not include slot marking times 1: for SSENT, the slot marking times will be applied prior to the start of a frame	rw	1		23
				CFG_SLOT_SYNC	0: Slot marking will not resynchronize the slot counter 1: for SSENT and CFG_SLOT_MARKING=1, then the sequencer will use the slot marking to synchronize the slot counter	rw	1		24
				CFG_ZERO_SAMPLE	0: A sample and hold will only be requested using an F_SAMPLE pulse 1: For SSENT, a sample_and_hold will be requested when the slot counter is 0	rw	1		25
		FILTER_CFG_C	0x15	BW_SEL	Bandwidth selection for IIR filter, or maximum code (minimum bandwidth) for the adaptive filter.	rw	3	2	0
				BW_SEL_MIN	Selects the minimum bw_sel code (maximum bandwidth) for the adaptive filter	rw	3	5	3
				FILT_ADA_GAIN	Adaptive filter gain parameter	rw	3	8	6
				unused		rw	17	25	9
		Reserved	0x15-0x1F		Addresses 0x22 through 0x3F are reserved for shadow memory, a volatile representation of EEPROM. 0x22 is shadow from 0x02.				
SHADOW			0x22-0x3F		Addresses 0x22 through 0x3F are reserved for shadow memory, a volatile representation of EEPROM. 0x22 is shadow from 0x02.				
VOLATILE (continued on the next page)		TEST_C	0x40	OUT_DIS	0: No effect 1: test mode to disable output	rw	1		0
				MANCH_COMM_EN	Allows for serial communication without raising V_{CC} 0: Default mode. V_{CC} must be raised to allow serial communication 1: Serial communication can occur with V_{CC} at nominal operating level	rw	1		22
		EE_DATA_C	0x41	EE_DATA	If margin or self test fails this is the failed data read from EEPROM.	rw	26	25	0
		EE_STATUS_C	0x42	EE_DBE_FLAG	Dual Bit Error Flag. Latched and held high when a dbe has occurred.	rw	1		0
				EE_SBE_FLAG	Single Bit Error Flag. Latched and held high when a sbe has occurred.	rw	1		1
				EE_ERR	Indicates an EEPROM write error occurred. This bit is latch and hold with clear on read.	rc	1		2
				EE_ERR_STATUS	When ee_err is asserted this parameter contains a factory error code for the aborted EEPROM write transaction.	ro	5	7	3
				EE_ADDR	Reflects the read/write address to the EEPROM. This allows for a manual write to the EEPROM or will contain data read from the EEPROM if margining or self check fails.	rw	5	12	8
				EE_ECC	Reflects bits [29:24] to be written to the EEPROM or read from the EEPROM. This allows for a manual write to the EEPROM or will contain data read from the EEPROM if magining or self check fails.	rw	6	18	13
				CP_ERR	High to indicate an error occurred during charge pump ramp. EE_ERR_STATUS stores information about the error.	rc	1		19

Continued on the next page…

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Table 24: Memory Address Map (continued)

Type[1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
VOLATILE (continued)		MARG_TST_C	0x43	EE_LOOP	When set margin test will loop until an error is detected.		1		13
				EE_TEST_ADDR	Optional start address for margin test.		5	11	7
				EE_USE_TEST_ADDR	Set bit to specify start address for margin test. 0: Margin test will start at the address 0 1: Margin test will start at address set in EE_TEST_ADDR	rw	1		6
				MARGIN_MIN_MAX_FAIL	If margining fails, this bit indicates if the min or max reference failed. 0: Min margining failed. 1: Max margining failed.	ro	1		5
				MARGIN_STATUS	Bits are cleared after a read or reset. 0: Reset condition (no result from margin testing) 1: Pass, no failure detected during margin testing 2: Fail, failure detected during margin testing 3: Running, margin test is still running	ro	2	4	3
				MARGIN_NO_MIN	Does not perform minimum margin testing 0: Margining done a min voltage. 1: No margining at min voltage	rw	1		2
				MARGIN_NO_MAX	Does not perform maximum margin testing 0: Margining done a max voltage. 1: No margining at max voltage.	rw	1		1
				MARGIN_START	Write to 1 to start margin testing. If EE_LOOP is low, this bit will self clear when address 0x1F is reached. If EE_LOOP is high, this bit must be written to 0 to stop test. This bit always clears on a fail.	rw	1		0
		ACCESS	0x44	CUST_ACCESS	Indicates customer access enabled	ro	1		0
				reserved	reserved for factory information	ro	31	31	1
		ERR_STATUS_C	0x45	DIAG_REG_C	Status bits to report diagnostic errors. 0 = no errors Bit [0] = 1: EEPROM Dual Bit Error Bit [1] = 1: Unused Bit [2] = 1: Signal Path Diagnostic Error Bit [3] = 1: Undervoltage Error Bit [4] = 1: Overvoltage Error Bit [5] = 1: Overtemperature Error Bit [6] = 1: Signal Out of Range Low Error Bit [7] = 1: Signal Out of Range High Error	rw	8	23	16
	SIGPATH_C	SIGPATH_BYP_C	0x46	BYP_TRIM_C	0: No effect 1: Bypass Customer Sensitivity and Offset trim	rw	1		0
				BYP_TC_C	0: No effect 1: Bypass Customer sensitivity and offset temp. compensation	rw	1		1
				BYP_LIN	0: No effect 1: Bypass Linearization block	rw	1		2
				BYP_PLIN	0: No effect 1: Bypass Post-Linearization Trim block	rw	1		3
				BYP_CLAMP	0: No effect 1: Bypass Clamp block	rw	1		4
		TEMP_OUT_C	0x47	TEMP_OUT	Output of Temp Sensor Trim block; Temperature (°C) = TEMP_OUT / 8 + 25°C	ro	12	11	0
		MAG_OUT_C	0x48	MAG_OUT	Output of the magnetic signal path	ro	16	15	0
		Reserved	0x49-0X59		Addresses 0x49 through 0x59 reserved for factory use				

[1] All EEPROM addresses contain 32 bits. Bits 26 through 31 are used for EEPROM diagnostics. For more information see Application Information, EEPROM Diagnostics.

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PROGRAMMABLE PARAMETER REFERENCE

Table 25: DIE_ADDR_0: Address 0x02, bit 22
DIE_ADDR_1: Address 0x02, bit 23

Function	Sets address of the die for SENT and Addressable Manchester
Syntax	Quantity of bits 2 (1 for each parameter)
Related Commands	OUTMSG_MODE, SENT_SCN_CFG
Values	<table><tr><th>DIE_ADDR_1</th><th>DIE_ADDR_0</th><th>Device Address</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>3</td></tr></table> When multiple Sensors are to be used on a shared output bus, they must first be programmed to different device addresses to avoid conflict in addressable Manchester and Shared SENT responses. Factory default programming is die 1 programmed to device address 0 and die 2 programmed to device address 1.
Options	

Table 26: BW_SEL: Address 0x15, bits 2:0

Function	Sets the 3 dB frequency of the magnetic signal path filter used to reduce noise on the output
Syntax	Quantity of bits: 3
Related Commands	FILT_ADA_GAIN, BW_SEL_MIN
Values	Code: Typical 3 dB (Hz) 0: 8500 Hz, 1: 6660 Hz, 2: 3330 Hz, 3: 1520 Hz, 4: 733 Hz, 5: 360 Hz, 6: 179 Hz, 7: 89 Hz
Options	The settings of BW_SEL_MIN correspond with the BW_SEL values.

Table 27: CLAMPH: Address 0x08, bits 11:0

Function	Sets level for the upper output clamp
Syntax	Quantity of bits: 12 Inverted, unsigned
Related Commands	CLAMPL
Values	0x0: Default, Upper output clamp is at $OUT_{CLP(HIGH)}$(max) 0xFFF: Upper output clamp is at $OUT_{CLP(HIGH)}$(min)
Options	
Examples	See Clamp

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Table 28: CLAMPL: Address 0x08, bits 23:12

Function	Sets level for the lower output clamp
Syntax	Quantity of bits: 12
	unsigned
Related Commands	CLAMPH
Values	0x0: Default, lower output clamp is at $OUT_{CLP(LOW)}$(min) 0xFFF: Upper output clamp is at $OUT_{CLP(LOW)}$(max)
Options	
Examples	See Clamp

Table 29: SENT_PWM_RATE: Address 0x14, bits 7:3

Function	Sets the PWM frequency or SENT Tick Time.
Syntax	Quantity of bits: 5
Related Commands	OUTMSG_MODE
Values	Refer to Table 15: PWM Frequency/SENT Tick Times for values
Options	
Examples	

Table 30: QO_C: Address 0x06, bits 17:0

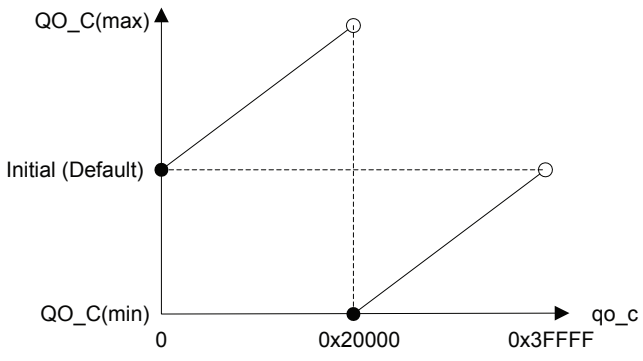
Function	Fine quiescent output adjustment, shifts the output from the factory default Quiescent Output, QO_{INIT}.
Syntax	Quantity of bits: 18 signed
Related Commands	
Values	
Options	
Examples	See Operating Characteristics and Compensation Block

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Table 31: OUTMSG_MODE: Address 0x14 Bits [2:0]

Function	Sets the output format.
Syntax	Quantity of bits: 3
	unsigned
Values	0: PWM 1: SENT, Internal Synchronous Mode 2: TSENT, External Asynchronous Mode 3: SSENT, Long Trigger Mode 4: SSENT, Short Trigger Mode 5: ASENT 6-7: TSENT, External Synchronous Mode
Options	
Examples	See section, Linear Output Protocols

Table 32: SENSM_C: Address 0x03, bits 14:12

Function	Coarse Sensitivity adjustment, SENS_COARSE. Multiplier applied to the nominal factory Sensitivity, $SENS_{INIT}$.	
Syntax	Quantity of bits: 3	
Related Commands	SENS_C	
Values	0 = 1× (default)	4 = 16×
	1 = 2×	5 = 32×
	2 = 4×	6 = Not used
	3 = 8×	7 = Not used
Options		
Examples	See Operating Characteristics and Compensation Block	

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Table 33: SENS_C: Address 0x03, bits 10:0

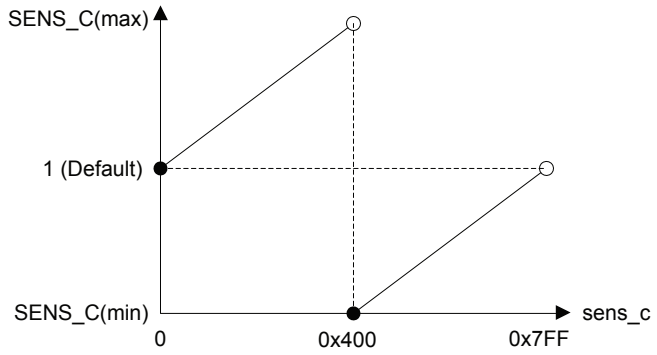
Function	Fine Sensitivity adjustment, SENS_C. Multiplier applied after the Coarse Sensitivity adjustment to scale from the factory default Sensitivity, $SENS_{INIT}$.
Syntax	Quantity of bits: 11 signed
Related Commands	SENSM_C
Values	
Options	
Examples	See Operating Characteristics and Compensation Block

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Table 34: SENSTC1_HOT_C: Address 0x04, bits 10:0
SENSTC1_CLD_C: Address 0x04, bits 22:12

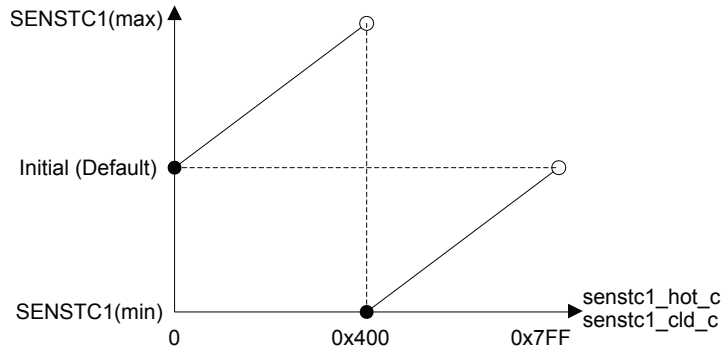
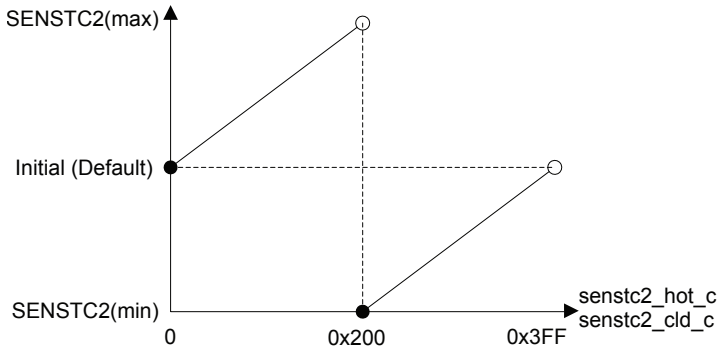
Function	First order Sensitivity Temperature Compensation, segmented for hot (25°C < T_A ≤ 150°C) and cold (–40°C ≤ T_A < 25°C)
Syntax	Quantity of bits: 11 signed
Related Commands	
Values	
Options	
Examples	See Compensation Block

Table 35: SENSTC2_HOT_C: Address 0x04, bits 9:0
SENSTC2_CLD_C: Address 0x04, bits 21:12

Function	Second order Sensitivity Temperature Compensation, segmented for hot (25°C < T_A ≤ 150°C) and cold (–40°C ≤ T_A < 25°C)
Syntax	Quantity of bits: 10 signed
Related Commands	
Values	
Options	
Examples	See Compensation Block

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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 AB-1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

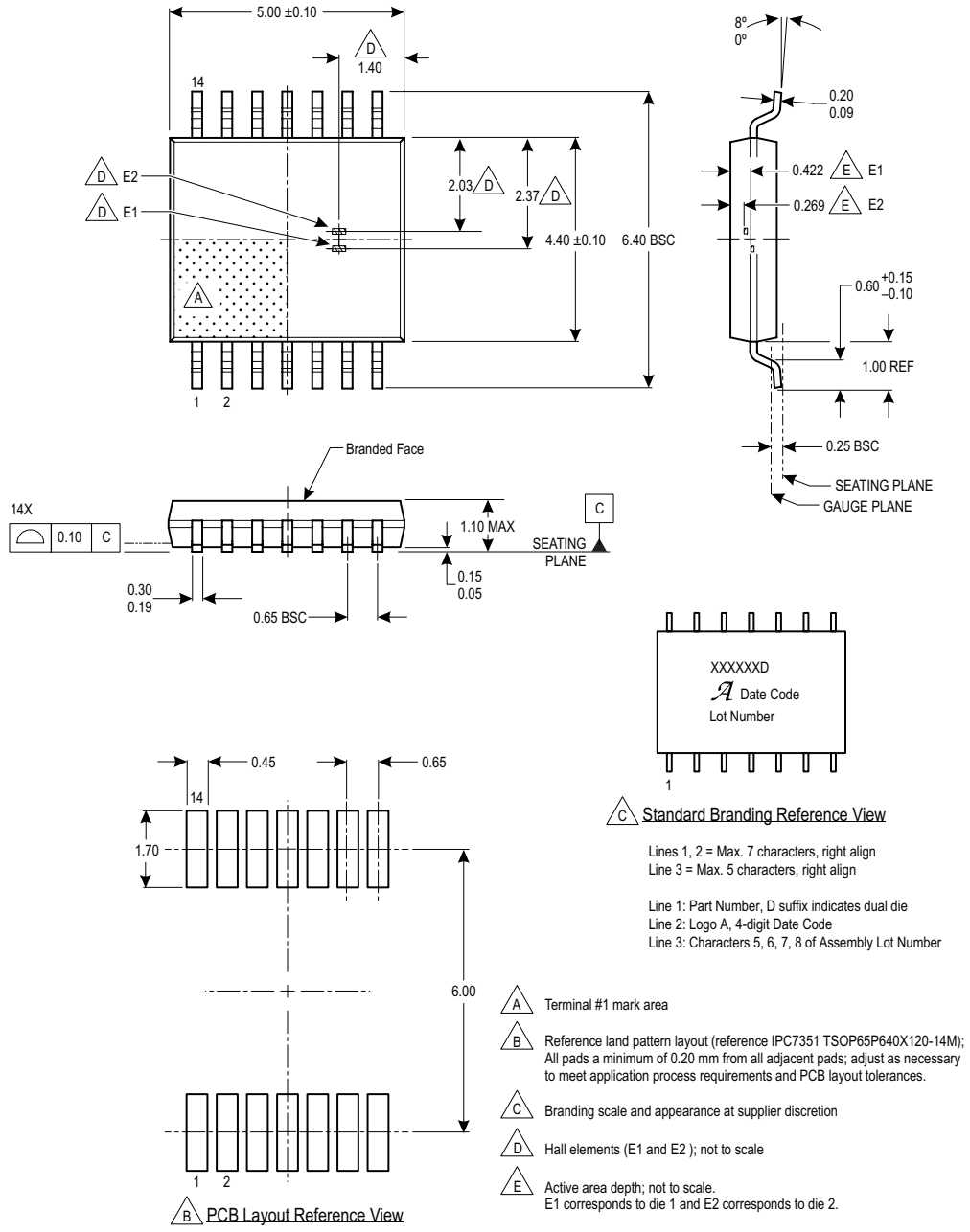

Figure 32: Package LU, 14-Pin TSSOP, Dual Die

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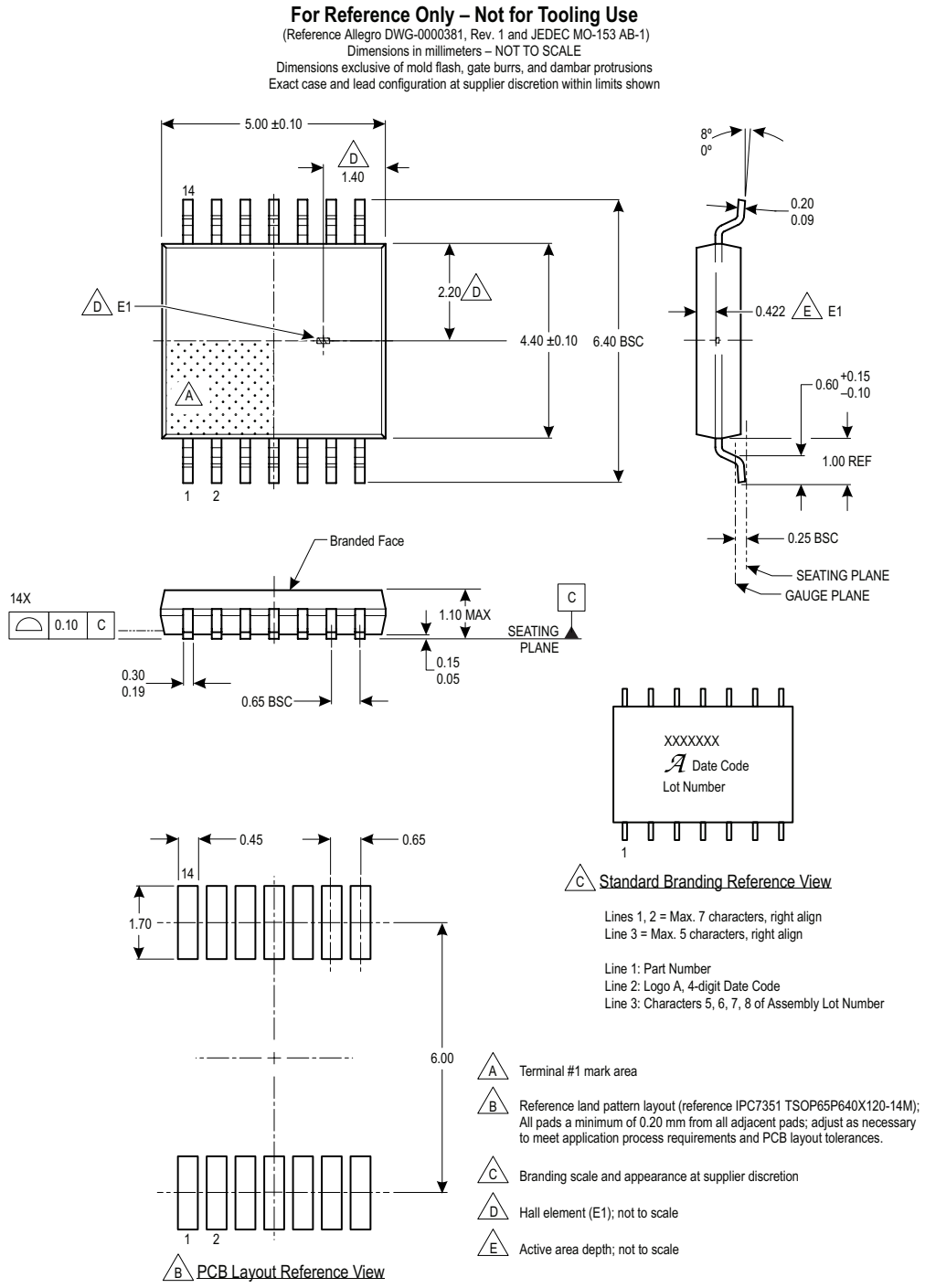

Figure 33: Package LU, 14-Pin TSSOP, Single Die

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Revision History

Number	Date	Description		
		Page	Section	Change
–	March 7, 2019	All	All	Initial release
1		1-3, 5-6, 8-9, 12, 54-55	All	Added single die part option
2	October 3, 2022	6	Operating Characteristics	Added Footnotes to Supply Voltage, Undervoltage Detection Threshold, and Overvoltage Detection Threshold. Removed duplicate Output Saturation Voltage characteristic.. Added minimum and typical values for Output Saturation Voltage.
		19	Linearization	Corrected Table 4
		21	Linearization Binning Mode (Bin Mode)	Updated Equation 7 and description
		36	ASENT Function Pulses	Removed bullet for F_DIAG
		37	Programming Information	Corrected Table 20, mem_lock
		42	Serial Interface Message Structure	Added Table 22
		50	Programmable Parameters Reference	Updated Table 30 heading
		54-55	Package Outline Drawing	Updated drawings
3	February 8, 2024	1, 3-5	–	Fixed broken links
		All	–	All references to registers updated to Allegro standard notation (all caps)
4	July 30, 2024	1	Features and Benefits	Updated info about ISO standard assessment
		15	ASIL Diagnostic Conditions	Updated Diagnostic Summary Table
		42	Serial Interface Message Structure	Updated Serial Interface Read Acknowledge Format Table

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