

# Memory FRAM

## 256K (256 K × 8) Bit SPI

## MB85RS2MLY (AEC-Q100 Compliant)

### ■ DESCRIPTION

MB85RS2MLY is a FRAM (Ferroelectric Random Access Memory) chip in a configuration of 262,144 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. This product is specifically targeted for high-temperature environment such as automotive applications.

MB85RS2MLY adopts the Serial Peripheral Interface (SPI).

The MB85RS2MLY is able to retain data without using a back-up battery, as is needed for SRAM.

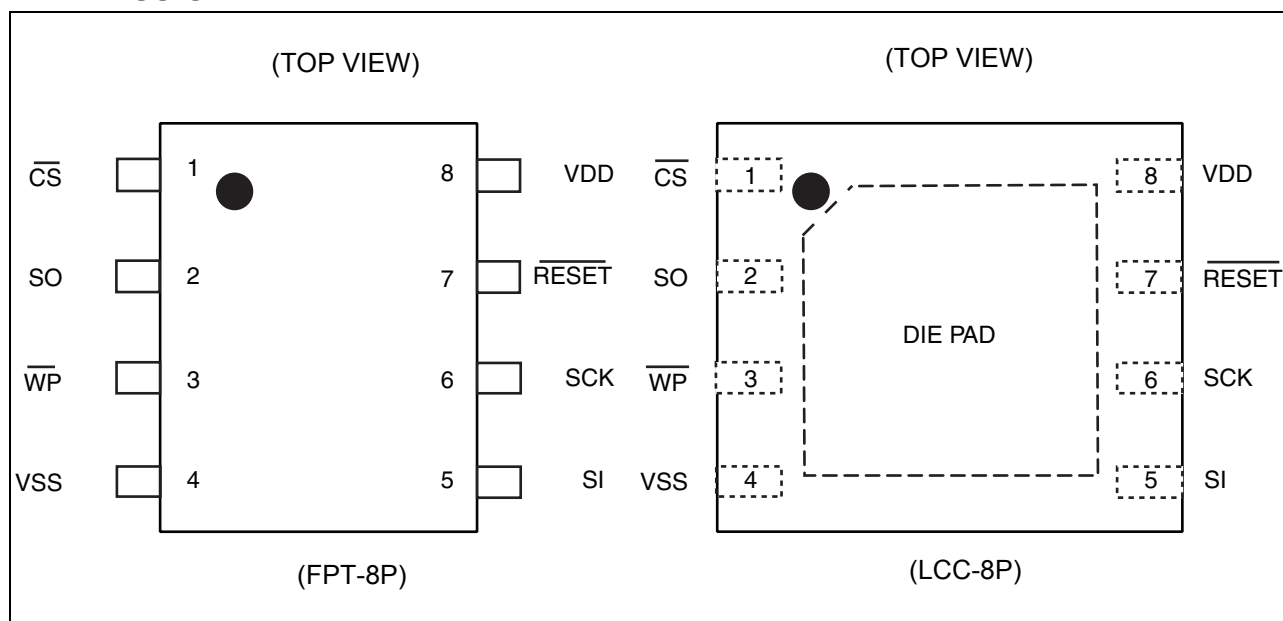
The memory cells used in the MB85RS2MLY can be used for  $10^{13}$  read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E<sup>2</sup>PROM.

As MB85RS2MLY does not need any waiting time in writing process, the write cycle time of MB85RS2MLY is much shorter than that of Flash memories or E<sup>2</sup>PROM.

### ■ FEATURES

- Bit configuration : 262,144 words × 8 bits
- Serial Sector Region : 256 words × 8 bits  
In this region, data storage after (by) three times reflow based on JEDEC MSL-3 standard condition is guaranteed.
- Unique ID
- Serial Number : In this region, data storage after (by) three times reflow based on JEDEC MSL-3 standard condition is guaranteed.
- Serial Peripheral Interface : SPI (Serial Peripheral Interfaces)  
Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 50 MHz (Max)
- High endurance :  $10^{13}$  times / byte
- Data retention : 10 years (+85 °C)  
2.75 years (+105 °C)  
0.85 years (+125 °C) or more  
Under evaluation for more than 2.5 years (+125 °C)
- Operating power supply voltage : 1.7 V to 1.95 V
- Low power consumption : Operating power supply current 3.5 mA (Max@50 MHz)  
Standby current 200 μA (Max)
- Operation ambient temperature range : -40 °C to +125 °C
- Package : 8-pin plastic SOP 150mil (FPT-8P)  
8-pin plastic DFN 5mm × 6mm (LCC-8P)  
AEC-Q100 Grade 1 compliant  
RoHS compliant

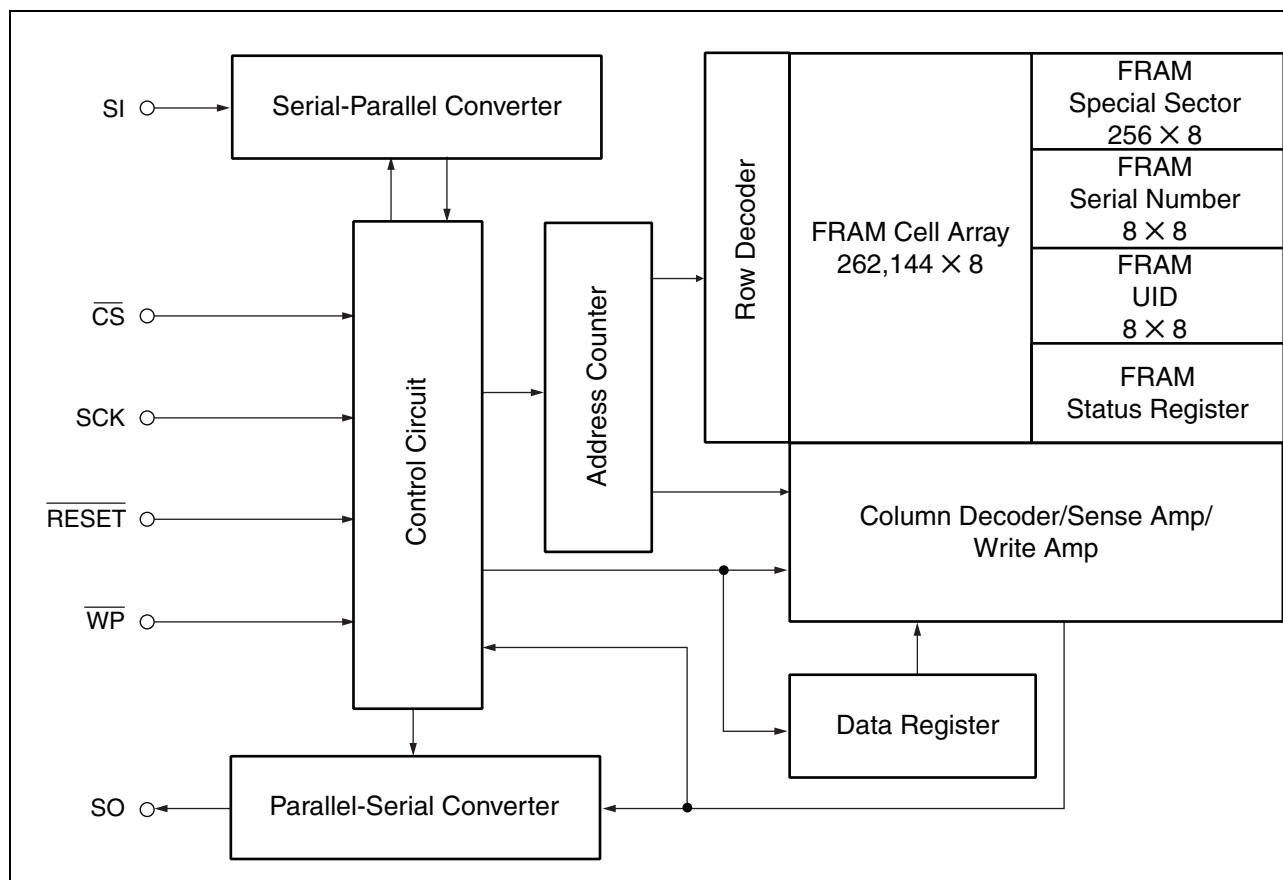
## PIN ASSIGNMENT



## PIN FUNCTIONAL DESCRIPTIONS

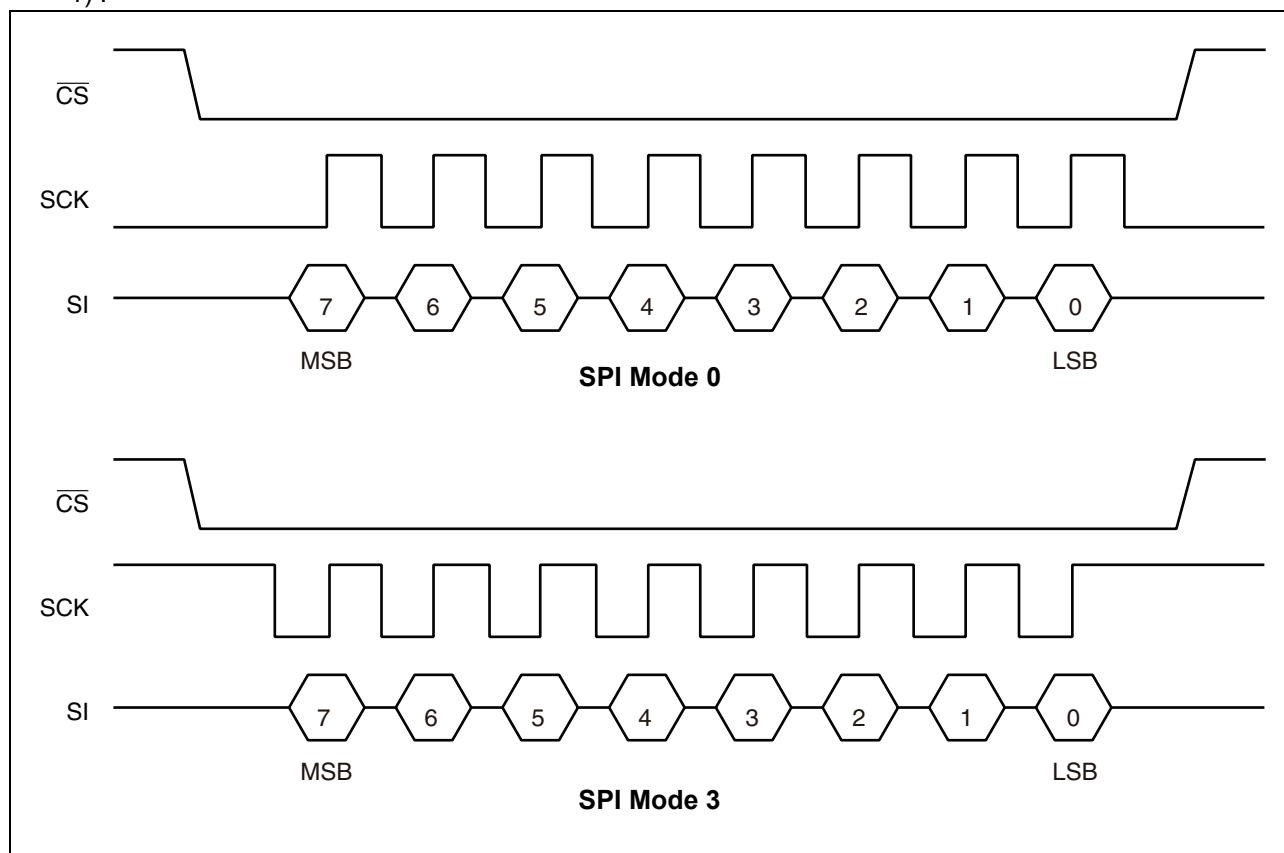
Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is "L" level, device is in select (active) status. $\overline{CS}$ has to be "L" level before inputting op-code.
3	$\overline{WP}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with $\overline{WP}$ and WPEN. See "■ WRITING PROTECT" for detail.
7	RESET	RESET pin This is an input pin to make chips reset. When RESET is "L" level, device is reset, initializing status of SPI interface. While power voltage is rising up, RESET have to be kept "L".
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin
DIE PAD	—	It is allowed for the DIE PAD on the bottom of the DFN8 package to be floating (no connection to anything) or to be connected to VSS.

## ■ BLOCK DIAGRAM



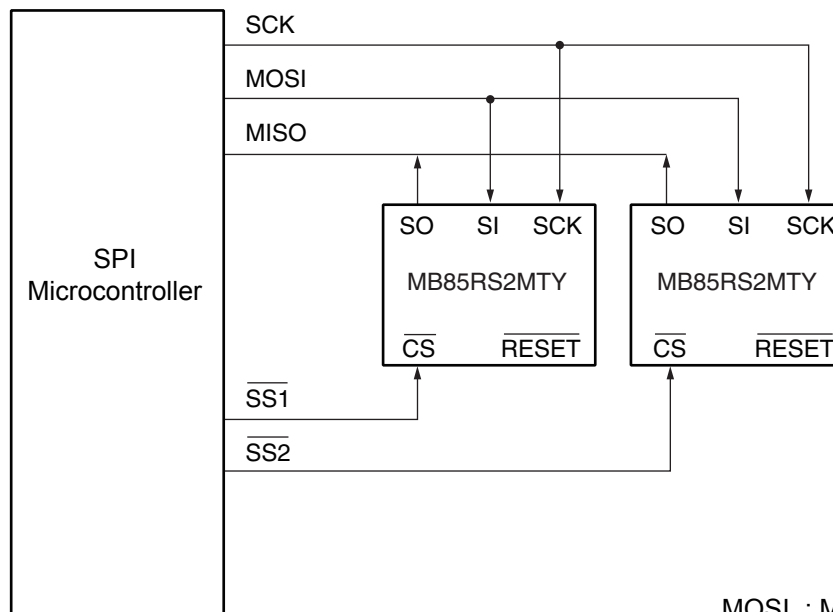
## ■ SPI MODE

MB85RS2MLY corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .



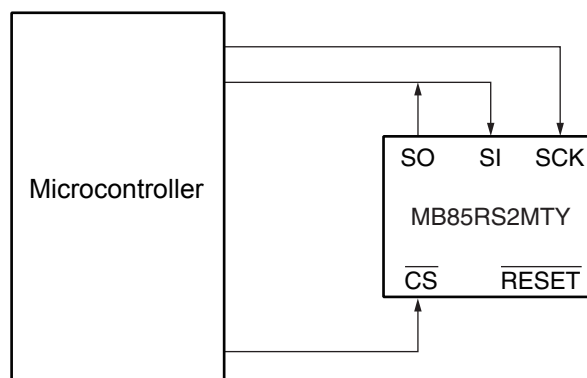
## ■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS2MLY works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



MOSI : Master Out Slave In  
MISO : Master In Slave Out  
SS : Slave Select

**System Configuration with SPI Port**



**System Configuration without SPI Port**

## ■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FRAM). WPEN protects writing to a status register (refer to “■ WRITING PROTECT”) relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to “■ BLOCK PROTECT”). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. Achieving continuous writing mode, WEL is not reset after following operations making it possible to execute writing commands continuously. After WRSR command recognition. After WRITE command recognition. After WRSN command recognition. After SSWR command recognition.
0	0	This is a bit fixed to “0”.

## ■ OP-CODE

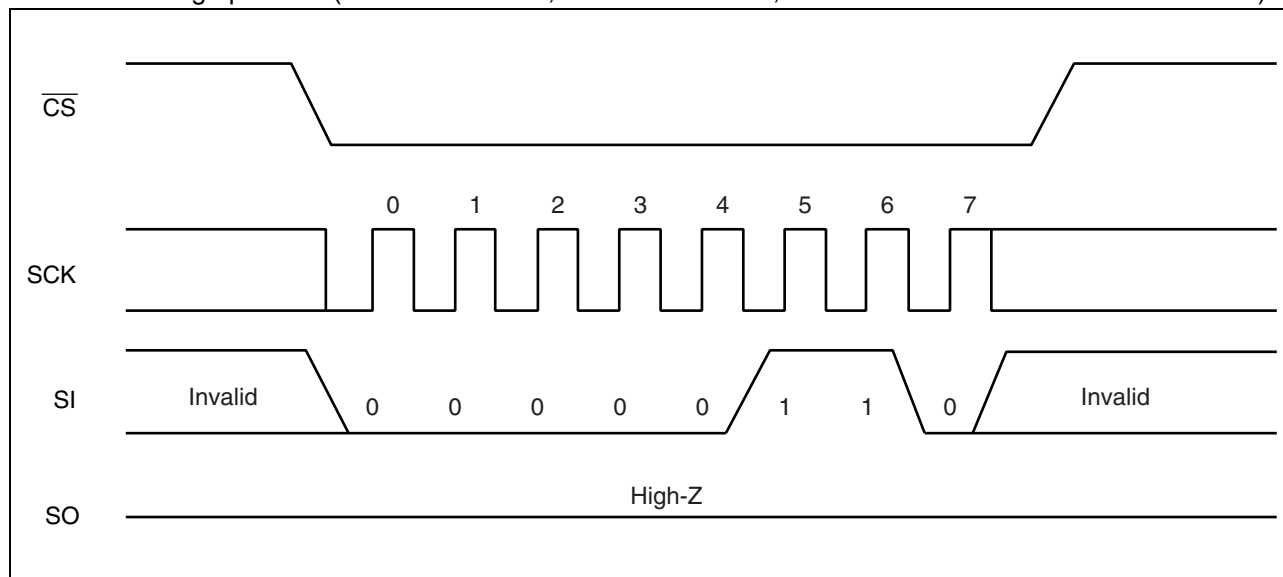
MB85RS2MLY accepts 14 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If  $\overline{CS}$  is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110 <sub>B</sub>
WRDI	Reset Write Enable Latch	0000 0100 <sub>B</sub>
RDSR	Read Status Register	0000 0101 <sub>B</sub>
WRSR	Write Status Register	0000 0001 <sub>B</sub>
READ	Read Memory Code	0000 0011 <sub>B</sub>
WRITE	Write Memory Code	0000 0010 <sub>B</sub>
FSTRD	Fast Read Memory Code	0000 1011 <sub>B</sub>
RDID	Read Device ID	1001 1111 <sub>B</sub>
RUID	Read Unique ID	0100 1100 <sub>B</sub>
WRSN	Write Serial Number	1100 0010 <sub>B</sub>
RDSN	Read Serial Number	1100 0011 <sub>B</sub>
SSWR	Write Special Sector	0100 0010 <sub>B</sub>
SSRD	Read Special Sector	0100 1011 <sub>B</sub>
FSSRD	Fast Read Special Sector	0100 1001 <sub>B</sub>
RFU	Reserved	1011 1001 <sub>B</sub>
		1100 0001 <sub>B</sub>
		1100 0110 <sub>B</sub>
		1100 1110 <sub>B</sub>
		1100 1111 <sub>B</sub>

## ■ COMMAND

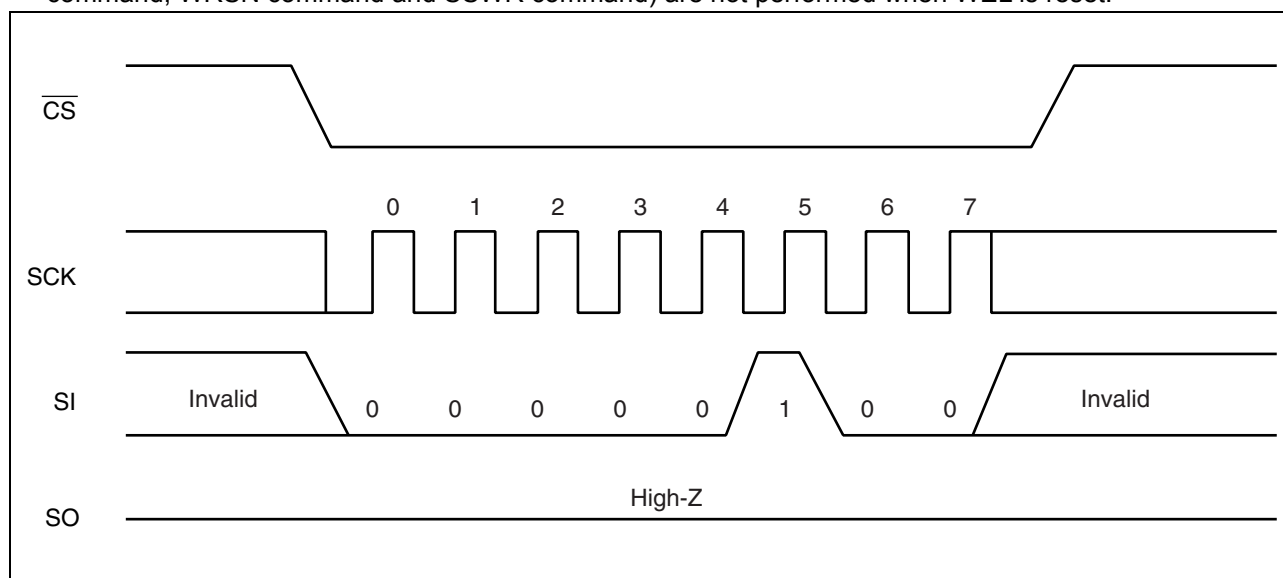
### • WREN

The WREN command sets WEL (Write Enable Latch) bit to 1. WEL has to be set with the WREN command before writing operation (WRSR command, WRITE command, WRSN command and SSWR command) .



### • WRDI

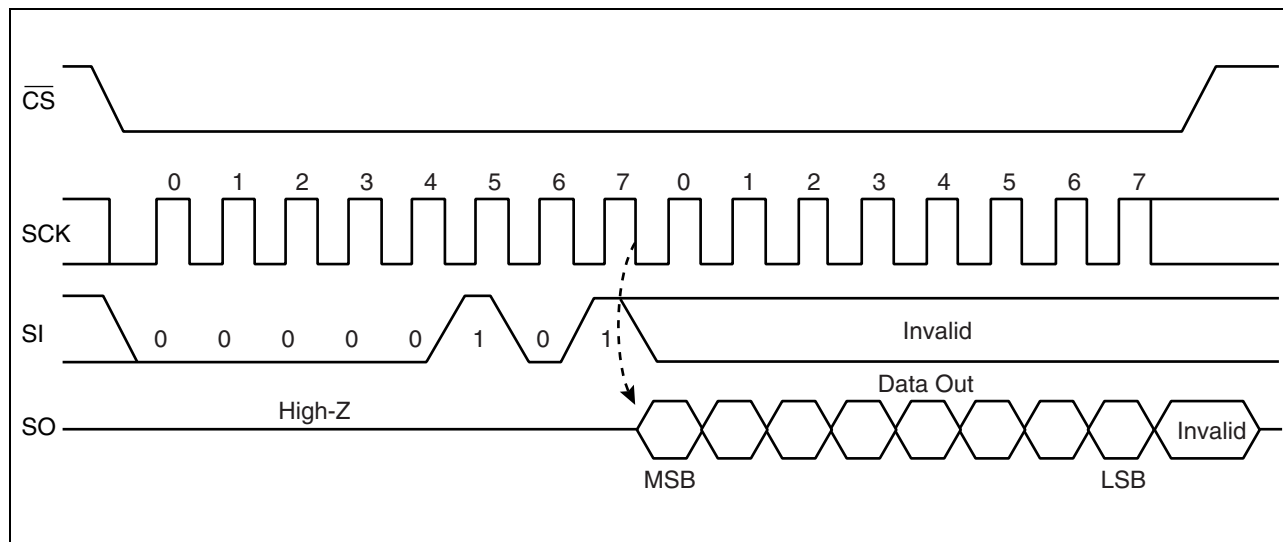
The WRDI command resets WEL (Write Enable Latch) bit to 0. Writing operation (WRSR command, WRITE command, WRSN command and SSWR command) are not performed when WEL is reset.





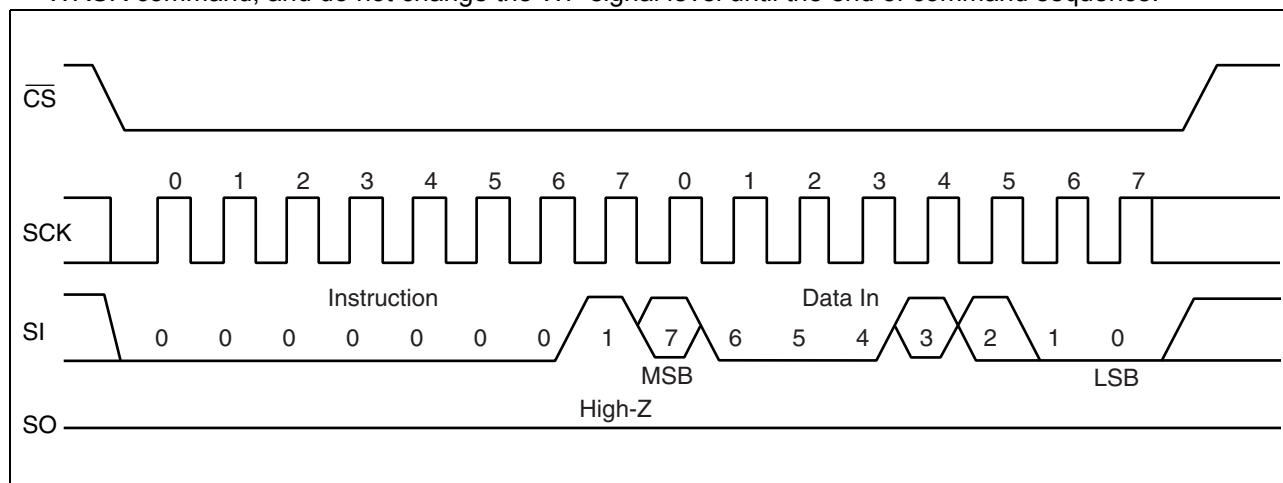
## • RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of  $\overline{CS}$ .



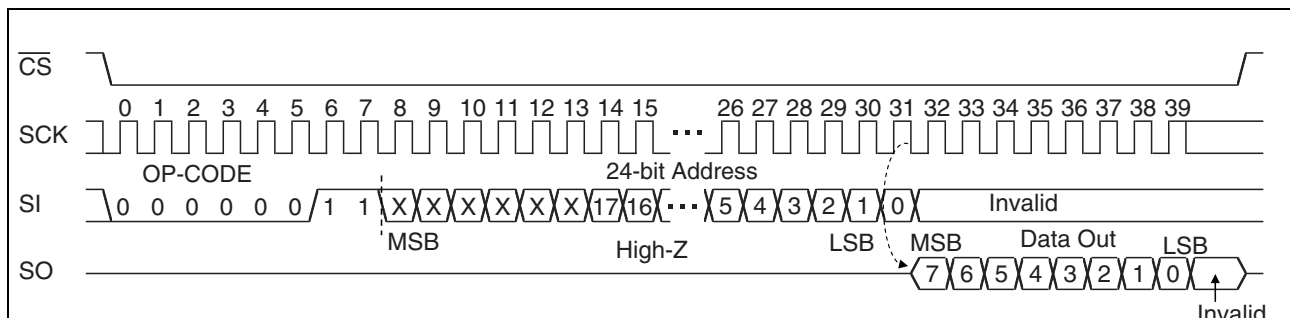
## • WRSR

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored.  $\overline{WP}$  signal level shall be fixed before performing WRSR command, and do not change the  $\overline{WP}$  signal level until the end of command sequence.



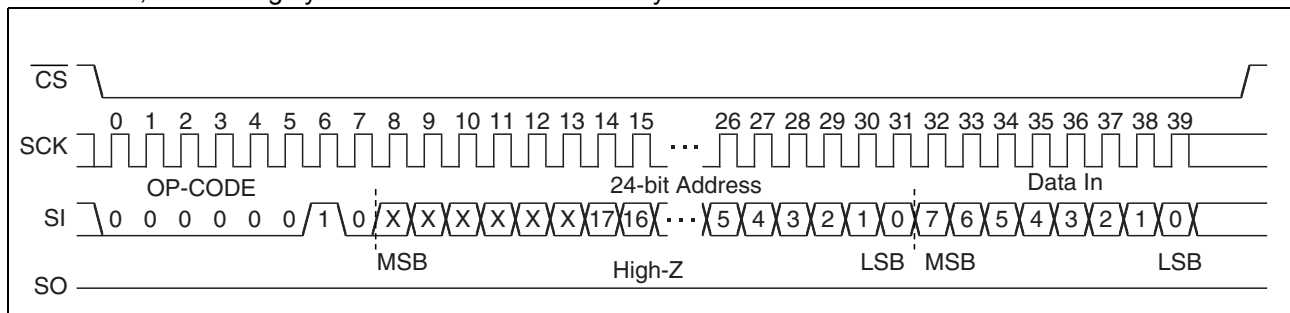
## • READ

The READ command reads FRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The most significant address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before  $\overline{CS}$  rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



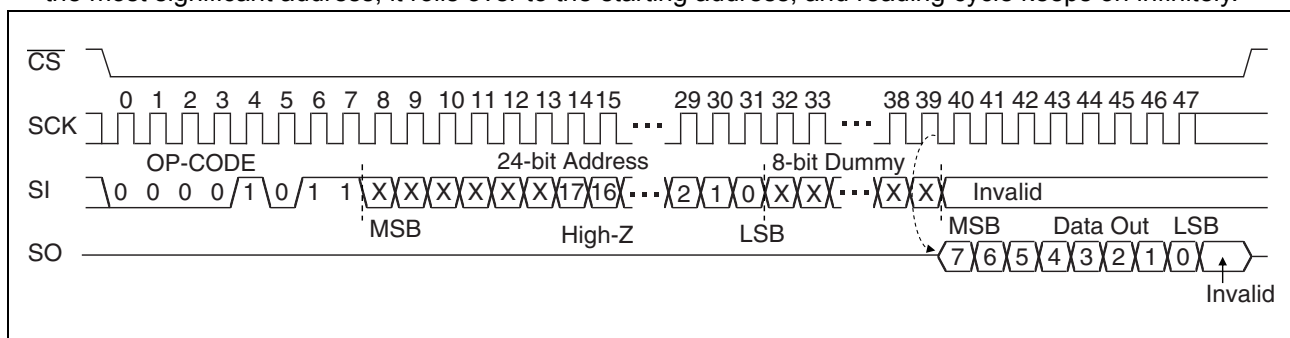
## • WRITE

The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The most significant address bit is invalid. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen  $\overline{CS}$  will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before  $\overline{CS}$  rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely.



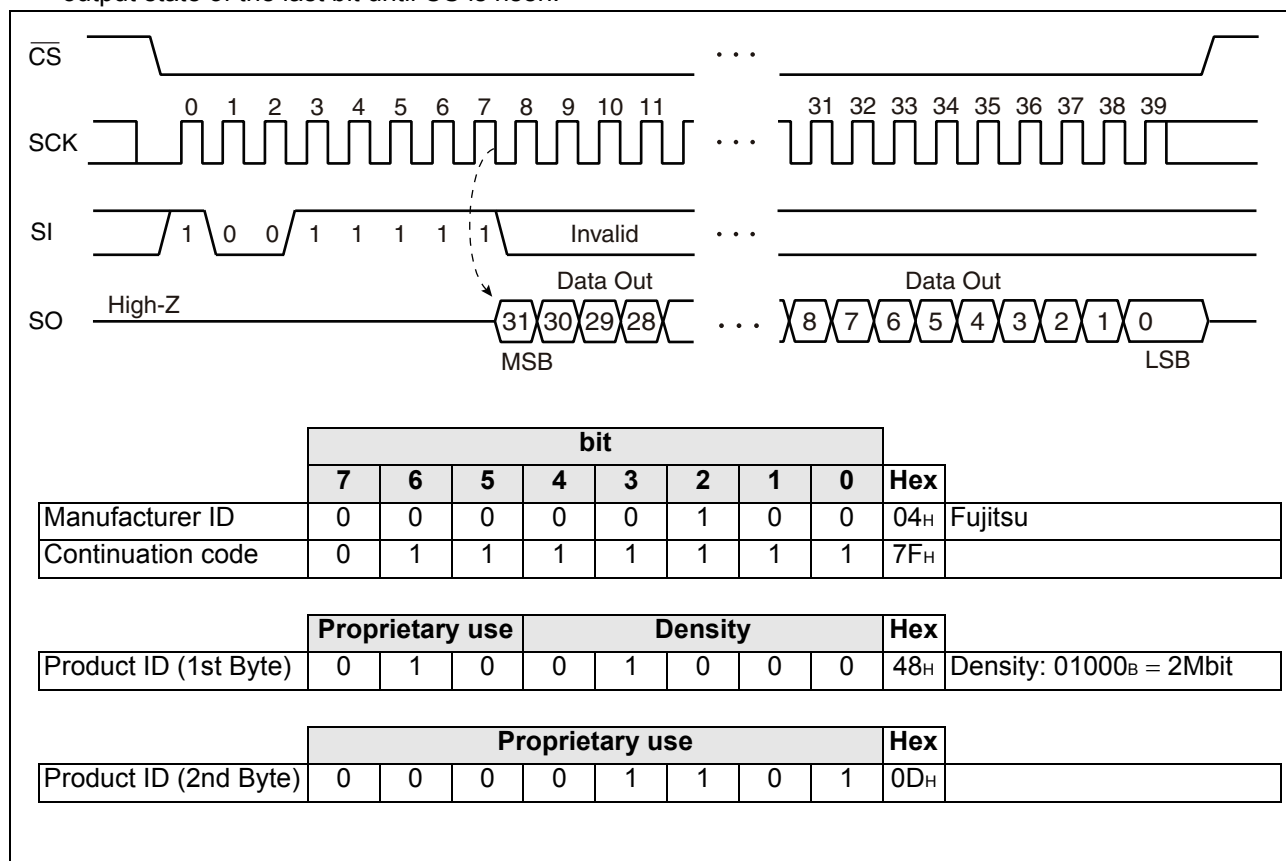
## • FSTRD

The FSTRD command reads FRAM memory cell array data. Arbitrary 24 bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 6-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the FSTRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before  $\overline{CS}$  rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



## • RDID

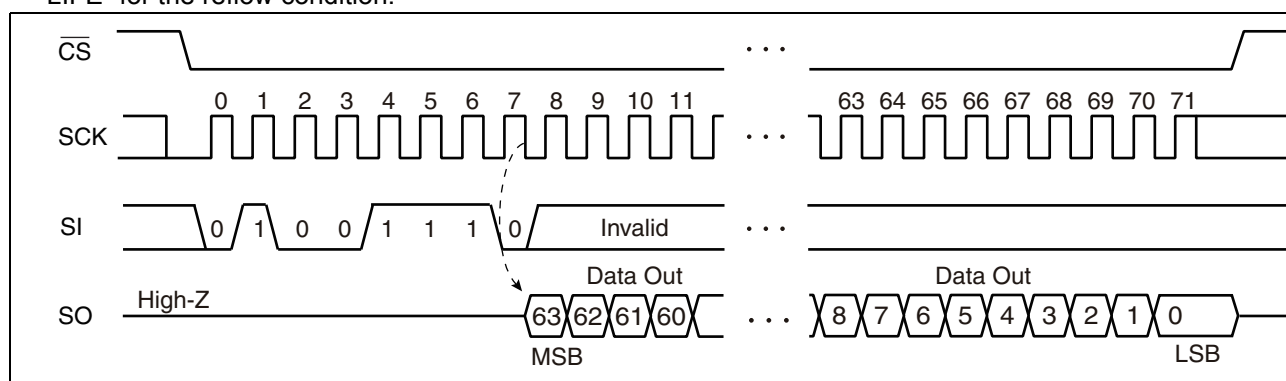
The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, 32-bit Device ID is output by continuously sending SCK clock, and SO holds the output state of the last bit until  $\overline{CS}$  is risen.



## • RUID

The RUID command reads an unique ID which is defined in 64bits for each device. After performing RUID op-code to SI, 64-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK.

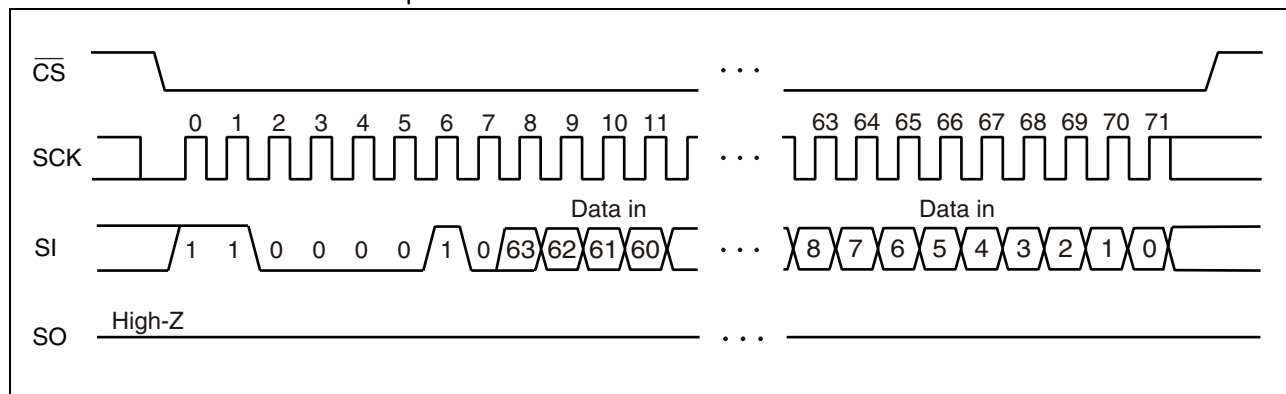
The unique ID is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



## •WRSN

The WRSN command writes data to serial number region which is allowed to write only one time. After performing WRSN op-code to SI, 64bits of writing data is input. Once wrote, the serial number region is protected, disabling to overwrite even when issuing WRSN command.

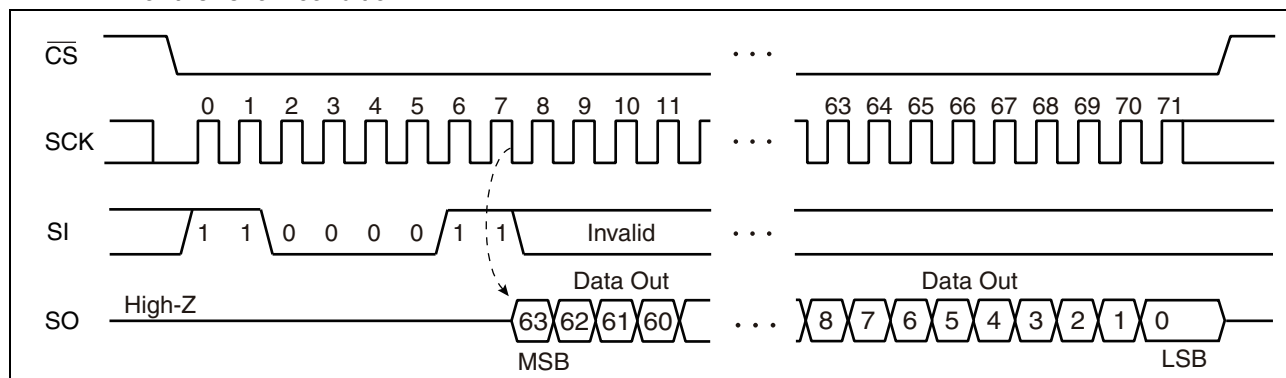
$\overline{WP}$  signal level shall be fixed before performing WRSN command, and do not change the  $\overline{WP}$  signal level until the end of command sequence.



## •RDSN

The RDSN command reads 64 bits of serial number which is written using WRSN command. After performing RDSN op-code to SI, 64-cycle clock to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. When reading serial number from devices which no WRSN command is executed, "0" for all bits are output.

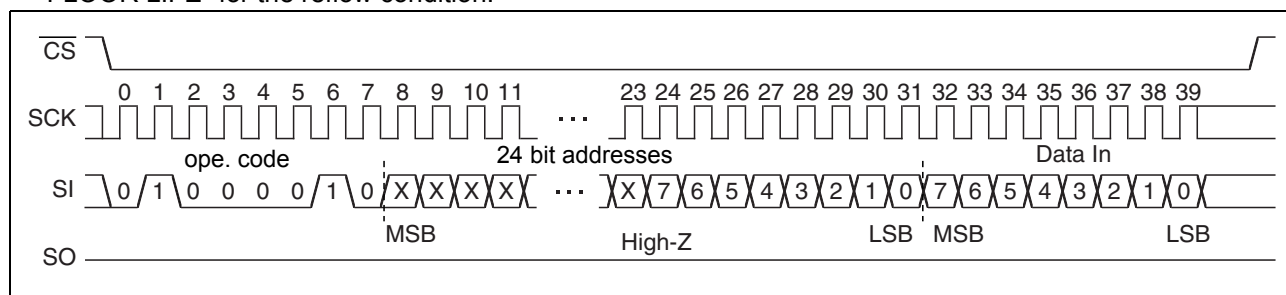
The serial number is stable between before and after reflow. Refer "■ REFLOW CONDITIONS AND FLOOR LIFE" for the reflow condition.



## • SSWR

The SSWR command writes data to special sector (a special region of 256 Byte in FRAM). SSWR op-code, arbitrary 24 bits address and 8-bit writing data are input to SI. The 16-bit upper address is invalid. When input of 8-bit writing data is completed, it starts writing data to special sector. Risen  $\overline{CS}$  will terminate the SSWR command, but if you continue the writing data for each before  $\overline{CS}$  rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, roll over is not happen, the data hereafter is ignored.

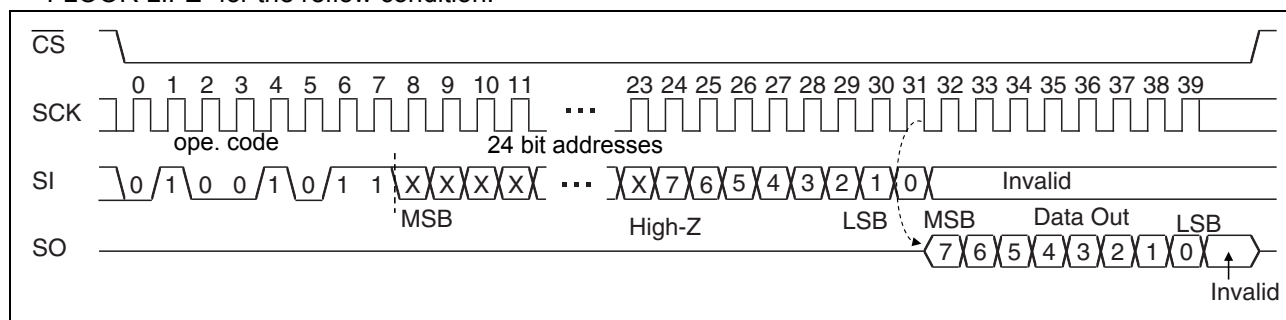
The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



## • SSRD

The SSRD command reads data from special sector (a special region of 256 Byte in FRAM). SSWR op-code and arbitrary 24 bits address are input to SI. The 16-bit upper address is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the SSRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before  $\overline{CS}$  rising. When it reaches the most significant address, roll over is not happen.

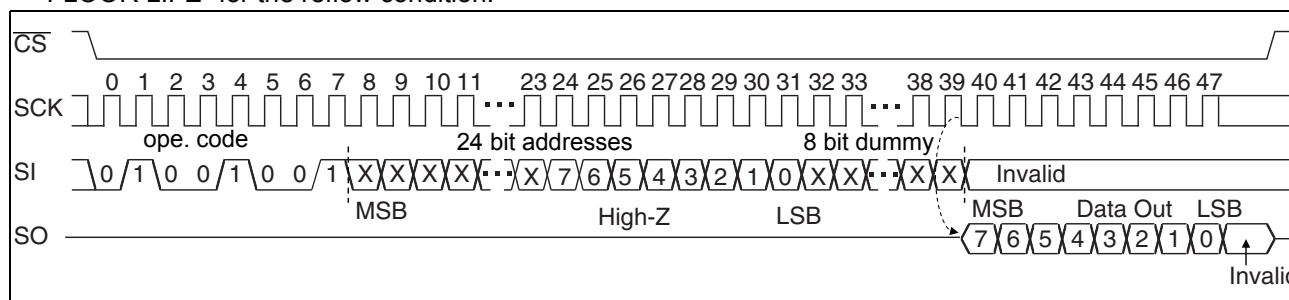
The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



## • FSSRD

The SSRD command reads data from special sector (a special region of 256 Byte in FRAM). SSWR op-code and arbitrary 24 bits address are input to SI followed by 8 bits dummy. The 16-bit upper address is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the SSRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before  $\overline{CS}$  rising. When it reaches the most significant address, roll over is not happen.

The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



## ■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	6000 <sub>H</sub> to 7FFF <sub>H</sub> (upper 1/4)
1	0	4000 <sub>H</sub> to 7FFF <sub>H</sub> (upper 1/2)
1	1	0000 <sub>H</sub> to 7FFF <sub>H</sub> (all)

## ■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, WP as shown in the table.

WEL	WPEN	WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	$V_{DD}$	- 0.5	+ 2.5	V
Input voltage*	$V_{IN}$	- 0.5	$V_{DD} + 0.5 (\leq 2.5)$	V
Output voltage*	$V_{OUT}$	- 0.5	$V_{DD} + 0.5 (\leq 2.5)$	V
Operation ambient temperature	$T_A$	- 40	+ 125	°C
Storage temperature	$T_{stg}$	- 55	+ 150	°C

\*: These parameters are based on the condition that  $V_{SS}$  is 0 V.

**WARNING:** Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.  
Do not exceed any of these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	$V_{DD}$	1.70	1.80	1.95	V
Operation ambient temperature*2	$T_A$	- 40	—	+ 125	°C

\*1: These parameters are based on the condition that  $V_{SS}$  is 0 V.

\*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.  
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input leakage current*1	$ I_{Li} $	$\overline{CS} = V_{DD}$	25 °C	—	—	1	$\mu A$
			125 °C			2	
		$\overline{WP}, \overline{SCK}, \overline{CS}, SI, \overline{RESET} = 0 \text{ V to } V_{DD}$	25 °C	—	—	1	
			125 °C			2	
Output leakage current*2	$ I_{Lo} $	$SO = 0 \text{ V to } V_{DD}$	25 °C	—	—	1	$\mu A$
			125 °C			2	
Operating power supply current*3	$I_{DD}$	$SCK = 50 \text{ MHz}$	FSSRD/SSWR	—	TBD	TBD	mA
			other than above	—	TBD	4	
Standby current	$I_{SB}$	$\overline{SCK} = SI = \overline{CS} = \overline{WP} = \overline{RESET} = V_{DD}$		—	TBD	220	$\mu A$
Input high voltage	$V_{IH}$	$V_{DD} = 1.7 \text{ V to } 1.95 \text{ V}$		$V_{DD} \times 0.7$	—	$V_{DD} + 0.3$	V
Input low voltage	$V_{IL}$	$V_{DD} = 1.7 \text{ V to } 1.95 \text{ V}$		- 0.3	—	$V_{DD} \times 0.3$	V
Output high voltage	$V_{OH}$	$I_{OH} = -2 \text{ mA}$		$V_{DD} - 0.5$	—	—	V
Output low voltage	$V_{OL}$	$I_{OL} = 2 \text{ mA}$		—	—	0.4	V

\*1 : Applicable pin :  $\overline{CS}, \overline{WP}, \overline{SCK}, SI, \overline{RESET}$

\*2 : Applicable pin :  $SO$

\*3 : Input voltage magnitude :  $V_{DD} - 0.2 \text{ V}$  or  $V_{SS}$



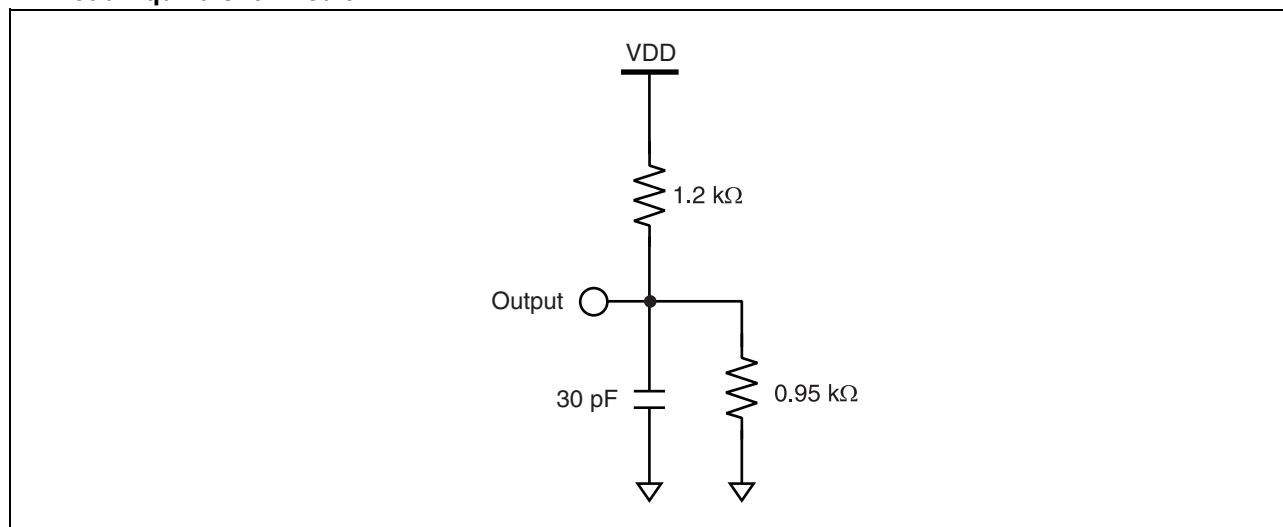
## 2. AC Characteristics

Parameter	Symbol	Value		Unit	Condition $V_{DD}$
		Min	Max		
SCK clock frequency	$f_{CK}$	—	50(TBD)	MHz	2.7V to 3.6V all commands except for READ/ SSRD
		—	40		READ command
		—	10		SSRD command
Clock high time	$t_{CH}$	9	—	ns	
Clock low time	$t_{CL}$	9	—	ns	
Chip select set up time	$t_{CSU}$	11	—	ns	
Chip select hold time	$t_{CSH}$	5	—	ns	
Output disable time	$t_{OD}$	—	10	ns	
Output data valid time	$t_{ODV}$	—	11(TBD)	ns	
Output hold time	$t_{OH}$	0	—	ns	
Deselect time	$t_D$	40	—	ns	
Data in rising time	$t_R$	—	50	ns	
Data falling time	$t_F$	—	50	ns	
Data set up time	$t_{SU}$	5	—	ns	
Data hold time	$t_H$	5	—	ns	

## AC Test Condition

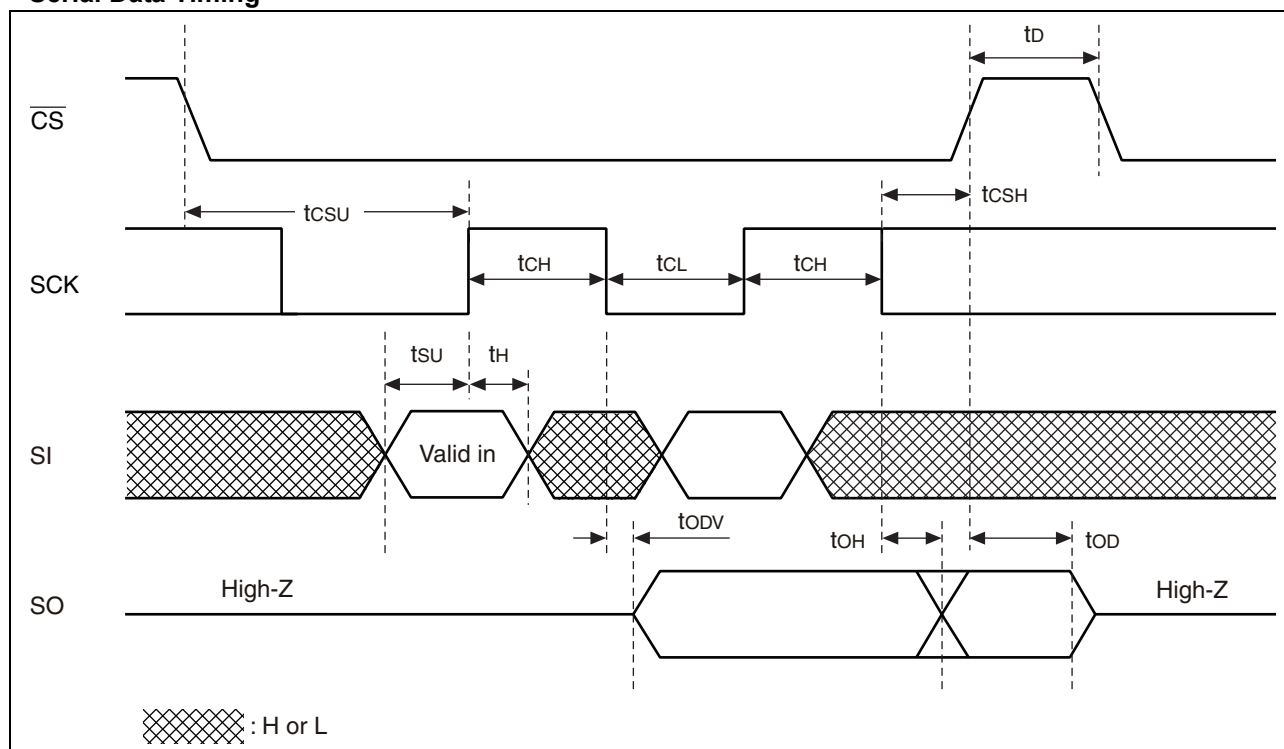
Power supply voltage : 1.7 V to 1.95 V Operation  
 Operation ambient temperature : - 40 °C to + 125 °C  
 Input voltage magnitude :  $V_{DD} \times 0.8 \leq V_{IH} \leq V_{DD}$   
    $0 \leq V_{IL} \leq V_{DD} \times 0.2$   
 Input rising time : 5 ns  
 Input falling time : 5 ns  
 Input judge level :  $V_{DD}/2$   
 Output judge level :  $V_{DD}/2$

## AC Load Equivalent Circuit

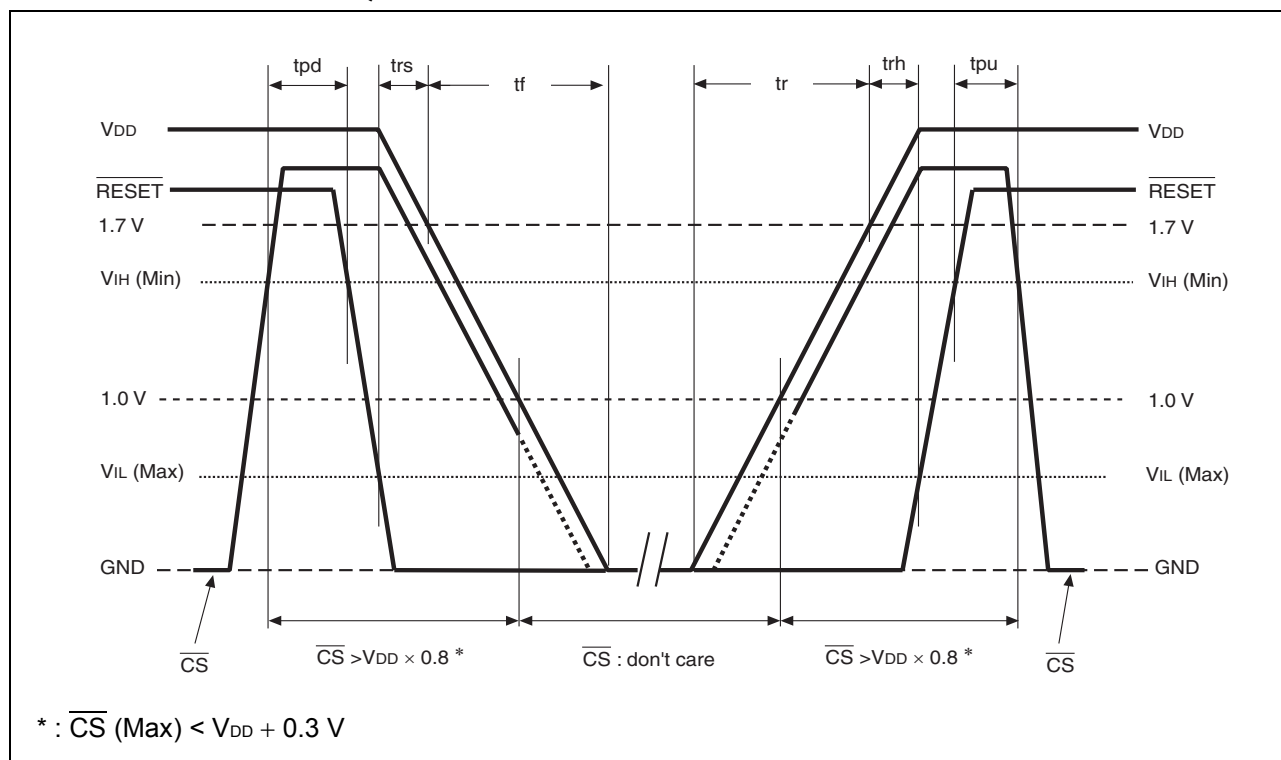


## 3. Pin Capacitance

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	$C_O$	$V_{DD} = 1.8 \text{ V}$ , $V_{IN} = V_{OUT} = 0 \text{ V to } V_{DD}$ , $f = 1 \text{ MHz}$ , $T_A = +25 \text{ }^\circ\text{C}$	—	8	pF
Input capacitance	$C_I$		—	6	pF



## ■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value		Unit
		Min	Max	
$\overline{CS}$ and $\overline{RESET}$ level hold time at power OFF	tpd	400	—	ns
$\overline{RESET}$ high to first access start	tpu	450	—	$\mu\text{s}$
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V
$\overline{RESET}$ setup time to $V_{DD}(\text{min})$ at power OFF	trs	0	—	$\mu\text{s}$
$\overline{RESET}$ hold time to $V_{DD}(\text{min})$ at power ON	trh	1	—	$\mu\text{s}$

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, the device may lose its function.

## ■ FRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance*1	$10^{13}$	—	Times/byte	Operation Ambient Temperature $T_A = +125^\circ\text{C}$
Data Retention*2	0.85 or more*3	—	Years	Operation Ambient Temperature $T_A = +125^\circ\text{C}$
	2.75	—		Operation Ambient Temperature $T_A = +105^\circ\text{C}$
	10	—		Operation Ambient Temperature $T_A = +85^\circ\text{C}$

\*1 : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

\*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

\*3: Under evaluation for more than 0.85years(+125 °C).

## ■ NOTE ON USE

We recommend programming of the device after reflow except for special sector region and serial number region. Data written before reflow cannot be guaranteed.

## ■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RS2MLYPNF-GS-AWE2 MB85RS2MLYPNF-GS-AWERE2 MB85RS2MLYPN-GS-AWEWE2	$\geq  2000 \text{ V} $
ESD CDM (Charged Device Model) AEC-Q100-011(FI-CDM) compliant		$\geq  500 \text{ V} $
Latch-Up (I-test) JESD78 compliant		$\geq  125\text{mA} $
Latch-Up ( $V_{\text{supply}}$ overvoltage test) JESD78 compliant		$\geq 2.93\text{V}$

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

## ■ Current status on Contained Restricted Substances

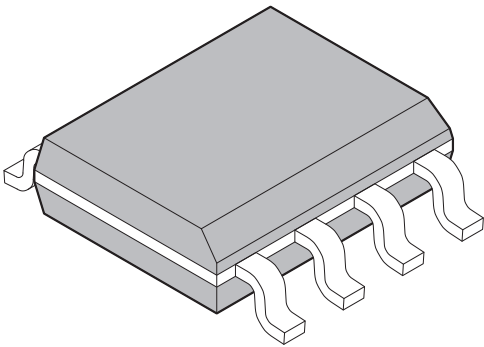
This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

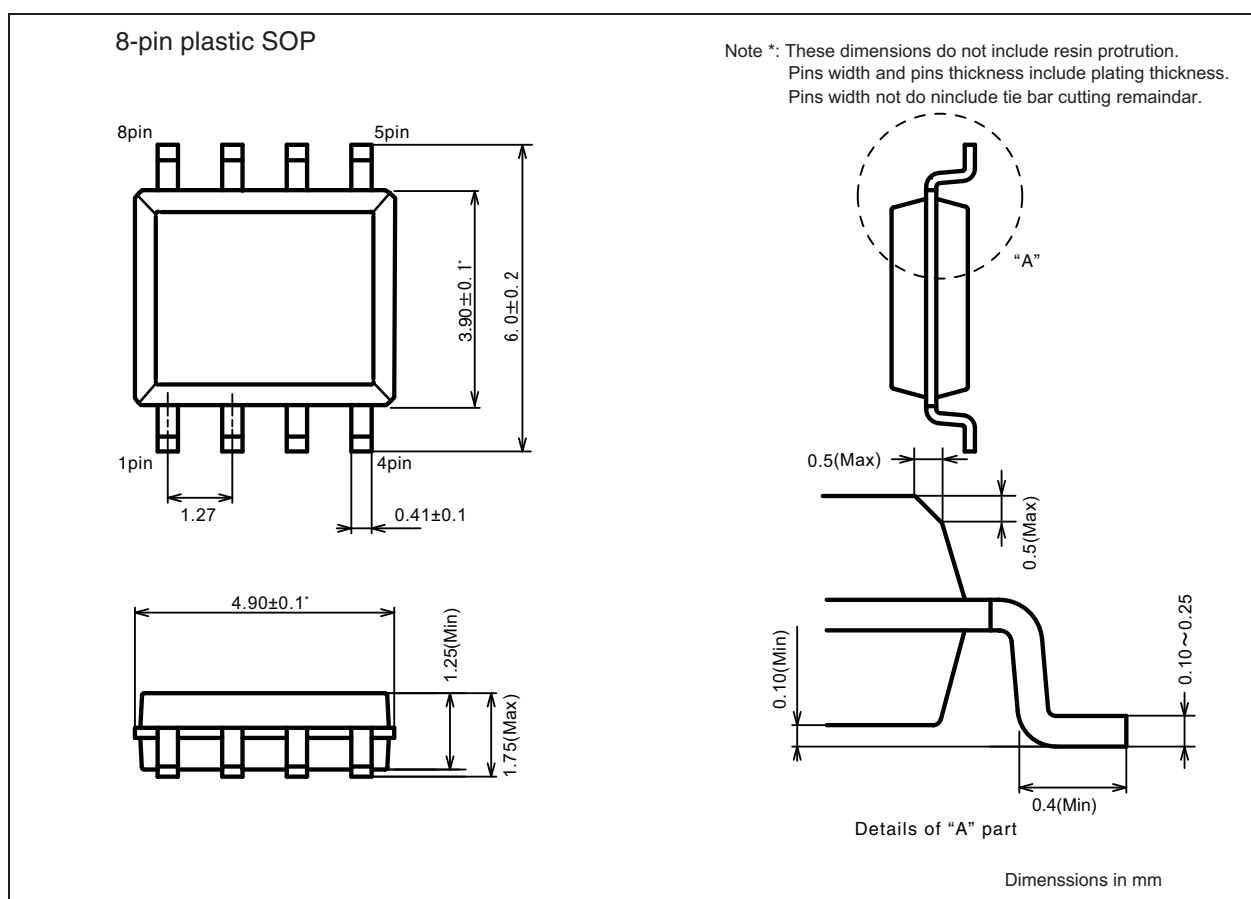
## ■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RS2MLYPNF-GS-AWE2	8-pin plastic SOP (FPT-8P)	Tube	— *
MB85RS2MLYPNF-GS-AWERE2	8-pin plastic SOP (FPT-8P)	Embossed Carrier tape	1500
MB85RS2MLYPN-GS-AWEWE2	8-pin plastic DFN (LCC-8P)	Embossed Carrier tape	1500

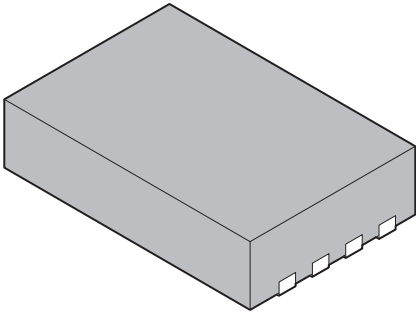
\* : Please contact our sales office about minimum shipping quantity.

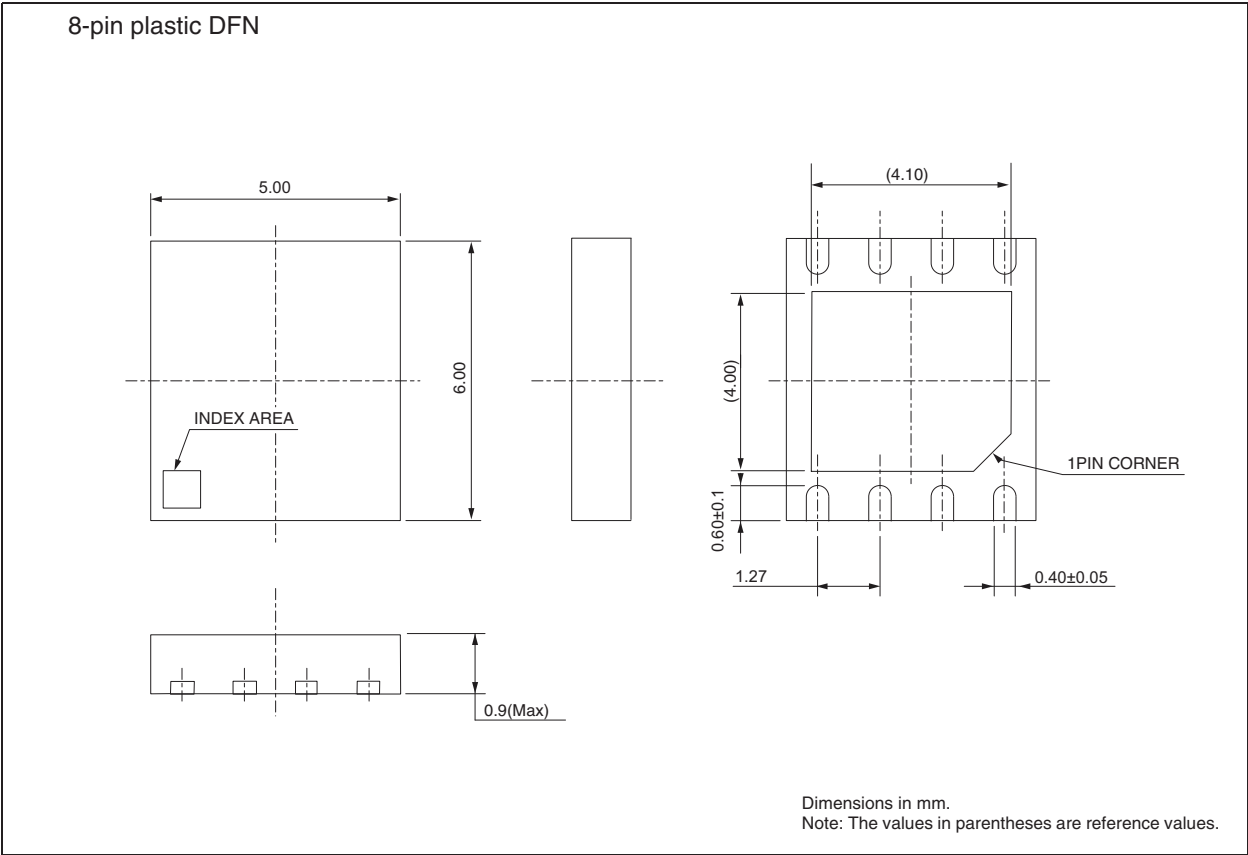
## ■ PACKAGE DIMENSION

<p>8-pin plastic SOP</p>  <p>(FPT-8P)</p>	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 4.9 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX



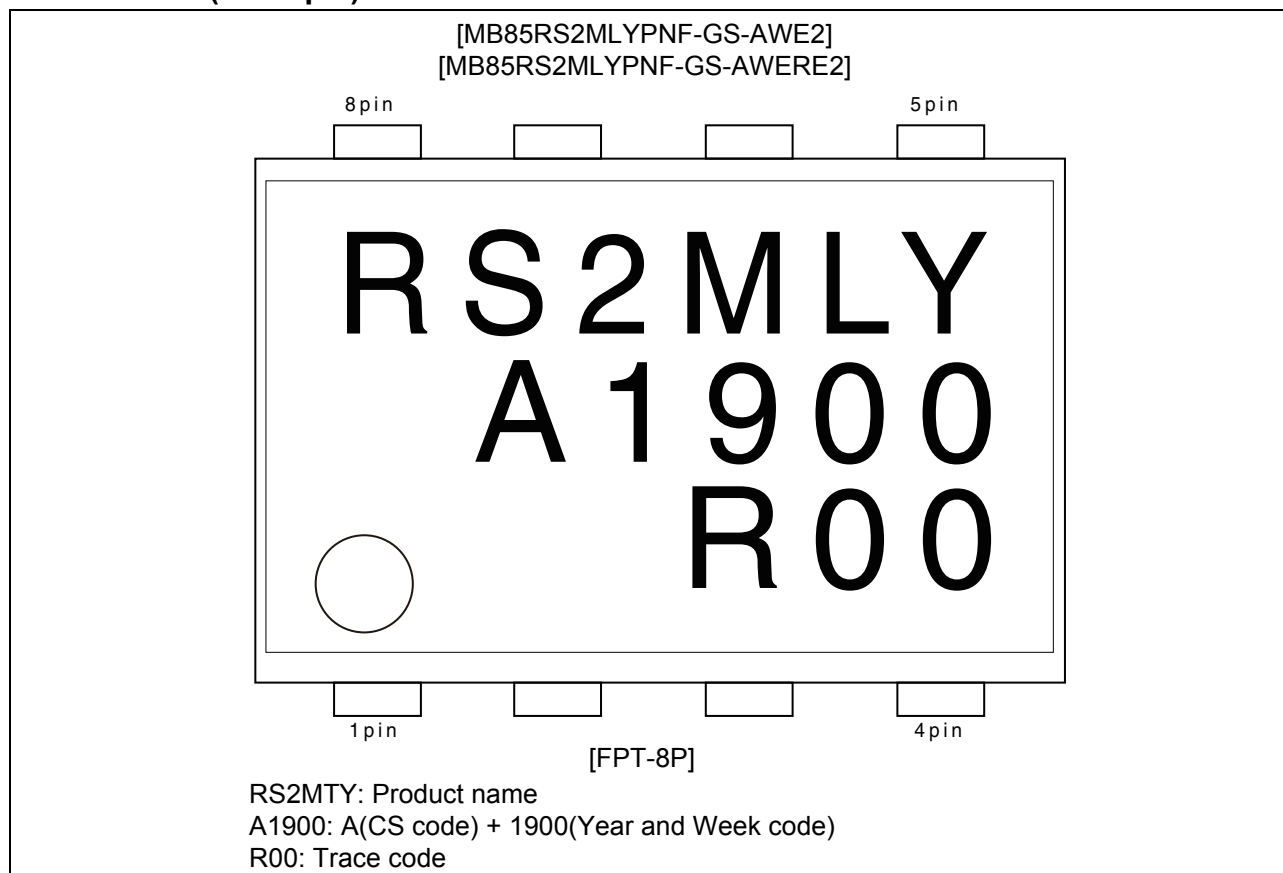
(Continued)

<div>8-pin plastic DFN</div> <div></div> <div>(LCC-8P)</div>	Lead pitch	1.27 mm
	Package width × package length	5.0 mm × 6.0 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX





## ■ MARKING (Example)

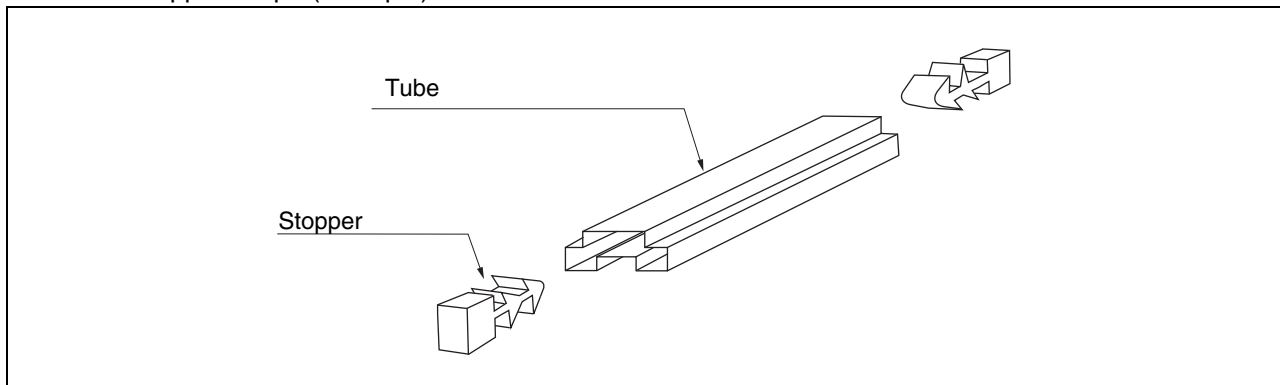


## ■ PACKING INFORMATION

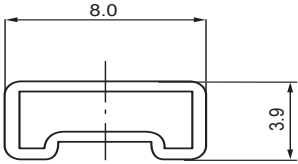
### 1. Tube

#### 1.1 Tube Dimensions

- Tube/stopper shape (example)



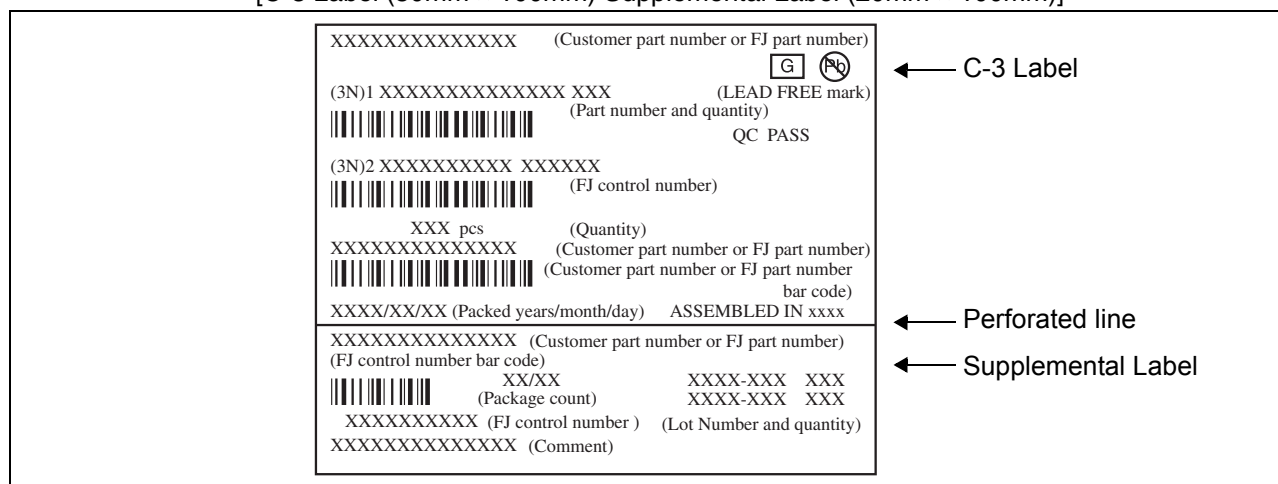
- Tube cross-sections and Maximum quantity

 <p>No heat resistance. Package should not be baked by using tube.</p>	Maximum quantity		
	pcs/tube(509mm)	pcs/inner box	pcs/outer box
	85	4,250	25,500

Dimensions in mm)

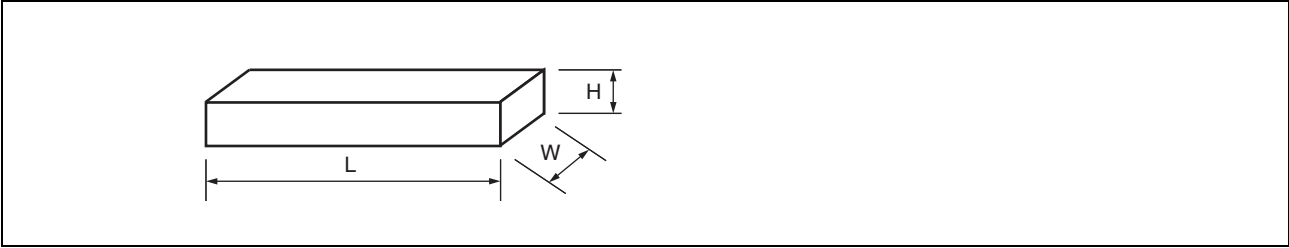
### 1.2 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)  
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



1.3 Dimensions for Containers

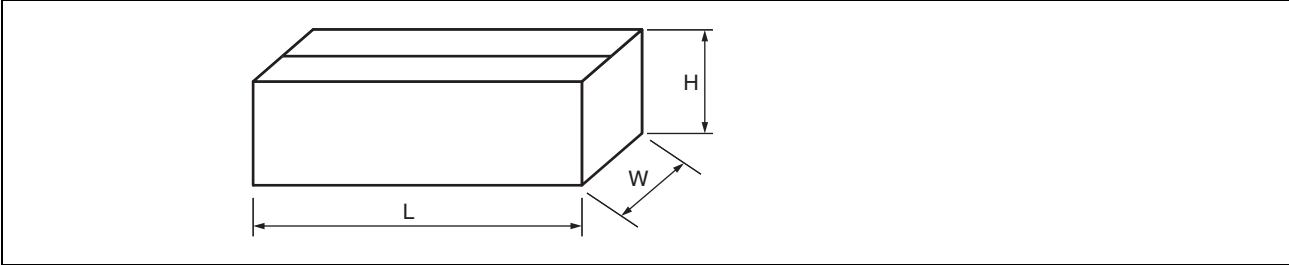
(1) Dimensions for inner box



L	W	H
549	125	81

(Dimensions in mm)

(2) Dimensions for outer box

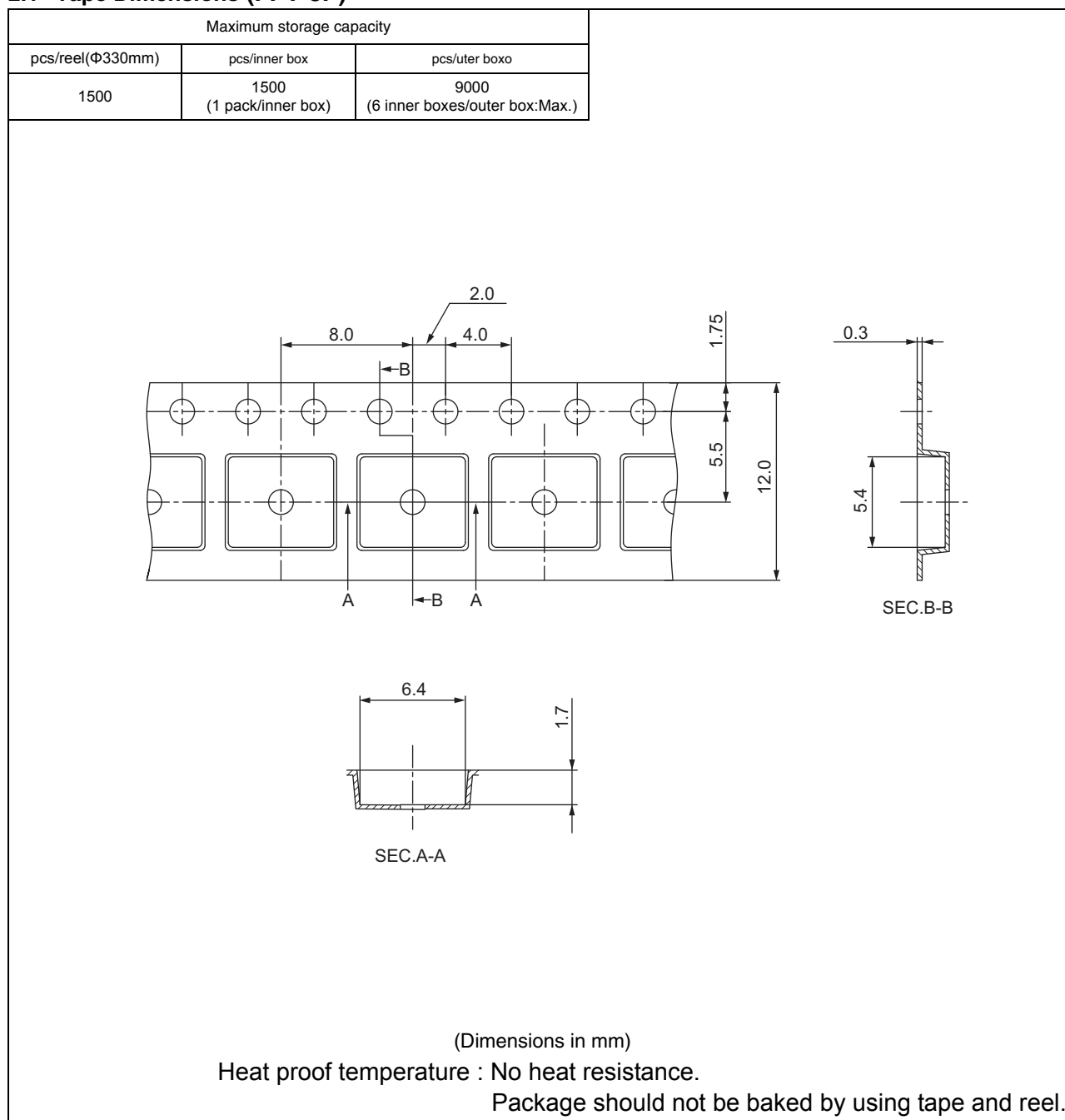


L	W	H
567	272	269

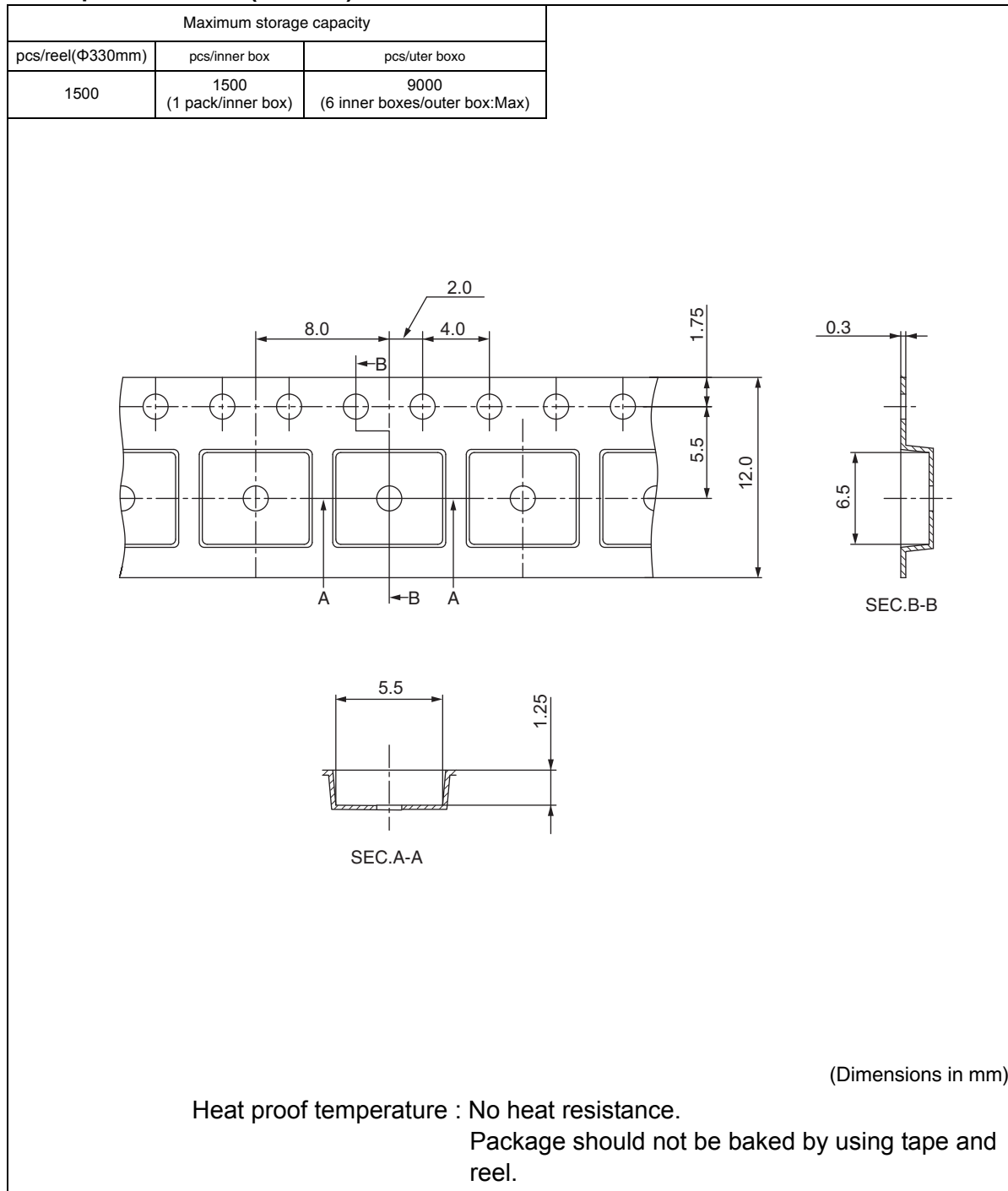
(Dimensions in mm)

## 2. Emboss Tape

### 2.1 Tape Dimensions (FPT-8P)

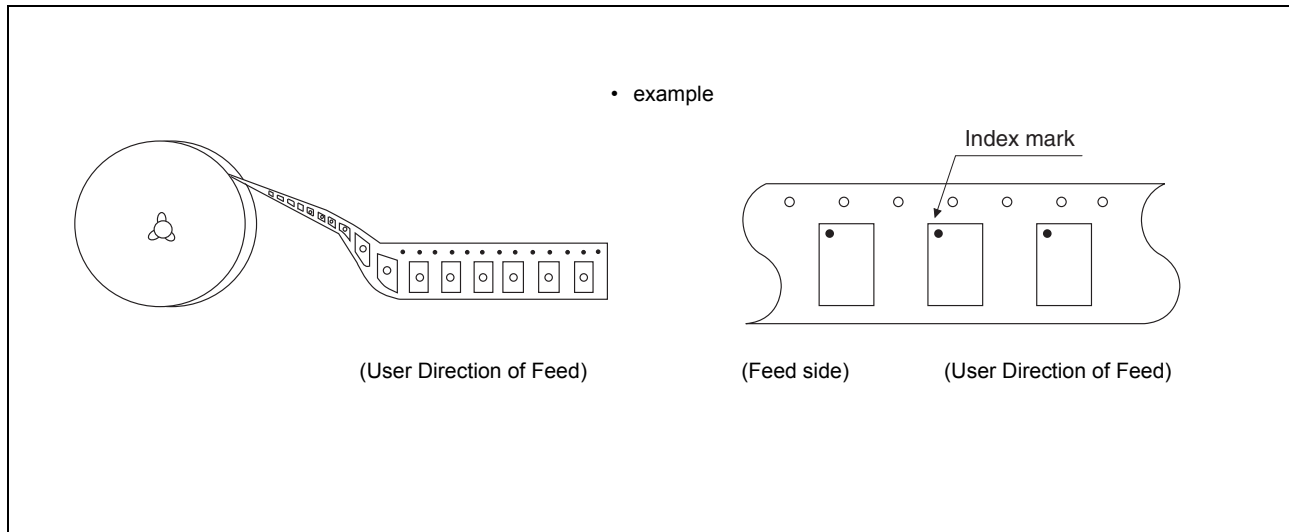


## 2.2 Tape Dimensions (LCC-8P)

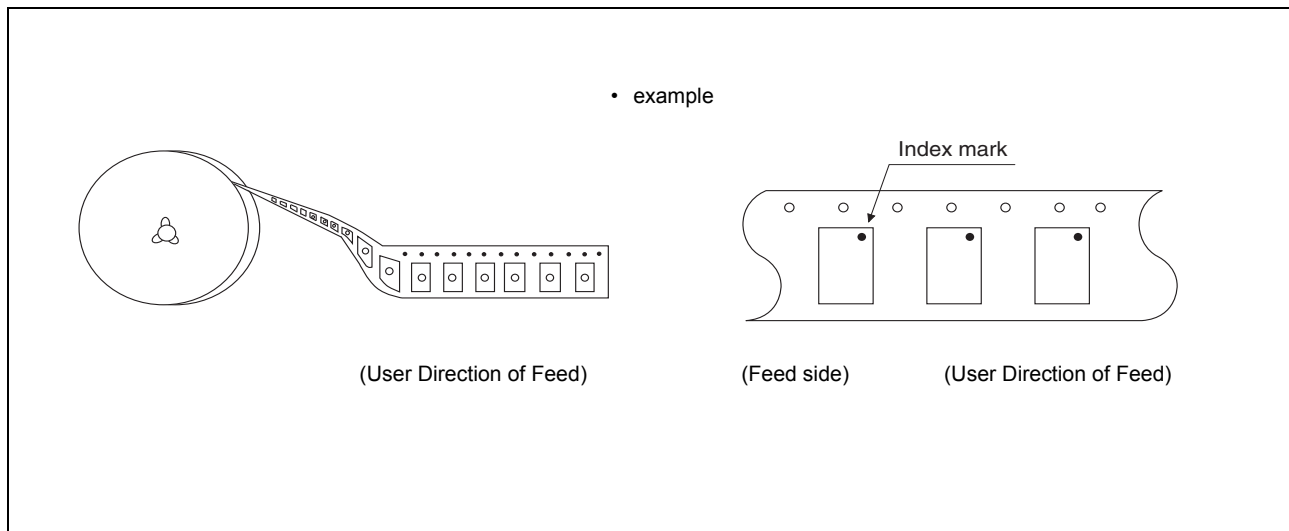


## 2.3 IC orientation

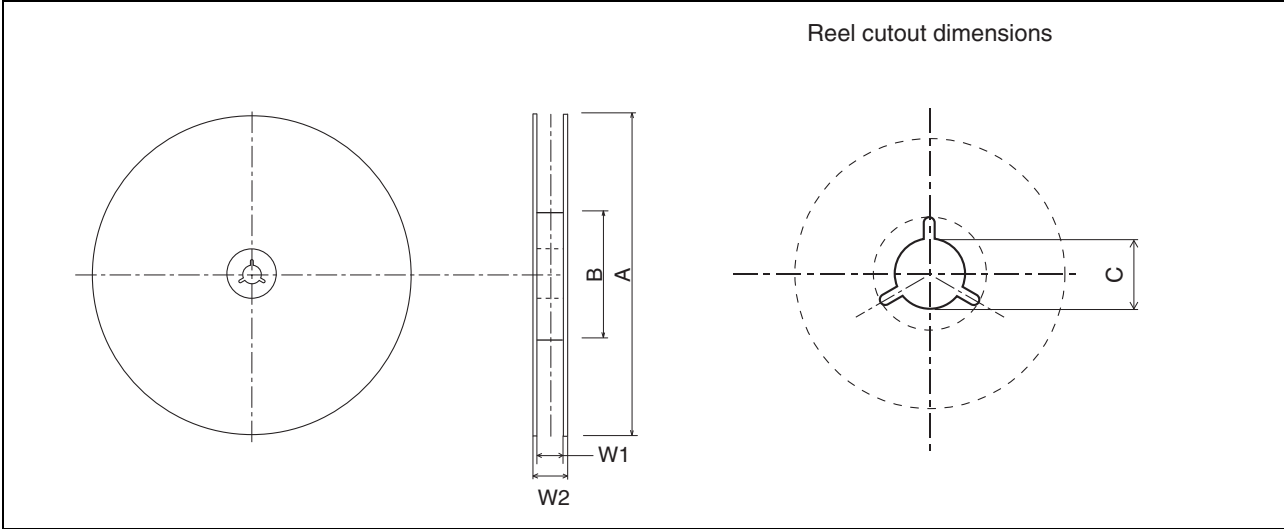
### FTP-8P



### LCC-8P



2.4 Reel dimensions



Dimensions in mm

A	B	C	W1	W2
300	100	13	13.5	17.5

2.5 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss tapping)  
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

XXXXXXXXXXXXXXXX (Customer part number or FJ part number)

(3N)1 XXXXXXXXXXXXXXX XXX (LEAD FREE mark)

XXXXXXXXXXXXXXXX

QC PASS

(3N)2 XXXXXXXXXXXXXXX XXXXXXX

XXXXXXXXXXXXXXXX

(FJ control number)

XXX pcs (Quantity)

XXXXXXXXXXXXXXXX (Customer part number or FJ part number)

XXXXXXXXXXXXXXXX

(Customer part number or FJ part number bar code)

XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx

XXXXXXXXXXXXXXXX (Customer part number or FJ part number)

(FJ control number bar code)

XX/XX XXXX-XXX XXX

(Package count) XXXX-XXX XXX

XXXXXXXXXXXX (FJ control number) (Lot Number and quantity)

XXXXXXXXXXXXXXXX (Comment)

← C-3 Label

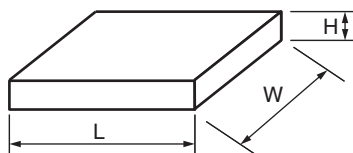
← Perforated line

← Supplemental Label



## 2.6 Dimensions for Containers

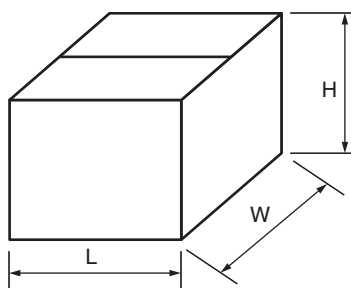
### (1) Dimensions for inner box



Tape width	L	W	H
12	350	335	35

(Dimensions in mm)

### (2) Dimensions for outer box



L	W	H
384	368	225

(Dimensions in mm)

# MB85RS2MLY(AEC-Q100 Compliant)

## FUJITSU SEMICONDUCTOR LIMITED

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