

# Memory FRAM

## 64 K (8 K × 8) Bit I<sup>2</sup>C

# MB85RC64TA

### ■ DESCRIPTION

The MB85RC64TA is an FRAM (Ferroelectric Random Access Memory) chip in a configuration of 8,192 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

Unlike SRAM, the MB85RC64TA is able to retain data without using a data backup battery.

The read/write endurance of the nonvolatile memory cells used for the MB85RC64TA has improved to be at least 10<sup>13</sup> cycles, significantly outperforming Flash memory and E<sup>2</sup>PROM in the number.

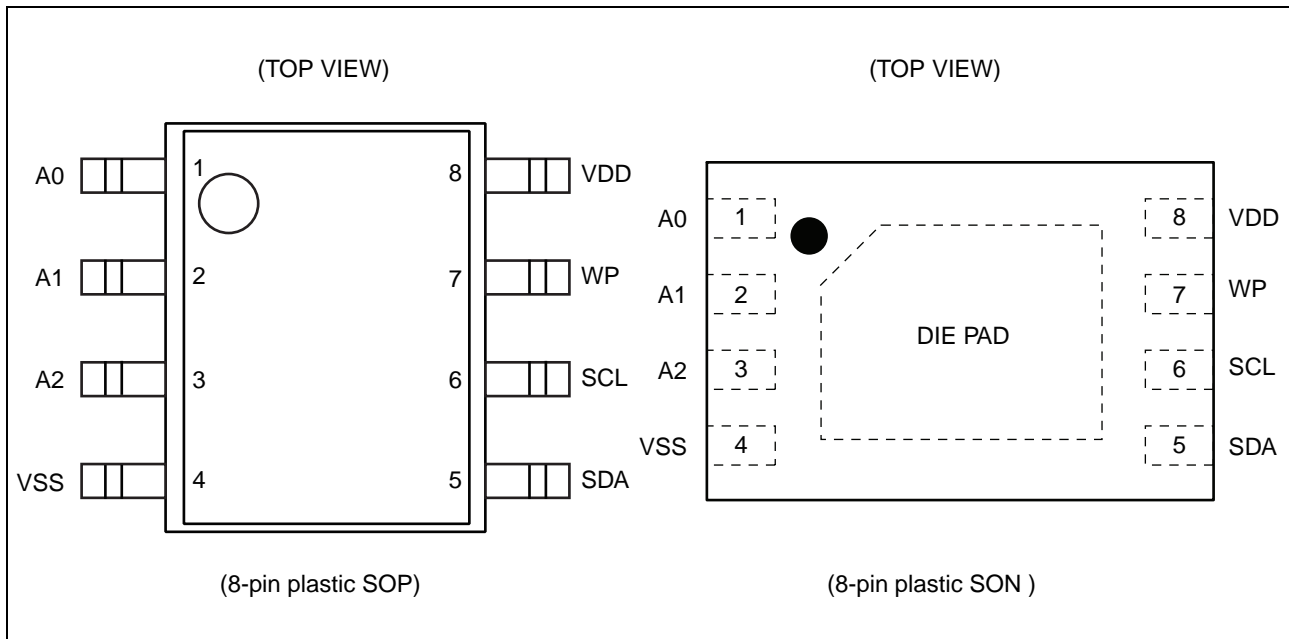
The MB85RC64TA does not need a polling sequence after writing to the memory such as the case of Flash memory or E<sup>2</sup>PROM.

### ■ FEATURES

- Bit configuration : 8,192 words × 8 bits
- Two-wire serial interface : Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating frequency : 3.4 MHz (Max @HIGH SPEED MODE)  
1 MHz (Max @FAST MODE PLUS)
- Read/write endurance : 10<sup>13</sup> times / byte
- Data retention : 19.1 years (+ 105 °C), 70.4 years (+ 85 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power consumption : Operating power supply current 170 μA (Typ @3.4 MHz)  
Standby current 8 μA (Typ)  
Sleep current 4 μA (Typ)
- Operation ambient temperature range : - 40 °C to + 105 °C
- Package : 8-pin plastic SOP  
8-pin plastic SON  
RoHS compliant

# MB85RC64TA

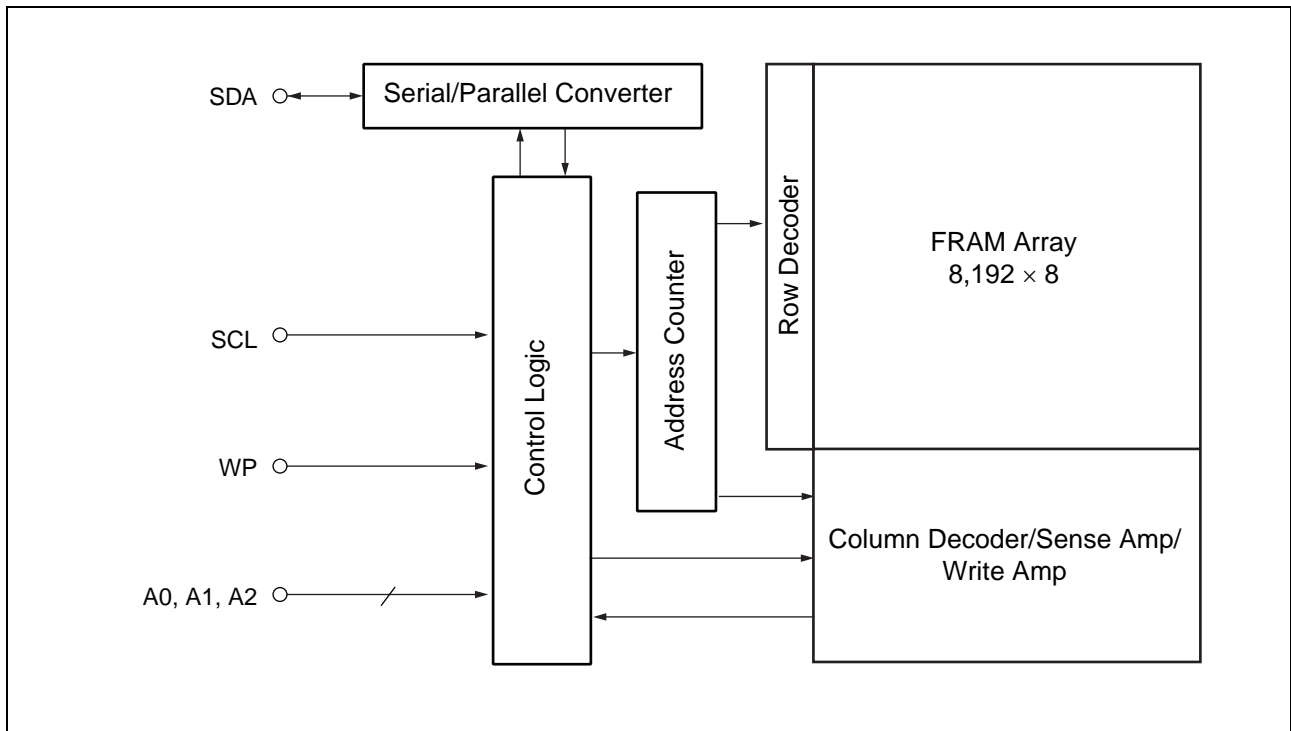
## ■ PIN ASSIGNMENT



## ■ PIN FUNCTIONAL DESCRIPTIONS

| Pin Number | Pin Name | Functional Description  |
|------------|----------|---|
| 1 to 3     | A0 to A2 | Device Address pins<br>The MB85RC64TA can be connected to the same data bus up to 8 devices. Device addresses are used in order to identify each of these devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pins matches a Device Address Code inputted from the SDA pin, the device operates. In the open pin state, A0, A1 and A2 pins are internally pulled-down and recognized as the "L" level. |
| 4          | VSS      | Ground pin  |
| 5          | SDA      | Serial Data I/O pin<br>This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit.   |
| 6          | SCL      | Serial Clock pin<br>This is a clock input pin for input/output serial data. Data is sampled on the rising edge of the clock and output on the falling edge.   |
| 7          | WP       | Write Protect pin<br>When the Write Protect pin is the "H" level, the writing operation is disabled. When the Write Protect pin is the "L" level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin input level. The Write Protect pin is internally pulled down to VSS pin, and that is recognized as the "L" level (write enabled) when the pin is the open state.             |
| 8          | VDD      | Supply Voltage pin  |
| DIE PAD    | —        | It is allowed for the DIE PAD on the bottom of the DFN8 package to be floating (no connection to anything) or to be connected to VSS.   |

## ■ BLOCK DIAGRAM

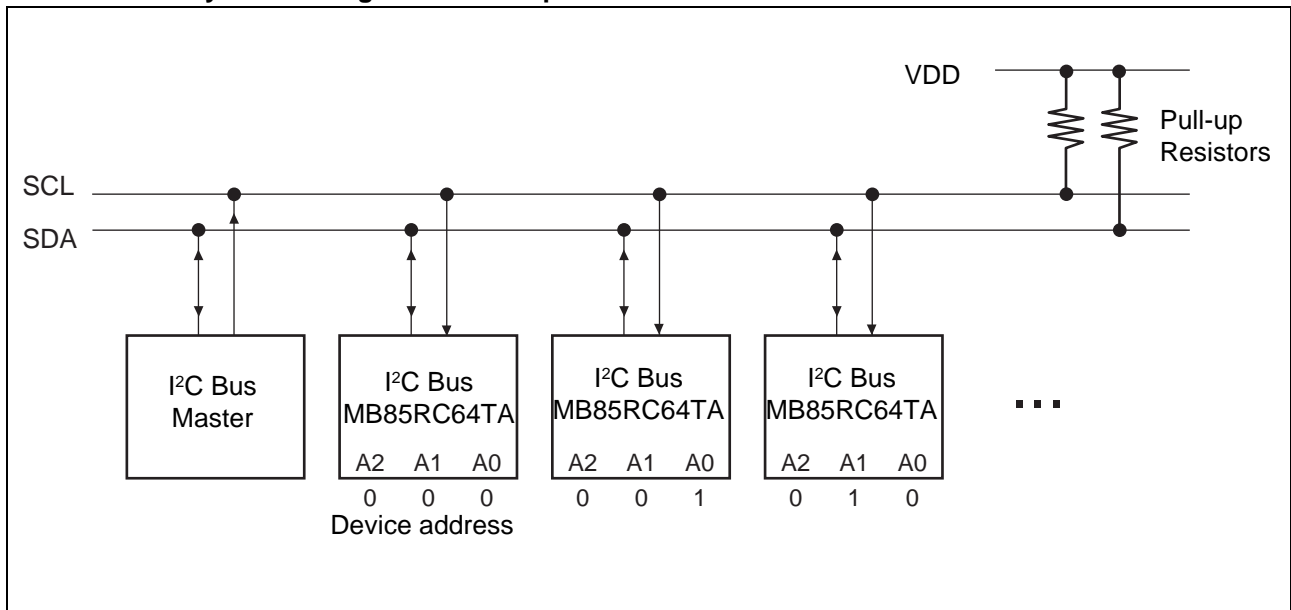


## ■ I<sup>2</sup>C (Inter-Integrated Circuit)

The MB85RC64TA has the two-wire serial interface; the I<sup>2</sup>C bus, and operates as a slave device.

The I<sup>2</sup>C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, an I<sup>2</sup>C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.

### ● I<sup>2</sup>C Interface System Configuration Example



## ■ I<sup>2</sup>C COMMUNICATION PROTOCOL

The I<sup>2</sup>C bus is a two wire serial interface that uses a bidirectional data bus (SDA) and serial clock (SCL). A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The SDA signal should change while the SCL is the "L" level. However, as an exception, when starting and stopping communication sequence, the SDA is allowed to change while the SCL is the "H" level.

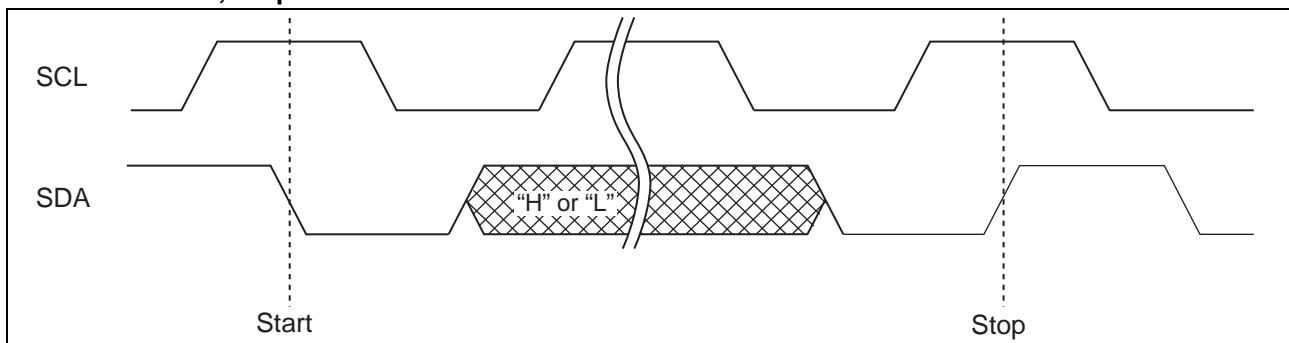
- Start Condition

To start read or write operations by the I<sup>2</sup>C bus, change the SDA input from the "H" level to the "L" level while the SCL input is in the "H" level.

- Stop Condition

To stop the I<sup>2</sup>C bus communication, change the SDA input from the "L" level to the "H" level while the SCL input is in the "H" level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data and enters the standby state.

- Start Condition, Stop Condition



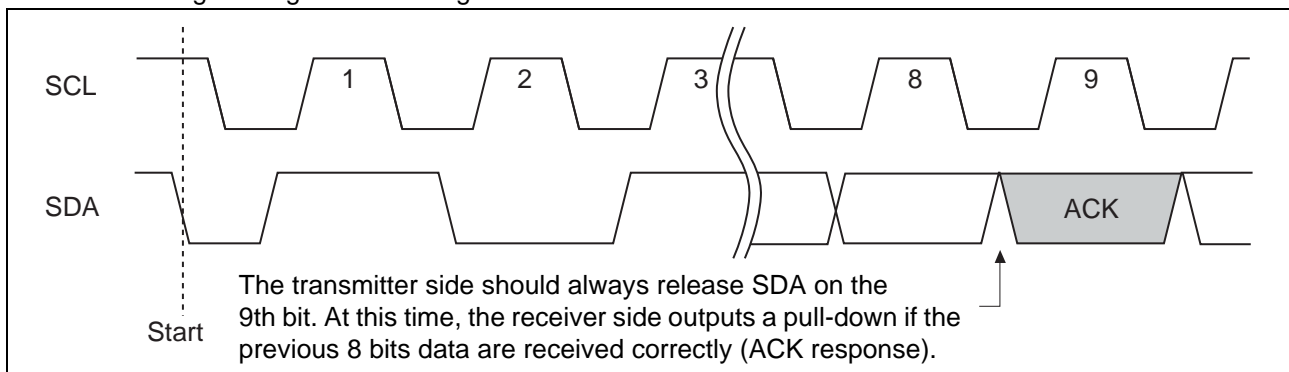
Note : At the write operation, the FRAM device does not need the programming wait time ( $t_{wc}$ ) after issuing the Stop Condition.

## ■ ACKNOWLEDGE (ACK)

In the I<sup>2</sup>C bus, serial data including address or memory information is sent in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the "L" level every time on the 9th SCL clock after each 8 bits are successfully transmitted and received. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z-released period, the receiver side pulls the SDA line down to indicate the "L" level that the previous 8 bits communication is successfully received.

In case the slave side receives Stop condition before sending or receiving the ACK "L" level, the slave side stops the operation and enters to the standby state. On the other hand, the slave side releases the bus state after sending or receiving the NACK "H" level. The master side generates Stop condition or Start condition in this released bus state.

- Acknowledge timing overview diagram



## ■ DEVICE ADDRESS WORD (Slave address)

Following the start condition, the master sends the 8 bits device address word to start I<sup>2</sup>C communication. The device address word (8 bits) consists of a device Type code (4 bits), device address code (3 bits), and a read/write code (1 bit).

- Device Type Code (4 bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at "1010" for the MB85RC64TA.

- Device Address Code (3 bits)

Following the device type code, the 3 bits of the device address code are input in order of A2, A1 and A0. The device address code identifies one device from up to eight devices connected to the bus.

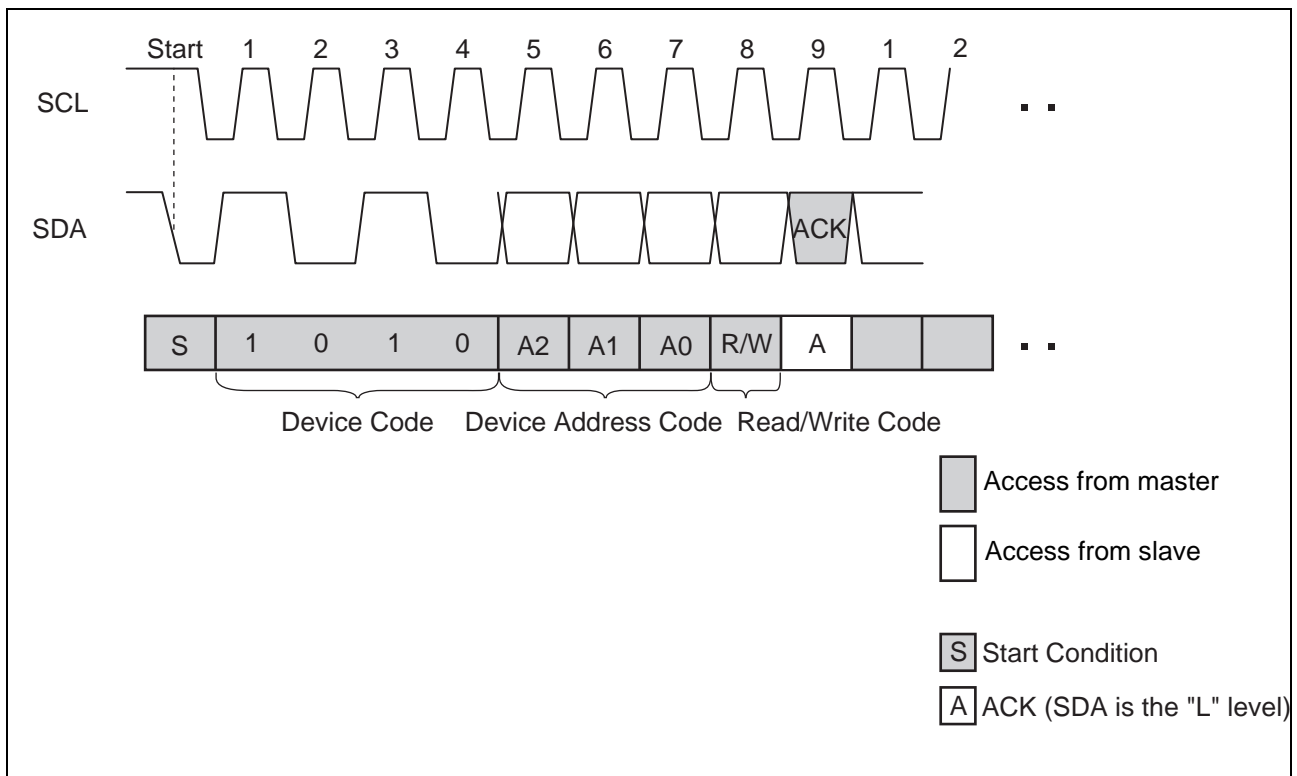
Each MB85RC64TA is given a unique 3 bits code on the device address pin (external hardware pin A2, A1 and A0). The slave only responds if the received device address code is equal to this unique 3 bits code.

- Read/Write Code (1 bit)

The 8th bit of the device address word is the R/W (read/write) code. When the R/W code is "0", a write operation is enabled, and the R/W code is "1", a read operation is enabled for the MB85RC64TA.

It turns to a stand-by state if the device code is not "1010" or device address code does not equal to pins A2, A1 and A0.

### • Device Address Word



## ■ DATA STRUCTURE

In the I<sup>2</sup>C bus, the acknowledge “L” level is output on the 9th bit by a slave, after the 8 bits of the device address word following the start condition are input by a master. After confirming the acknowledge response by the master, the master outputs 8 bits × 2 memory address to the slave. When the each memory address input ends, the slave again outputs the acknowledge “L” level. After this operation, the I/O data follows in units of 8 bits, with the acknowledge “L” level output after every 8 bits.

It is determined by the R/W code whether the data line is driven by the master or the slave. However, the clock line shall be driven by the master. For a write operation, the slave will accept 8 bits from the master, then send an acknowledge. If the master detects the acknowledge, the master will transfer the next 8 bits. For a read operation, the slave will place 8 bits on the data line, then wait for an acknowledge from the master.

## ■ FRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC64TA performs write operations at the same speed as read operations, so any waiting time for an ACK polling\* does not occur. The write cycle takes no additional time.

\*: In E<sup>2</sup>PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

## ■ WRITE PROTECT (WP)

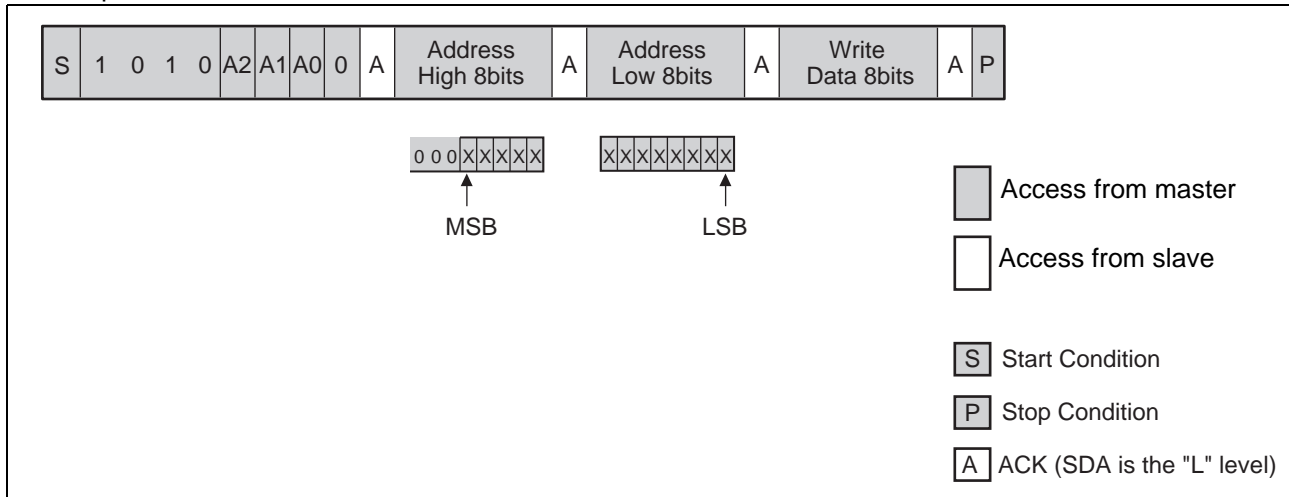
The entire memory array can be write protected using the Write Protect pin. When the Write Protect pin is set to the “H” level, the entire memory array will be write protected. When the Write Protect pin is the “L” level, entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

Note : The Write Protect pin is pulled down internally to VSS pin, therefore if the Write Protect pin is open, the pin status is detected as the “L” level (write enabled).

## ■ COMMAND

### • Byte Write

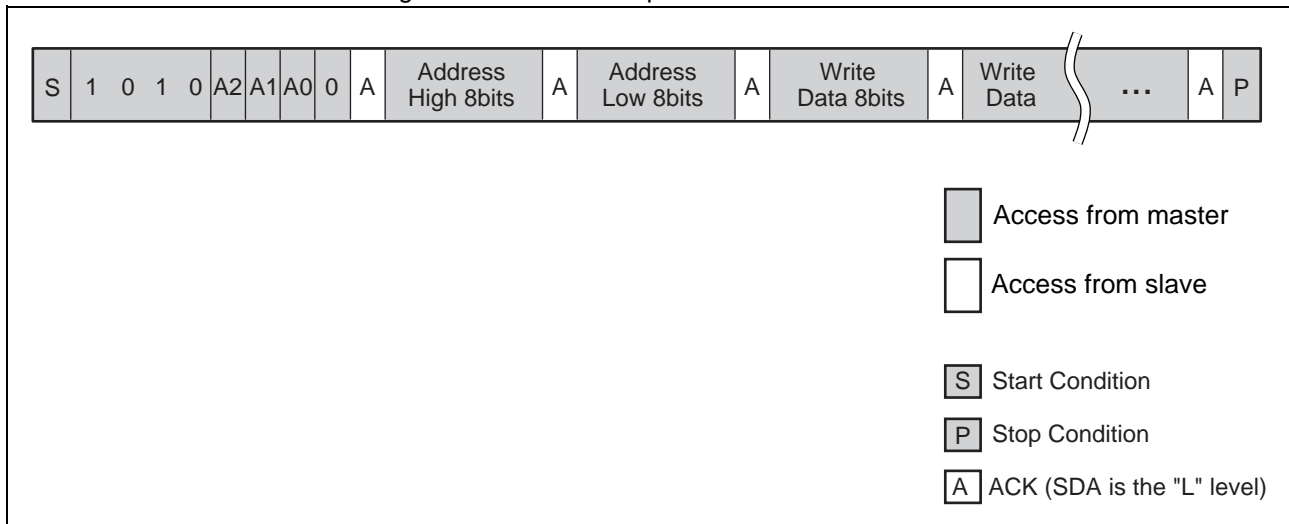
If the device address word (R/W "0" input) is sent following the start condition, the slave responds with an ACK. After this ACK, write addresses and data are sent in the same way, and the write ends by generating a stop condition at the end.



Note : In the MB85RC64TA, input "000" as the upper 3 bits of the MSB.

### • Page Write

If additional 8 bits are continuously sent after the same command (except stop condition) as Byte Write, a page write is performed. The memory address rolls over to first memory address (0000<sub>H</sub>) at the end of the address. Therefore, if more than 8 Kbytes are sent, the data is overwritten in order starting from the start of the memory address that was written first. Because FRAM performs the high-speed write operations, the data will be written to FRAM right after the ACK response finished.

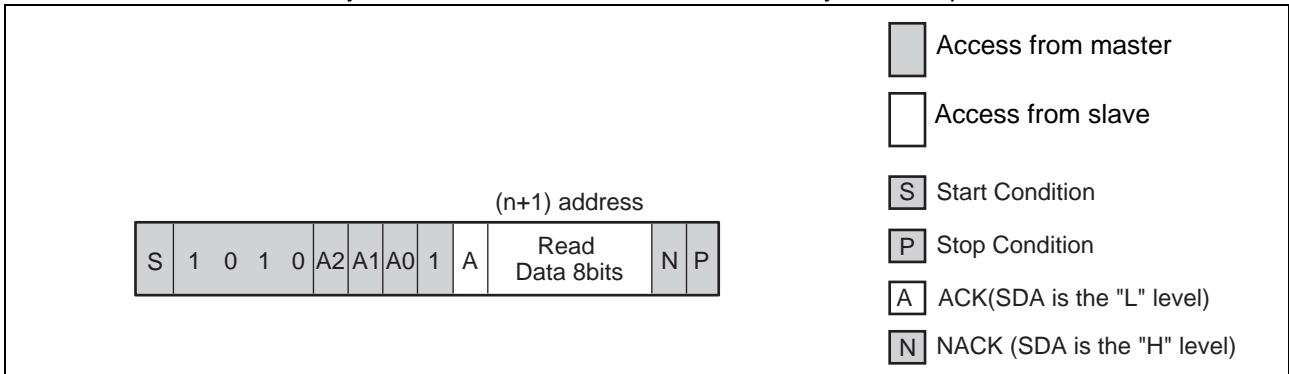


Note : It is not necessary to take a period for internal write operation cycles from the buffer to the memory after the stop condition is generated.

# MB85RC64TA

- Current Address Read

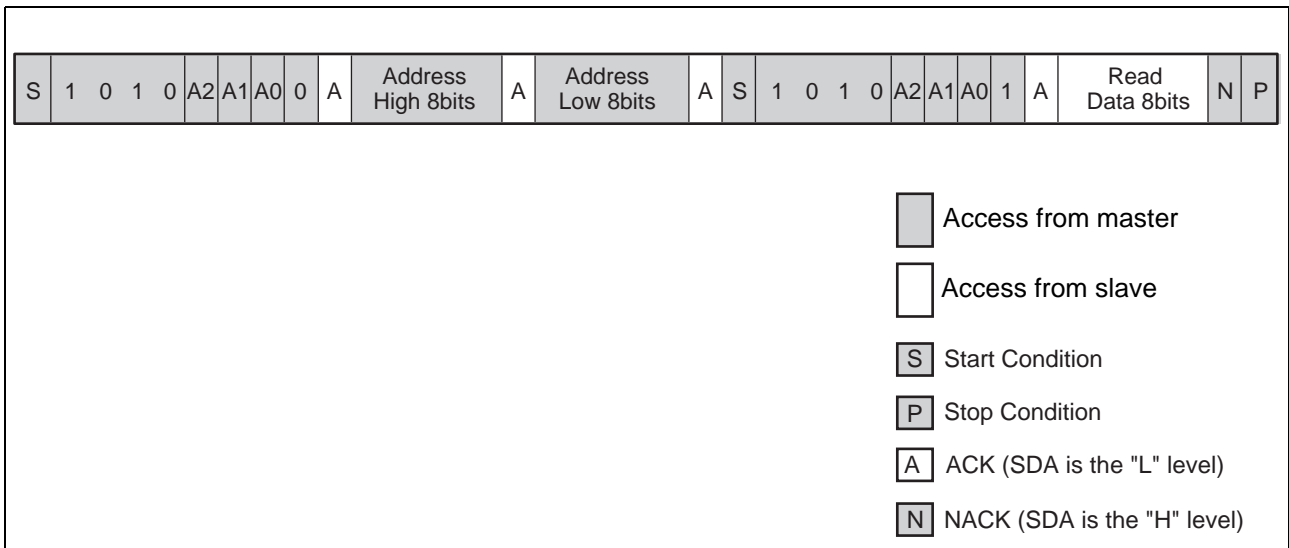
When the previous write or read operation finishes successfully up to the stop condition and assumes the last accessed address is “n”, then the address at “n+1” is read by sending the following command unless turning the power off. If the memory address is last address, the address counter will roll over to 0000<sub>H</sub>. The current address in memory address buffer is undefined immediately after the power is turned on.



- Random Read

The one byte of data from the memory address saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W “1” input).

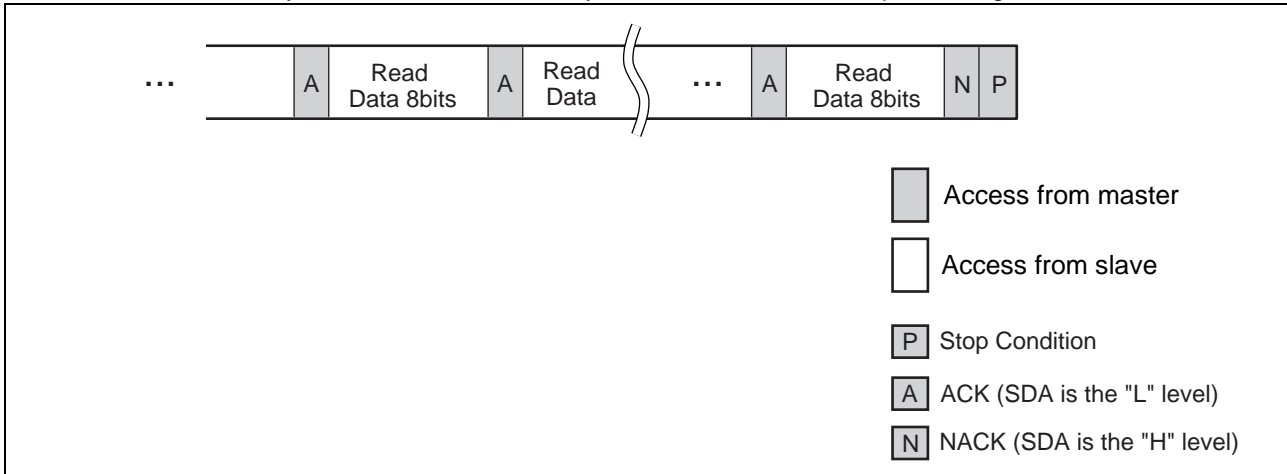
The final NACK is issued by the receiver that receives the data. In this case, this bit is issued by the master side.





- Sequential Read

Data can be received continuously following the Device address word (R/W "1" input) after specifying the address in the same way as for Random Read. If the read reaches the end of address, the internal read address automatically rolls over to first memory address 0000<sub>H</sub> and keeps reading.



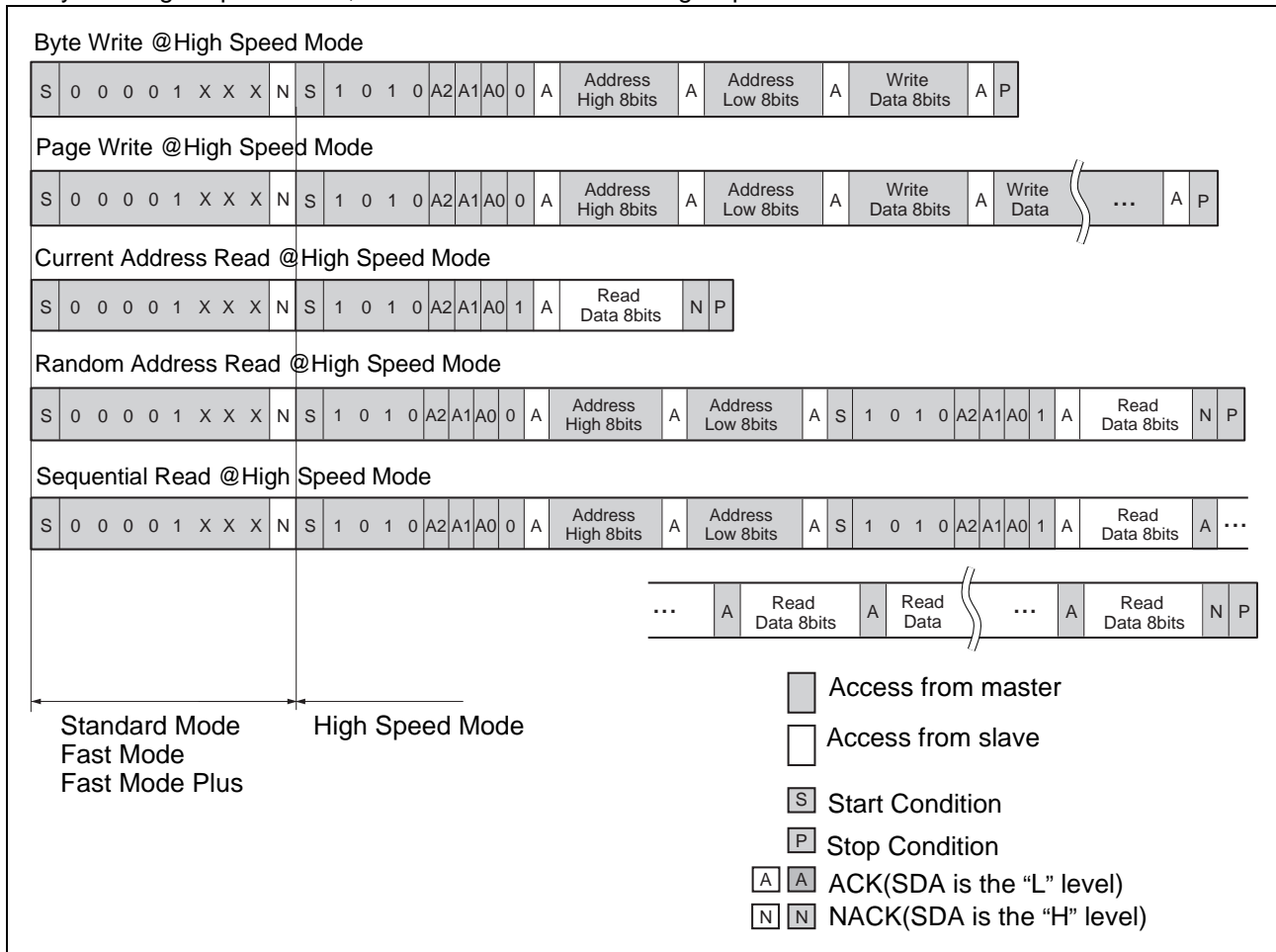
# MB85RC64TA

- High Speed Mode

MB85RC64TA supports High Speed mode up to 3.4 MHz. By sending an entry command (0000 1XXX) after start condition from the master side, it informs to the slave that the data transmission with High Speed mode will start.

Since there is no slave side which is allowed to respond to this entry command, NACK response continues from the slave side. After the master side recognizes this NACK response, the master side changes its state to High Speed mode and enables the bidirectional communication up to 3.4 MHz.

By sending Stop condition, it exits out of the state in High Speed communication.

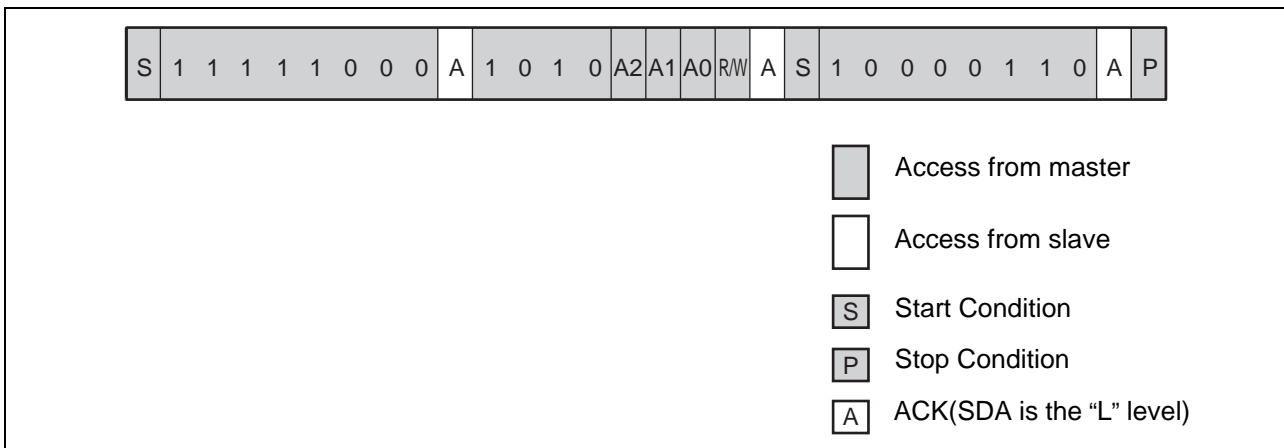


- Sleep Mode

MB85RC64TA provides Sleep mode which reduces less current consumption than Standby mode, by stooping the internal regulator circuits. Following sequences enable the Sleep mode transition.

<Transition to Sleep mode>

- The master sends start condition followed by F8<sub>H</sub>.
- After ACK response from slave, the master sends the device address word.  
In this device address word, Read/Write code are Don't care.
- After ACK response from slave, the master re-sends the start condition followed by 86<sub>H</sub>.
- The slave moves to Sleep mode after ACK response to the master.

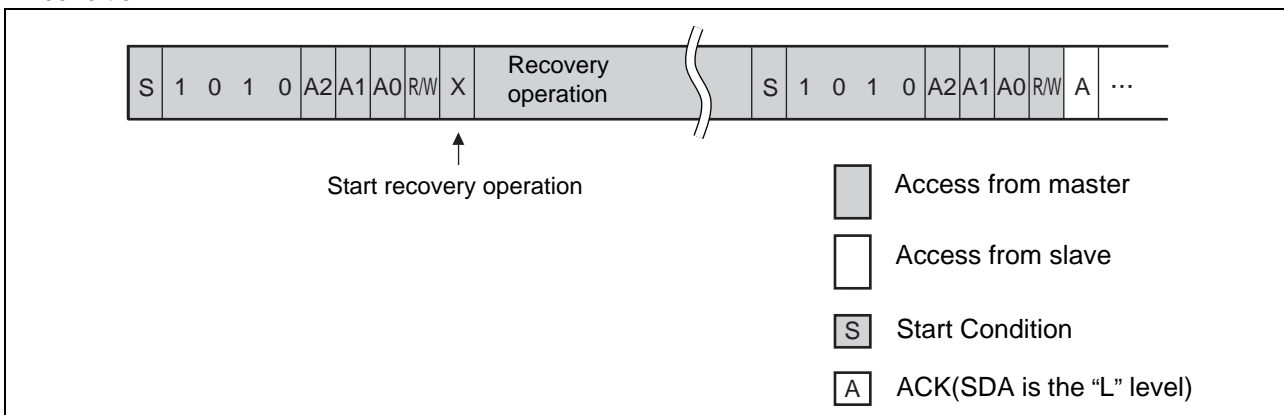


Even if the MB85RC64TA stays in the Sleep mode, SDA and SCL signals are monitored. Following sequences enable the transition to Standby mode after recovery time ( $t_{REC}$ ) of internal regulator circuits.

<Exit from Sleep mode>

- The master sends start condition followed by device address word.  
In this device address word, Read/Write code are Don't care.
- At the rising edge of 9th clock from start condition, an internal regulator starts to operate its recovery sequence.
- After the recovery time ( $t_{REC}$ ) passed, standby mode enabled.

After returning to Standby mode, reading and writing are enabled by sending each command starts with start condition.



# MB85RC64TA

- Device ID

The Device ID command reads fixed Device ID. The size of Device ID is 3 bytes and consists of manufacturer ID and product ID. The Device ID is read-only and can be read out by following sequences.

- The master sends the Reserved Slave ID F8<sub>H</sub> after the START condition.
- The master sends the device address word after the ACK response from the slave.  
In this device address word, R/W code are "Don't care".
- The master re-sends the START condition followed by the Reserved Slave ID F9<sub>H</sub> after the ACK response from the slave.
- The master read out the Device ID succeedingly in order of Data Byte 1st / 2nd / 3rd after the ACK response from the slave.
- The master responds the NACK (SDA is the "H" level) after reading 3 bytes of the Device ID.  
In case the master respond the ACK after reading 3 bytes of the Device ID, the master re-reading the Device ID from the 1st byte.



- Access from master
- Access from slave
- S Start Condition
- P Stop Condition
- A ACK (SDA is the "L" level)
- N NACK (SDA is the "H" level)

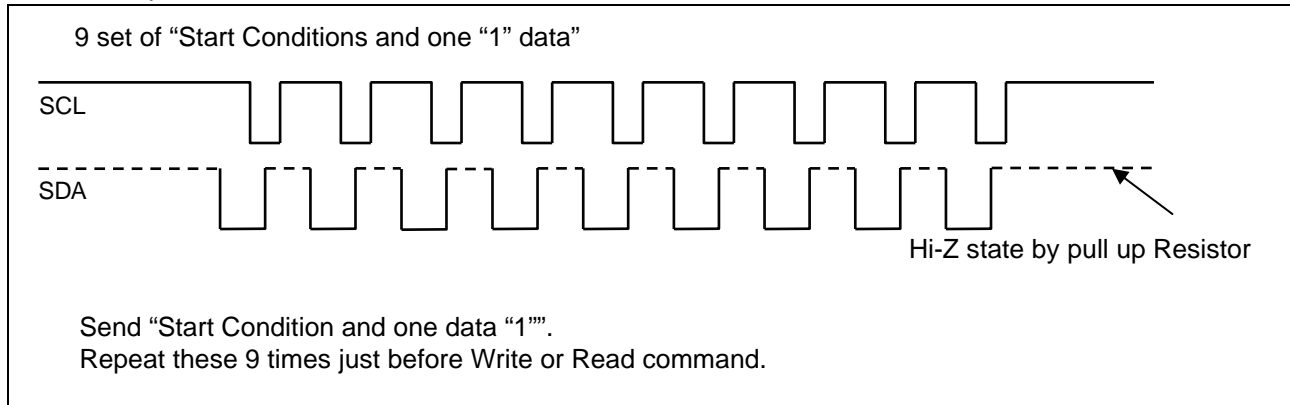
| Data Byte 1st                     |    |   |   |   |   |   |   |   |   | Data Byte 2nd                 |   |    |    |   |   | Data Byte 3rd   |   |   |   |   |   |   |   |
|-----------------------------------|----|---|---|---|---|---|---|---|---|-------------------------------|---|----|----|---|---|-----------------|---|---|---|---|---|---|---|
| Manufacture ID = 00A <sub>H</sub> |    |   |   |   |   |   |   |   |   | Product ID = 358 <sub>H</sub> |   |    |    |   |   |                 |   |   |   |   |   |   |   |
| 11                                | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1                             | 0 | 11 | 10 | 9 | 8 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Fujitsu Semiconductor             |    |   |   |   |   |   |   |   |   | Density = 3 <sub>H</sub>      |   |    |    |   |   | Proprietary use |   |   |   |   |   |   |   |
| 0                                 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0                             | 1 | 0  | 1  | 1 | 0 | 1               | 0 | 1 | 1 | 0 | 0 | 0 |   |

## ■ SOFTWARE RESET SEQUENCE OR COMMAND RETRY

In case the malfunction has occurred after power on, the master side stopped the I<sup>2</sup>C communication during processing, or unexpected malfunction has occurred, execute the following (1) software recovery sequence just before each command, or (2) retry command just after failure of each command.

### (1) Software Reset Sequence

Since the slave side may be outputting "L" level, do not force to drive "H" level, when the master side drives the SDA port. This is for preventing a bus conflict. The additional hardware is not necessary for this software reset sequence.



### (2) Command Retry

Command retry is useful to recover from failure response during I<sup>2</sup>C communication.

# MB85RC64TA

## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter                     | Symbol    | Rating |                           | Unit |
|-------------------------------|-----------|--------|---------------------------|------|
|                               |           | Min    | Max                       |      |
| Power supply voltage*         | $V_{DD}$  | - 0.5  | + 4.0                     | V    |
| Input voltage*                | $V_{IN}$  | - 0.5  | $V_{DD} + 0.5 (\leq 4.0)$ | V    |
| Output voltage*               | $V_{OUT}$ | - 0.5  | $V_{DD} + 0.5 (\leq 4.0)$ | V    |
| Operation ambient temperature | $T_A$     | - 40   | + 105                     | °C   |
| Storage temperature           | $T_{stg}$ | - 55   | + 125                     | °C   |

\*: These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter                                   | Symbol   | Value |     |       | Unit |
|---|----------|-------|-----|-------|------|
|   |          | Min   | Typ | Max   |      |
| Power supply voltage <sup>*1</sup>          | $V_{DD}$ | 1.8   | 3.3 | 3.6   | V    |
| Operation ambient temperature <sup>*2</sup> | $T_A$    | - 40  | —   | + 105 | °C   |

\*1: These parameters are based on the condition that VSS is 0 V.

\*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

| Parameter                                      | Symbol          | Condition  | Value                 |     |                       | Unit |
|--|-----------------|--|-----------------------|-----|-----------------------|------|
|  |                 |  | Min                   | Typ | Max                   |      |
| Input leakage current*1                        | I <sub>LI</sub> | V <sub>IN</sub> = 0 V to V <sub>DD</sub>   | —                     | —   | 1                     | μA   |
| Output leakage current*2                       | I <sub>LO</sub> | V <sub>OUT</sub> = 0 V to V <sub>DD</sub>  | —                     | —   | 1                     | μA   |
| Operating power supply current                 | I <sub>DD</sub> | SCL = 0.1 MHz  | —                     | 35  | —                     | μA   |
|  |                 | SCL = 1 MHz  | —                     | 80  | 100                   | μA   |
|  |                 | SCL = 3.4 MHz  | —                     | 170 | 190                   | μA   |
| Standby current                                | I <sub>SB</sub> | SCL, SDA = V <sub>DD</sub><br>A0, A1, A2, WP = 0 V or<br>V <sub>DD</sub> or Open<br>Under Stop Condition | —                     | 8   | 10                    | μA   |
| Sleep current                                  | I <sub>ZZ</sub> | SCL, SDA = V <sub>DD</sub><br>A0, A1, A2, WP = 0 V   | —                     | 4   | 6                     | μA   |
| “H” level input voltage                        | V <sub>IH</sub> | V <sub>DD</sub> = 1.8 V to 3.6 V   | V <sub>DD</sub> × 0.7 | —   | V <sub>DD</sub>       | V    |
| “L” level input voltage                        | V <sub>IL</sub> | V <sub>DD</sub> = 1.8 V to 3.6 V   | V <sub>SS</sub>       | —   | V <sub>DD</sub> × 0.3 | V    |
| “L” level output voltage                       | V <sub>OL</sub> | I <sub>OL</sub> = 3 mA   | —                     | —   | 0.4                   | V    |
| Input resistance for<br>WP, A0, A1 and A2 pins | R <sub>IN</sub> | V <sub>IN</sub> = V <sub>IL</sub> (Max)  | 50                    | —   | —                     | kΩ   |
|  |                 | V <sub>IN</sub> = V <sub>IH</sub> (Min)  | 1                     | —   | —                     | MΩ   |

\*1: Applicable pin: SCL,SDA

\*2: Applicable pin: SDA

# MB85RC64TA

## 2. AC Characteristics

| Parameter                            | Symbol              | Value         |      |           |     |                |       |                 |      | Unit |
|--------------------------------------|---------------------|---------------|------|-----------|-----|----------------|-------|-----------------|------|------|
|                                      |                     | STANDARD MODE |      | FAST MODE |     | FAST MODE PLUS |       | HIGH SPEED MODE |      |      |
|                                      |                     | Min           | Max  | Min       | Max | Min            | Max   | Min             | Max  |      |
| SCL clock frequency                  | FSCL                | 0             | 100  | 0         | 400 | 0              | 1000  | 0               | 3400 | kHz  |
| Clock high time                      | T <sub>HIGH</sub>   | 4000          | —    | 600       | —   | 260*1          | —     | 60              | —    | ns   |
| Clock low time                       | T <sub>LOW</sub>    | 4700          | —    | 1300      | —   | 500*2          | —     | 160             | —    | ns   |
| SCL/SDA rising time                  | T <sub>r</sub>      | —             | 1000 | —         | 300 | —              | 300   | —               | 80   | ns   |
| SCL/SDA falling time                 | T <sub>f</sub>      | —             | 300  | —         | 300 | —              | 120   | —               | 80   | ns   |
| Start condition hold                 | T <sub>HD:STA</sub> | 4000          | —    | 600       | —   | 250            | —     | 160             | —    | ns   |
| Start condition setup                | T <sub>SU:STA</sub> | 4700          | —    | 600       | —   | 250            | —     | 160             | —    | ns   |
| SDA input hold                       | T <sub>HD:DAT</sub> | 0             | —    | 0         | —   | 0              | —     | 0               | —    | ns   |
| SDA input setup                      | T <sub>SU:DAT</sub> | 250           | —    | 100       | —   | 50             | —     | 15*4            | —    | ns   |
| SDA output hold                      | T <sub>DH:DAT</sub> | 0             | —    | 0         | —   | 0              | —     | 0               | —    | ns   |
| Stop condition setup                 | T <sub>SU:STO</sub> | 4000          | —    | 600       | —   | 250            | —     | 160             | —    | ns   |
| SDA output access after SCL falling  | T <sub>AA</sub>     | —             | 3000 | —         | 900 | —              | 450*3 | —               | 130  | ns   |
| Pre-charge time                      | T <sub>BUF</sub>    | 4700          | —    | 1300      | —   | 500            | —     | 300             | —    | ns   |
| Noise suppression time (SCL and SDA) | T <sub>SP</sub>     | —             | 50   | —         | 50  | —              | 50    | —               | 5    | ns   |

\*1: 300 ns @VDD ≤ 2.7 V

\*2: 600 ns @VDD ≤ 2.7 V

\*3: 550 ns @VDD ≤ 2.7 V

\*4: 20 ns @VDD ≤ 2.7 V

AC characteristics were measured under the following measurement conditions.

Power supply voltage : 1.8 V to 3.6 V

Operation ambient temperature : - 40 °C to + 105 °C

Input voltage magnitude : V<sub>SS</sub> to V<sub>DD</sub>

Input rising time : 5 ns

Input falling time : 5 ns

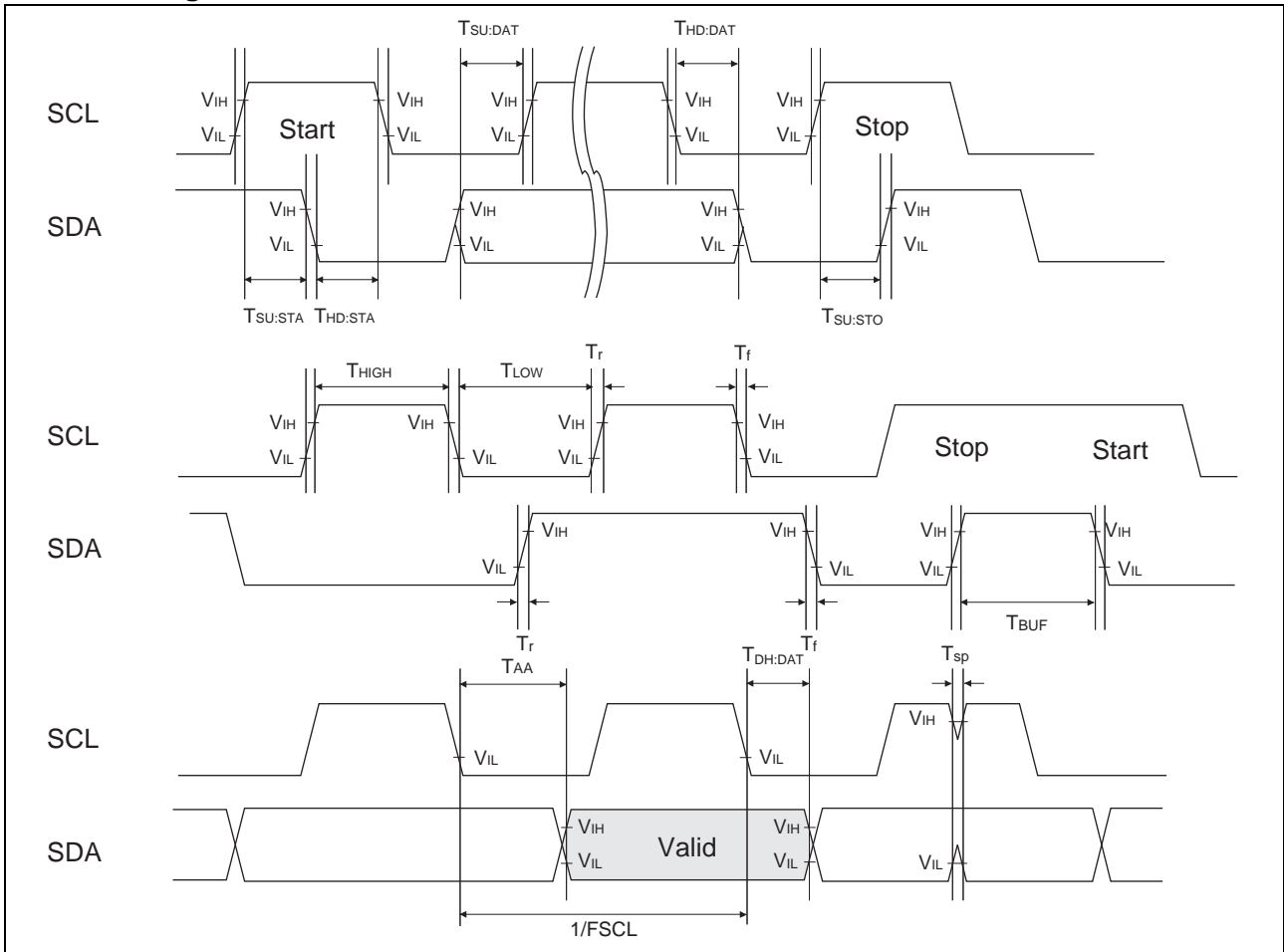
Input judge level : V<sub>DD</sub>/2

Output judge level : V<sub>DD</sub>/2

Output load capacitance : 100 pF



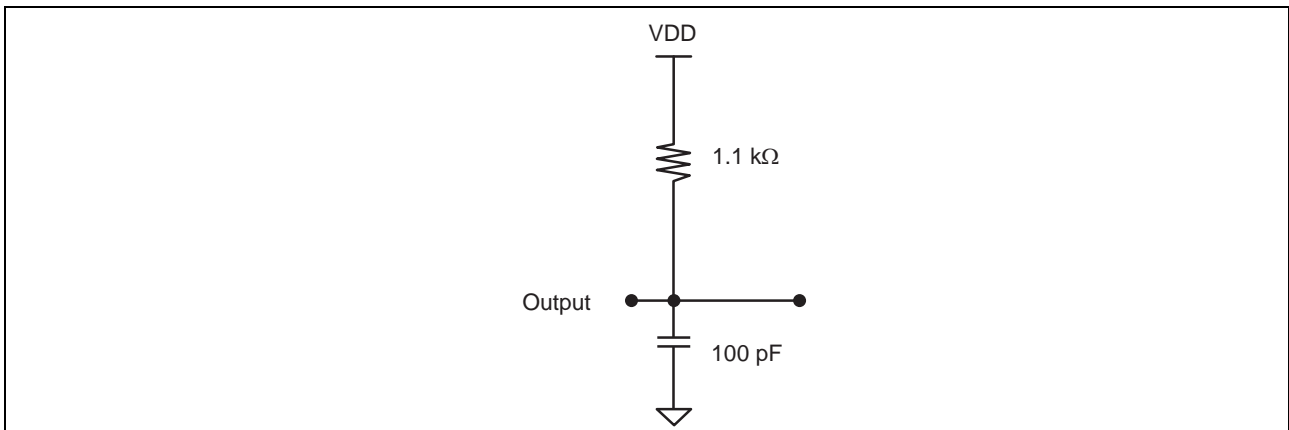
### 3. AC Timing Definitions



### 4. Pin Capacitance

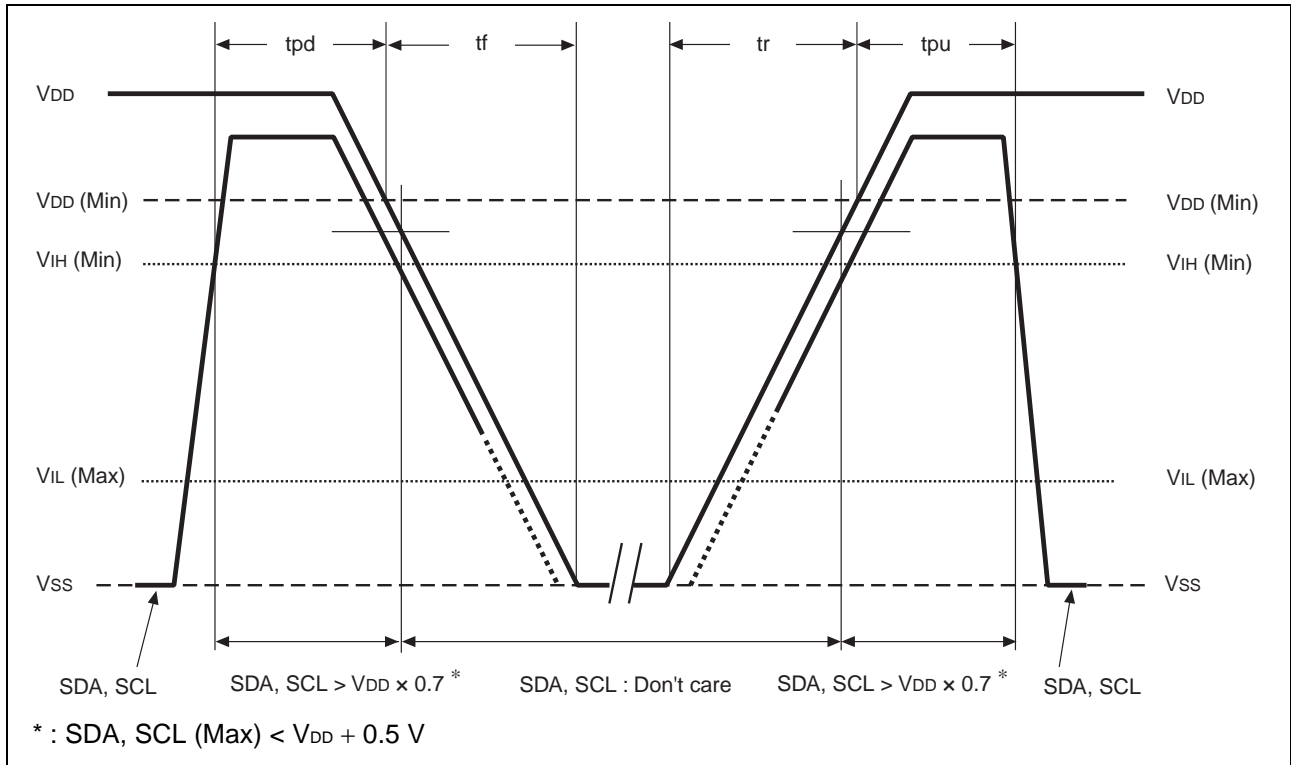
| Parameter         | Symbol    | Conditions   | Value |     |     | Unit |
|-------------------|-----------|--|-------|-----|-----|------|
|                   |           |  | Min   | Typ | Max |      |
| I/O capacitance   | $C_{I/O}$ | $V_{DD} = 3.3 \text{ V}$ ,<br>$f = 1 \text{ MHz}$ , $T_A = +25 \text{ }^\circ\text{C}$ | —     | —   | 8   | pF   |
| Input capacitance | $C_{IN}$  |  | —     | —   | 8   | pF   |

### 5. AC Test Load Circuit



# MB85RC64TA

## POWER ON/OFF SEQUENCE



| Parameter                                  | Symbol           | Value |     | Unit |
|--|------------------|-------|-----|------|
|  |                  | Min   | Max |      |
| SDA, SCL level hold time during power down | tpd              | 85    | —   | ns   |
| SDA, SCL level hold time during power up   | tpu              | 250   | —   | μs   |
| Power supply rising time                   | tr               | 0.05  | —   | ms/V |
| Power supply falling time                  | tf               | 0.1   | —   | ms/V |
| Internal regulator recovery time           | t <sub>REC</sub> | —     | 400 | μs   |

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

## FRAM CHARACTERISTICS

| Item                               | Min              | Max | Unit       | Parameter   |
|------------------------------------|------------------|-----|------------|---|
| Read/Write Endurance* <sup>1</sup> | 10 <sup>13</sup> | —   | Times/byte | Operation Ambient Temperature T <sub>A</sub> = + 105 °C |
| Data Retention* <sup>2</sup>       | 19.1             | —   | Years      | Operation Ambient Temperature T <sub>A</sub> = + 105 °C |
|                                    | 70.4             | —   |            | Operation Ambient Temperature T <sub>A</sub> = + 85 °C  |

\*1 : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

\*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

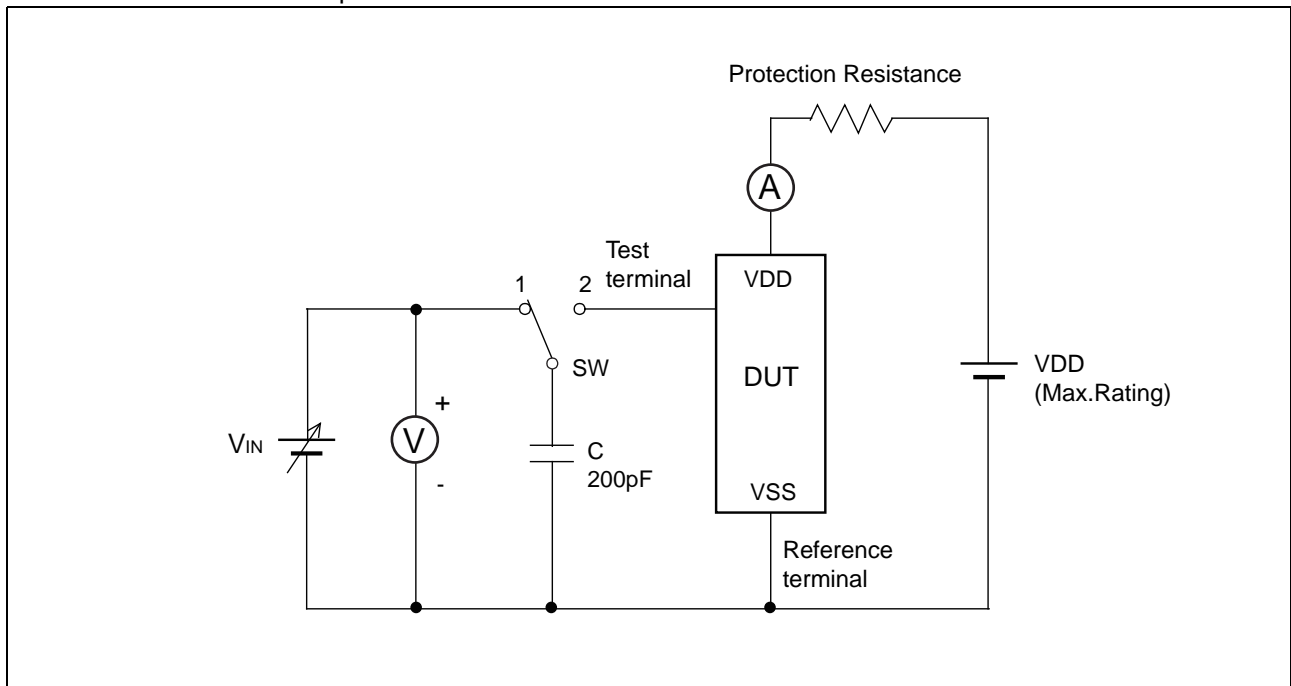
## ■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.
- During the access period from the start condition to the stop condition, keep the level of WP, A0, A1 and A2 pins to the “H” level or the “L” level.

## ■ ESD AND LATCH-UP

| Test  | DUT                  | Value                   |
|---|----------------------|-------------------------|
| ESD HBM (Human Body Model)<br>JESD22-A114 compliant     | MB85RC64TAPNF-G-BDE1 | $\geq  2000 \text{ V} $ |
| ESD CDM (Charged Device Model)<br>JESD22-C101 compliant |                      | $\geq  1000 \text{ V} $ |
| Latch-Up (C-V Method)<br>Proprietary method             |                      | $\geq  200 \text{ V} $  |

- C-V method of Latch-Up Resistance Test



Note Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.  
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020D)

## ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

# MB85RC64TA

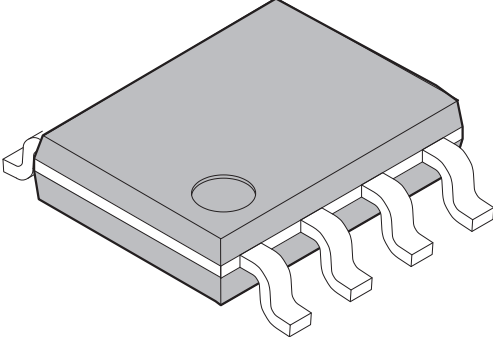
## ■ ORDERING INFORMATION

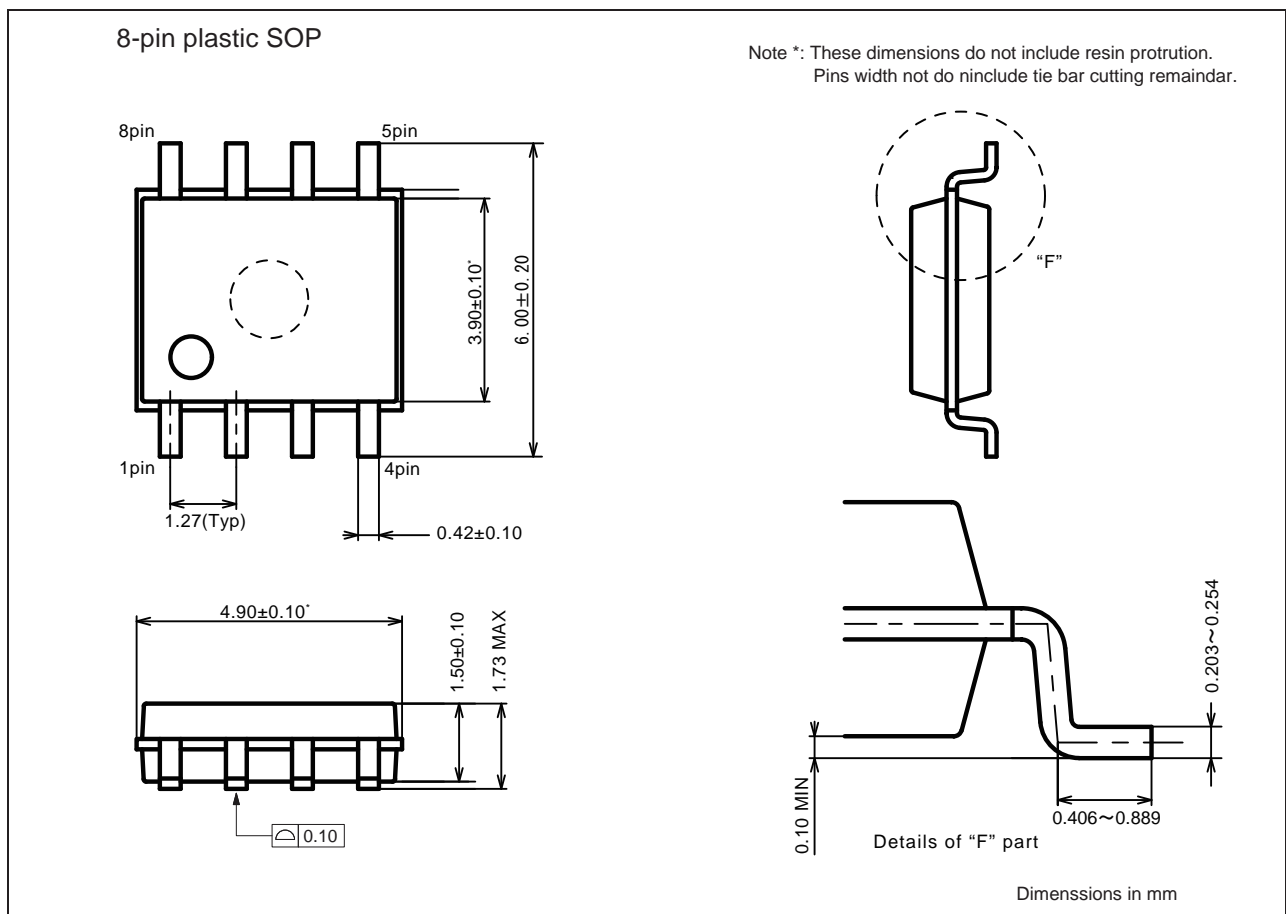
| Part number            | Package            | Shipping form         | Minimum shipping quantity |
|------------------------|--------------------|-----------------------|---------------------------|
| MB85RC64TAPNF-G-BDE1   | 8-pin, plastic SOP | Tube                  | —*                        |
| MB85RC64TAPNF-G-BDERE1 | 8-pin, plastic SOP | Embossed Carrier tape | 1500                      |
| MB85RC64TAPN-G-AMEWE1  | 8-pin, plastic SON | Embossed Carrier tape | 1500                      |

\*: Please contact our sales office about minimum shipping quantity.

## ■ PACKAGE DIMENSION

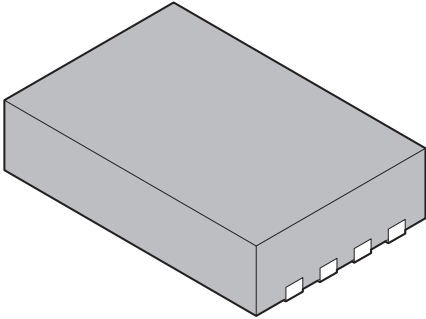
(1) MB85RC64TAPNF-G-BDE1/MB85RC64TAPNF-G-BDERE1

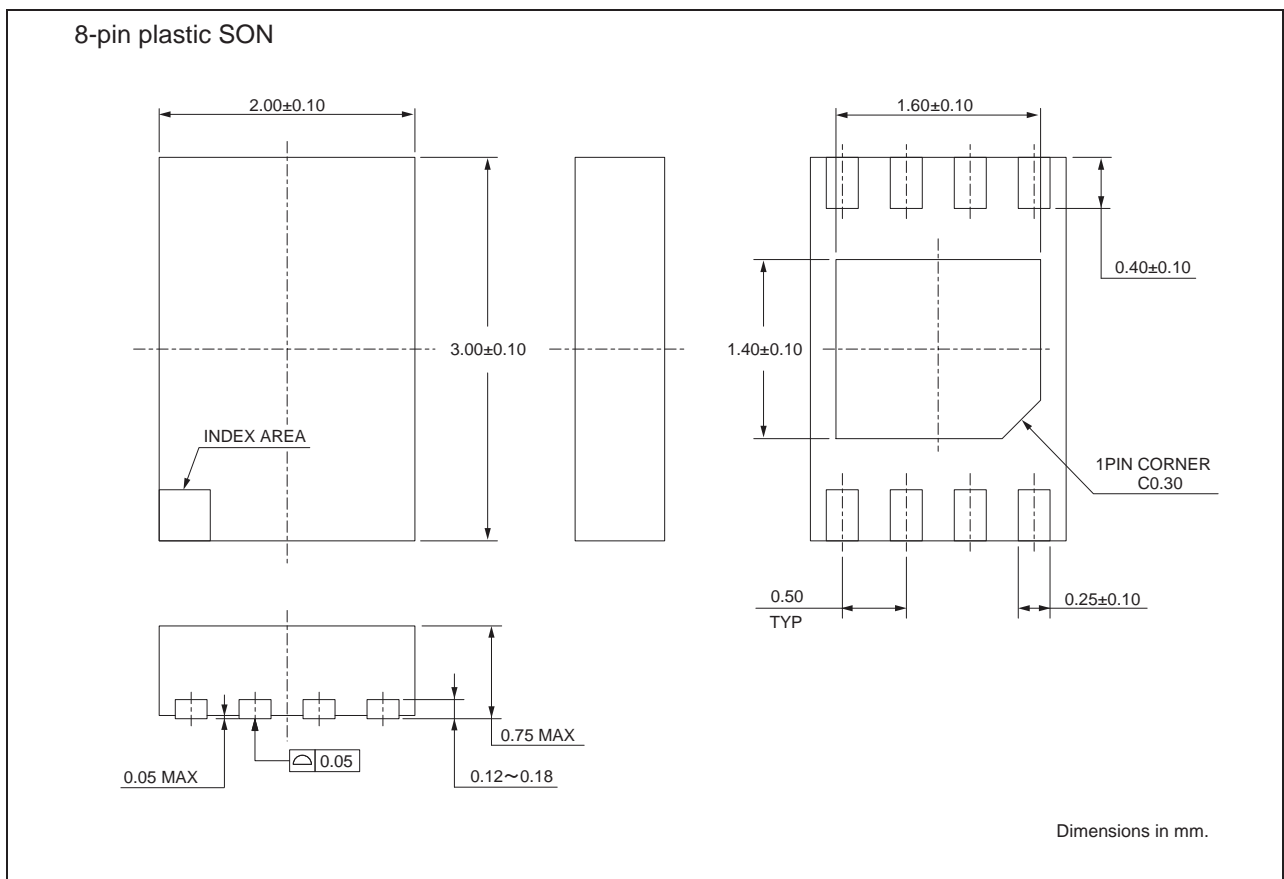
|   |                                |                  |  |
|---|--------------------------------|------------------|--|
| <p>8-pin plastic SOP</p>  <p>MB85RC64TAPNF-G-BDE1<br/>MB85RC64TAPNF-G-BDERE1</p> | Lead pitch                     | 1.27 mm          |  |
|   | Package width × package length | 3.9 mm × 4.89 mm |  |
|   | Lead shape                     | Gullwing         |  |
|   | Sealing method                 | Plastic mold     |  |
|   | Mounting height                | 1.73 mm MAX      |  |
|   |                                |                  |  |
|   |                                |                  |  |



# MB85RC64TA

## (2)MB85RC64TAPN-G-AMEWE1

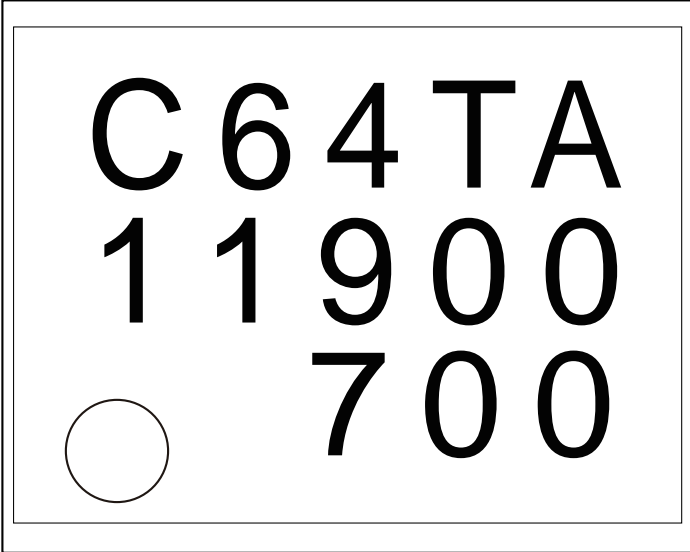
|   |                                |                 |
|---|--------------------------------|-----------------|
| <p>8-pin plastic SON</p>  <p>MB85RC64TAPN-G-AMEWE1</p> | Lead pitch                     | 0.5 mm          |
|   | Package width × package length | 2.0 mm × 3.0 mm |
|   | Sealing method                 | Plastic mold    |
|   | Mounting height                | 0.75 mm MAX     |
|   |                                |                 |



## ■ MARKING(Example)

(1)MB85RC64TAPNF-G-BDE1/MB85RC64TAPNF-G-BDERE1

[MB85RC64TAPNF-G-BDE1]  
[MB85RC64TAPNF-G-BDERE1]



C 6 4 T A

1 1 9 0 0

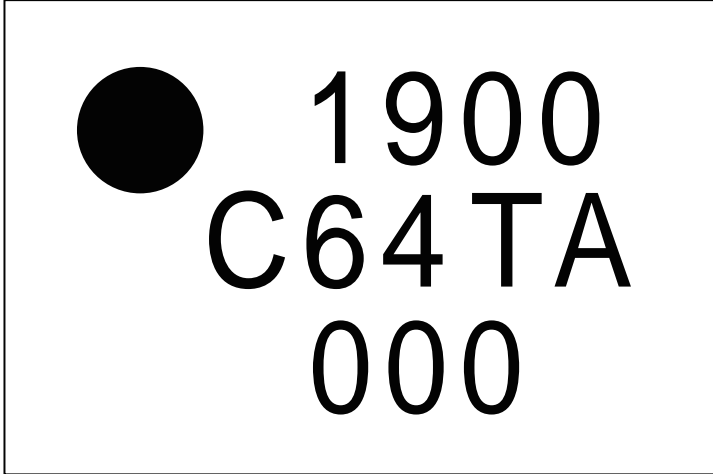
7 0 0

[8-pin plastic SOP]

C64TA : Product name  
11900 : 1 (CS code) + 1900(Year and Week code)  
700 : Trace code

(2)MB85RC64TAPN-G-AMEWE1

[MB85RC64TAPN-G-AMEWE1]



1 9 0 0

C 6 4 T A

0 0 0

[8-pin plastic SON ]

C64TA : Product name  
1900 : Year and Week code  
000 : Trace code

# MB85RC64TA

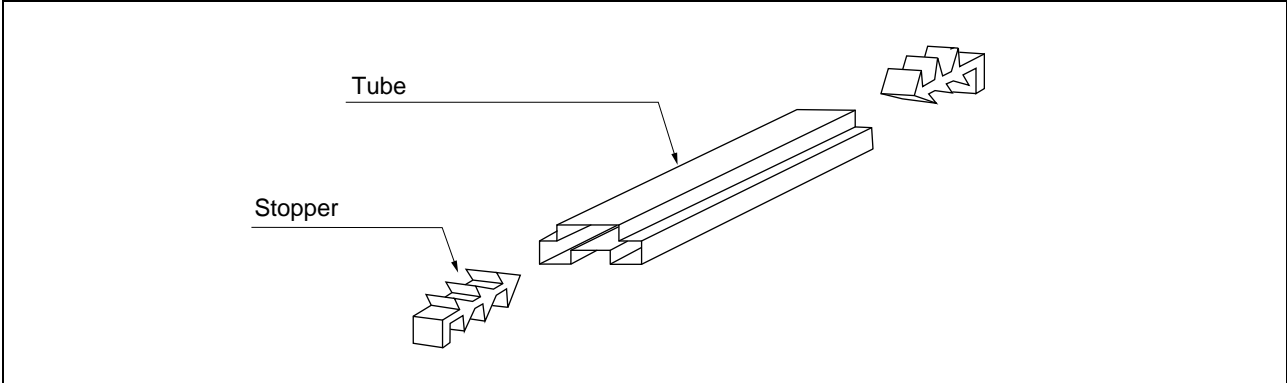
## ■ PACKING INFORMATION

(1)MB85RC64TA-G-BDE1/MB85RC64TA-G-BDERE1

### 1. Tube(MB85RC64TA-G-BDE1)

#### 1.1 Tube Dimensions

- Tube/stopper shape (example)



#### Tube cross-sections and Maximum quantity

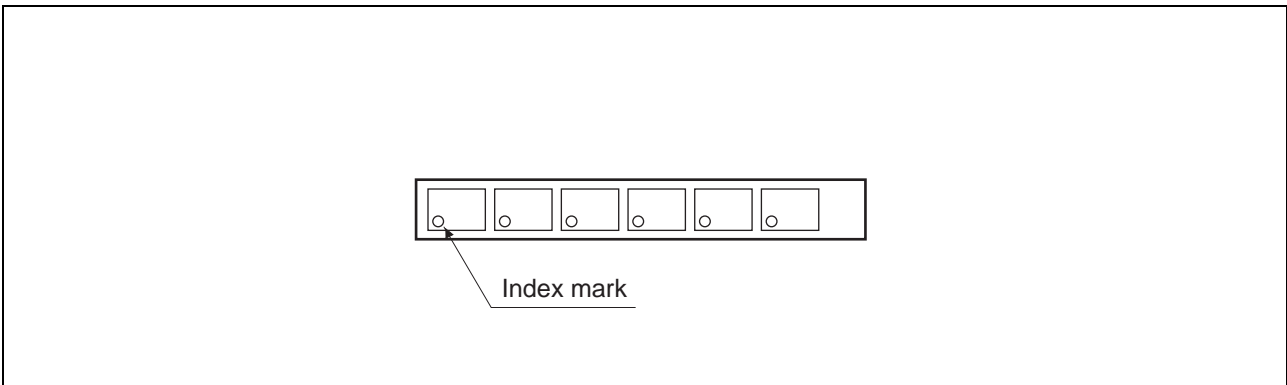
| Maximum quantity |               |               |
|------------------|---------------|---------------|
| pcs/tube(500mm)  | pcs/inner box | pcs/outer box |
| 85               | 4,250         | 17,000        |

No heat resistance.  
Package should not be baked by using tube.

(Dimensions in mm)





- Direction of index in tube





## 1.2 Product label indicators (Example)

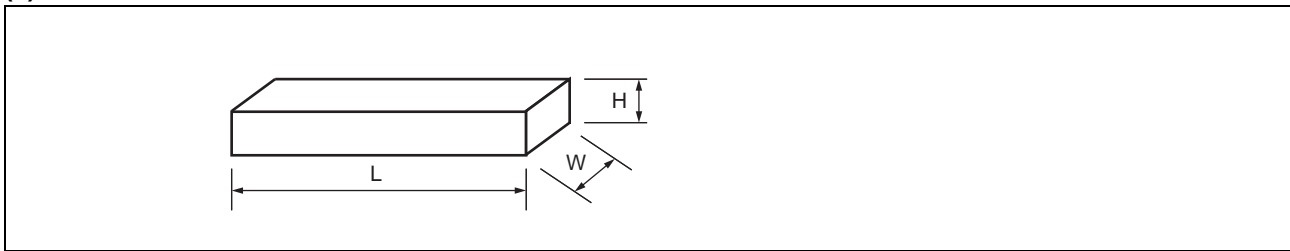
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)  
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

|  |  |
|--|--|
| XXXXXXXXXXXXXXXX (Customer part number or FJ part number)<br>(3N)1 XXXXXXXXXXXXXXXX XXX (LEAD FREE mark)<br>(Part number and quantity)<br><br>QC PASS<br>(3N)2 XXXXXXXXXXXXXXXX XXXXXXXX<br>(FJ control number)<br><br>XXX pcs (Quantity)<br>XXXXXXXXXXXXXXXX (Customer part number or FJ part number)<br> (Customer part number or FJ part number bar code)<br>XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx | ← C-3 Label<br><br><br><br><br><br><br><br><br><br>← Perforated line<br>← Supplemental Label |
| XXXXXXXXXXXXXXXX (Customer part number or FJ part number)<br>(FJ control number bar code)<br> XX/XX (Package count) XXXX-XXX XXX<br>XXXX-XXX XXX<br>XXXXXXXXXXXXXXXX (FJ control number) (Lot Number and quantity)<br>XXXXXXXXXXXXXXXX (Comment)  |  |

# MB85RC64TA

## 1.3 Dimensions for Containers

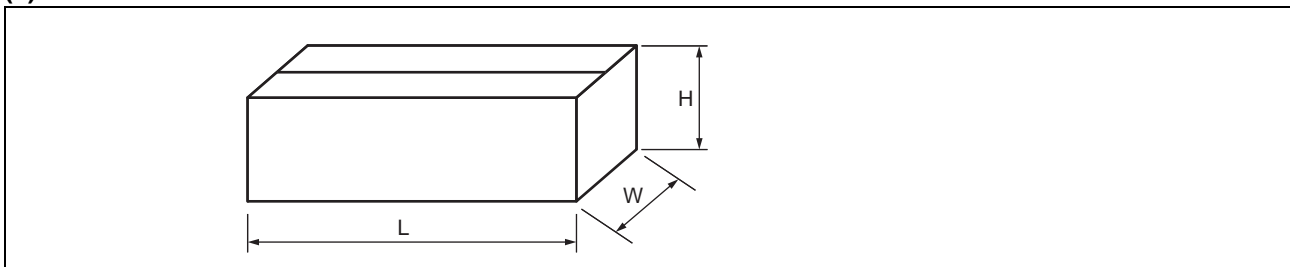
### (1) Dimensions for inner box



| L   | W   | H  |
|-----|-----|----|
| 540 | 125 | 75 |

(Dimensions in mm)

### (2) Dimensions for outer box

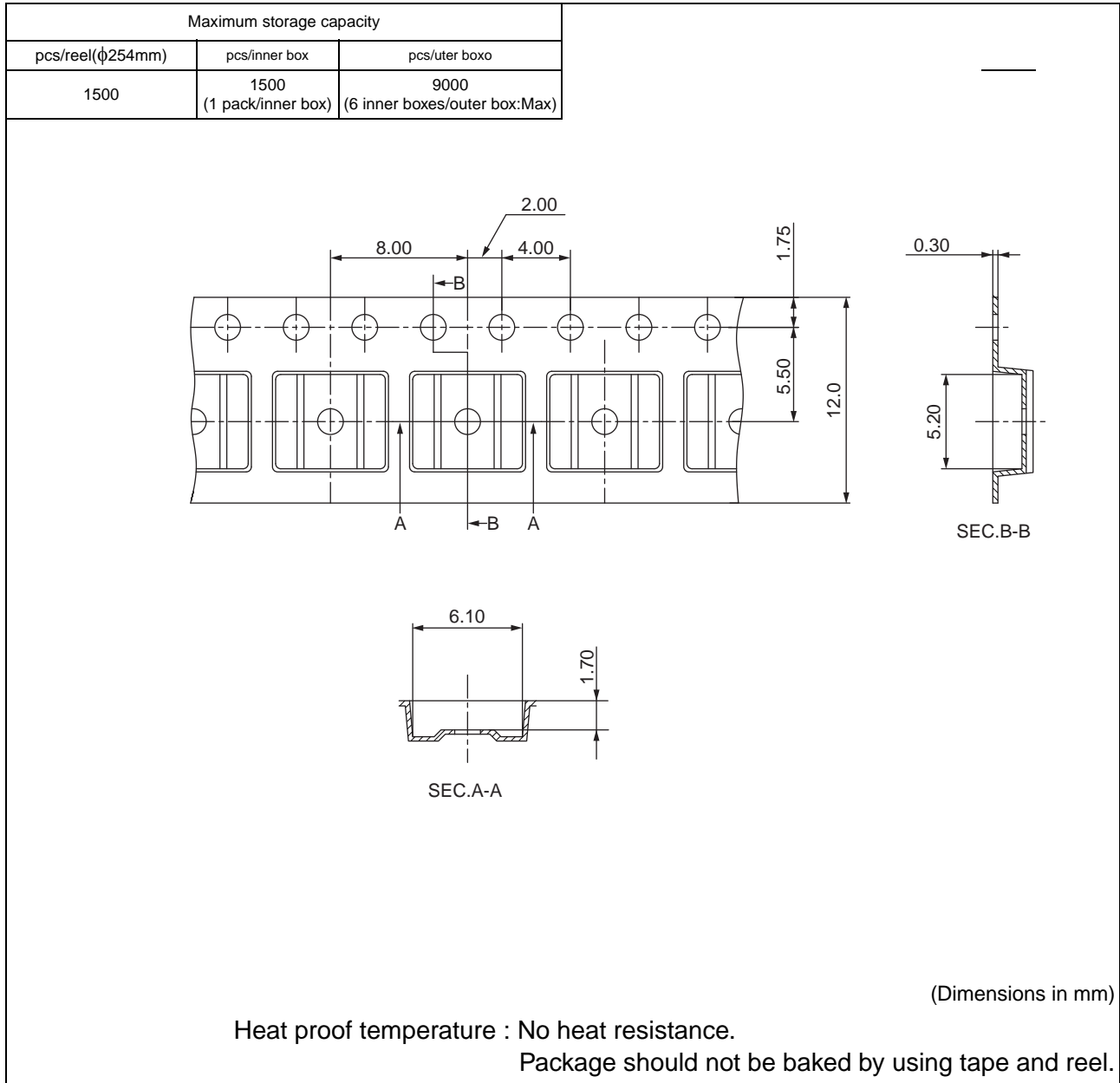


| L   | W   | H   |
|-----|-----|-----|
| 549 | 277 | 180 |

(Dimensions in mm)

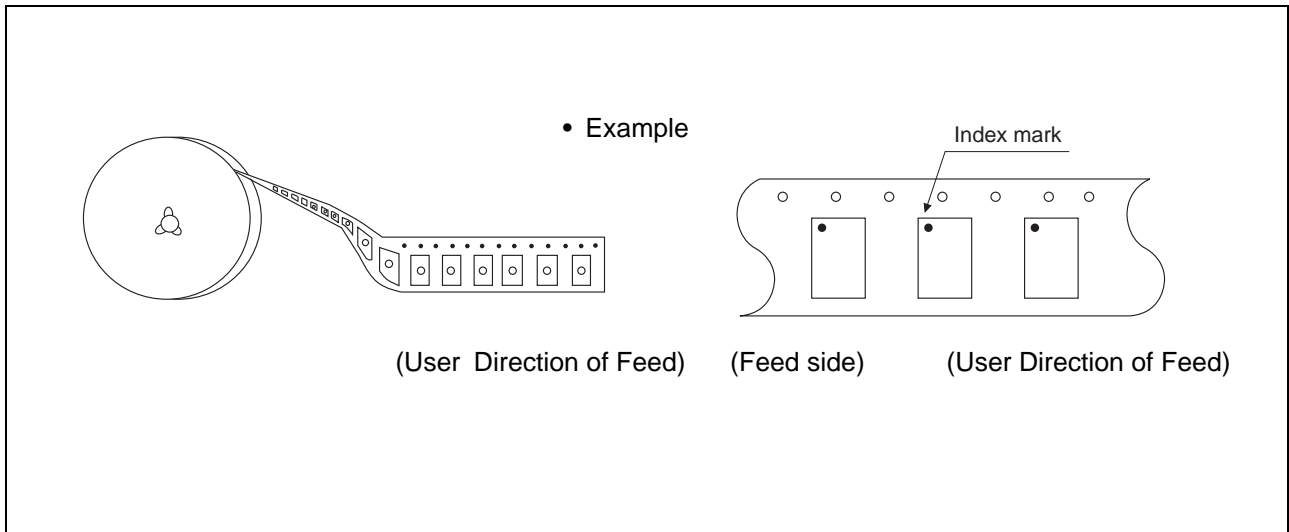
## 2. Emboss Tape (MB85RC64TAPNF-G-BDERE1)

### 2.1 Tape Dimensions(not drawn to scale) (8-pin plastic SON)

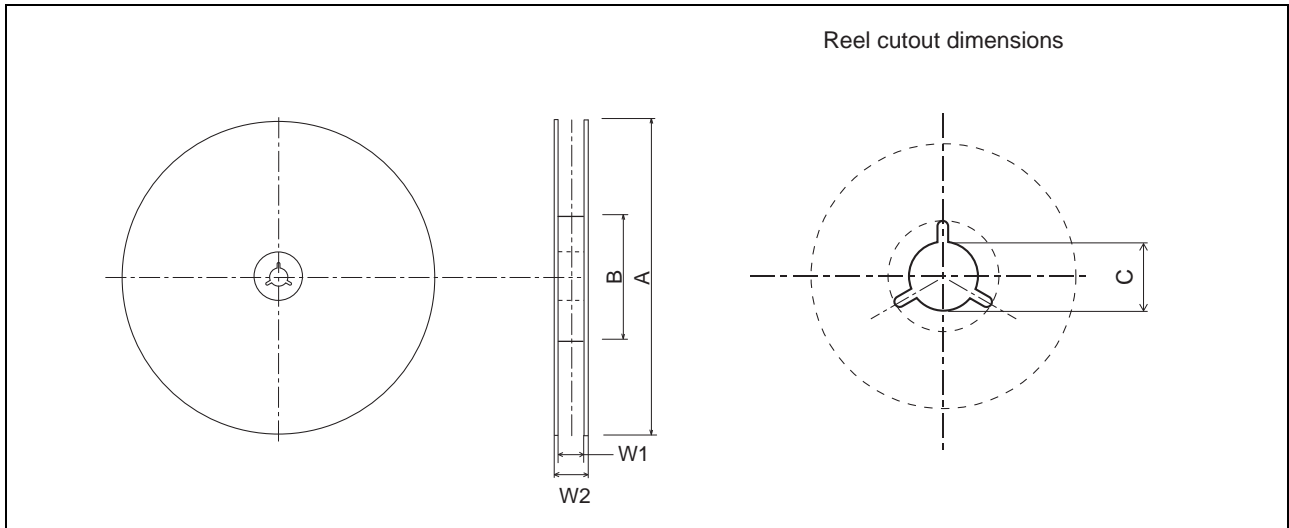


# MB85RC64TA

## 2.2 IC orientation



## 2.3 Reel dimensions









Dimensions in mm


| Tape width | A   | B   | C  | W1   | W2   |
|------------|-----|-----|----|------|------|
| 12         | 254 | 100 | 13 | 13.5 | 17.5 |

## 2.4 Product label indicators (Example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)  
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

|   |  |                      |
|---|--|----------------------|
| XXXXXXXXXXXXXXXXXX (Customer part number or FJ part number)                       |   | ← C-3 Label          |
| (3N)1 XXXXXXXXXXXXXXXXXX XXX (Part number and quantity)                           | (LEAD FREE mark)   |                      |
|  | QC PASS  |                      |
| (3N)2 XXXXXXXXXXXXXXXXXX (FJ control number)                                      |  |                      |
|  |  |                      |
| XXX pcs (Quantity)  |  |                      |
| XXXXXXXXXXXXXXXXXXXX (Customer part number or FJ part number)                     |  |                      |
|  | (Customer part number or FJ part number bar code)  |                      |
| XXXX/XX/XX (Packed years/month/day)   | ASSEMBLED IN xxxx  | ← Perforated line    |
| XXXXXXXXXXXXXXXXXXXX (Customer part number or FJ part number)                     |  | ← Supplemental Label |
| (FJ control number bar code)  |  |                      |
|  | XX/XX (Package count)  |                      |
| XXXXXXXXXXXX (FJ control number)  | XXXX-XXX XXX (Lot Number and quantity)   |                      |
| XXXXXXXXXXXXXXXXXXXX (Comment)  |  |                      |

Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)  
 [MSL Label (100mm × 70mm)]

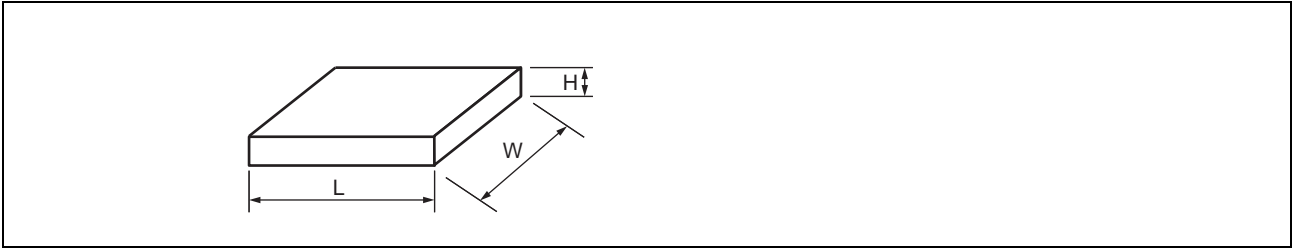
|   |  |          |
|---|--|----------|
|    | <b>Caution</b>   | LEVEL    |
|   | This bag contains<br><b>MOISTURE-SENSITIVE DEVICES</b> | <b>3</b> |
| <p>1. Calculated shelf life in sealed bag: 24 months at &lt;40°C and &lt;90% relative humidity (RH)</p> <p>2. Peak package body temperature: 260°C</p> <p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be</p> <p>a) Mounted within: 168 hours of factory conditions<br/>                 &lt;30°C/60% RH, or</p> <p>b) Stored per J-STD-033</p> <p>4. Devices require bake, before mounting, if:</p> <p>a) Humidity Indicator Card reads &gt;10% for level 2a - 5a devices or &gt;60% for level 2 devices when read at 23 ± 5°C</p> <p>b) 3a or 3b are not met</p> <p>5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure</p> <p>Bag Seal Date: see adjacent bar code label.</p> <p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p> |  |          |

← MSL label

# MB85RC64TA

## 2.5 Dimensions for Containers

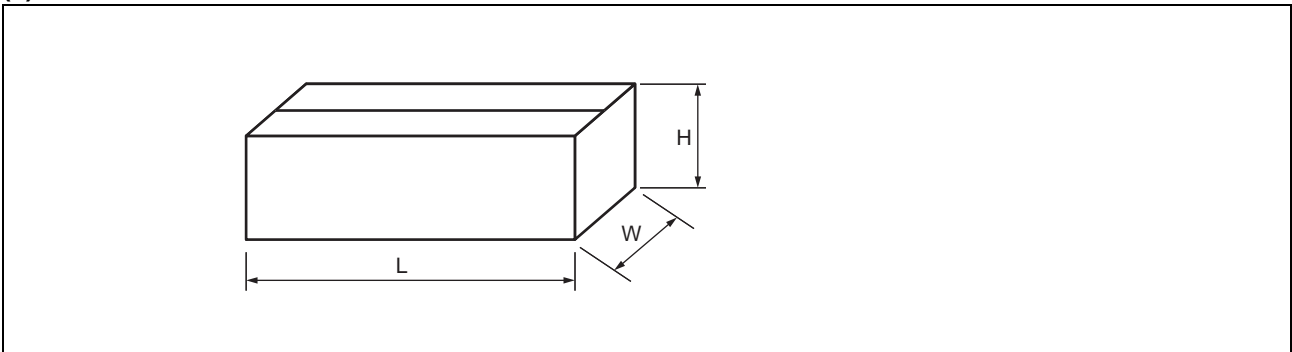
### (1) Dimensions for inner box



| Tape width | L   | W   | H  |
|------------|-----|-----|----|
| 12         | 265 | 262 | 51 |

(Dimensions in mm)

### (2) Dimensions for outer box



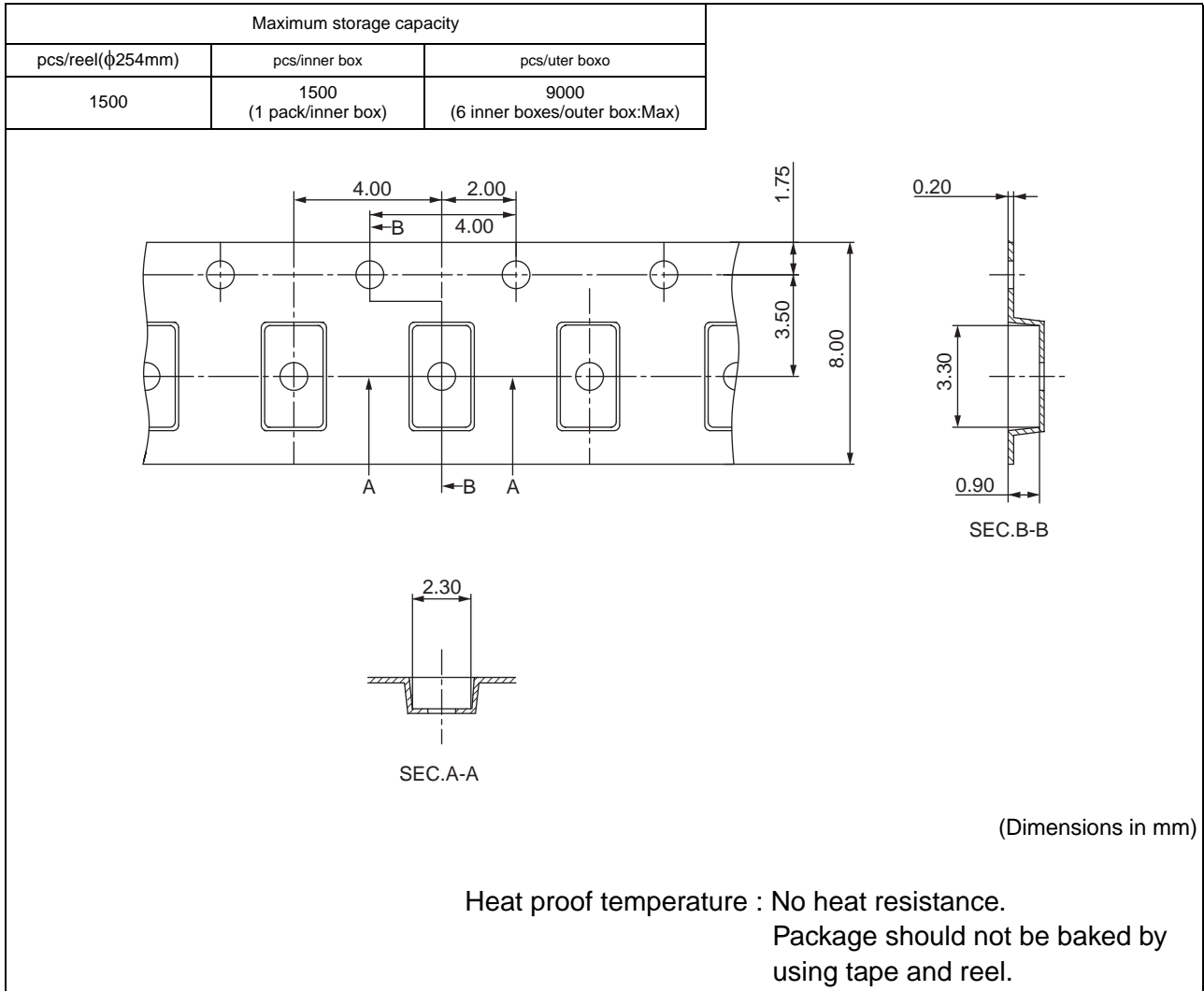
| L   | W   | H   |
|-----|-----|-----|
| 549 | 277 | 180 |

(Dimensions in mm)

## (2)MB85RC64TAPN-G-AMEWE1

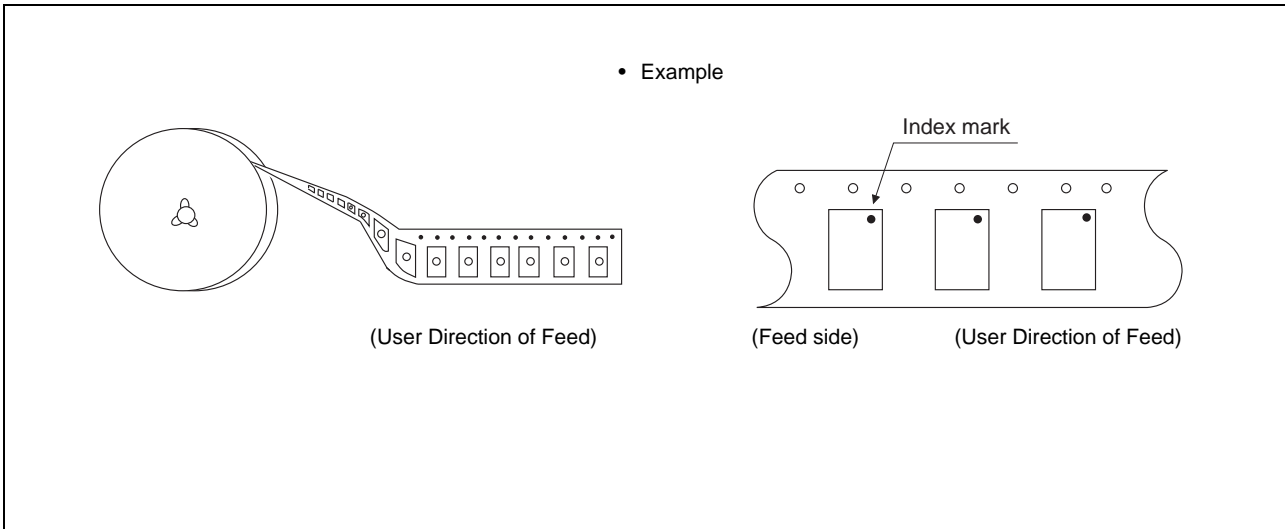
### 1. Emboss Tape (MB85RC64TAPN-G-AMEWE1)

#### 1.1 Tape Dimensions (not drawn to scale) (8-pin plastic SON)

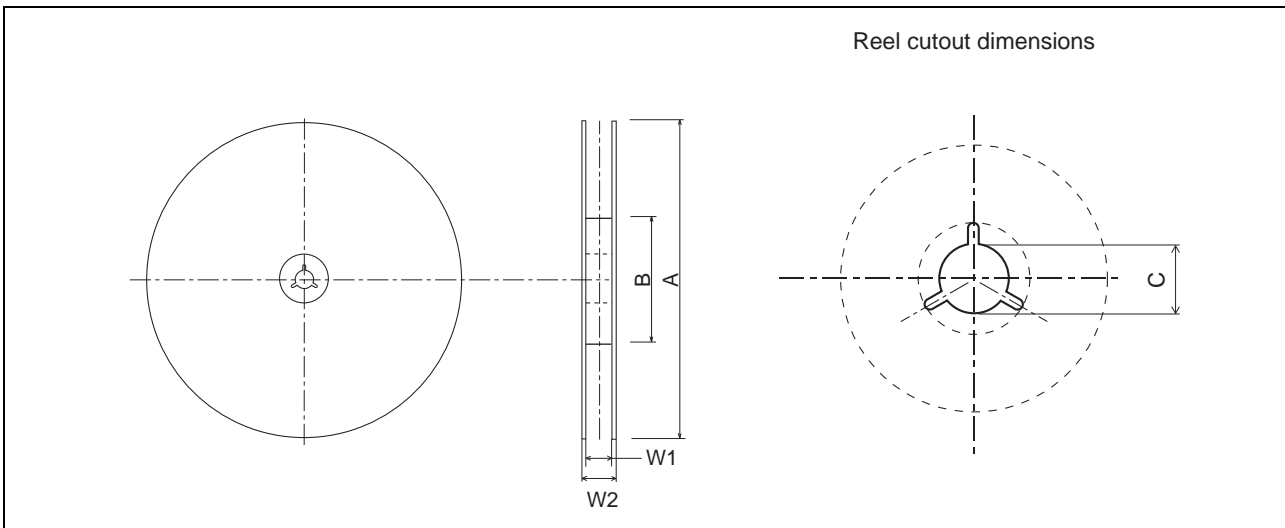


# MB85RC64TA

## 1.2 IC orientation



## 1.3 Reel dimensions



Dimensions in mm

| Tape width | A   | B   | C  | W1  | W2   |
|------------|-----|-----|----|-----|------|
| 8          | 254 | 100 | 13 | 9.5 | 13.5 |



## 1.4 Product label indicators (Example)

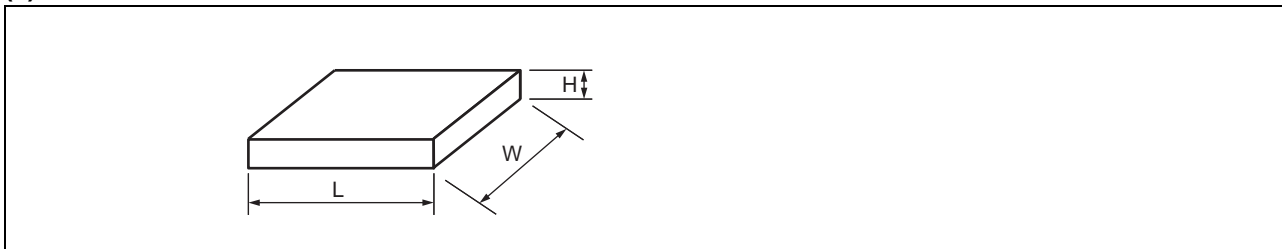
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)  
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

|  |                      |
|--|----------------------|
| XXXXXXXXXXXXXXXXXX (Customer part number or FJ part number)          |                      |
| (3N)1 XXXXXXXXXXXXXXXXXXXX XXX (LEAD FREE mark)                      | ← C-3 Label          |
| XXXXXXXXXXXXXXXXXX (Part number and quantity)                        |                      |
| XXXXXXXXXXXXXXXXXX (FJ control number)                               |                      |
| XXXXXXXXXXXXXXXXXX (Customer part number or FJ part number)          |                      |
| XXXXXXXXXXXXXXXXXX (Customer part number or FJ part number bar code) |                      |
| XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx                | ← Perforated line    |
| XXXXXXXXXXXXXXXXXX (Customer part number or FJ part number)          |                      |
| XXXXXXXXXXXXXXXXXX (FJ control number bar code)                      |                      |
| XXXXXXXXXXXXXXXXXX (FJ control number ) (Lot Number and quantity)    | ← Supplemental Label |
| XXXXXXXXXXXXXXXXXX (Comment)   |                      |

# MB85RC64TA

## 1.5 Dimensions for Containers

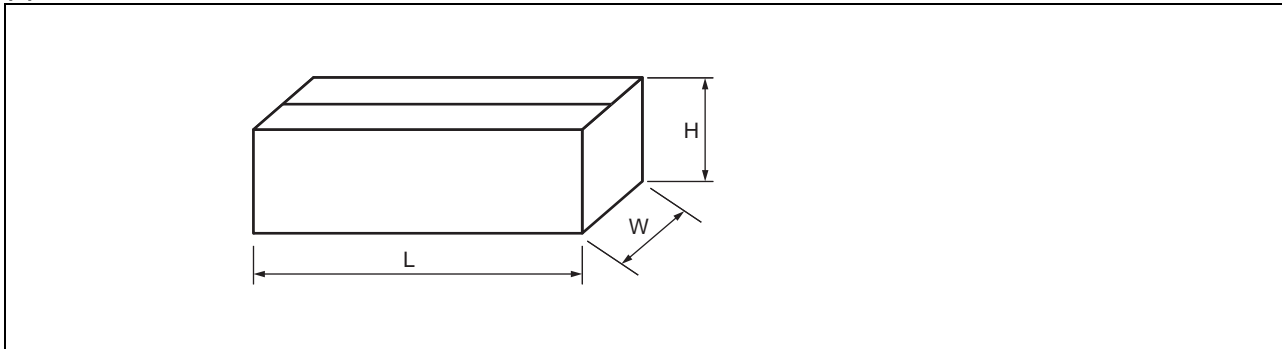
### (1) Dimensions for inner box



| Tape width | L   | W   | H  |
|------------|-----|-----|----|
| 8          | 265 | 262 | 51 |

(Dimensions in mm)

### (2) Dimensions for outer box



| L   | W   | H   |
|-----|-----|-----|
| 549 | 277 | 180 |

(Dimensions in mm)

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page  | Section  | Results  |
|-------|--|--|
| 1     | ■ FEATURES   | <ul style="list-style-type: none"> <li>• Data Retention:19.1 years(+105 °C), 70.4years(+85 °C)</li> <li>• Operation ambient temperature range: – 40 °C to +105 °C</li> </ul> |
| 2     | <ul style="list-style-type: none"> <li>■ PIN ASSIGNMENT</li> <li>■ PIN FUNCTIONAL DESCRIPTIONS</li> </ul>                | DIE PD is added.   |
| 14    | <ul style="list-style-type: none"> <li>■ ABSOLUTE MAXIMUM RATINGS</li> <li>■ RECOMMENDED OPERATING CONDITIONS</li> </ul> | Operation ambient temperature: – 40 °C to +105 °C  |
| 16    | <ul style="list-style-type: none"> <li>■ ELECTRICAL CHARACTERISTICS</li> <li>2. AC Characteristics</li> </ul>            | Operation ambient temperature: – 40 °C to +105 °C  |
| 18    | ■ POWER ON/OFF SEQUENCE  | SDA,SCL specification changed partially.   |
| 18    | ■ FRAM Characteristics   | Data Retention:19.1 years(+105 °C), 70.4 years(+85 °C)   |
| 19    | ■ ESD AND LATCH-UP   | ESD MM (Machine Model) omitted.  |
| 21,22 | ■ PACKAGE DIMENSION  | Weight omitted.  |
| 23    | ■ MARKING  | Marking example changed, comments added.   |
| 29    | ■ PACKING INFORMATION  | Added MSL label for MB85RC64TAPNF-G-BDERE1.  |
| 31    | ■ PACKING INFORMATION  | Added packing information for MB85RC64TAPN-G-AWEWE1.   |

## FUJITSU SEMICONDUCTOR MEMORY SOLUTION LIMITED

Shin-Yokohama TECH Building, 3-9-1 Shin-Yokohama,

Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan

<https://www.fujitsu.com/jp/fsm/en/>

### All Rights Reserved.

FUJITSU SEMICONDUCTOR MEMORY SOLUTION LIMITED, its subsidiaries and affiliates (collectively, "FUJITSU SEMICONDUCTOR MEMORY SOLUTION") reserves the right to make changes to the information contained in this document without notice. Please contact your FUJITSU SEMICONDUCTOR MEMORY SOLUTION sales representatives before order of FUJITSU SEMICONDUCTOR MEMORY SOLUTION device.

Information contained in this document, such as descriptions of function and application circuit examples is presented solely for reference to examples of operations and uses of FUJITSU SEMICONDUCTOR MEMORY SOLUTION device. FUJITSU SEMICONDUCTOR MEMORY SOLUTION disclaims any and all warranties of any kind, whether express or implied, related to such information, including, without limitation, quality, accuracy, performance, proper operation of the device or non-infringement. If you develop equipment or product incorporating the FUJITSU SEMICONDUCTOR MEMORY SOLUTION device based on such information, you must assume any responsibility or liability arising out of or in connection with such information or any use thereof. FUJITSU SEMICONDUCTOR MEMORY SOLUTION assumes no responsibility or liability for any damages whatsoever arising out of or in connection with such information or any use thereof.

Nothing contained in this document shall be construed as granting or conferring any right under any patents, copyrights, or any other intellectual property rights of FUJITSU SEMICONDUCTOR MEMORY SOLUTION or any third party by license or otherwise, express or implied. FUJITSU SEMICONDUCTOR MEMORY SOLUTION assumes no responsibility or liability for any infringement of any intellectual property rights or other rights of third parties resulting from or in connection with the information contained herein or use thereof.

The products described in this document are designed, developed and manufactured as contemplated for general use including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high levels of safety is secured, could lead directly to death, personal injury, severe physical damage or other loss (including, without limitation, use in nuclear facility, aircraft flight control system, air traffic control system, mass transport control system, medical life support system and military application), or (2) for use requiring extremely high level of reliability (including, without limitation, submersible repeater and artificial satellite). FUJITSU SEMICONDUCTOR MEMORY SOLUTION shall not be liable for you and/or any third party for any claims or damages arising out of or in connection with above-mentioned uses of the products.

Any semiconductor devices fail or malfunction with some probability. You are responsible for providing adequate designs and safeguards against injury, damage or loss from such failures or malfunctions, by incorporating safety design measures into your facility, equipments and products such as redundancy, fire protection, and prevention of overcurrent levels and other abnormal operating conditions.

The products and technical information described in this document are subject to the Foreign Exchange and Foreign Trade Control Law of Japan, and may be subject to export or import laws or regulations in U.S. or other countries. You are responsible for ensuring compliance with such laws and regulations relating to export or re-export of the products and technical information described herein.

All company names, brand names and trademarks herein are property of their respective owners.