Memory FRAM

$8 M (1 M \times 8) Bit$

MB85R8M1TA

DESCRIPTIONS

The MB85R8M1TA is an FRAM (Ferroelectric Random Access Memory) chip consisting of 1,048,576 words \times 8 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R8M1TA is able to retain data without using a back-up battery, as is needed for SRAM.

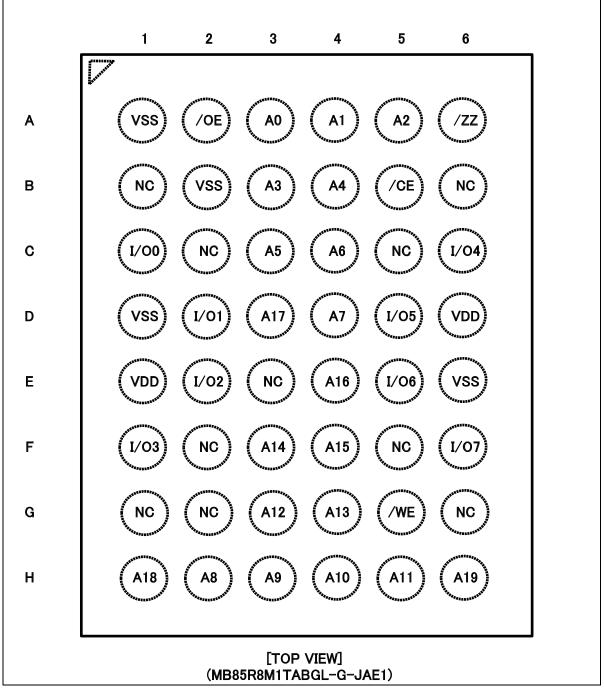
The memory cells used in the MB85R8M1TA can be used for 10^{14} read/write operations for 64bits, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MB85R8M1TA uses a pseudo-SRAM interface.

FEATURES

Bit configuration	: 1,048,576 words × 8 bits
Read/write endurance	$: 10^{14}$ times / 64 bits
Data retention	: 10 years (+85 °C), 95 years (+55 °C), over 200 years (+35 °C)
 Operating power supply voltage 	: 1.8 V to 3.6 V
 Low power operation 	: Operating power supply current 18 mA (Max)
	Standby current 150 µA (Max)
	Sleep current 10 µA (Max)
• Operation ambient temperature range	e : -40 °C to + 85 °C
Package	: 48-pin plastic FBGA
2	44-pin plastic TSOP
	RoHS compliant



PIN ASSIGNMENTS



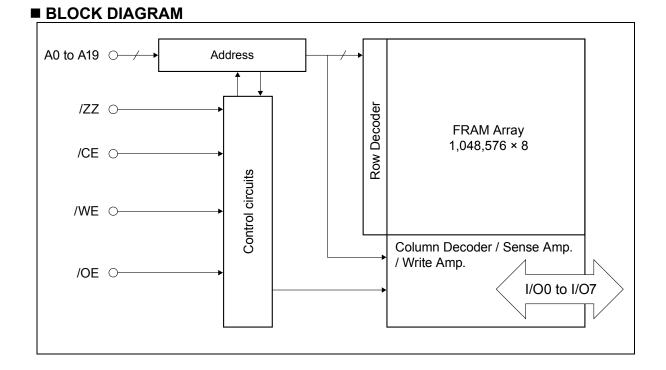
PIN ASSIGNMENTS(Continued)

A5 A4 A3 A2 A1 /CE NC I/O0 I/O1 VDD VDD VSS I/O2 I/O3 NC VD2 I/O3 NC A19 A18 A17 A16	1 () 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24	A6 A7 A8 /OE /ZZ A0 VSS VSS VSS I/O7 I/O6 VSS VDD I/O5 I/O4 I/O4 NC A9 A10 A11 A12 A13					
A15	22	24	□ A13 □ A14					
	[TOP VIEW]							
	(MB85R8M1TAFN-G-J	AE2)						

■ PIN DESCRIPTIONS

Pin DESCRIPTION	Pin Number(TSOP)	Pin Name	Functional Description
		A0 to A19	Address Input pins
A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3, H1, H6	39, 5 to 1, 44 to 42, 28 to 23, 22 to 18	A0 10 A19	Select 1,048,576 words in FRAM memory array by 20 Address Input pins. When these address inputs are
			changed during /CE equals to "L" level, reading operation of data selected in the address after transition will start.
C1, D2, E2, F1, C6, D5, E5, F6	9 to 10, 13 to 14, 31 to 32, 35 to 36	I/O0 to I/O7	Data Input/Output pins These are 8 bits bidirectional pins for reading and writing.
B5	6	/CE	Chip Enable Input pin In case the /CE equals to "L" level and /ZZ equals to "H" level, device is activated and enables to start memory access. In writing operation, input data from I/O pins are latched at the rising edge of /CE and written to FRAM memory array.
G5	17	/WE	Write Enable Input pin Writing operation starts at the falling edge of /WE. Input data from I/O pins are latched at the rising edge of /WE and written to FRAM memory array.
A2	41	/OE	Output Enable Input pin When the /OE is "L" level, valid data are output to data bus. When the /OE is "H" level, all I/O pins become high impedance (High-Z) state.
A6	40	/ZZ	Sleep Mode Input pin When the /ZZ becomes to "L" level, device transits to the Sleep Mode. During reading and writing operation, /ZZ pin shall be hold "H" level.
D6, E1	11, 33	VDD	Supply Voltage pins Connect all two pins to the power supply.
A1, B2, D1, E6	12, 34, 37 to 38	VSS	Ground pins Connect all four pins to ground.
B1, B6, C2, C5, E3, F2, F5, G1 to G2, G6	7 to 8, 15 to 16, 29 to 30	NC	No connected pin Left open or connect to VDD/VSS.

Note: Please refer to the timing diagram for functional description of each pin.



■ FUNCTIONAL TRUTH TABLE

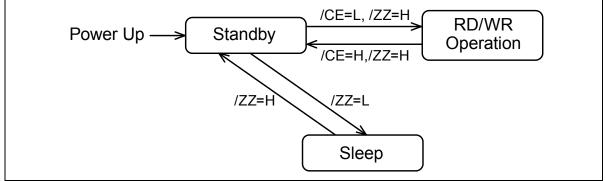
Operation Mode	/CE	/WE	/OE	A0 to A2	A3 to A19	/ZZ
Sleep	×	×	×	×	×	L
Standby	Н	×	×	×	×	Н
Read	\downarrow	Н	L	H or L	H or L	Н
Address Access Read	L	Н	L	H or L	↑ or ↓	Н
Write(/CE Control)*1	\downarrow	L	×	H or L	H or L	Н
Write(/WE Control) ^{*1*2}	L	\downarrow	×	H or L	H or L	Н
Address Access Write ^{*1*3}	L	\downarrow	×	H or L	↑ or ↓	Н
Pre-charge	↑	×	×	×	×	Н
Page Read	L	Н	L	↑ or ↓	H or L	Н
Page Address Write	L	\downarrow	Н	↑ or ↓	H or L	Н
ote: $H=$ "H" level, $L=$ "	'L'' level,	↑= Risin	g edge,	↓= Falling ed	$ ge, \times = H,]$	L,↓or↑

*1: In writing cycle, input data is latched at early rising edge of /CE or /WE.

*2: In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.

*3: In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

State Transition Diagram



ABABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rat	ting	Unit
Farameter	Symbol	Min	Max	Unit
Power Supply Voltage*	V _{DD}	- 0.5	+ 4.0	V
Input Pin Voltage*	V _{IN}	- 0.5	$V_{DD} + 0.5 \ (\leq 4.0)$	V
Output Pin Voltage*	V _{OUT}	- 0.5	$V_{DD} + 0.5 \ (\leq 4.0)$	V
Operation Ambient Temperature	T _A	- 40	+ 85	°C
Storage Temperature	Tstg	- 55	+ 125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Value		Unit
Farameter	Symbol	Min	Тур	Max	Unit
Power Supply Voltage ^{*1}	V _{DD}	1.8	3.3	3.6	V
Operation Ambient Temperature ^{*2}	T _A	-40	—	+ 85	°C

*1: All voltages are referenced to VSS (ground 0 V).

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

		(within recomm		perating condi	tions)
Parameter	Symbol	Condition	Min	Value	Mov	Unit
Input Leakage Current	ILI	$V_{IN} = 0V$ to V_{DD}		Тур —	Max 5	μΑ
Output Leakage Current	$ I_{LO} $	$V_{OUT} = 0V$ to V_{DD} /CE = V_{IH} or /OE = V_{IH}	—	_	5	μΑ
Operating Power Supply Current ^{*1}	I _{DD}	$/CE = 0.2 \text{ V}, I_{out} = 0 \text{ mA}$	—	13.5	18	mA
Standby Current	I_{SB}	$\label{eq:constraint} \begin{array}{l} /ZZ \geq V_{DD} - 0.2V \\ /CE, /WE, /OE \geq V_{DD} - 0.2V \\ Others \geq V_{DD} - 0.2V \text{ or } \leq 0.2V \end{array}$	_	12	150	μΑ
Sleep Current	I _{ZZ}	$\label{eq:constraint} \begin{array}{l} /ZZ = V_{SS} \\ /CE, /WE, /OE \geq V_{DD} - 0.2V \\ Others \geq V_{DD} - 0.2V \mbox{ or } \leq 0.2V \end{array}$	_	3.5	10	μΑ
High Level Input Voltage	V _{IH}	$V_{DD} = 1.8V$ to 3.6V	$V_{\text{DD}} \times 0.8$	_	$V_{DD} + 0.3$	V
Low Level Input Voltage	V _{IL}	$V_{DD} = 1.8V$ to 3.6V	- 0.3	—	$V_{\text{DD}} \times 0.2$	V
High Level	V _{OH1}	$V_{DD} = 2.5V \text{ to } 3.6V$ $I_{OH} = -1.0\text{mA}$	$V_{\text{DD}} \times 0.8$	_	—	v
Output Voltage V _{OH2}		$V_{DD} = 1.8V$ to 2.5V $I_{OH} = -100\mu A$	$V_{DD}\!-\!0.2$	—	—	v
Low Level Output	V _{OL1}	$V_{DD} = 2.5V$ to 3.6V $I_{OL} = 2.0mA$	_	_	0.4	v
Voltage	V _{OL2}	$V_{DD} = 1.8V$ to 2.5V $I_{OL} = 150\mu A$	—	_	0.2	V

*1: During the measurement of I_{DD}, all Address and I/O were taken to only change once per active cycle. Iout : output current

2. AC Characteristics

AC Test Conditions

Power Supply Voltage	: 1.8 V to 3.6 V
Operation Ambient Temperature	$:-40 \ ^{\circ}C \ to + 85 \ ^{\circ}C$
Input Voltage Amplitude	: 0 V / V _{DD}
Input Rising Time	: 3 ns
Input Falling Time	: 3 ns
Input Evaluation Level	: V _{DD} /2
Output Evaluation Level	: V _{DD} /2
Output Load Capacitance	: 30 pF

(1) Read Cycle

Parameter	Symbol	Value bol (V _{DD} =1.8V to 2.5V)		Value (V _{DD} =2.5V to 3.6V)		Unit
	,	Min	Max	Min	Max	
Read Cycle time(/CE control)	t _{RC}	120	_	120	_	ns
Read Cycle time(Address access)	t _{RCA}	135	—	120		ns
/CE Access Time	t _{CE}	_	65	_	65	ns
Address Access Time	t _{AA}	_	135	_	120	ns
/CE Output Data Hold time	t _{OH}	0	_	0		ns
Address Access Output Data Hold time	t _{OAH}	20	—	20	_	ns
/CE Active Time	t _{CA}	65	—	65	_	ns
Pre-charge Time	t _{PC}	55	_	55		ns
Address Setup Time	t _{AS}	0	_	0	_	ns
Address Hold Time	t _{AH}	65	_	65	_	ns
/CE↑ to Address Transition time*1	tсан	0	—	0	—	ns
/OE Access Time	t _{OE}	_	35	_	20	ns
/CE Output Floating Time ^{*1}	t _{HZ}	_	10	_	10	ns
/OE Output Floating Time	t _{OHZ}	_	10		10	ns
Address Transition Time ^{*1}	t _{AX}	_	15		15	ns

*1: Same parameters with the Write cycle.

(2) Write Cycle

Parameter	Value Symbol (V _{DD} =1.8V to 2.5V)			Va (V _{DD} =2.5)	Unit	
	-,	Min	Max	Min	Max	
Write Cycle Time	t _{wc}	120		120	—	ns
/CE Active Time	t _{CA}	65		65	_	ns
/CE↓ to /WE↑ Time	t _{CW}	65		65	_	ns
Pre-charge Time	t _{PC}	55		55	_	ns
Write Pulse Width	t _{WP}	20		20	_	ns
Address Setup Time	t _{AS}	0		0	_	ns
Address Hold Time	t _{AH}	65		65	—	ns
/WE↓ to /CE↑ Time	t _{WLC}	20	_	20	—	ns
Address Transition to /WE↑ Time	$t_{\rm AWH}$	135	_	120	—	ns
/WE↑ to Address Transition Time	t _{WHA}	0	_	0	—	ns
Data Setup Time	t _{DS}	10	_	10	—	ns
Data Hold Time	t _{DH}	0	_	0	—	ns
/WE Output Floating Time	t _{WZ}	_	10	_	10	ns
/WE Output Access Time ^{*1}	t _{WX}	10	_	10	—	ns
Write Setup Time ^{*1}	tws	0	_	0	—	ns
Write Hold Time ^{*1}	t _{WH}	0	_	0	_	ns
/CE Output Floating Time	t _{HZ}	_	10	_	10	ns
Address transition Time	t _{AX}	_	15	_	15	ns

(3) Page Mode Read/Write Cycle

Parameter	Symbol	Value (V _{DD} =1.8V to 2.5V)		Value (V _{DD} =2.5V to 3.6V)		Unit
	-	Min	Max	Min	Max	
Page Mode Write Cycle Time	t _{PWC}	25	—	25	—	ns
Page Mode Write Pulse Width	t _{WPP}	16	—	16	—	ns
Page Address Setup Time (/WE=L)	t _{ASP}	8	—	8	—	ns
Page Address Hold Time (/WE=L)	t _{AHP}	15	—	15	—	ns
Page Address Access Time	t _{AAP}		25	—	25	ns
Page Address Data Hold Time	t _{OHP}	3	—	3	—	ns
Page Mode Read Cycle Time	t _{PRCA}	25	—	25	—	ns
Page Mode Write Pre Charge Width	t_{WPHP}	6	—	6	_	ns

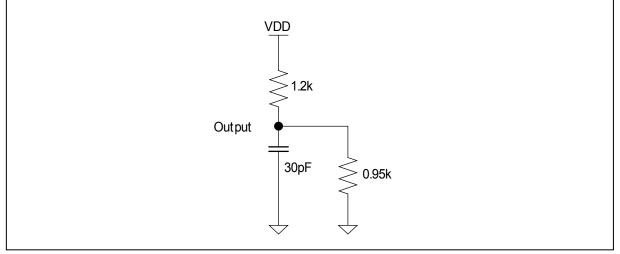
(4) Power ON/OFF Sequence and Sleep Mode Cycle

Parameter	Symbol	Va	lue	Unit
Parameter	Symbol	Min	Max	Unit
/CE level hold time for Power ON	t_{PU}	450		μs
/CE level hold time for Power OFF	t _{PD}	85		ns
Power supply rising time	t _{VR}	50		μs/V
Power supply falling time	$t_{\rm VF}$	100		μs/V
/ZZ active time	t _{ZZL}	1		μs
Sleep mode enable time	t _{ZZEN}	_	0	μs
/CE level hold time for Sleep mode release	t _{ZZEX}	450		μs

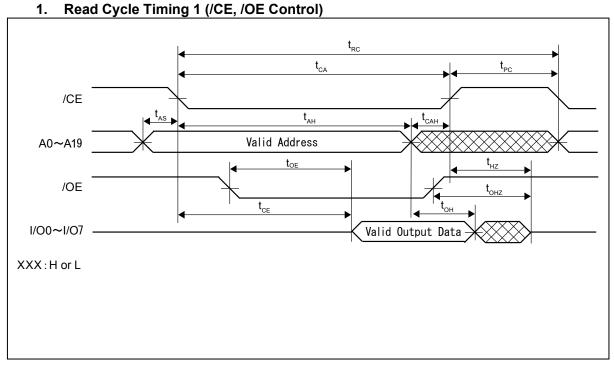
3. Pin Capacitance

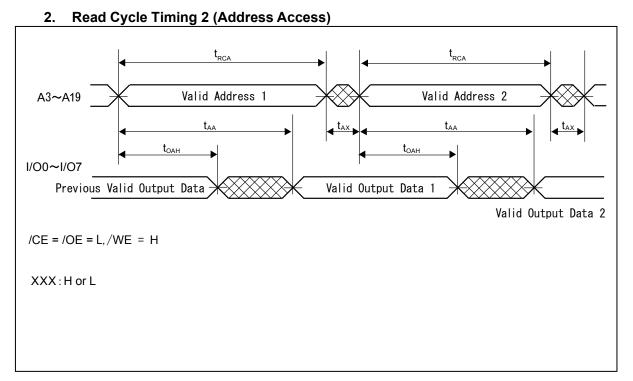
Parameter	Symbol	Condition	Value			Unit
Falameter	Symbol	Condition	Min	Тур	Max	Onit
Input Capacitance	C _{IN}	N - 2 2 N	-		9	pF
Input/Output Capacitance (I/O pin)	C _{I/O}	$V_{DD} = 3.3 V,$ f = 1 MHz, T _A = + 25 °C	_	_	9	pF
/ZZ Pin Input Capacitance	C _{ZZ}	$1 - 1$ WI11Z, $1_{\rm A} - + 25$ C	_	_	9	pF

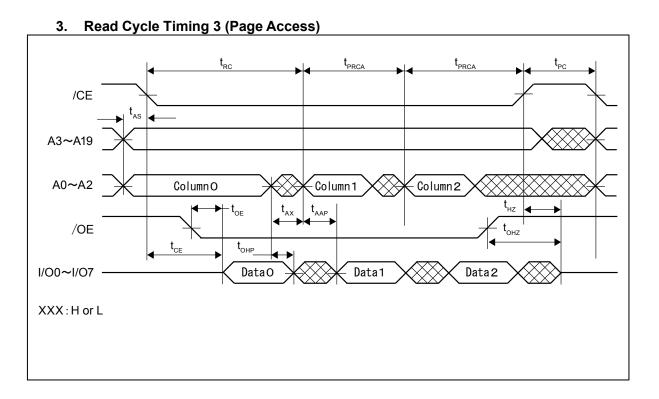
■ AC Test Load Circuit



TIMING DIAGRAMS







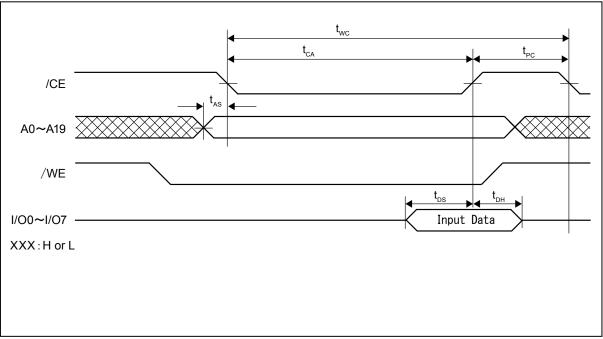
 \mathbf{t}_{RC} $\mathbf{t}_{_{\mathrm{CA}}}$ \mathbf{t}_{cw} /CE t_{AS} t_{wLC} 4 A0~A19 💥

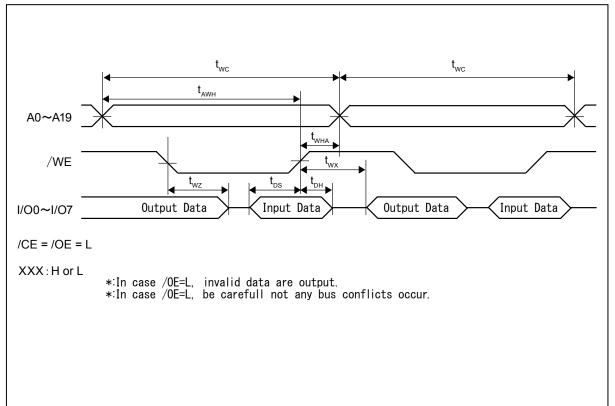
Write Cycle Timing 1 (/WE Control)

t_{PC} t_{AH} t_{wP} t_{wH} /WE t_{HZ} t_{DH} twz t_{DS} Output Data Input Data Output Data I/00~I/07 XXX : H or L *:In case /OE=L, invalid data are output. *:In case /OE=L, be carefull not any bus conflicts occur.

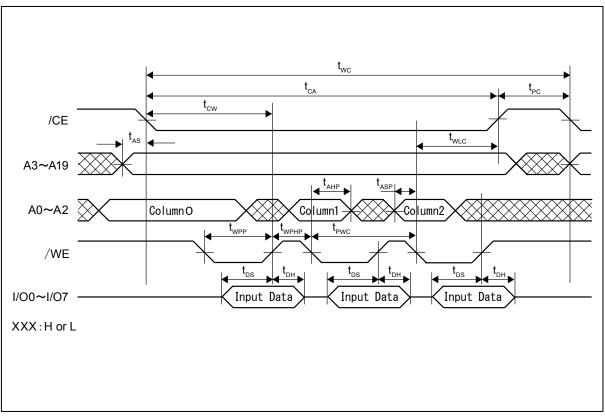
4.

5. Write Cycle Timing 2 (/CE Control)



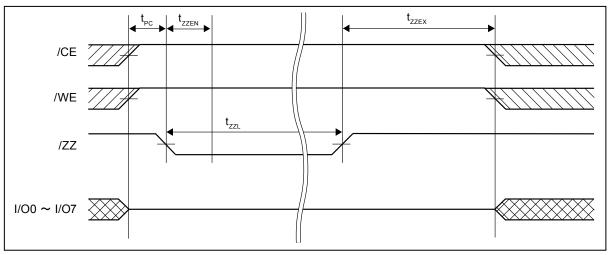


6. Write Cycle Timing 3 (Address Access and /WE Control)

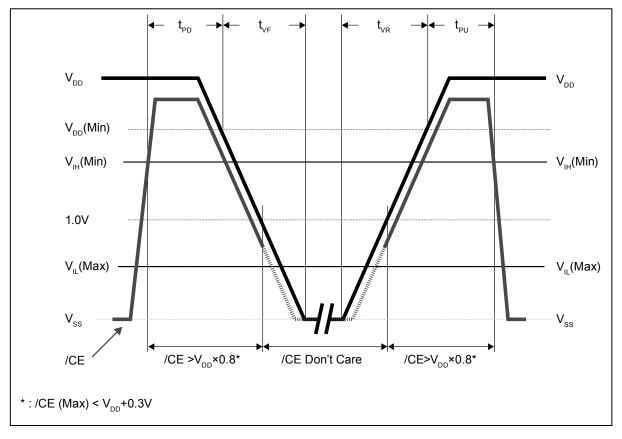


7. Write Cycle Timing 4 (Page Address Access)

8. Sleep Mode Timing



■ POWER ON/OFF SEQUENCE



■ FRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance ^{*1}	1014	_	Times/64bits	Operation Ambient Temperature $T_A = +85 ^{\circ}\text{C}$
	10	_		Operation Ambient Temperature $T_A = +85 ^{\circ}\text{C}$
Data Retention ^{*2}	95	_	Years	Operation Ambient Temperature $T_A = +55 \text{ °C}$
	\geq 200	_		Operation Ambient Temperature $T_A = +35 \text{ °C}$

*1: Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

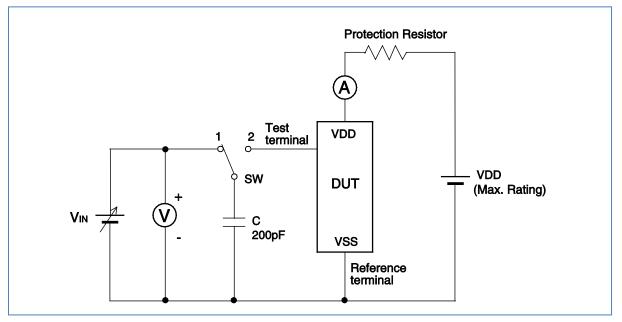
NOTE ON USE

• We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant		$\geq 2000 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant	MB85R8M1TAFN-G-JAE2 MB85R8M1TABGL-G-JAE1	$\geq 1000 \text{ V} $
Latch-Up (C-V Method) Proprietary method		$\geq 200 \text{ V} $

- C-V method of Latch-Up Resistance Test



Note: Charge voltage alternately switching 1 and 2 approximately 2 sec intervals. This switching process is considered as one cycle.

Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

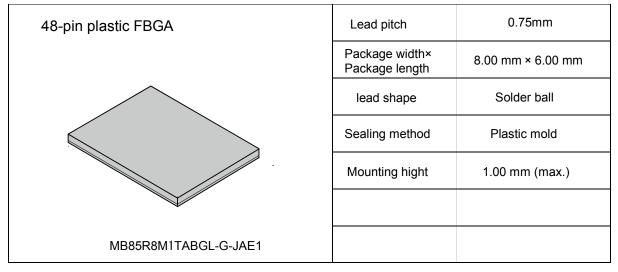
This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

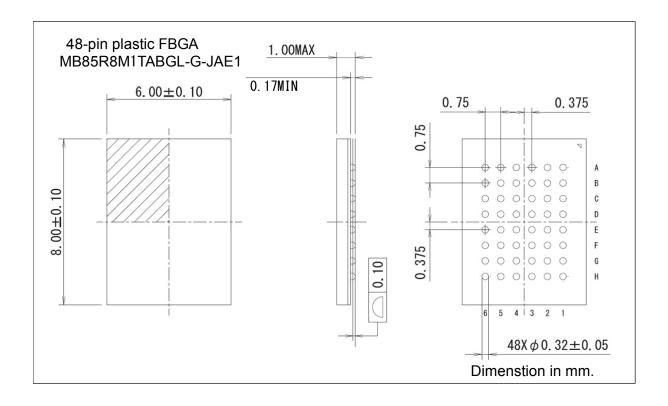
ORDERING INFORMATION

Part Number	Package	Shipping form	Minimum shipping quantity	
MB85R8M1TAFN-G-JAE2	44-pin plastic TSOP	Tray	*	
MB85R8M1TABGL-G-JAE1	48-pin plastic FBGA	Tray	*	

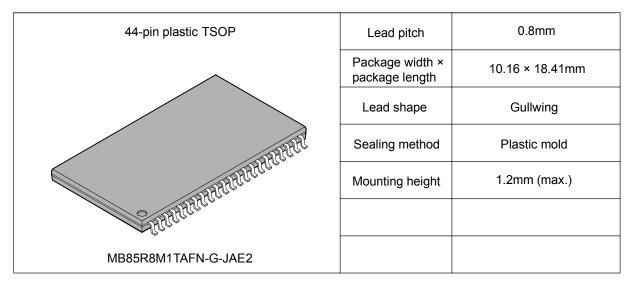
*: Please contact our sales office about minimum shipping quantity.

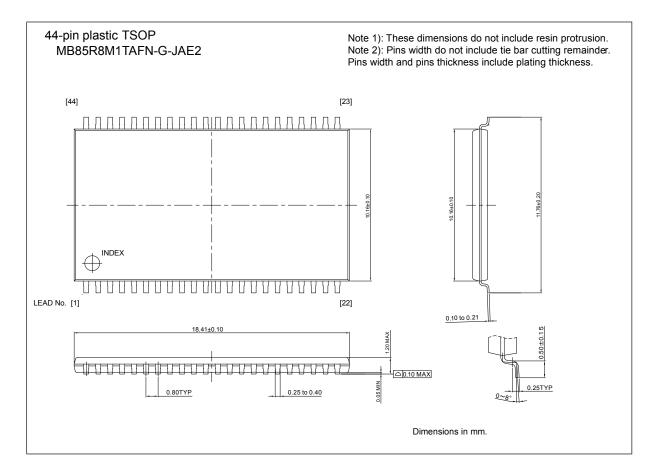
■ PACKAGE DIMENSIONS





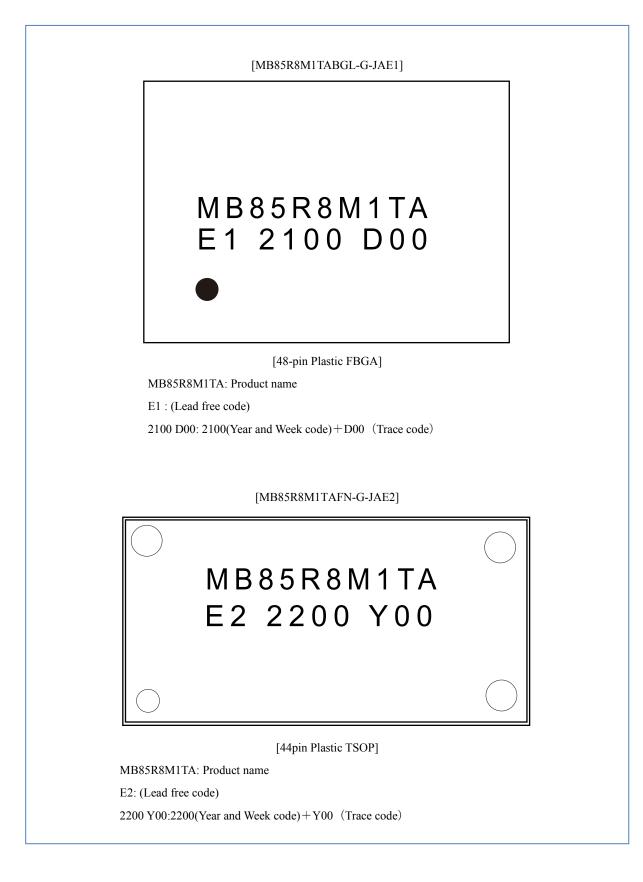
PACKAGE DIMENSIONS(Continued)





FUjitsu

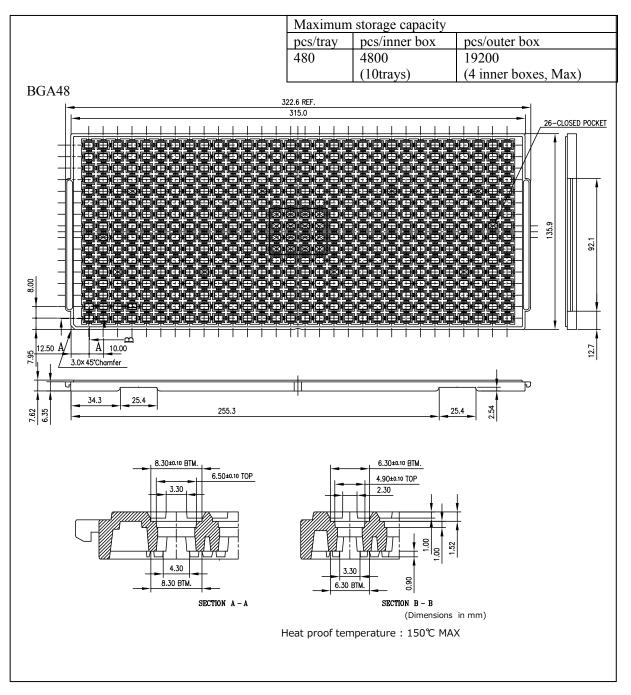
MARKING(Examples)



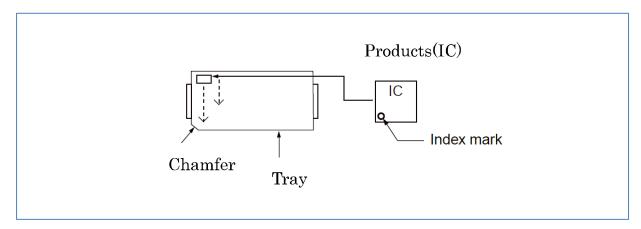
■ PACKING

(1)MB85R8M1TABGL-G-JAE1

1.1 Tray dimensions



1.2 IC orientation

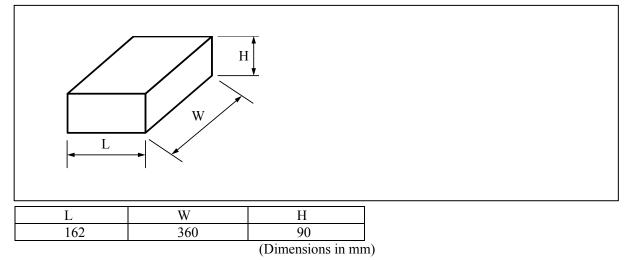


1.3 Product label indicators

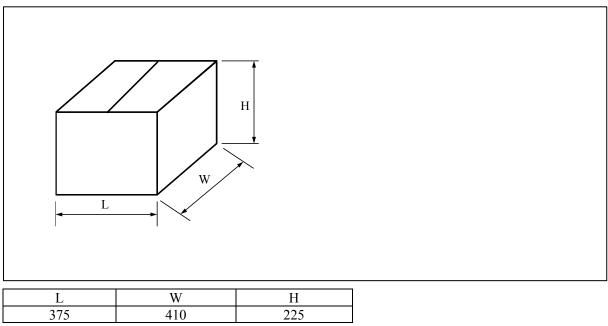
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping) [C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	ustomer part number or FJ part number)	← C3-Label
	XXX (LEAD FREE mark) (Part number and quantity) QC PASS	
(3N)2 XXXXXXXXX XXXXX 	(X (FJ control number)	
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	(Quantity) Sustomer part number or FJ part number) (Customer part number or FJ part number	
XXXX/XX/XX (Packed years/month/	bar code) /day) ASSEMBLED IN xxxx	← Perforated line
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	omer part number or FJ part number)	
XXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX		Supplemental Label

- 1.4 Dimensions for container
- (1) Dimensions for inner box



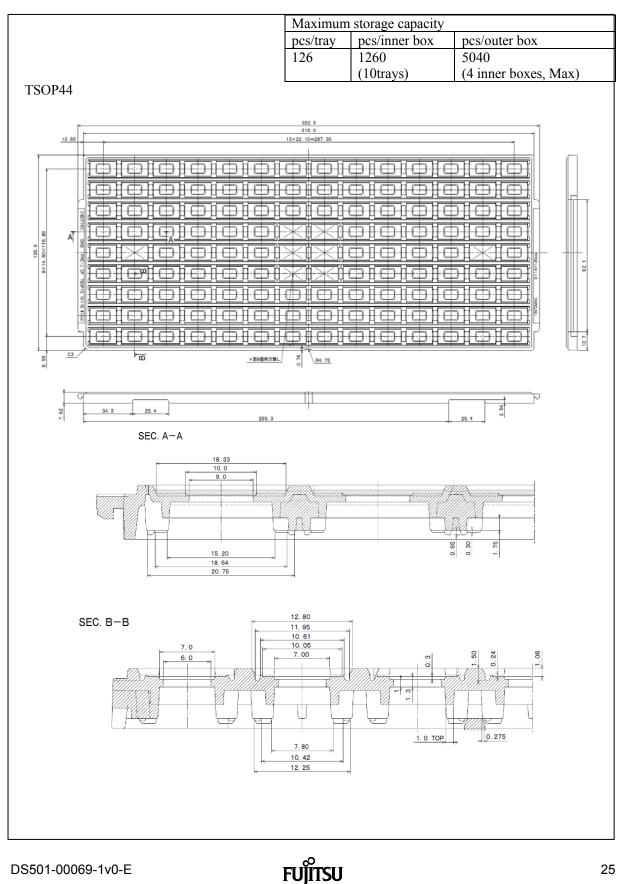
(2) Dimensions for outer box



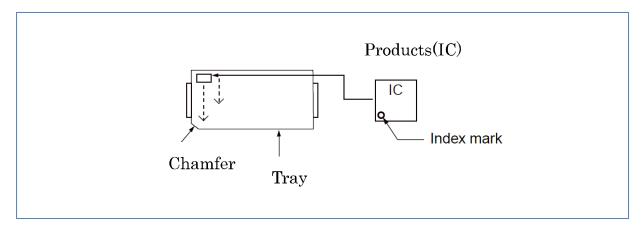
(Dimensions in mm)

(2)MB85R8M1TAFN-G-JAE2

2.1 Tray dimensions

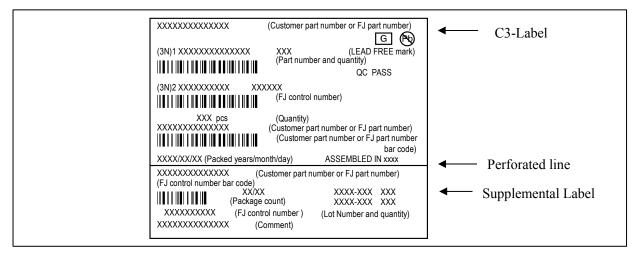


2.2 IC orientation



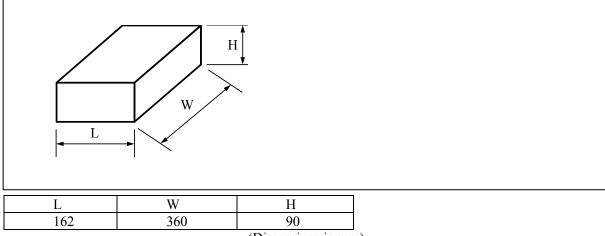
2.3 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping) [C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



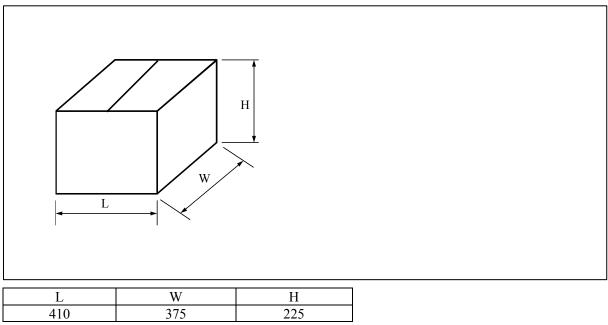
2.4 Dimensions for container

(1) Dimensions for inner box



(Dimensions in mm)

(2) Dimensions for outer box



(Dimensions in mm)

FUJITSU SEMICONDUCTOR MEMORY SOLUTION LIMITED

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