FUJITSU SEMICONDUCTOR
MEMORY SOLUTION DATA SHEET

DS501-00069-1v0-E

Memory FRAM

8 M (1 M × 8) Bit

MB85R8M1TA

■ DESCRIPTIONS

The MB85R8M1TA is an FRAM (Ferroelectric Random Access Memory) chip consisting of 1,048,576 words × 8 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R8M1TA is able to retain data without using a back-up battery, as is needed for SRAM.

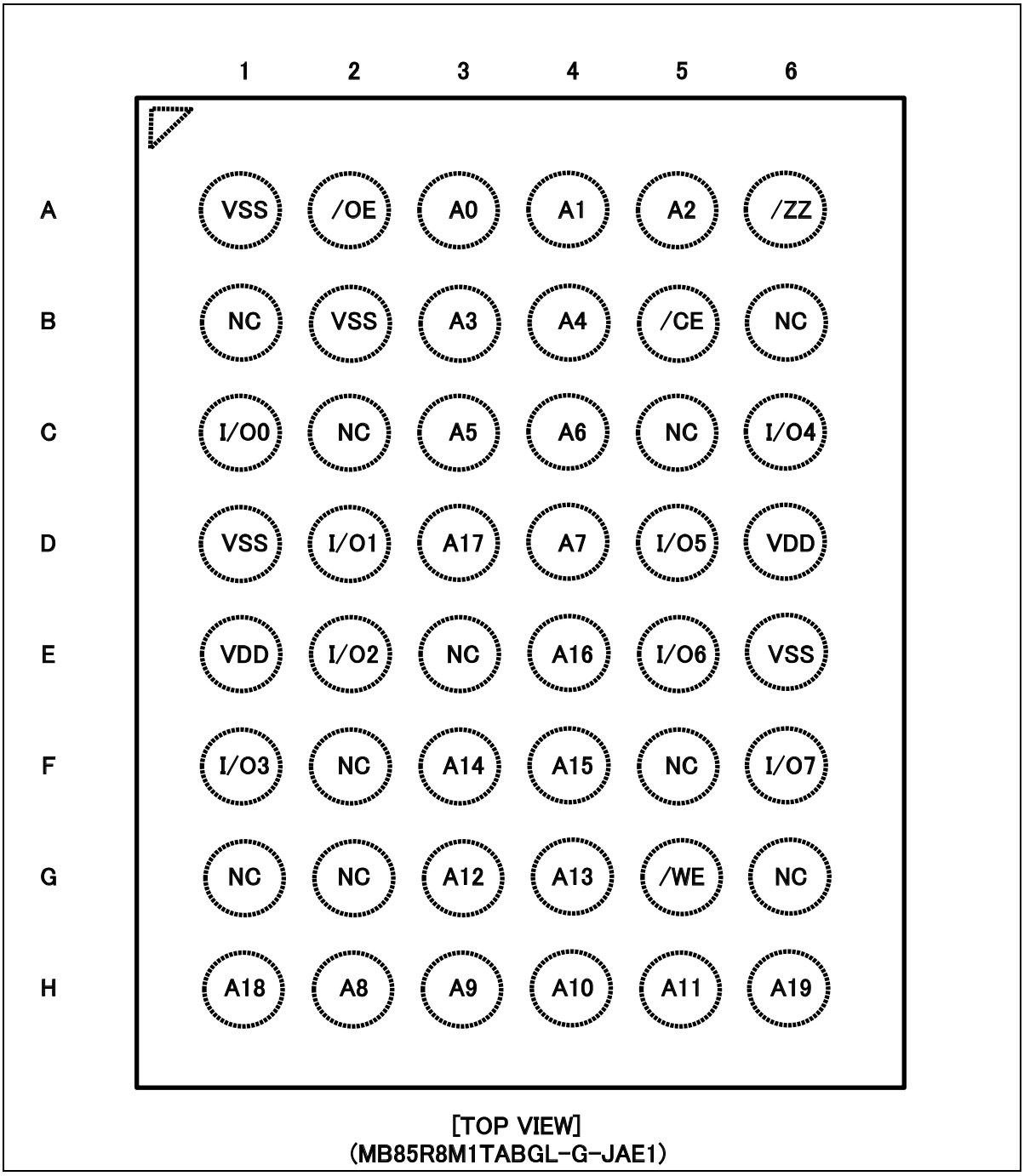
The memory cells used in the MB85R8M1TA can be used for 10^{14} read/write operations for 64bits, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MB85R8M1TA uses a pseudo-SRAM interface.

■ FEATURES

• Bit configuration	: 1,048,576 words × 8 bits
• Read/write endurance	: 10^{14} times / 64 bits
• Data retention	: 10 years (+ 85 °C), 95 years (+ 55 °C), over 200 years (+ 35 °C)
• Operating power supply voltage	: 1.8 V to 3.6 V
• Low power operation	: Operating power supply current 18 mA (Max) Standby current 150 µA (Max) Sleep current 10 µA (Max)
• Operation ambient temperature range	: − 40 °C to + 85 °C
• Package	: 48-pin plastic FBGA 44-pin plastic TSOP RoHS compliant

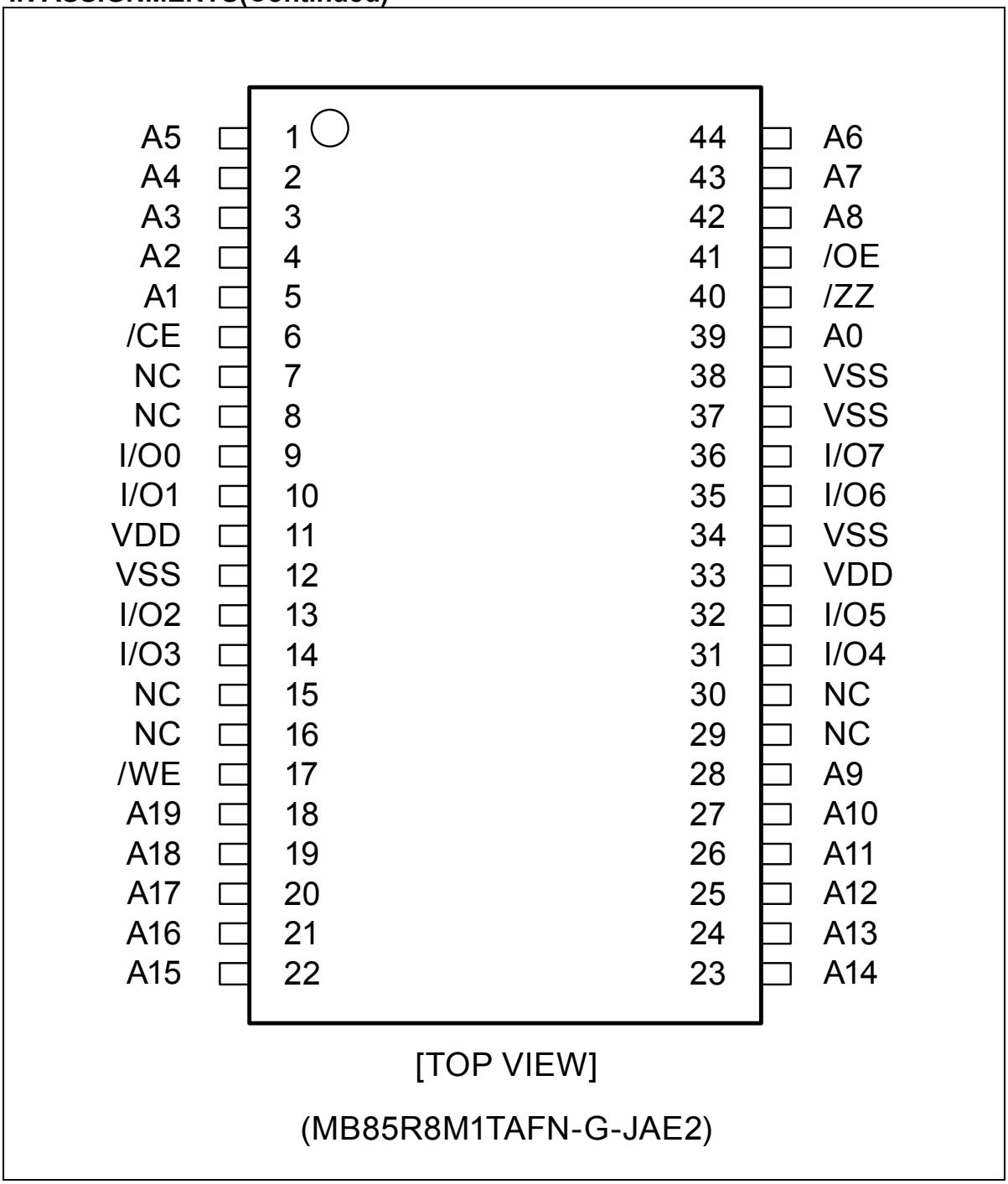
2022.02

■ PIN ASSIGNMENTS



[TOP VIEW]
(MB85R8M1TABGL-G-JAE1)

PIN ASSIGNMENTS(Continued)



[TOP VIEW]

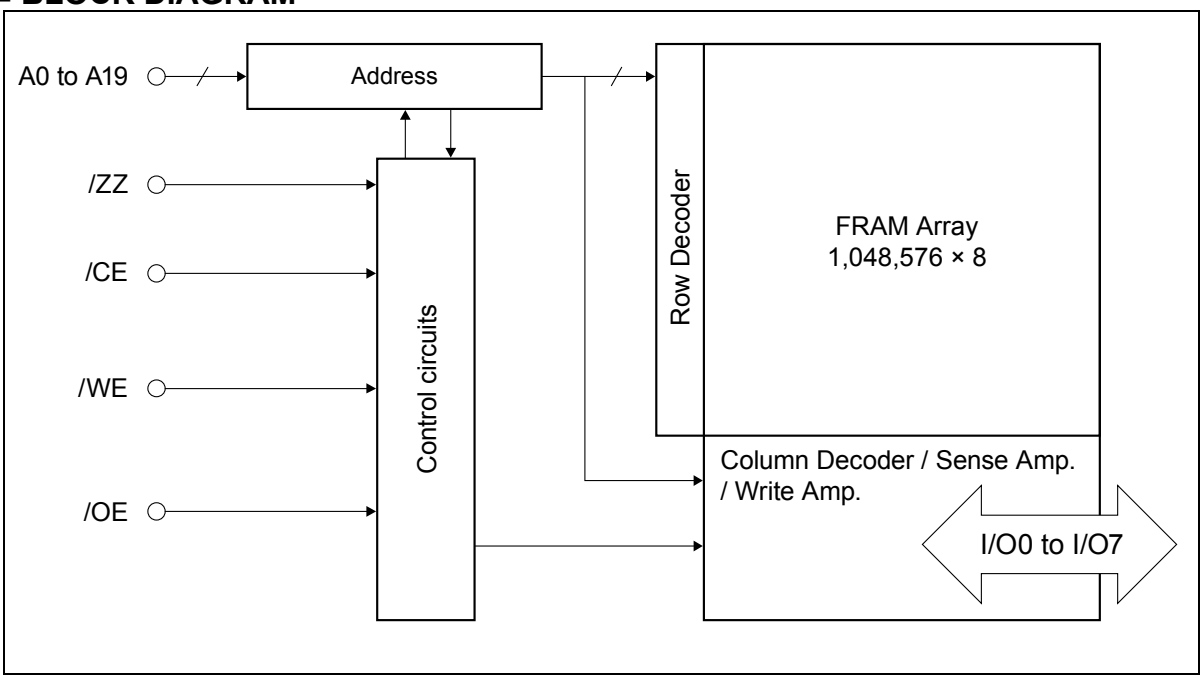
(MB85R8M1TAFN-G-JAE2)

■ PIN DESCRIPTIONS

Pin Number(FBGA)	Pin Number(TSOP)	Pin Name	Functional Description
A3, A4, A5, B3, B4 ,C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3, H1, H6	39, 5 to 1, 44 to 42, 28 to 23, 22 to 18	A0 to A19	Address Input pins Select 1,048,576 words in FRAM memory array by 20 Address Input pins. When these address inputs are changed during /CE equals to “L” level, reading operation of data selected in the address after transition will start.
C1, D2, E2, F1, C6, D5, E5, F6	9 to 10, 13 to 14, 31 to 32, 35 to 36	I/O0 to I/O7	Data Input/Output pins These are 8 bits bidirectional pins for reading and writing.
B5	6	/CE	Chip Enable Input pin In case the /CE equals to “L” level and /ZZ equals to “H” level, device is activated and enables to start memory access. In writing operation, input data from I/O pins are latched at the rising edge of /CE and written to FRAM memory array.
G5	17	/WE	Write Enable Input pin Writing operation starts at the falling edge of /WE. Input data from I/O pins are latched at the rising edge of /WE and written to FRAM memory array.
A2	41	/OE	Output Enable Input pin When the /OE is “L” level, valid data are output to data bus. When the /OE is “H” level, all I/O pins become high impedance (High-Z) state.
A6	40	/ZZ	Sleep Mode Input pin When the /ZZ becomes to “L” level, device transits to the Sleep Mode. During reading and writing operation, /ZZ pin shall be hold “H” level.
D6, E1	11, 33	VDD	Supply Voltage pins Connect all two pins to the power supply.
A1, B2, D1, E6	12, 34, 37 to 38	VSS	Ground pins Connect all four pins to ground.
B1, B6, C2, C5, E3, F2, F5, G1 to G2, G6	7 to 8, 15 to 16, 29 to 30	NC	No connected pin Left open or connect to VDD/VSS.

Note: Please refer to the timing diagram for functional description of each pin.

■ BLOCK DIAGRAM



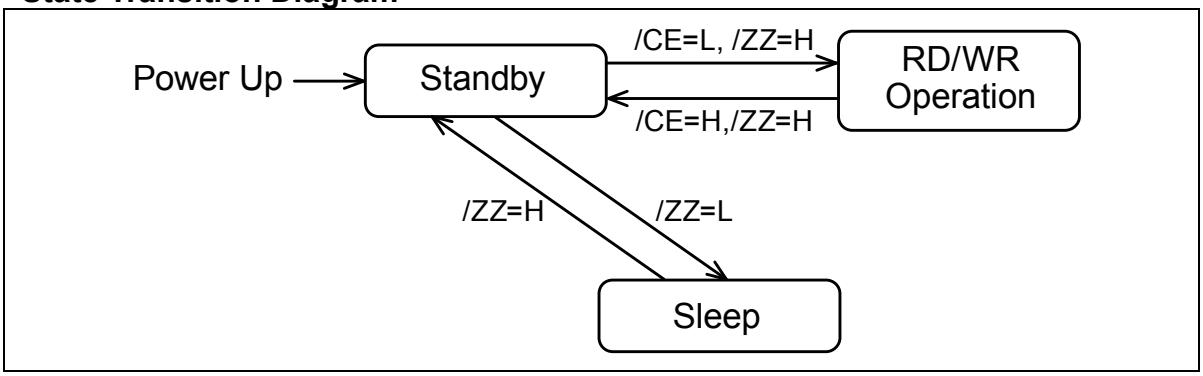
■ FUNCTIONAL TRUTH TABLE

Operation Mode	/CE	/WE	/OE	A0 to A2	A3 to A19	/ZZ
Sleep	×	×	×	×	×	L
Standby	H	×	×	×	×	H
Read	↓	H	L	H or L	H or L	H
Address Access Read	L	H	L	H or L	↑ or ↓	H
Write(/CE Control)*1	↓	L	×	H or L	H or L	H
Write(/WE Control)*1*2	L	↓	×	H or L	H or L	H
Address Access Write*1*3	L	↓	×	H or L	↑ or ↓	H
Pre-charge	↑	×	×	×	×	H
Page Read	L	H	L	↑ or ↓	H or L	H
Page Address Write	L	↓	H	↑ or ↓	H or L	H

Note: H= “H” level, L= “L” level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑

*1: In writing cycle, input data is latched at early rising edge of /CE or /WE.
*2: In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.
*3: In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

■ **State Transition Diagram**



■ ABABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V_{DD}	− 0.5	+ 4.0	V
Input Pin Voltage*	V_{IN}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Operation Ambient Temperature	T_A	− 40	+ 85	°C
Storage Temperature	Tstg	− 55	+ 125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*1	V_{DD}	1.8	3.3	3.6	V
Operation Ambient Temperature*2	T_A	− 40	—	+ 85	°C

*1: All voltages are referenced to VSS (ground 0 V).

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = 0V to V_{DD}	—	—	5	µA
Output Leakage Current	$\|I_{LO}\|$	V_{OUT} = 0V to V_{DD} /CE = V_{IH} or /OE = V_{IH}	—	—	5	µA
Operating Power Supply Current*1	I_{DD}	/CE = 0.2 V, I_{out} = 0 mA	—	13.5	18	mA
Standby Current	I_{SB}	/ZZ ≥ V_{DD} − 0.2V /CE, /WE, /OE ≥ V_{DD} − 0.2V Others ≥ V_{DD} − 0.2V or ≤ 0.2V	—	12	150	µA
Sleep Current	I_{ZZ}	/ZZ = V_{SS} /CE, /WE, /OE ≥ V_{DD} − 0.2V Others ≥ V_{DD} − 0.2V or ≤ 0.2V	—	3.5	10	µA
High Level Input Voltage	V_{IH}	V_{DD} = 1.8V to 3.6V	V_{DD} × 0.8	—	V_{DD} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{DD} = 1.8V to 3.6V	− 0.3	—	V_{DD} × 0.2	V
High Level Output Voltage	V_{OH1}	V_{DD} = 2.5V to 3.6V I_{OH} = − 1.0mA	V_{DD} × 0.8	—	—	V
	V_{OH2}	V_{DD} = 1.8V to 2.5V I_{OH} = − 100µA	V_{DD} − 0.2	—	—	
Low Level Output Voltage	V_{OL1}	V_{DD} = 2.5V to 3.6V I_{OL} = 2.0mA	—	—	0.4	V
	V_{OL2}	V_{DD} = 1.8V to 2.5V I_{OL} = 150µA	—	—	0.2	

*1: During the measurement of I_{DD}, all Address and I/O were taken to only change once per active cycle.
Iout : output current

2. AC Characteristics

▪ AC Test Conditions

Power Supply Voltage	: 1.8 V to 3.6 V
Operation Ambient Temperature	: − 40 °C to + 85 °C
Input Voltage Amplitude	: 0 V / V_{DD}
Input Rising Time	: 3 ns
Input Falling Time	: 3 ns
Input Evaluation Level	: $V_{DD}/2$
Output Evaluation Level	: $V_{DD}/2$
Output Load Capacitance	: 30 pF

(1) Read Cycle

Parameter	Symbol	Value (V_{DD}=1.8V to 2.5V)		Value (V_{DD}=2.5V to 3.6V)		Unit
		Min	Max	Min	Max	
Read Cycle time(/CE control)	t_{RC}	120	—	120	—	ns
Read Cycle time(Address access)	t_{RCA}	135	—	120	—	ns
/CE Access Time	t_{CE}	—	65	—	65	ns
Address Access Time	t_{AA}	—	135	—	120	ns
/CE Output Data Hold time	t_{OH}	0	—	0	—	ns
Address Access Output Data Hold time	t_{OAH}	20	—	20	—	ns
/CE Active Time	t_{CA}	65	—	65	—	ns
Pre-charge Time	t_{PC}	55	—	55	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Hold Time	t_{AH}	65	—	65	—	ns
/CE↑ to Address Transition time*1	t_{CAH}	0	—	0	—	ns
/OE Access Time	t_{OE}	—	35	—	20	ns
/CE Output Floating Time*1	t_{HZ}	—	10	—	10	ns
/OE Output Floating Time	t_{OHZ}	—	10	—	10	ns
Address Transition Time*1	t_{AX}	—	15	—	15	ns

*1: Same parameters with the Write cycle.

(2) Write Cycle

Parameter	Symbol	Value (V_{DD}=1.8V to 2.5V)		Value (V_{DD}=2.5V to 3.6V)		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	120	—	120	—	ns
/CE Active Time	t_{CA}	65	—	65	—	ns
/CE↓ to /WE↑ Time	t_{CW}	65	—	65	—	ns
Pre-charge Time	t_{PC}	55	—	55	—	ns
Write Pulse Width	t_{WP}	20	—	20	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Hold Time	t_{AH}	65	—	65	—	ns
/WE↓ to /CE↑ Time	t_{WLC}	20	—	20	—	ns
Address Transition to /WE↑ Time	t_{AWH}	135	—	120	—	ns
/WE↑ to Address Transition Time	t_{WHA}	0	—	0	—	ns
Data Setup Time	t_{DS}	10	—	10	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
/WE Output Floating Time	t_{WZ}	—	10	—	10	ns
/WE Output Access Time[*1]	t_{WX}	10	—	10	—	ns
Write Setup Time[*1]	t_{WS}	0	—	0	—	ns
Write Hold Time[*1]	t_{WH}	0	—	0	—	ns
/CE Output Floating Time	t_{HZ}	—	10	—	10	ns
Address transition Time	t_{AX}	—	15	—	15	ns

(3) Page Mode Read/Write Cycle

Parameter	Symbol	Value (V_{DD}=1.8V to 2.5V)		Value (V_{DD}=2.5V to 3.6V)		Unit
		Min	Max	Min	Max	
Page Mode Write Cycle Time	t_{PWC}	25	—	25	—	ns
Page Mode Write Pulse Width	t_{WPP}	16	—	16	—	ns
Page Address Setup Time (/WE=L)	t_{ASP}	8	—	8	—	ns
Page Address Hold Time (/WE=L)	t_{AHP}	15	—	15	—	ns
Page Address Access Time	t_{AAP}	—	25	—	25	ns
Page Address Data Hold Time	t_{OHP}	3	—	3	—	ns
Page Mode Read Cycle Time	t_{PRCA}	25	—	25	—	ns
Page Mode Write Pre Charge Width	t_{WPHP}	6	—	6	—	ns

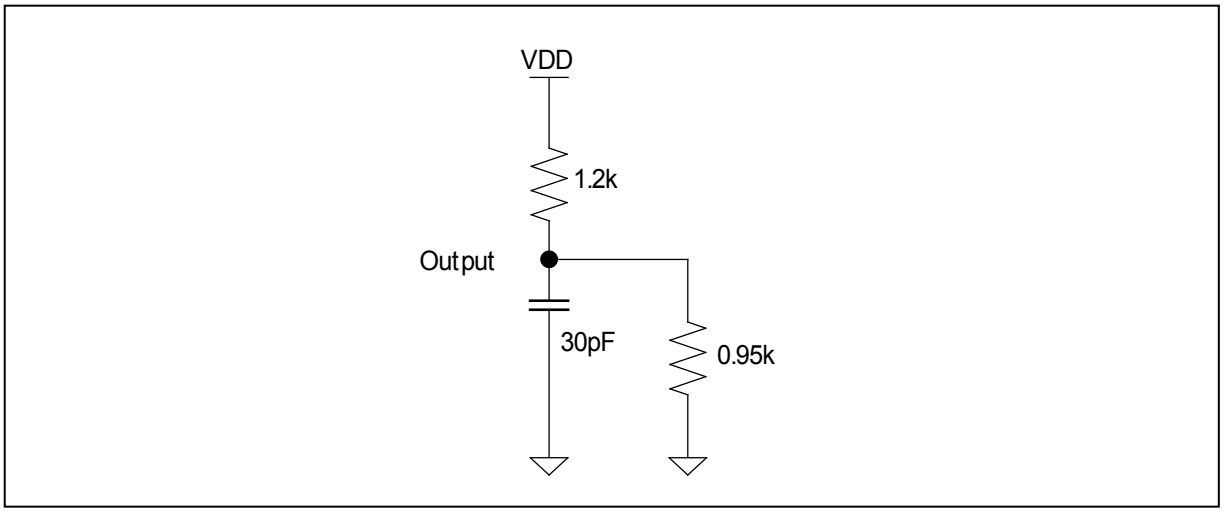
(4) Power ON/OFF Sequence and Sleep Mode Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
/CE level hold time for Power ON	t_{PU}	450	—	µs
/CE level hold time for Power OFF	t_{PD}	85	—	ns
Power supply rising time	t_{VR}	50	—	µs/V
Power supply falling time	t_{VF}	100	—	µs/V
/ZZ active time	t_{ZZL}	1	—	µs
Sleep mode enable time	t_{ZZEN}	—	0	µs
/CE level hold time for Sleep mode release	t_{ZZEX}	450	—	µs

3. Pin Capacitance

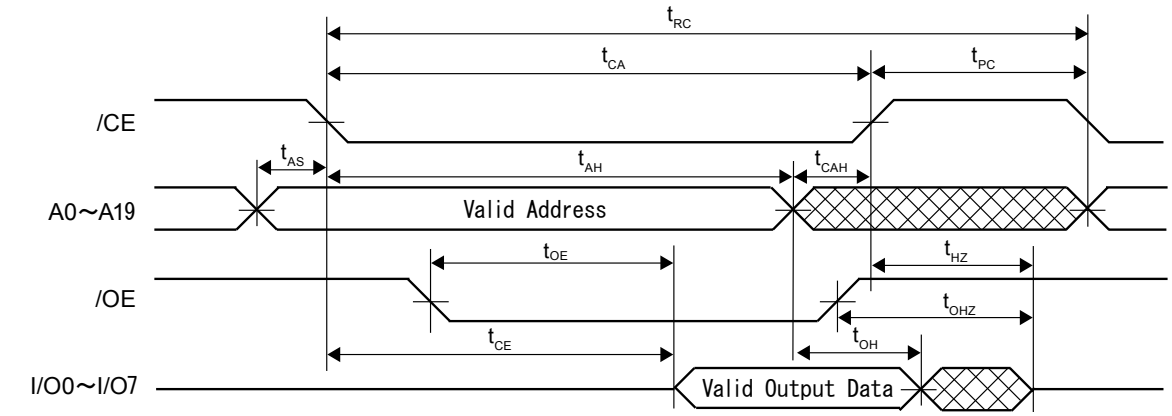
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	V_{DD} = 3.3 V, f = 1 MHz, T_A = + 25 °C	—	—	9	pF
Input/Output Capacitance (I/O pin)	$C_{I/O}$		—	—	9	pF
/ZZ Pin Input Capacitance	C_{ZZ}		—	—	9	pF

■ AC Test Load Circuit



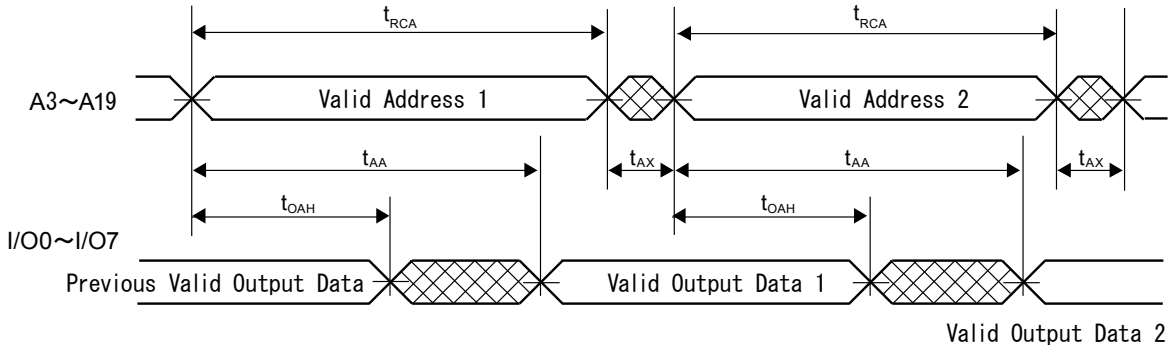
■ TIMING DIAGRAMS

1. Read Cycle Timing 1 (/CE, /OE Control)



XXX : H or L

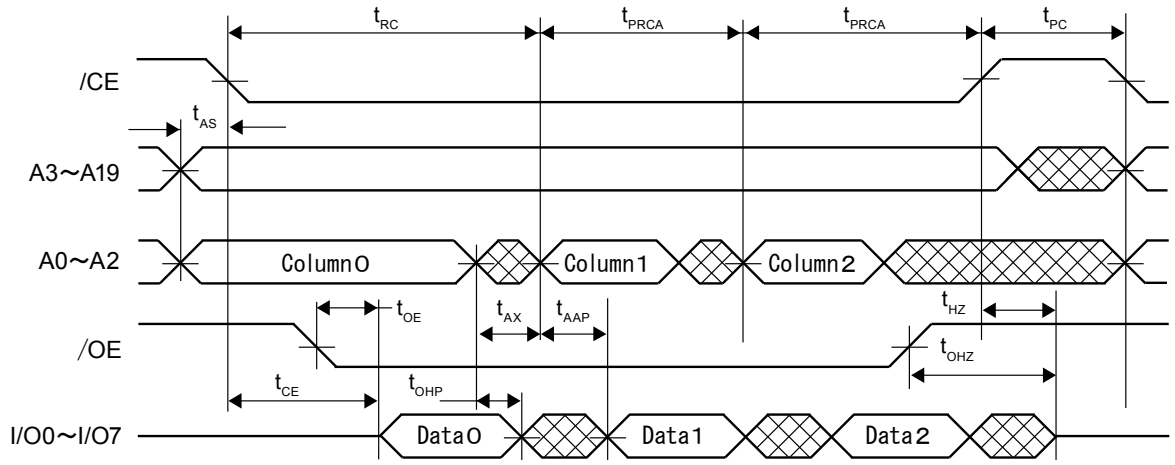
2. Read Cycle Timing 2 (Address Access)



/CE = /OE = L, /WE = H

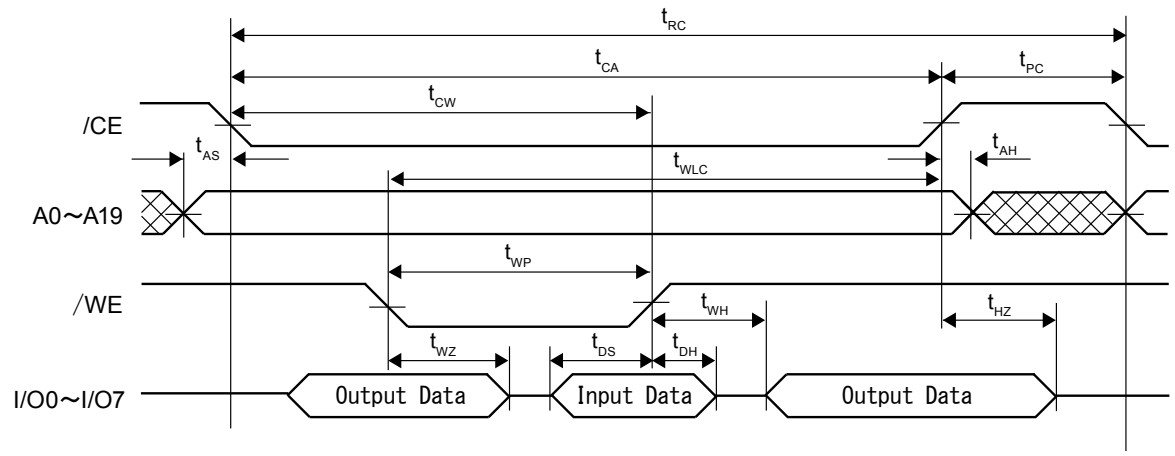
XXX : H or L

3. Read Cycle Timing 3 (Page Access)



XXX : H or L

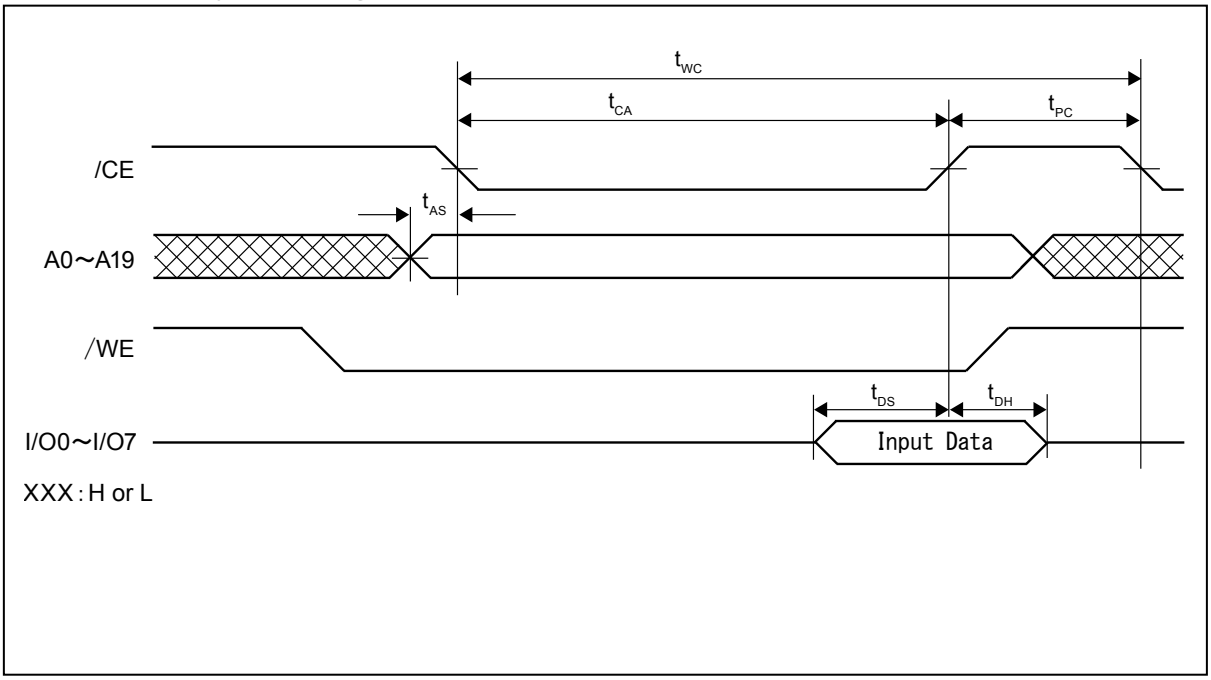
4. Write Cycle Timing 1 (/WE Control)



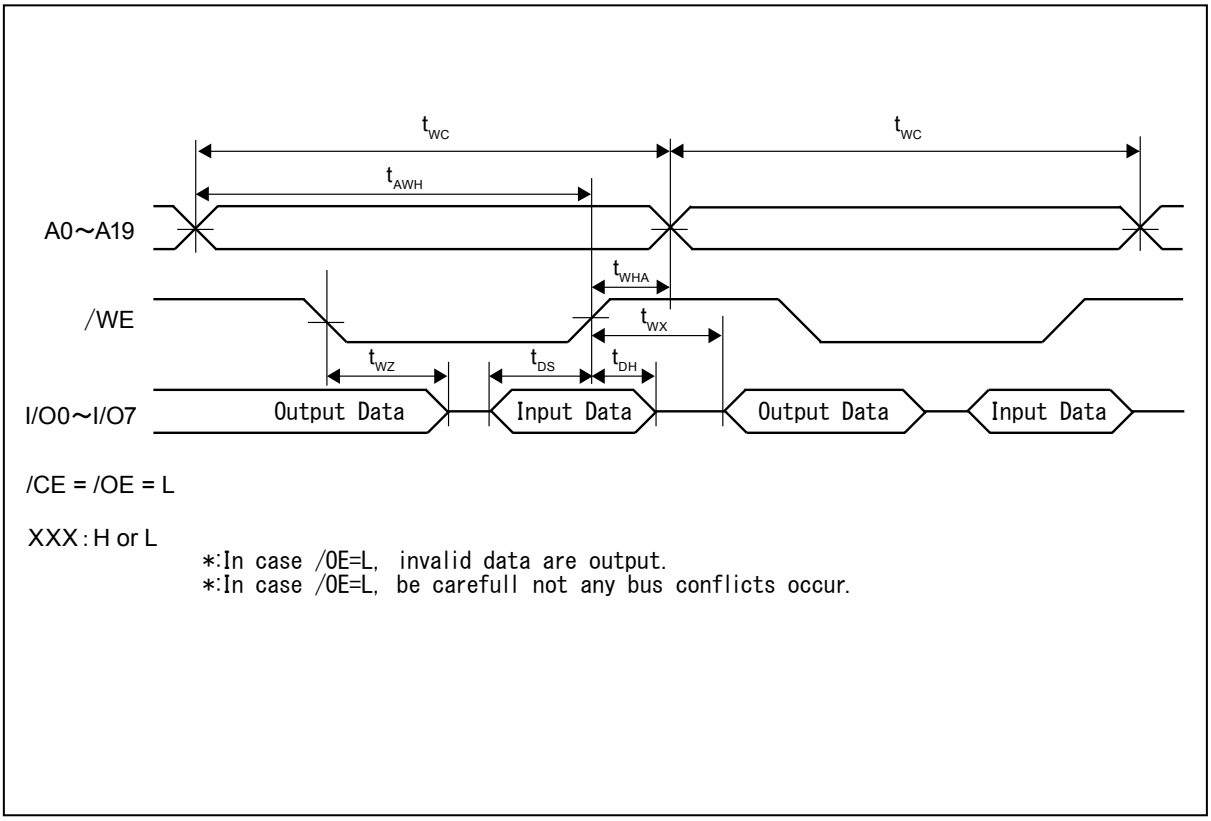
XXX : H or L

*:In case /OE=L, invalid data are output.
*:In case /OE=L, be carefull not any bus conflicts occur.

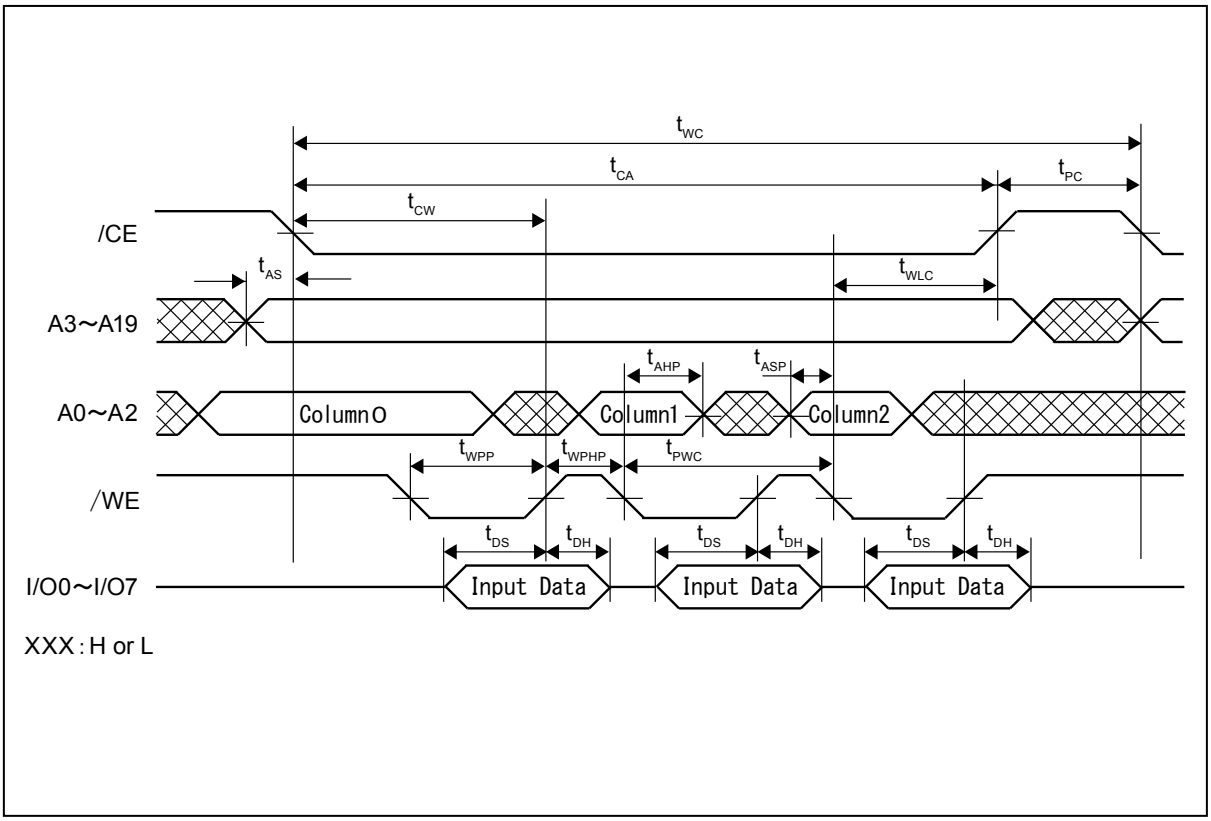
5. Write Cycle Timing 2 (/CE Control)



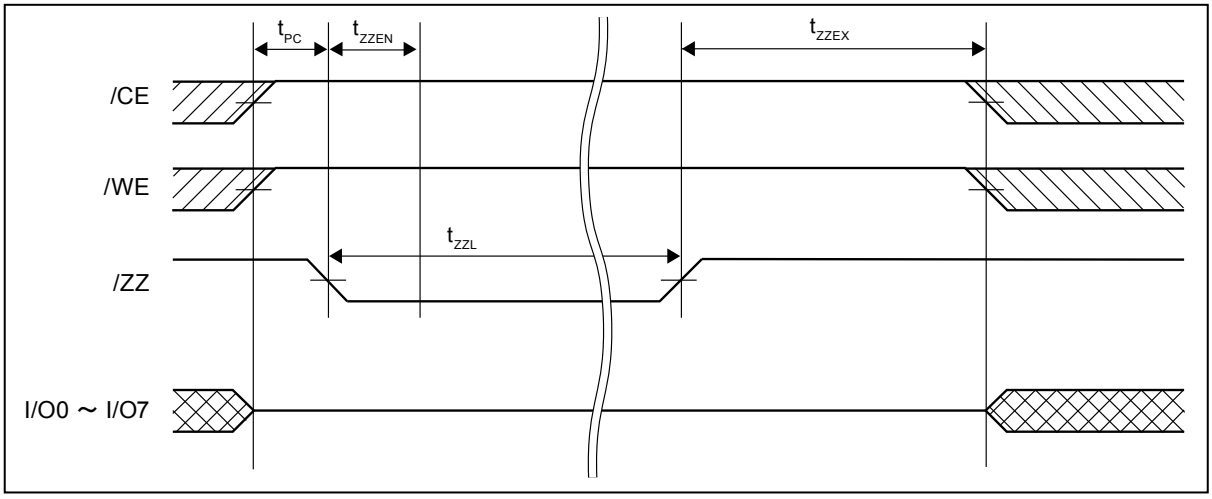
6. Write Cycle Timing 3 (Address Access and /WE Control)



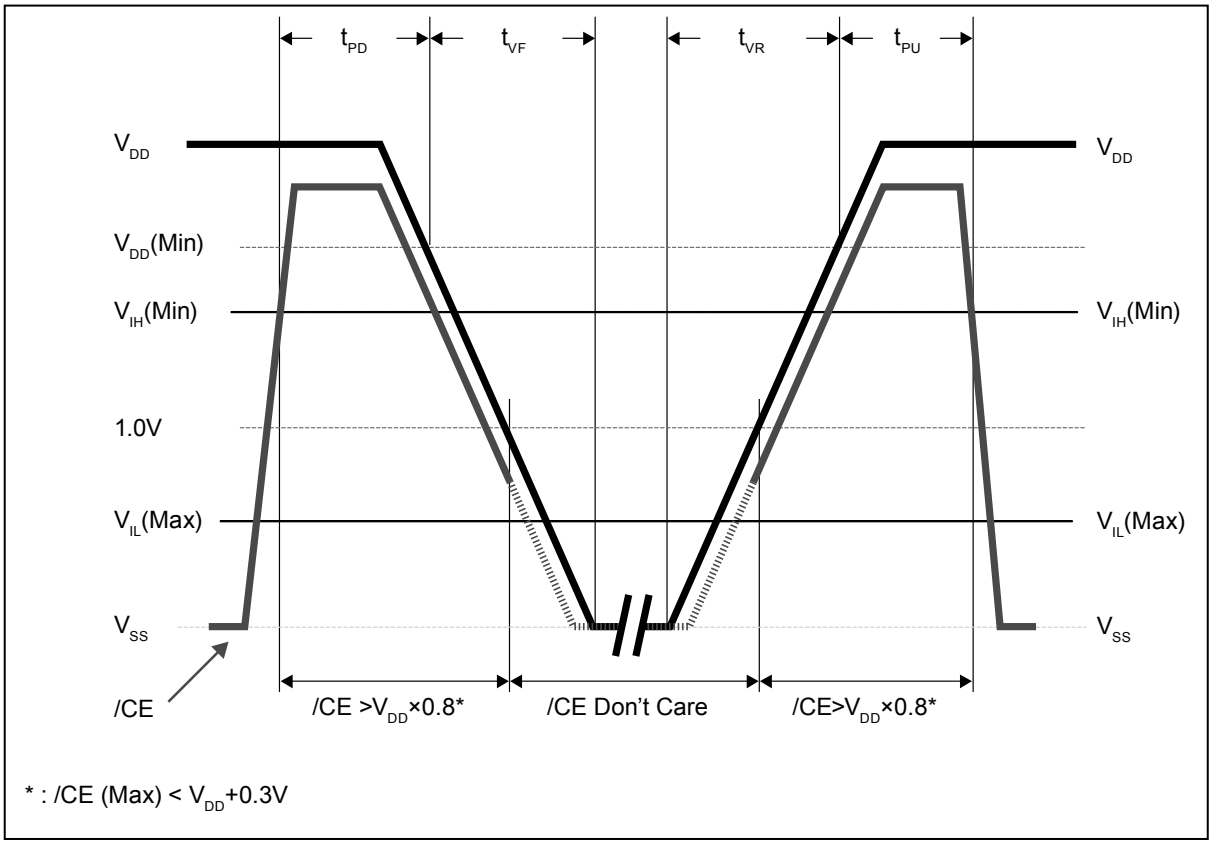
7. Write Cycle Timing 4 (Page Address Access)



8. Sleep Mode Timing



■ POWER ON/OFF SEQUENCE



■ FRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{14}	—	Times/64bits	Operation Ambient Temperature T_A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 85 °C
	95	—		Operation Ambient Temperature T_A = + 55 °C
	≥ 200	—		Operation Ambient Temperature T_A = + 35 °C

*1: Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

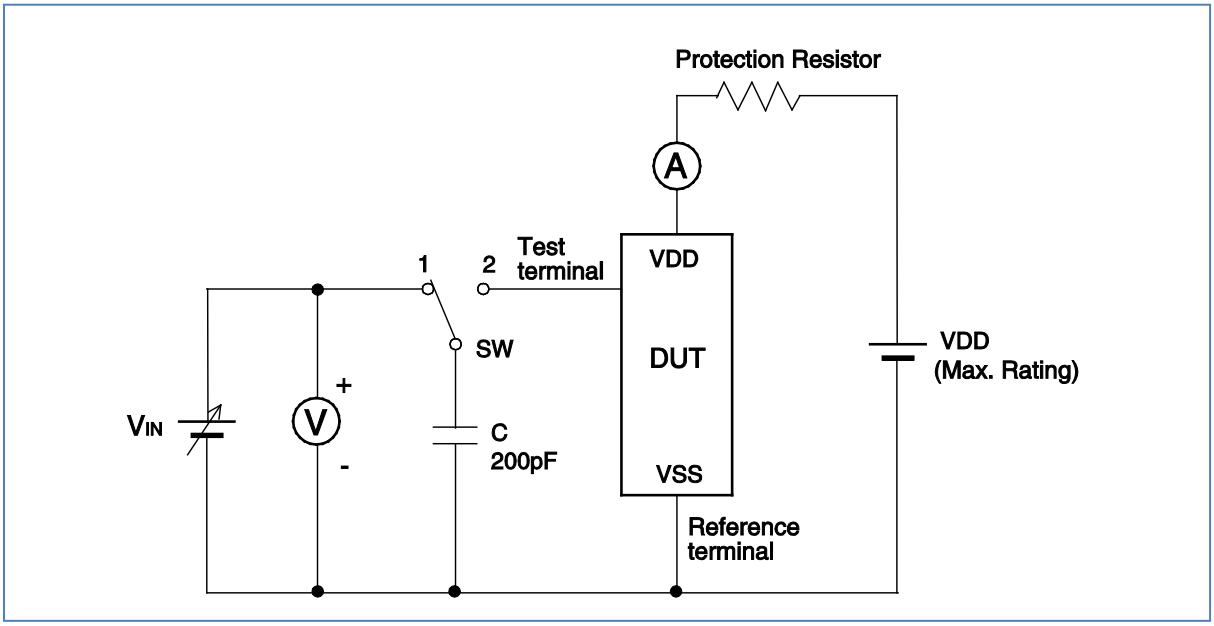
■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85R8M1TAFN-G-JAE2 MB85R8M1TABGL-G-JAE1	≥ |2000 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |1000 V|
Latch-Up (C-V Method) Proprietary method		≥ |200 V|

▪ C-V method of Latch-Up Resistance Test



Note: Charge voltage alternately switching 1 and 2 approximately 2 sec intervals. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

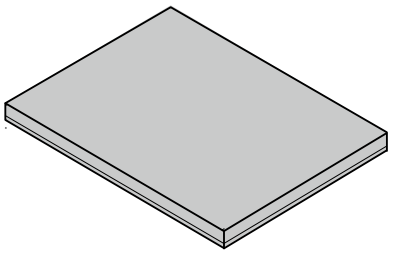
■ ORDERING INFORMATION

Part Number	Package	Shipping form	Minimum shipping quantity
MB85R8M1TAFN-G-JAE2	44-pin plastic TSOP	Tray	—*
MB85R8M1TABGL-G-JAE1	48-pin plastic FBGA	Tray	—*

*: Please contact our sales office about minimum shipping quantity.

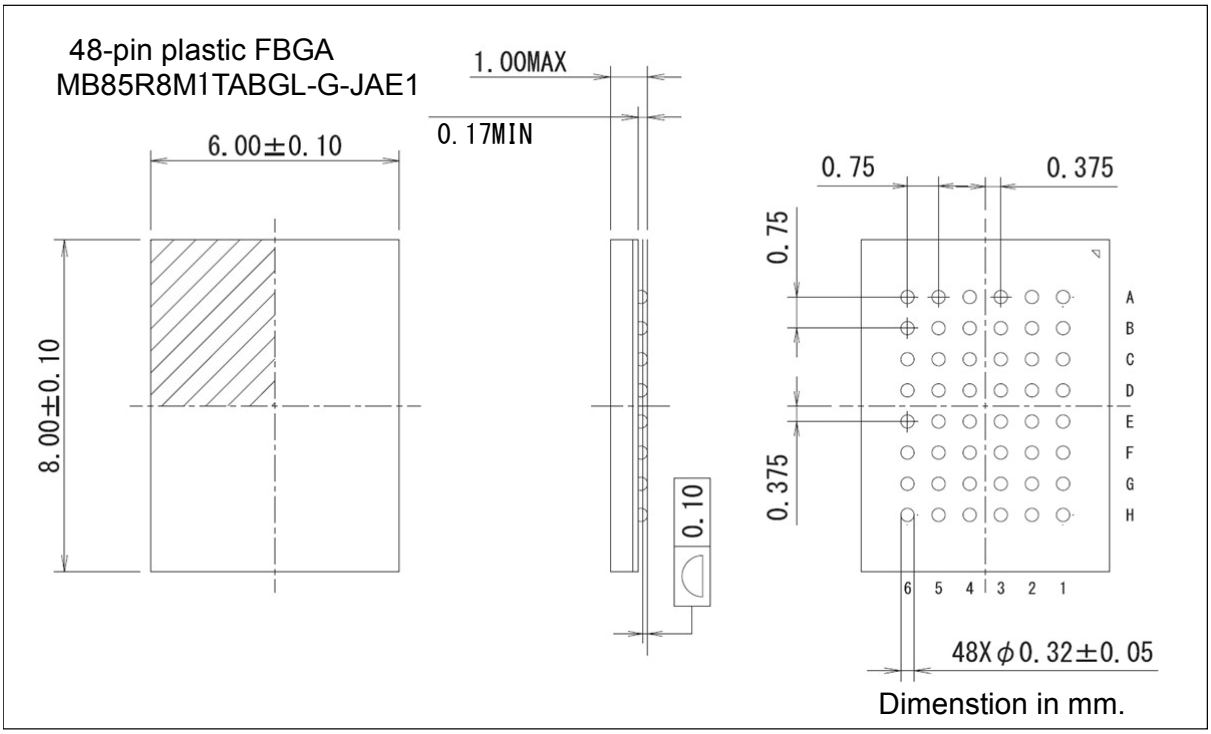
■ PACKAGE DIMENSIONS

48-pin plastic FBGA

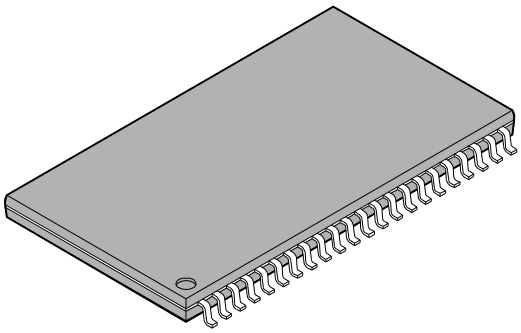


MB85R8M1TABGL-G-JAE1

Lead pitch	0.75mm
Package width× Package length	8.00 mm × 6.00 mm
lead shape	Solder ball
Sealing method	Plastic mold
Mounting hight	1.00 mm (max.)

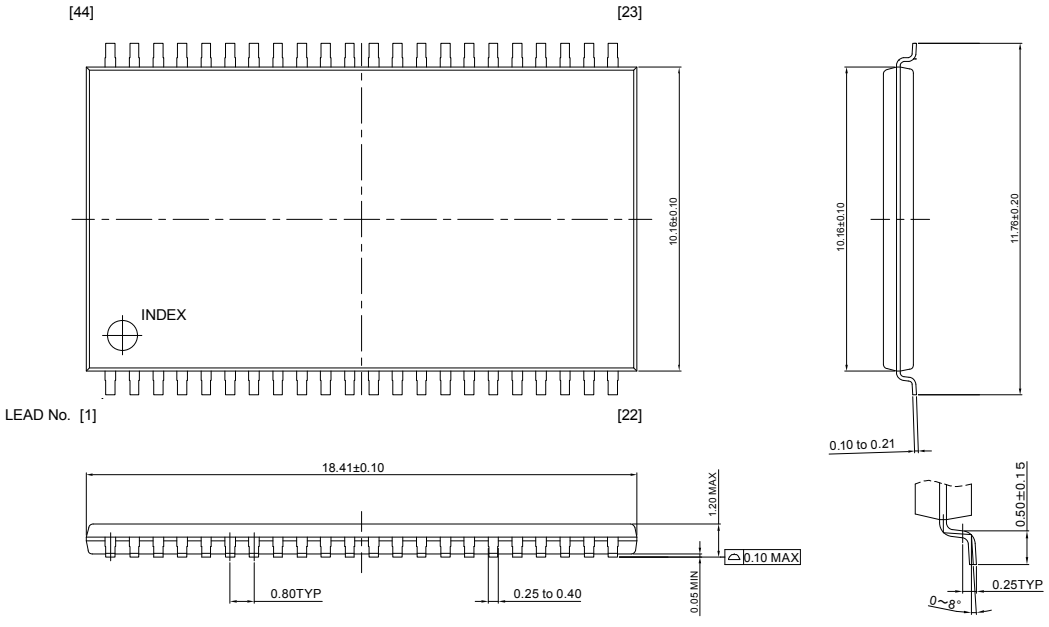


PACKAGE DIMENSIONS(Continued)

44-pin plastic TSOP		
 MB85R8M1TAFN-G-JAE2	Lead pitch	0.8mm
	Package width × package length	10.16 × 18.41mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.2mm (max.)

44-pin plastic TSOP
MB85R8M1TAFN-G-JAE2

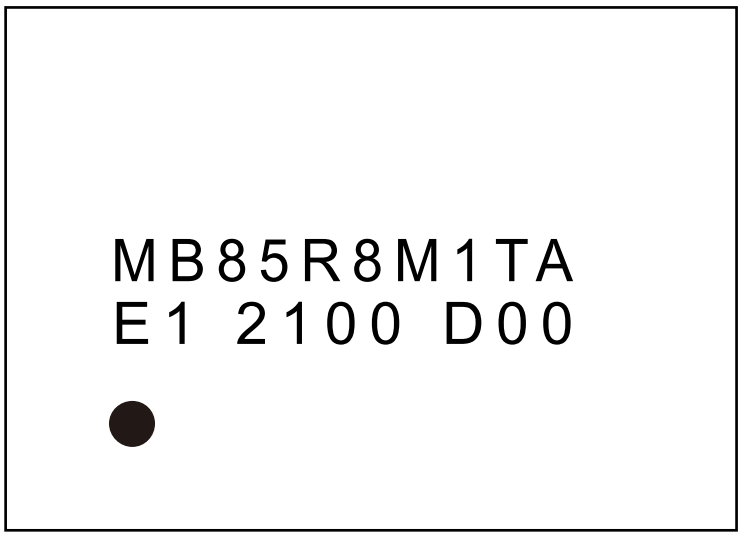
Note 1): These dimensions do not include resin protrusion.
Note 2): Pins width do not include tie bar cutting remainder.
Pins width and pins thickness include plating thickness.



Dimensions in mm.

■ MARKING(Examples)

[MB85R8M1TABGL-G-JAE1]



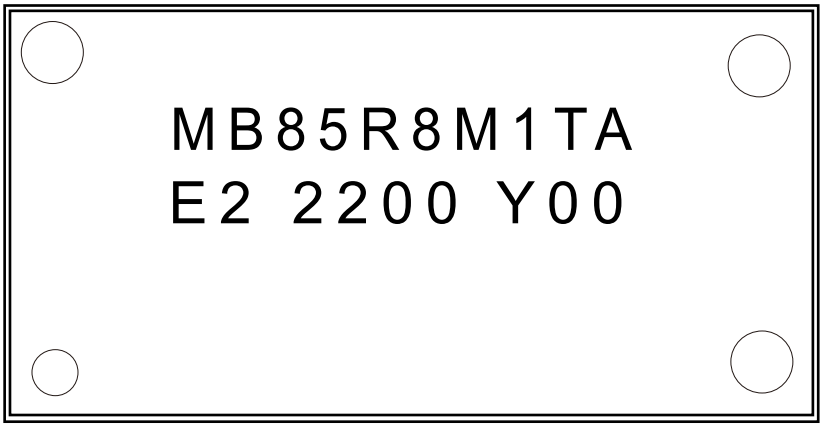
[48-pin Plastic FBGA]

MB85R8M1TA: Product name

E1 : (Lead free code)

2100 D00: 2100(Year and Week code)＋D00（Trace code）

[MB85R8M1TAFN-G-JAE2]



[44pin Plastic TSOP]

MB85R8M1TA: Product name

E2: (Lead free code)

2200 Y00:2200(Year and Week code)＋Y00（Trace code）

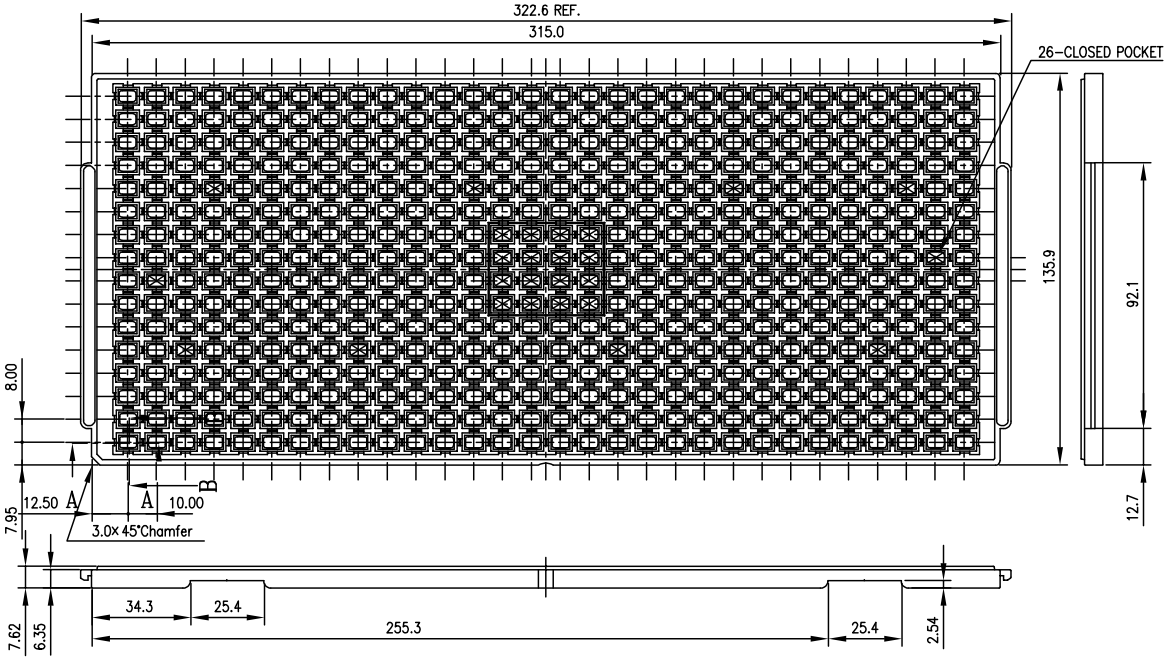
■ PACKING

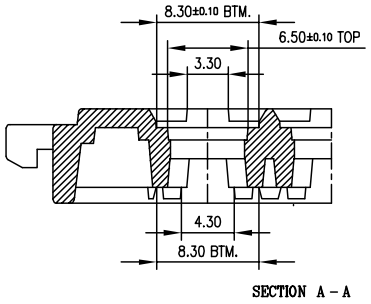
(1)MB85R8M1TABGL-G-JAE1

1.1 Tray dimensions

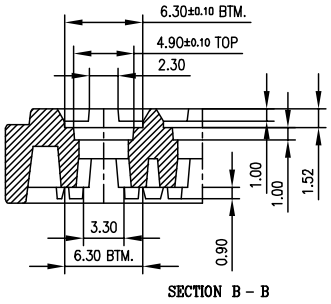
Maximum storage capacity		
pcs/tray	pcs/inner box	pcs/outer box
480	4800 (10trays)	19200 (4 inner boxes, Max)

BGA48





SECTION A – A

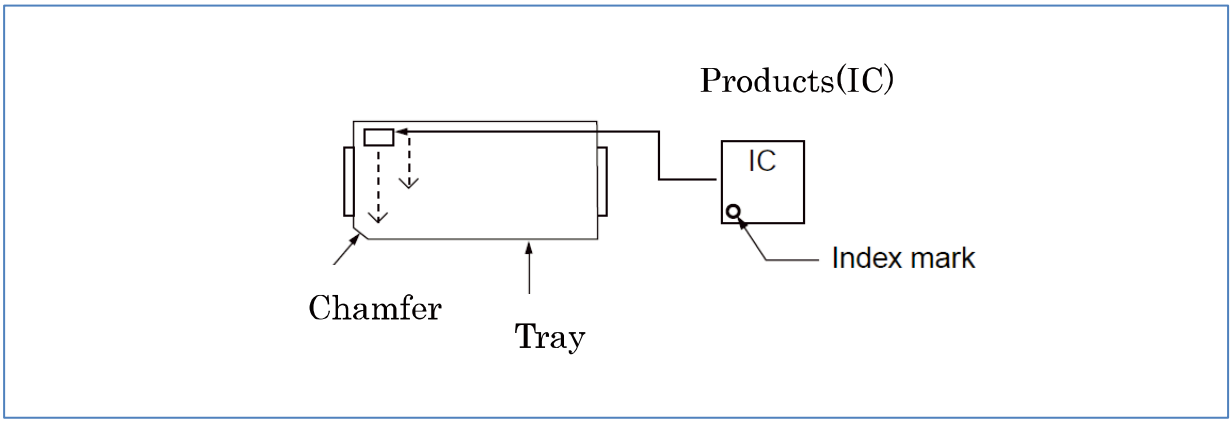


SECTION B – B

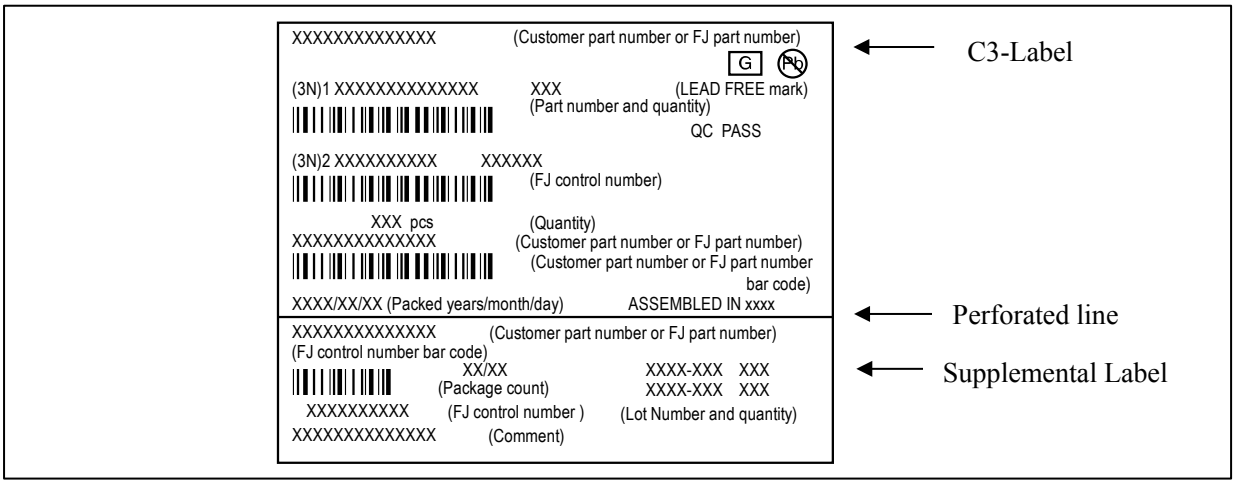
(Dimensions in mm)

Heat proof temperature : 150℃ MAX

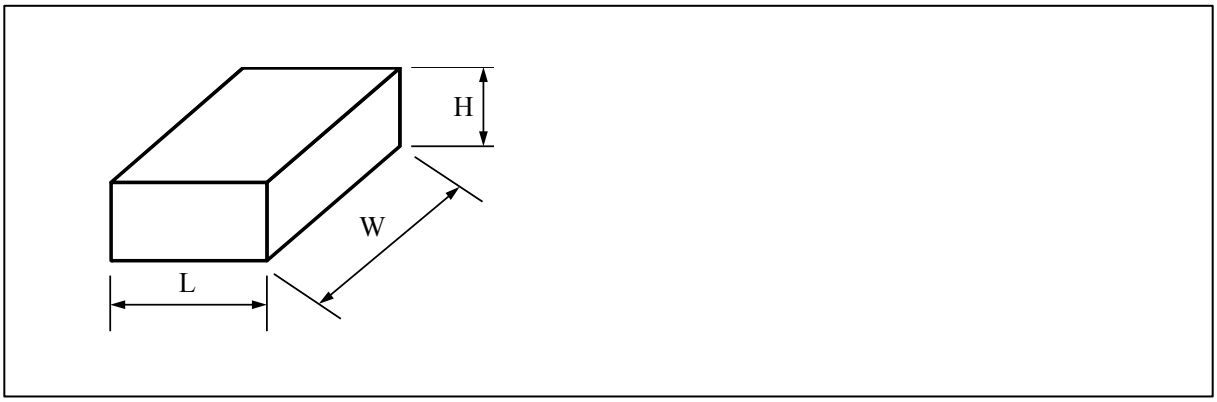
1.2 IC orientation



1.3 Product label indicators
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



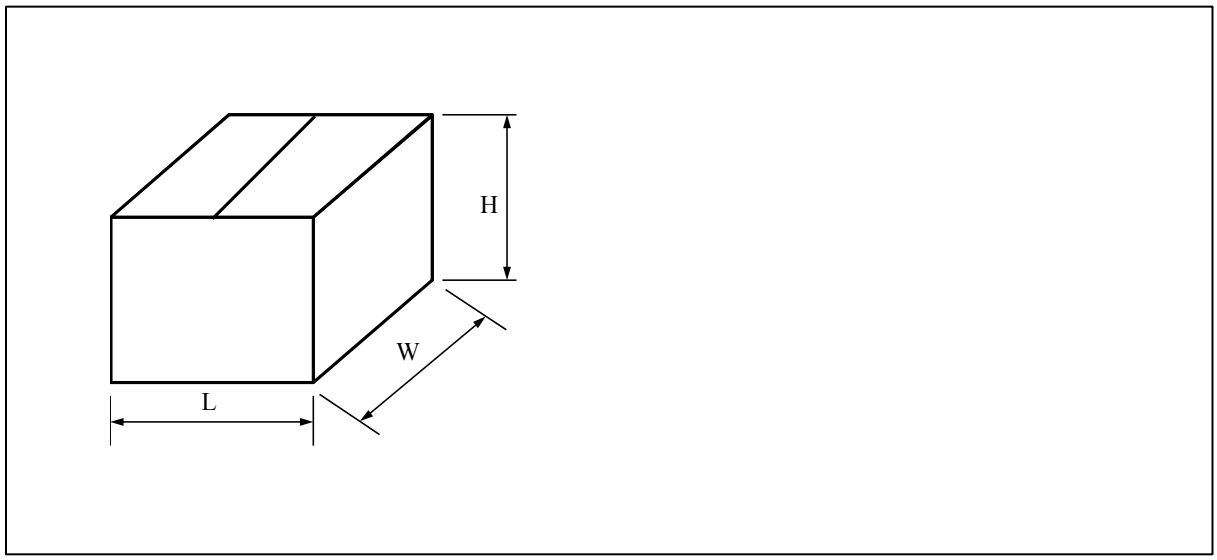
1.4 Dimensions for container
(1) Dimensions for inner box



L	W	H
162	360	90

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
375	410	225

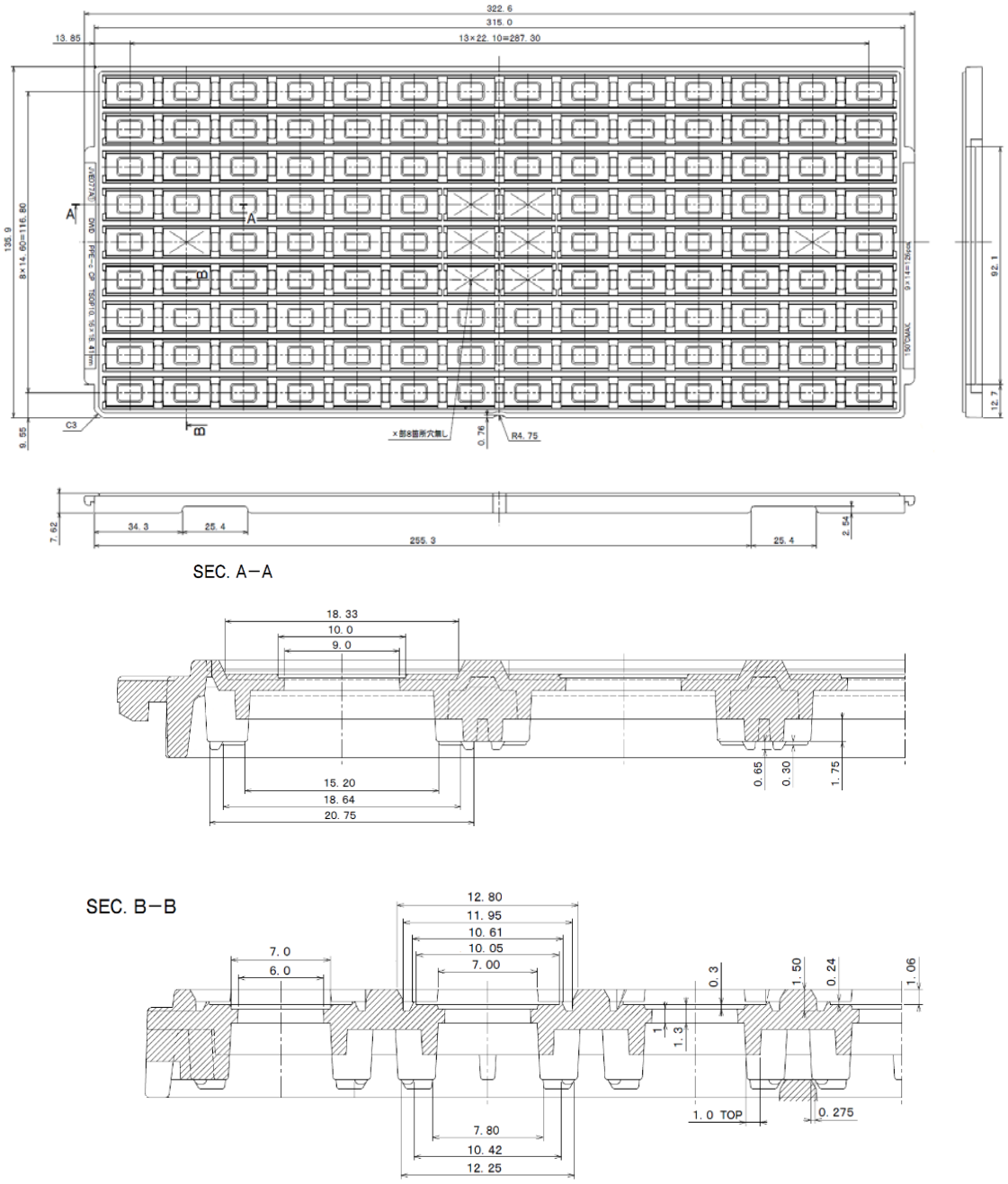
(Dimensions in mm)

(2)MB85R8M1TAFN-G-JAE2

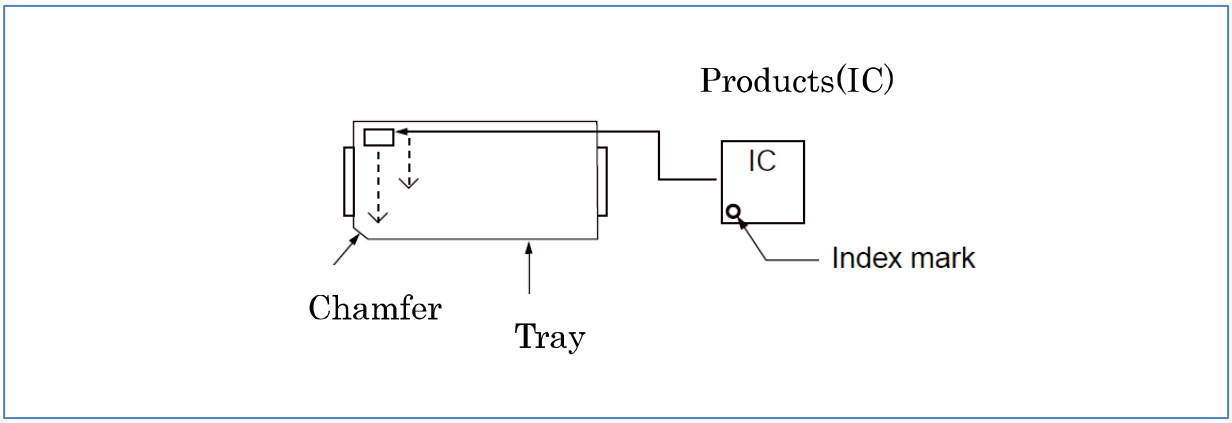
2.1 Tray dimensions

Maximum storage capacity		
pcs/tray	pcs/inner box	pcs/outer box
126	1260 (10trays)	5040 (4 inner boxes, Max)

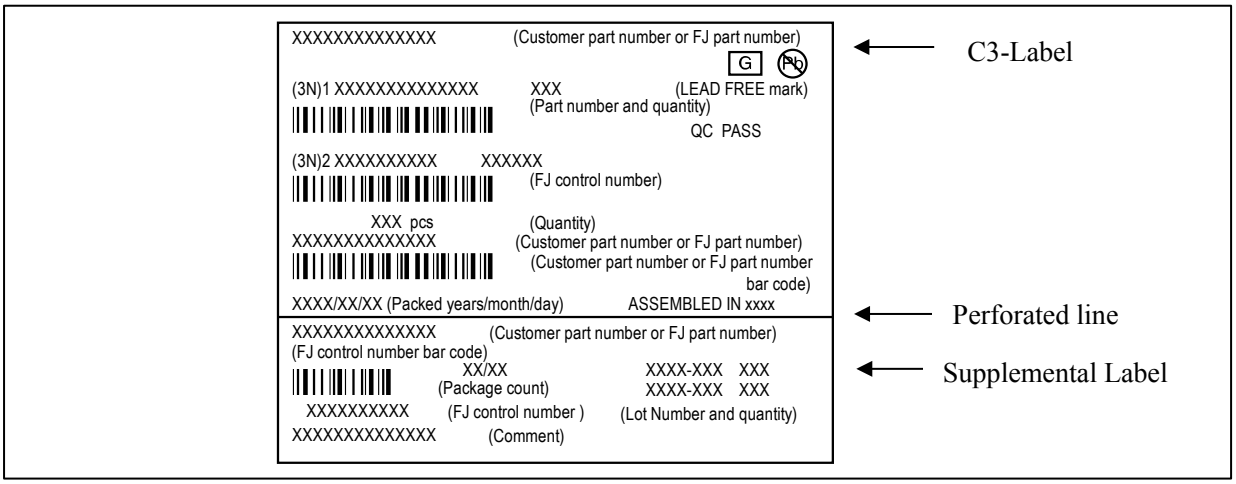
TSOP44



2.2 IC orientation

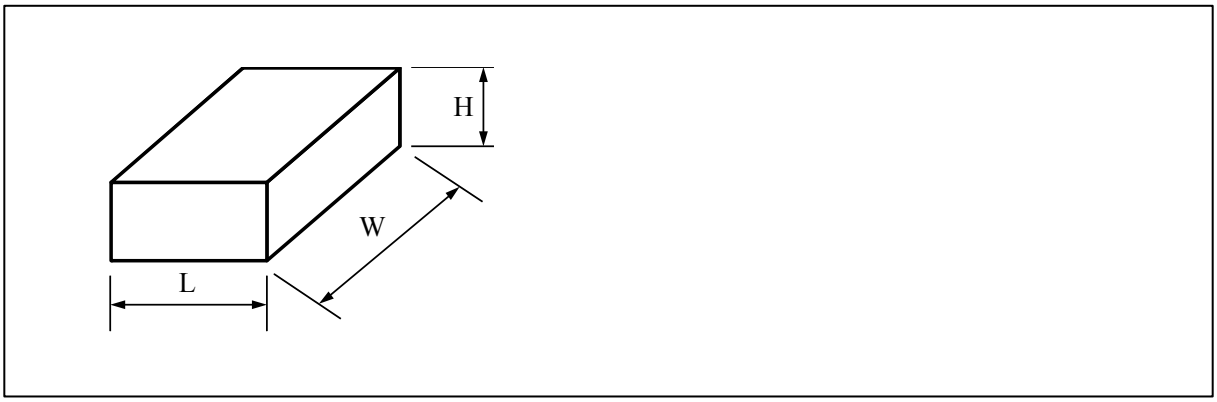


2.3 Product label indicators
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



2.4 Dimensions for container

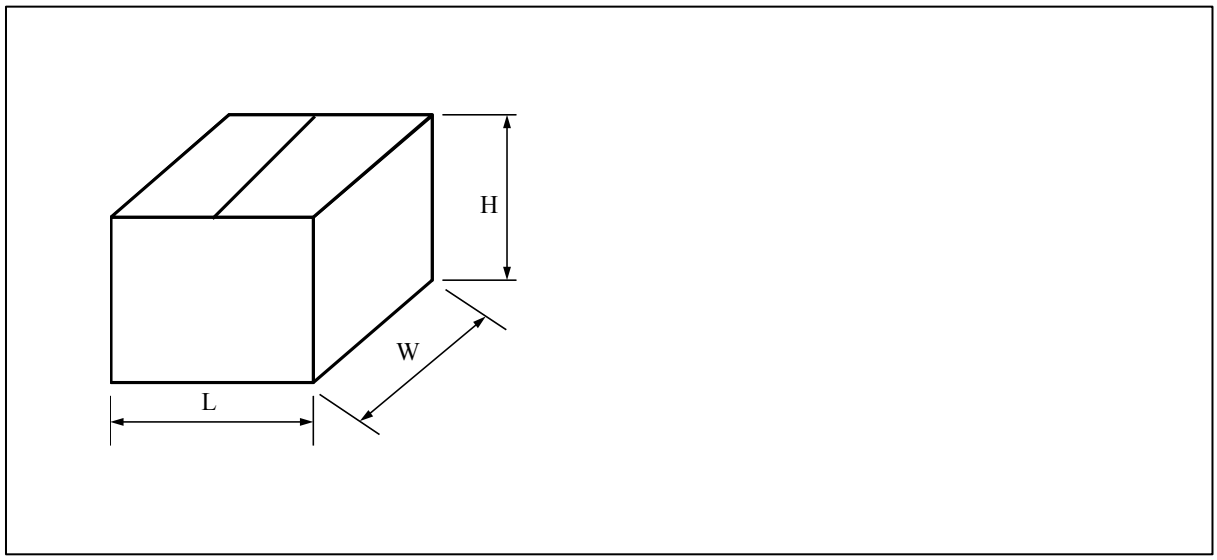
(1) Dimensions for inner box



L	W	H
162	360	90

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
410	375	225

(Dimensions in mm)

FUJITSU SEMICONDUCTOR MEMORY SOLUTION LIMITED

Shin-Yokohama TECH Building, 3-9-1 Shin-Yokohama,
Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan
https://www.fujitsu.com/jp/fsm/en/

Edited: Marketing Division

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Kaga FEI:

MB85R8M1TABGL-G-JAE1 MB85R8M1TAFN-G-JAE2