Highly Versatile Buck-Boost Ambient Energy Manager Battery Charger For Up to 7-cell Solar Panels

Feature

Ultra-low power start-up

- Cold start from 275 mV input voltage and 3 µW input power (typical).

Very efficient energy extraction

- Open-circuit voltage sensing for Maximum Power Point Tracking (MPPT).
- Selectable open-circuit voltage ratios from 60% to 90% or fixed impedance.
- Programmable MPPT sensing period.
- MPPT voltage operation range from 100 mV to 4.5 V.

Adaptive and smart energy management

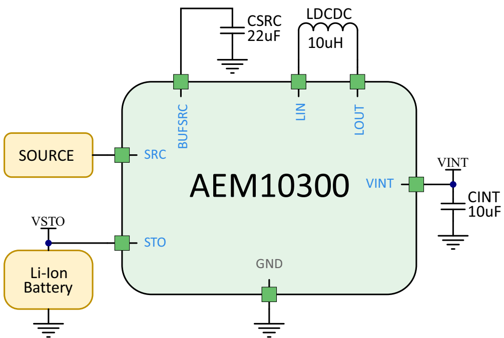
- DCDC switches automatically between boost, buck-boost and buck operation, according to input and output voltages, to maximize energy transfer.

Battery protection features

- Selectable over-charge and over-discharge protection for any type of rechargeable battery or (super-)capacitor.
- Fast super-capacitor charging.
- Dual cell super-capacitor balancing circuit.

Smallest footprint, smallest BOM

- Only three external components are required.
- One 10 µH inductor.
- Two capacitors: one 10 µF and one 22 µF.



Description

The AEM10300 is an integrated energy management circuit that extracts DC power from an ambient energy harvesting source to store energy in a storage element. The AEM10300 allows to extend battery lifetime and ultimately eliminates the primary energy storage element in a large range of applications.

Thanks to its Maximum Power Point Tracking system, the AEM10300 extracts the maximum energy available from the source. It integrates an ultra-low power DCDC converter which operates with input voltages ranging from 100 mV to 4.5 V.

With its unique cold start circuit, the AEM10300 can start harvesting with an input voltage as low as 275 mV and from an input power of 3 µW. The preset protection levels determine the storage element voltages protection thresholds to avoid over-charging and over-discharging the storage element and thus avoiding damaging it. Those are set through configuration pins. Moreover, custom threshold voltages can be obtained at the expense of a few configuration resistors.

The chip integrates all active elements for powering a typical wireless sensor. Only two capacitors and one inductor are required.

Applications

Asset Tracking/Monitoring	Industrial applications
Retail ESL/Smart sensors	Aftermarket automotive
Smart home/Building	

Device Information

Part Number	Package	Body size [mm]
10AEM10300C0000	QFN 28-pin	4x4mm

Evaluation Board

Part Number
2AAEM10300C0010

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1. Introduction

Figure 1: Simplified Schematic View

The AEM10300 is a full-featured energy efficient power management circuit able to harvest energy from an energy source (connected to SRC) to charge a storage element (connected to STO). This is done with a minimal bill of material: only 2 capacitors and one inductor are needed for a basic setup.

The heart of the AEM10300 is a regulated switching DCDC converter with high power conversion efficiency.

At first start-up, as soon as a required cold-start voltage of 275 mV and a sparse amount of power of at least 3 µW is available at the source, the AEM10300 coldstarts. After the cold start, the AEM extracts the power available from the source if the working input voltage is at least 100 mV.

Through four configuration pins (STO_CFG[3:0]), the user can select a specific operating mode out of 15 modes that cover most application requirements without any dedicated external component. Those operating modes define the protection levels of the storage element. If none of those 15 modes fit the user's storage element, a custom mode is also available to allow the user to define a mode with custom specifications.

Status pin ST_STO provides information about the voltage levels of the storage element. ST_STO is HIGH when the voltage of the storage element V_{STO} is above V_{CHRDY} and is reset when the voltage drops below V_{OVDIS}.

The Maximum Power Point (MPP) ratio is configurable thanks to three configuration pins (R_MPP[2:0]) and ensures an optimum biasing of the harvester to maximize power extraction. Depending on the harvester, it is possible to adapt the timings of the MPP evaluations with the two configuration pins (T_MPP[1:0]) that sets the periodicity and the duration of the MPP evaluation.

The AEM10300's DCDC converter can work in two modes: LOW POWER MODE and HIGH POWER MODE, each one of these being optimized for a power range on SRC.

The charging of the storage element can be prevented by pulling EN_STO_CH to GND, typically to protect the storage element if the temperature is too low/high to safely charge it.

2. Pin Configuration and Functions

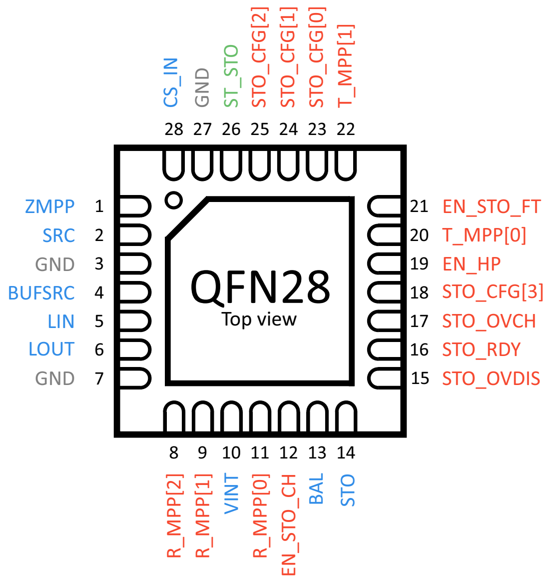

Figure 2: Pinout Diagram QFN 28-pin

NAME	PIN NUMBER	FUNCTION		
Power Pins				
CS_IN	28	Input for the eternal cold start circuit.		
ZMPP	1	Used for the configuration of the ZMPP (optional). Must be left floating if not used.		
SRC	2	Connection to the harvested energy source.		
BUFSRC	4	Connection to an external capacitor buffering the DCDC converter input.		
LIN	5	DCDC inductance connection.		
LOUT	6	DCDC inductance connection.		
VINT	10	Internal voltage supply.		
BAL	13	Connection to mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.		
STO	14	Connection to the energy storage element - battery or (super-)capacitor. Cannot be left floating. Must be connected to a minimum capacitance of 100 µF or to a rechargeable battery.		
Status Pins				
ST_STO	26	Logic Output	HIGH: V_{STO}	HIGH when the storage device voltage V_{STO} rises above V_{CHRDY} threshold. LOW when V_{STO} drops below the V_{OVDIS} threshold.

Table 1: Power and Status Pins

NAME	PIN NUMBER	HIGH LEVEL	FLOATING STATE	FUNCTION
Configuration Pins				
R_MPP[0]	11	V_{VINT}	HIGH	Used for the configuration of the MPP ratio. Read as HIGH when left floating.
R_MPP[1]	9			
R_MPP[2]	8			
T_MPP[0]	20	V_{VINT}	HIGH	Used for the configuration of the MPP timings. Read as HIGH when left floating.
T_MPP[1]	22			
STO_CFG[0]	23	V_{VINT}	HIGH	Used for the configuration of the threshold voltages for the energy storage element V_{OVDIS}, V_{CHRDY} and V_{OVCH}. Read as HIGH when left floating.
STO_CFG[1]	24			
STO_CFG[2]	25			
STO_CFG[3]	18			
STO_OVCH	17	Used for the configuration of the threshold voltages (V_{OVDIS}, V_{CHRDY} and V_{OVCH}) for the energy storage element when STO_CFG[3:0] are set to custom mode (optional). Must be left floating if not used.		
STO_RDY	16			
STO_OVDIS	15			
EN_STO_FT	21	V_{VINT}	HIGH	- Pulled up to VINT or floating: allows charges flowing directly from SRC to STO when SRC is above 5V. - Pulled down to GND: normal operation.
EN_STO_CH	12	V_{LOAD}	HIGH	- Pulled up to LOAD or floating: enables the charging of the battery - Pulled down to GND: disables the charging of the battery
EN_HP	19	V_{VINT}	HIGH	- Pulled up to VINTor floating: HIGH POWER MODE enabled - Pulled down to GND: HIGH POWER MODE disabled
Other				
GND	3, 7, 27 Exposed pad	Ground connection, best possible connection to PCB ground plane.		

Table 2: Configuration and Ground Pins

3. Absolute Maximum Ratings

Parameter	Value
Voltage on STO, SRC, BUFSRC, LIN, LOUT, ZMPP, BAL, CS_IN	-0.3 V to 5.5 V
Voltage on VINT, T_MPP[1:0], R_MPP[2:0], STO_CFG[3:0], STO_OVCH, STO_OVDIS, STO_RDY, EN_HP, EN_STO_CH	-0.3 V to 2.75 V
Operating junction temperature	-40 °C to 125 °C
Storage temperature	-65 °C to 150 °C
ESD HBM voltage	> 2000 V
ESD CDM voltage	> 500 V

Table 3: Absolute Maximum Ratings

4. Thermal Resistance

Package	θJA	θJC	Unit
QFN 28-pin	TBD	TBD	°C/W

Table 4: Thermal Resistance

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper EESD precautions should be taken to avoid performance degradation or loss of functionality

5. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Conversion						
$P_{SRC,CS}$	Source power required for cold start	V_{STO} > Vchrdy		3		µW
		V_{STO} < Vchrdy		6		µW
V_{SRC}	Input voltage of the energy source	During cold start		0.275	4.5	V
		After cold start	0.1		4.5	V
R_{ZMPP}	MPPT ratio	See Table 9	60, 65, 70, 75, 80, 85 or 90, depending on R_MPP[2:0] configuration			%
Timing						
$T_{MPP,EVAL}$	Duration of a MPP evaluation		50% of Table 10		200% of Table 10	ms
$T_{MPP,PERIOD}$	Time between two MPP evaluations		50% of Table 10		200% of Table 10	s
Storage element						
V_{OVCH}	Maximum voltage accepted on the storage element before disabling its charging	see Table 8	Depends on STO_CFG[3:0] configuration			V
V_{CHRDY}	Minimum voltage required on the storage element before asserting the ST_STO	see Table 8	Depends on STO_CFG[3:0] configuration			V
V_{OVDIS}	Minimum voltage accepted on the storage element before reseting ST_STO	see Table 8	Depends on STO_CFG[3:0] configuration			V
Internal supply & Quiescent Current						
V_{VINT}	Internal voltage supply			2.2		V
I_Q	Quiescent current on STO	V_{STO} = 3.7V V_{LOAD} = 2.5V EN_SLEEP = L EN_HP = L		5.9		nA
Symbol	**Logic Level**		LOW		HIGH	
Logic output pins						
ST_STO	Logic output levels on the status STO pin		GND		V_{STO}	

Table 5: Typical Electrical Characteristics

6. Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
External Components					
L_{DCDC}	Inductor of the DCDC converter		10		µH
C_{SRC}	Capacitor decoupling the SRC terminal	13[1]	22		µF
C_{INT}	Capacitor decoupling the VINT terminal	5[1]	10		µF
C_{STO}	Optional - Capacitor on STO if no storage element is connected (see Section 9.8.1)	100[1]			µF
R_{ZMPP}	Optional - Used for the configuration of the ZMPP tracking function	10	Section 9.6	100K	Ω
STO_OVCH	Configuration of V_{OVCH} in custom mode	1	Section 9.3	100	MΩ
STO_OVDIS	Configuration of V_{OVDIS} in custom mode				
STO_RDY	Configuration of V_{CHRDY} in custom mode				
Symbol	Logic Level	LOW		HIGH	
Logic input pins					
R_MPP[2:0]	Configuration pins for the MPP evaluation	GND		VINT	
T_MPP[1:0]	Configuration pins for the MPP timing	GND		VINT	
STO_CFG[3:0]	Configuration pins for the STO voltage	GND		VINT	
EN_STO_FT	Configuration pin for the controller	GND		VINT	
EN_STO_CH	Configuration pin for the controller	GND		VINT	
EN_HP	Configuration pin for the controller	GND		VINT	

Table 6: Recommended Operation Conditions

1.Consider all component tolerance and deratings. Typically, DC-bias derating has a major impact on capacitance on ceramic capacitors.

7. Functional Block Diagram

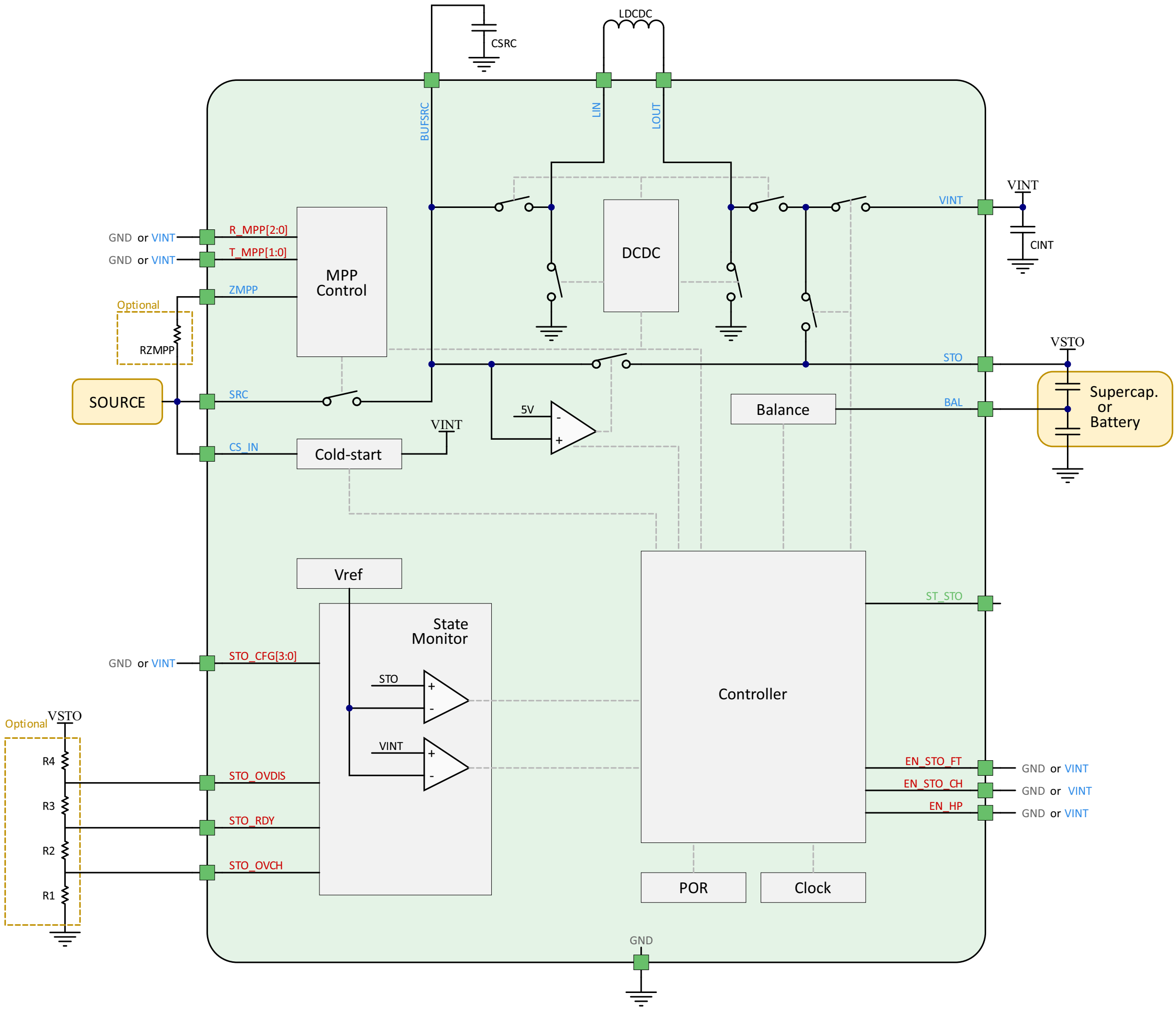

Figure 3: Functional Block Diagram

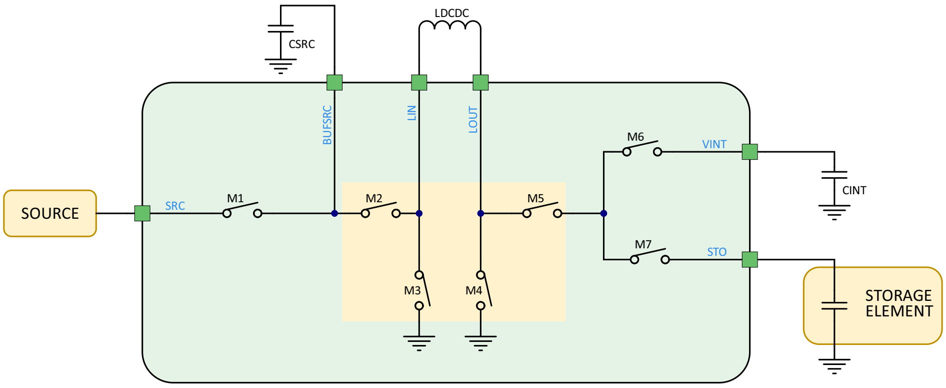

Figure 4: Simplified Schematic View of the AEM10300

8. Theory of Operation

8.1. DCDC Converter

The DCDC converter converts the voltage available at BUFSRC to a level suitable for charging the storage element STO or to regulate the internal supply VINT. The switching transistors of the DCDC converter are M2, M3, M4 and M5. Thanks to M6 and M7, the controller selects between VINT and STO respectively as the converter output. STO is selected as an output only when VINT does not need to be supplied.

The reactive power component of this converter is the external inductor L_{DCDC}. Periodically, the MPP control circuit disconnects the source from the BUFSRC pin with the transistor M1 in order to let the harvester on SRC rise to its open-circuit voltage V_{OC} and measure it. This is done to define the optimal voltage level V_{MPP}, which is determined by applying the MPP ratio on V_{OC}. BUFSRC is decoupled by the capacitor C_{SRC}, which smooths the voltage against the current pulses pulled by the DCDC converter. The storage element is connected to the STO pin.

Depending on its input voltage and its output voltage, the DCDC converter will work as a boost converter, a buck converter or a buck-boost converter. The maximum power that can be harvested and supplied to the output depends on the power mode (HIGH POWER MODE or LOW POWER MODE), which is configured through the EN_HP pin (see Section 9.1).

DCDC Converter Mode	Input Voltage / Output Voltage
Boost	$V_{IN} < V_{OUT}$ - 250 mV
Buck	$V_{IN} > V_{OUT}$ + 250 mV
Buck - Boost	V_{OUT} - 250 mV < V_{IN} < V_{OUT} + 250 mV

Table 7: DCDC Converter Modes

8.2. Cold-Start Circuit

The AEM10300 is able to coldstart if the voltage on CS_IN is above 0.275 V. The minimum available power is:

- 3 µW if V_{STO} is above V_{CHRDY}.
- 6 µW if V_{STO} is below V_{CHRDY}.

CS_IN is typically connected to SRC to allow the AEM10300 to coldstart from the energy available on the harvester. Nevertheless, any other energy source can be connected to CS_IN as long as it meets the electrical specifications constraints described in Sections 5 and 6.

8.3. AEM10300 States Description

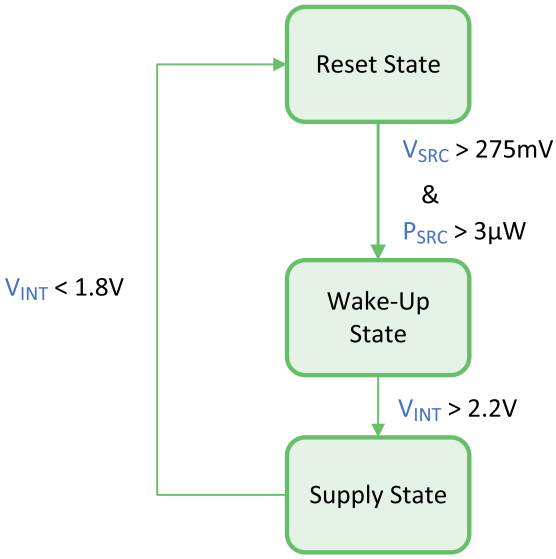

Figure 5: Diagram of the AEM10300 States

8.3.1. Reset and Wake Up States

The RESET STATE is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold start voltage of 275 mV and a sparse amount of power of just 3 µW become available on CS_IN (usually connected to SRC), the AEM10300 switches to WAKE-UP STATE, and energy is extracted from SRC to make V_{VINT} rise to 2.2 V. When V_{VINT} reaches those 2.2 V, the AEM10300 switches to SUPPLY STATE.

8.3.2. Supply State

In SUPPLY STATE, three scenarios are possible:

- There is enough power provided by the source (SRC) to keep V_{VINT} at 2.2 V. The excessive power is used to charge the storage element on STO. In that case, the circuit remains in SUPPLY STATE. If STO is fully charged, the DCDC converter is disabled to prevent over-charging the storage element, and the SRC pin is set to high impedance.
- Due to a lack of power from the source, V_{STO} falls below V_{OVDIS}. In this case, the circuit enters RESET STATE as explained in Section 8.3.1.
- There is no power on SRC. It is therefore not possible to maintain VINT to 2.2 V. In this case, the circuit enters in RESET STATE.

The AEM10300 internal circuit current consumption causes C_{INT} to discharge. When the voltage on VINT falls below its 2.2 V regulation set point, the DCDC converter switches its output to recharge C_{INT} from SRC, thus keeping VINT regulated. If no sufficient power is available on SRC to keep VINT regulated, the AEM10300 switches to RESET STATE.

8.4. Maximum Power Point Tracking

During SUPPLY STATE, the voltage on SRC is regulated by an internal Maximum Power Point Tracking (MPPT) module. The MPPT module evaluates V_{MPP}, the voltage at which the source provides the highest possible power, as a given fraction of the open-circuit voltage of the source V_{OC}. This ratio is set by the R_MPP[2:0] terminals according to Table 9. The sampling period and duration are set according to Table 10 by the T_MPP[1:0] terminals. The AEM10300 supports any V_{MPP} levels in the range from 100 mV to 4.5 V. It offers a choice of seven values for the V_{MPP} / V_{OC} fraction. It can also match the input impedance of the DCDC converter with an impedance connected to the ZMPP terminal as explain as explained in section 9.6.

8.5. Balancing for Dual-Cell Supercapacitor

The balancing circuit allows the user to balance the internal voltage of the dual-cell supercapacitor connected to STO in order to avoid damaging the supercapacitor because of excessive voltage on one cell.

If BAL is connected to GND, the balancing circuit is disabled. This configuration must be used if a battery, a capacitor or a single-cell supercapacitor is connected on STO.

If BAL is connected to the node between both cells of a supercapacitor, the balancing circuit compensates for any mismatch of the two cells that could lead to the over-charge of one of two cells. The balancing circuit ensures that BAL remains close to V_{STO} / 2. This configuration must be used if a dual-cell supercapacitor is connected to STO, and that this supercapacitor requires cells balancing.

The balancing circuit works as follows, with V_{BAL} the voltage on the BAL pin:

- $V_{BAL} > \frac{V_{STO}}{2}$: the AEM10300 enables a switch between BAL and GND to discharge the bottom supercapacitor cell to GND (up to 20 mA).
- $V_{BAL} < \frac{V_{STO}}{2}$: the AEM10300 enables a switch between STO and BAL to discharge the top supercapacitor cell to the bottom supercapacitor cell (up to 20 mA).

NOTE: the balancing feature is optimized for supercapacitors, for use with other storage elements (batteries, etc.), please contact e-peas support.

9. System Configuration

9.1. High Power / Low Power Mode

When EN_HP is pulled to VINT, the DCDC converter is configured to HIGH POWER MODE. This allows higher currents to be extracted from the DCDC converter input (SRC) to the DCDC converter output (STO).

9.2. Storage Element Configuration

Through four configuration pins (STO_CFG[3:0]), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 8. The three threshold levels are defined as:

- V_{OVCH}: maximum voltage accepted on the storage element before disabling its charging.
- V_{CHRDY}: minimum voltage required on the storage element before ST_STO is HIGH.
- V_{OVDIS}: minimum voltage accepted on the storage element before setting ST_STO LOW.

Configuration pins				Storage element threshold voltages			Typical use
STO_CFG[3:0]				V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
L	L	L	L	3.00 V	3.50 V	4.05 V	$LiCoO_2$ battery, Li-Po battery, Lithium Titanate (3.8 V) battery (long life).
L	L	L	H	2.80 V	3.10 V	3.60 V	$LiFePO_4$ battery, Lithium capacitor (LiC).
L	L	H	L	1.85 V	2.40 V	2.70 V	Dual-cell NiMH battery, Lithium-Titanate (2.4V) battery.
L	L	H	H	0.20 V	1.00 V	4.65 V	Dual-cell supercapacitor.
L	H	L	L	0.20 V	1.00 V	2.60 V	Single-cell supercapacitor.
L	H	L	H	1.00 V	1.20 V	2.95 V	Single-cell supercapacitor.
L	H	H	L	1.85 V	2.30 V	2.60 V	Lithium-Titanate battery (2.4V).
L	H	H	H	Custom Mode (single-cell NiMH battery, LiC, etc.)[1].			
H	L	L	L	1.10 V	1.25 V	1.50 V	Ni-Cd single-cell battery.
H	L	L	H	2.20 V	2.50 V	3.00 V	Ni-Cd dual-cell battery.
H	L	H	L	1.45 V	2.00 V	4.65 V	Dual-cell supercapacitor.
H	L	H	H	1.00 V	1.20 V	2.60 V	Single-cell supercapacitor.
H	H	L	L	2.00 V	2.30 V	2.60 V	Solid State battery.
H	H	L	H	3.00 V	3.50 V	4.35 V	$LiCoO_2$ battery, Li-Po battery, Lithium Titanate (3.8 V) battery.
H	H	H	L	2.60 V	2.70 V	4.00 V	Tadiran TLI.
H	H	H	H	2.60 V	3.50 V	3.90 V	Tadiran HLC.

Table 8: Storage Element Configuration Pins

1. An example of a single-cell NiMH batteries optimized custom mode setting can be found at Section 10.2.

9.3. Custom Mode Configuration

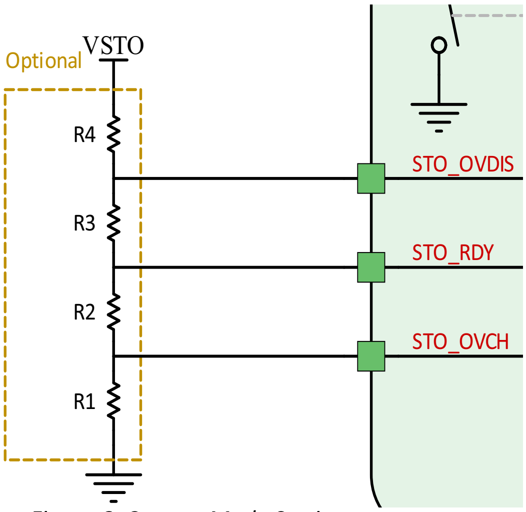

Figure 6: Custom Mode Settings

When STO_CFG[3:0] = LHHH, the custom mode is selected and all four configuration resistors must be wired as shown in Figure 6.

V_{OVCH}, V_{CHRDY} and, V_{OVDIS} are defined thanks to R1, R2, R3 and R4, which can be determined within the following constraints:

- $R_T = R_1 + R_2 + R_3 + R_4$
- $1M\Omega \leq R_T \leq 100M\Omega$
- $R_1 = R_T \cdot \frac{1V}{V_{OVCH}}$
- $R_2 = R_T \cdot \left(\frac{1V}{V_{CHRDY}} - \frac{1V}{V_{OVCH}}\right)$
- $R_3 = R_T \cdot \left(\frac{1V}{V_{OVDIS}} - \frac{1V}{V_{CHRDY}}\right)$
- $R_4 = R_T \cdot \left(1 - \frac{1V}{V_{OVDIS}}\right)$

The resistors should have high values to make the additional power consumption negligible. Moreover, the following constraints must be respected to ensure the functionality of the chip:

- $V_{CHRDY} + 0.05V \leq V_{OVCH} \leq 4.5V$
- $V_{OVDIS} + 0.05V \leq V_{CHRDY} \leq V_{OVCH} - 0.05V$
- $1V \leq V_{OVDIS}$

9.4. Disable Storage Element Charging

Pulling down EN_STO_CH pin to GND disables the charging of the storage element connected to STO. This can be done for example to protect the storage element when the system detects that the environment temperature is too low or too high to safely charge the storage element.

While EN_STO_CH is pulled down, VINT can still be supplied from SRC.

To enable charging the storage element on STO, EN_STO_CH must be pulled up to VINT or left floating (pin is pulled up internally).

9.5. MPPT Configuration

The MPPT module is configured through the following pins:

- R_MPP[2:0] allows for configuring the V_{MPP} / V_{OC} tracking ratio, that has to be chosen according to the characteristics of the source. Please note that if the selected mode is ZMPP, an external resistor must be added to the circuit as explained in Section 9.6.
- T_MPP[1:0] allows for configuring the duration of an MPP evaluation and the time between two MPP evaluations.

Configuration pins			MPPT ratio
R_MPP[2:0]			V_{MPP} / V_{OC}
L	L	L	60%
L	L	H	65%
L	H	L	70%
L	H	H	75%
H	L	L	80%
H	L	H	85%
H	H	L	90%
H	H	H	ZMPP

Table 9: MPP Ratio Configuration Pins

Configuration pins		MPPT timing	
T_MPP[1:0]		Sampling duration	Sampling period
L	L	5.19 ms	280 ms
L	H	70.8 ms	4.5 s
H	L	280 ms	17.9 s
H	H	1.12 s	71.7 s

Table 10: MPP Timing Configuration Pins

9.6. ZMPP Configuration

Instead of working at a ratio of the open-circuit voltage, the AEM10300 can regulate the input impedance of the DCDC converter so that it matches a constant impedance R_{ZMPP} connected to the ZMPP pin. In this case, the AEM10300 regulates V_{SRC} at a voltage that is the product of the ZMPP resistance R_{ZMPP} and the current available at the SRC input.

- $10\ \Omega \leq R_{ZMPP} \leq 100\ K\Omega$

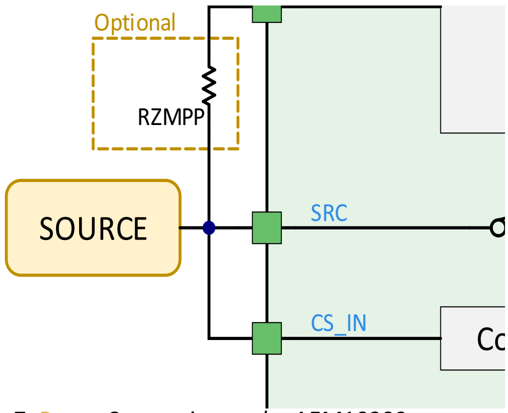

Figure 7: R_{ZMPP} Connection to the AEM10300

9.7. Source to Storage Element Feed-Through

When the harvester connected to SRC delivers a high amount of power, the AEM might not be able to pull enough current to regulate V_{SRC} to the MPP voltage. The voltage on SRC thus increases, eventually above 5V. To maximize the energy extracted in that case, the AEM30330 can be configured to create a direct feed-through current path from SRC to STO when V_{SRC} is above 5V. This is measured when the AEM is pulling current from the source (not during an MPP evaluation).

If the MPPT module detects that V_{SRC} is higher than 4 V and EN_STO_FT is set, the SRC is monitored. From that moment, if the AEM10300 detects that V_{SRC} rises above 5 V and if the storage element is not fully charged, the switch between the SRC and STO pins is closed until V_{SRC} drops below 5 V or until the storage element is fully charged.

This feature is enabled by pulling up EN_STO_FT pin to VINT. However, it is disabled if the storage element is fully charged, or when a MPP evaluation is occurring. Therefore the circuit must still be protected from any overshoot voltage on SRC above 5.5 V, for instance by a zener diode.

9.8. External Components

Refer to Figure 15 to have an illustration of the external components wiring.

9.8.1. Storage Element Information

The energy storage element of the AEM10300 can be a rechargeable battery, a supercapacitor or a capacitor. The size of the storage element must be determined so that its voltage does not fall below V_{OVDIS} even during current peaks pulled by the application. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to decouple the battery with a capacitor.

If the application expects a disconnection of the battery (e.g. because of a user removable connector), the PCB should include a capacitor C_{STO} of at least 100 µF connected between STO and GND. The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the whole subsystem.

9.8.2. External Inductor Information

The AEM10300 operates with one standard miniature inductor. L_{DCDC} must sustain a peak current of at least 1 A and a switching frequency of at least 10 MHz. Low equivalent series resistance (ESR) favors the power conversion efficiency of the DCDC converter. The recommended value is 10 µH.

9.8.3. External Capacitors Information

9.8.3.1. C_{SRC}

This capacitor acts as an energy buffer at the input of the DCDC converter. It prevents large voltage fluctuations when the DCDC converter is switching. The recommended nominal value is 22 µF.

9.8.3.2. C_{INT}

This capacitor acts as an energy buffer for the internal voltage supply. The recommended nominal value is 10 µF.

10. Typical Application Circuits

10.1. Example Circuit 1

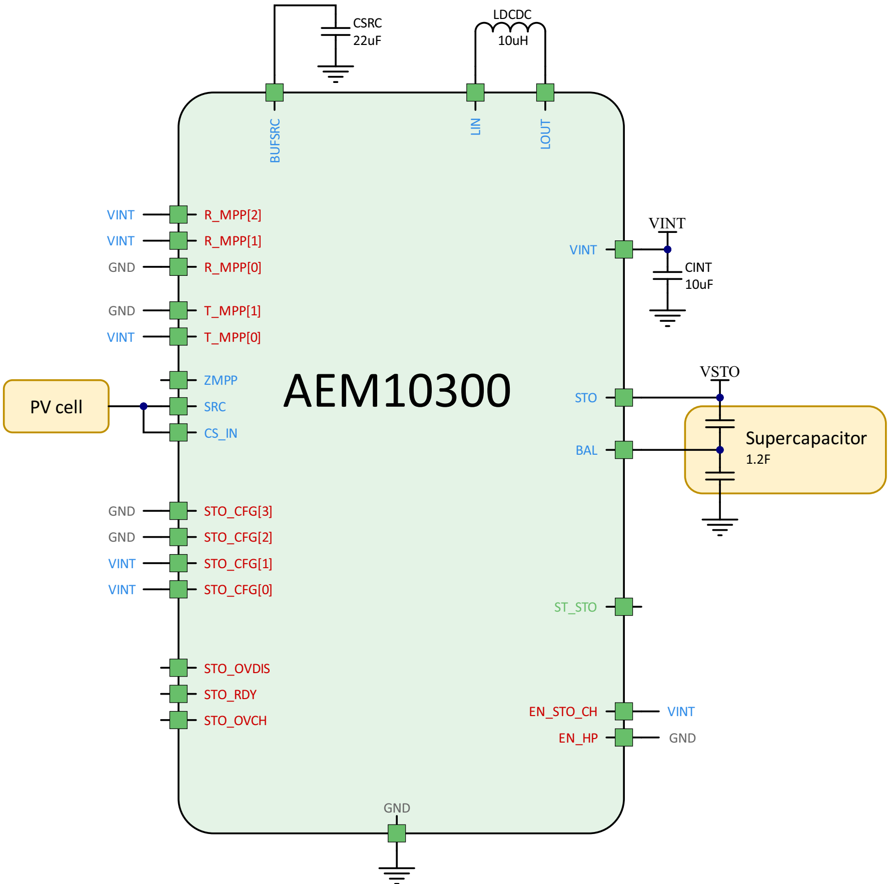

Figure 8: Typical Application Circuit 1

The circuit is an example of a system with solar energy harvesting. It uses a pre-defined operating mode that uses standard components, and a supercapacitor as energy storage.

- Energy source: PV cell.
- R_MPP[2:0] = HHL: the MPP tracker ratio is set to 90%.
- T_MPP[1:0] = LH: the MPP sampling period is 4.5 s and the MPP sampling duration is 70.8 ms.
- STO_CFG[3:0] = LLHH: the storage element is a dual-cell supercapacitor, with:
  - V_{OVCH} = 4.65 V
  - V_{CHRDY} = 1.00 V
  - V_{OVDIS} = 0.20 V
- The balancing pin of the dual-cell supercapacitor is connected to BAL.
- EN_STO_CH is connected to VINT: the charging of the storage element on STO is enabled.
- EN_HP is connected to GND: the DCDC converter is in LOW POWER MODE.
- EN_STO_FT is connected to VINT: SRC to STO feed-through is enabled when V_{SRC} is above 5 V.

10.2. Example Circuit 2

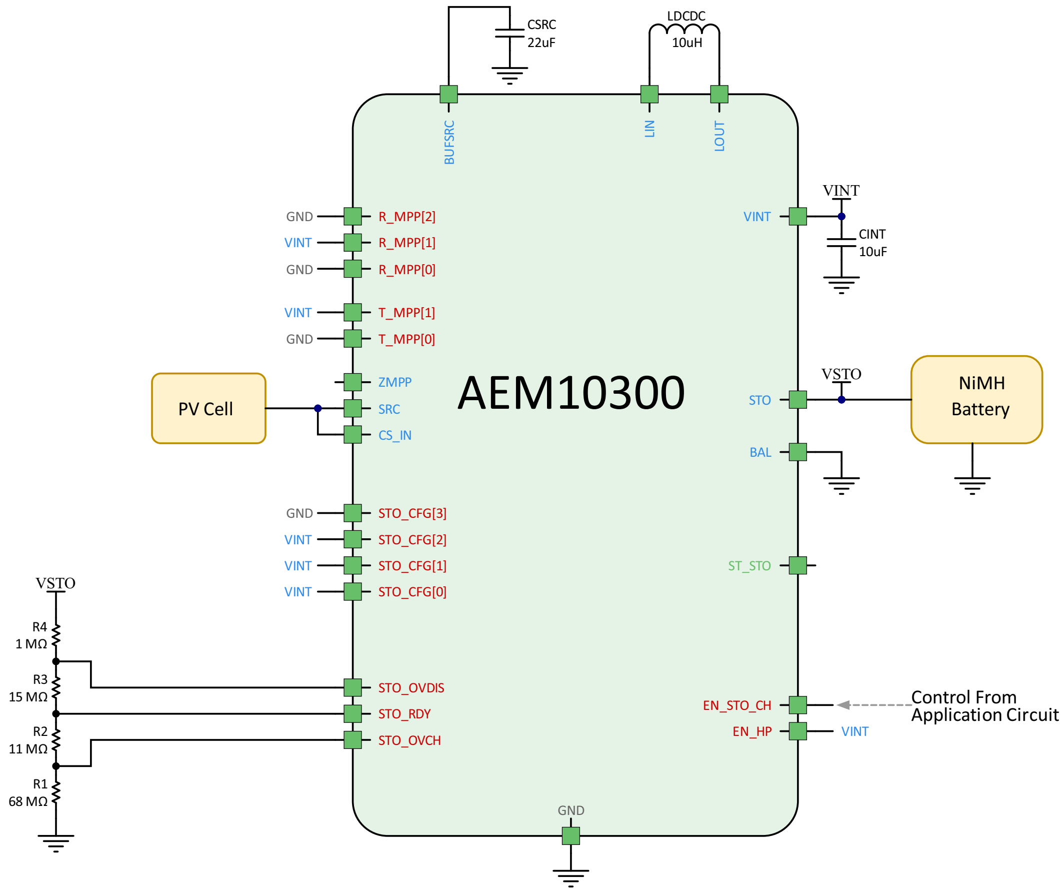

Figure 9: Typical Application Circuit 2

The circuit is an example of a system with solar energy harvesting. It uses a rechargeable NiMH battery as storage element. The voltage thresholds are set by the custom mode.

- Energy source: PV cell.
- R_MPP[2:0] = LHL: the MPP ratio is set to 70%.
- T_MPP[1:0] = HL: the MPP sampling period is 17.9 s and the MPP sampling duration is 280 ms.
- STO_CFG[3:0] = LHHH: the storage element is a NiMH rechargeable battery, used with custom mode:
  - V_{OVDIS} = 1.00 V
  - V_{CHRDY} = 1.20 V
  - V_{OVCH} = 1.40 V
- Custom mode resistor divider calculations (values have been chosen to match E24 series value):
  - $R_T = 95 M\Omega$
  - $R_1 = R_T \cdot \frac{1V}{V_{OVCH}} \approx 68 M\Omega$
  - $R_2 = R_T \cdot \left(\frac{1V}{V_{CHRDY}} - \frac{1V}{V_{OVCH}}\right) \approx 11 M\Omega$
  - $R_3 = R_T \cdot \left(\frac{1V}{V_{OVDIS}} - \frac{1V}{V_{CHRDY}}\right) \approx 15 M\Omega$
  - $R_4 = R_T \cdot \left(1 - \frac{1V}{V_{OVDIS}}\right) \approx 1 M\Omega$
- BAL is not used (not a dual-cell storage element) so it is connected to GND.
- EN_STO_CH: the charging of the storage element present on STO is controlled by the application circuit, typically by a micro-controller GPIO output.
- EN_HP is connected to VINT: the DCDC converter is in HIGH POWER MODE.
- EN_STO_FT is connected to VINT: SRC to STO feed-through is enabled when V_{SRC} is above 5 V.

NOTE: for LiC (Lithium-ion Capacitor) storage elements, or others that would not be covered by STO_CFG[3:0] presets, please apply the same equations as in the above example to determine custom mode resistors values. E24 series values for typical storage elements can be found in the AEM10300 Configuration Tool spreadsheet, to be downloaded on e-peas website.

11. Circuit Behavior

11.1. Wake-up state and Supply state

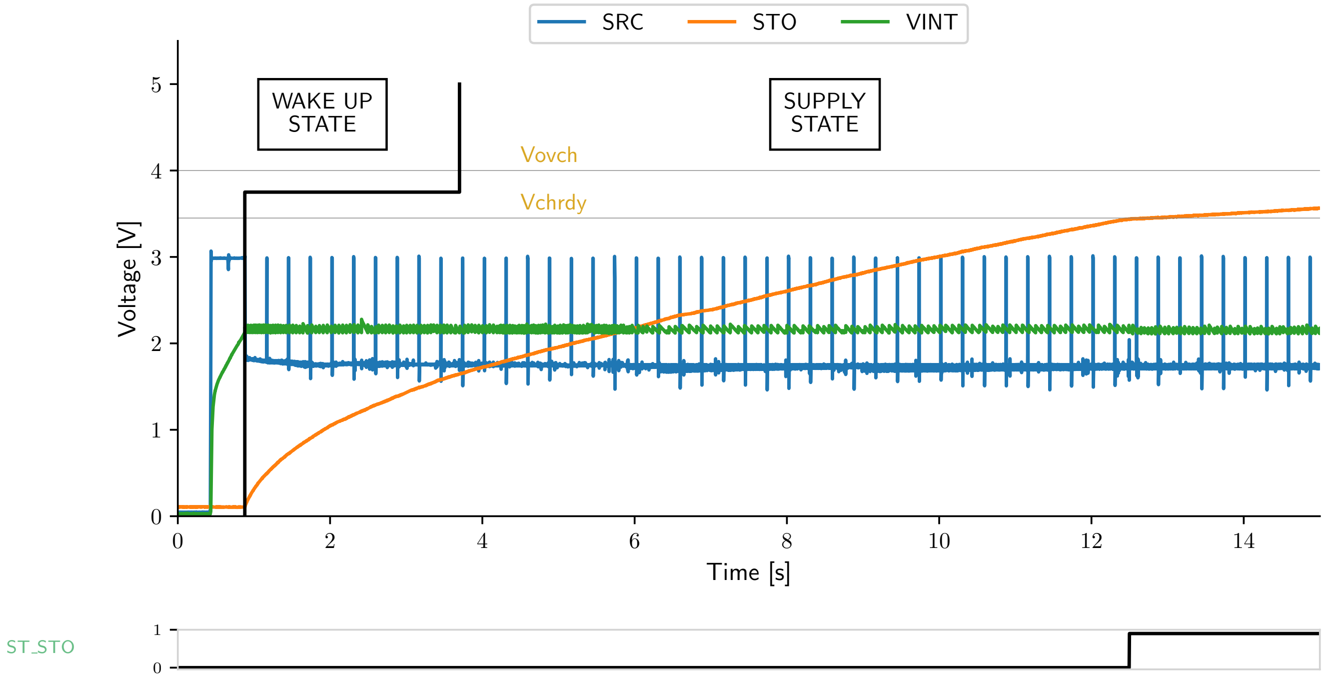

Figure 10: Wake-up state and Supply state

- STO_CFG[3:0] = LLLL
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.50 V
  - V_{OVCH} = 4.05 V
- R_MPP[2:0] = LLL (60%)
- T_MPP[1:0] = LL (5.19 ms / 280 ms)
- C_{STO} = 10 mF
- SRC: 5 mA current source with 3 V voltage compliance
- EN_HP = H (high power mode)
- EN_STO_CH = H (storage element charge enabled)

11.2. Supply state

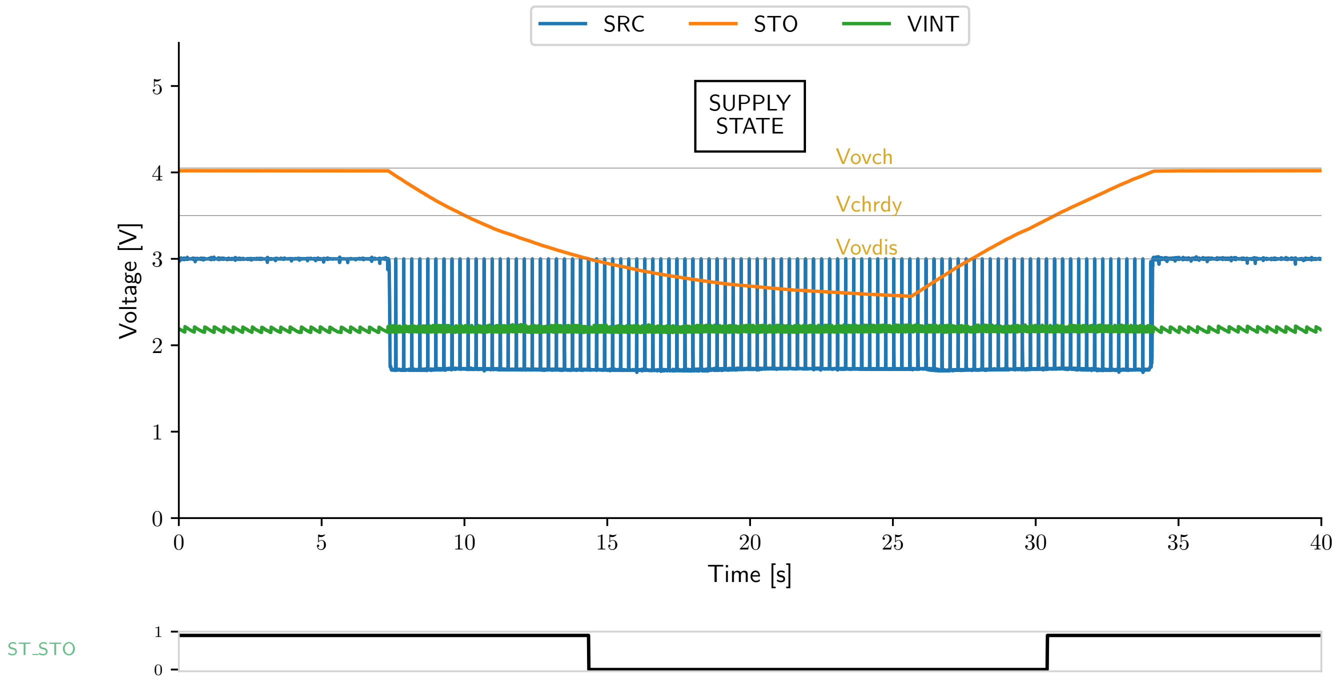

Figure 11: Supply state

- STO_CFG[3:0] = LLLL
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.50 V
  - V_{OVCH} = 4.05 V
- R_MPP[2:0] = LLL (60%)
- T_MPP[1:0] = LL (5.19 ms / 280 ms)
- C_{STO} = 10 mF
- SRC: 5 mA current source with 3 V voltage compliance
- EN_HP = H (high power mode)
- EN_STO_CH = H (storage element charge enabled)
- 1 kΩ between STO and GND, connected between 7 s and 25.5 s (no load on STO the rest of the time)

11.3. Supply state and Reset state

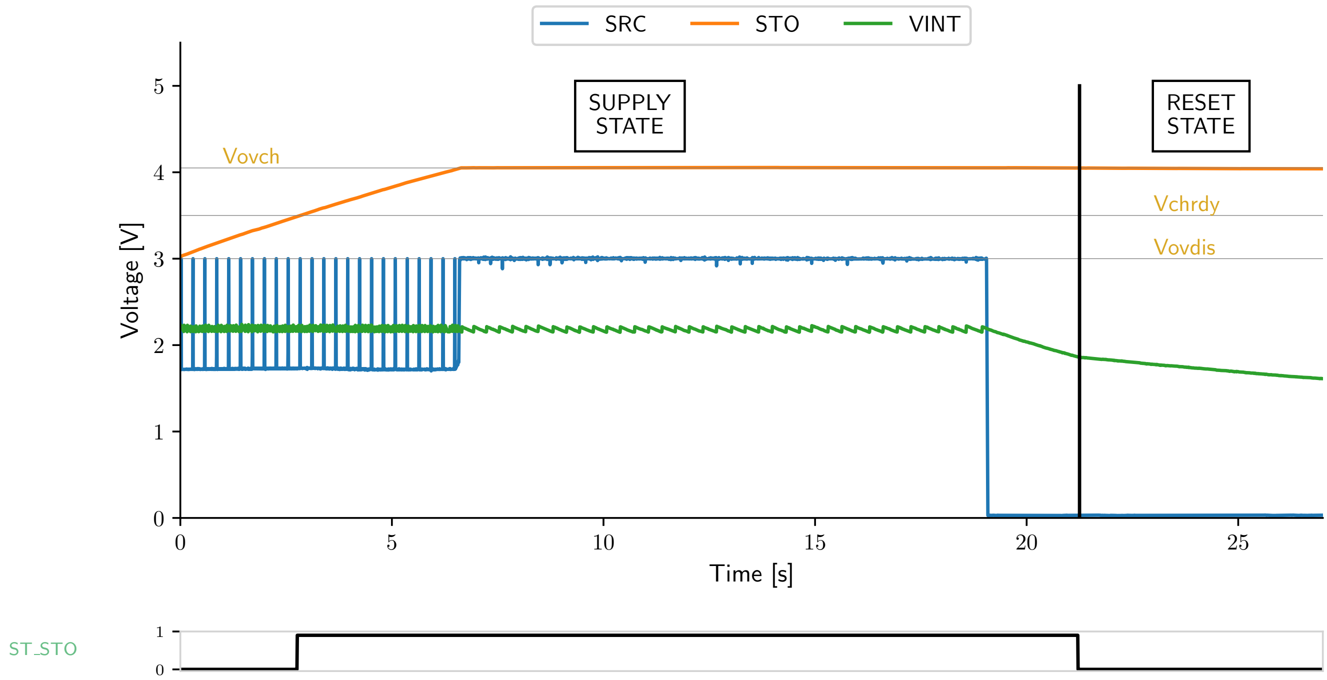

Figure 12: Supply state and Reset state

- STO_CFG[3:0] = LLLL
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.50 V
  - V_{OVCH} = 4.05 V
- R_MPP[2:0] = LLL (60%)
- T_MPP[1:0] = LL (5.19 ms / 280 ms)
- C_{STO} = 10 mF
- SRC: 5 mA current source with 3 V voltage compliance (stopped after 19 seconds)
- EN_HP = H (high power mode)
- EN_STO_CH = H (storage element charge enabled)

12. Performance Data

12.1. DCDC Conversion Efficiency From SRC to STO in Low Power Mode

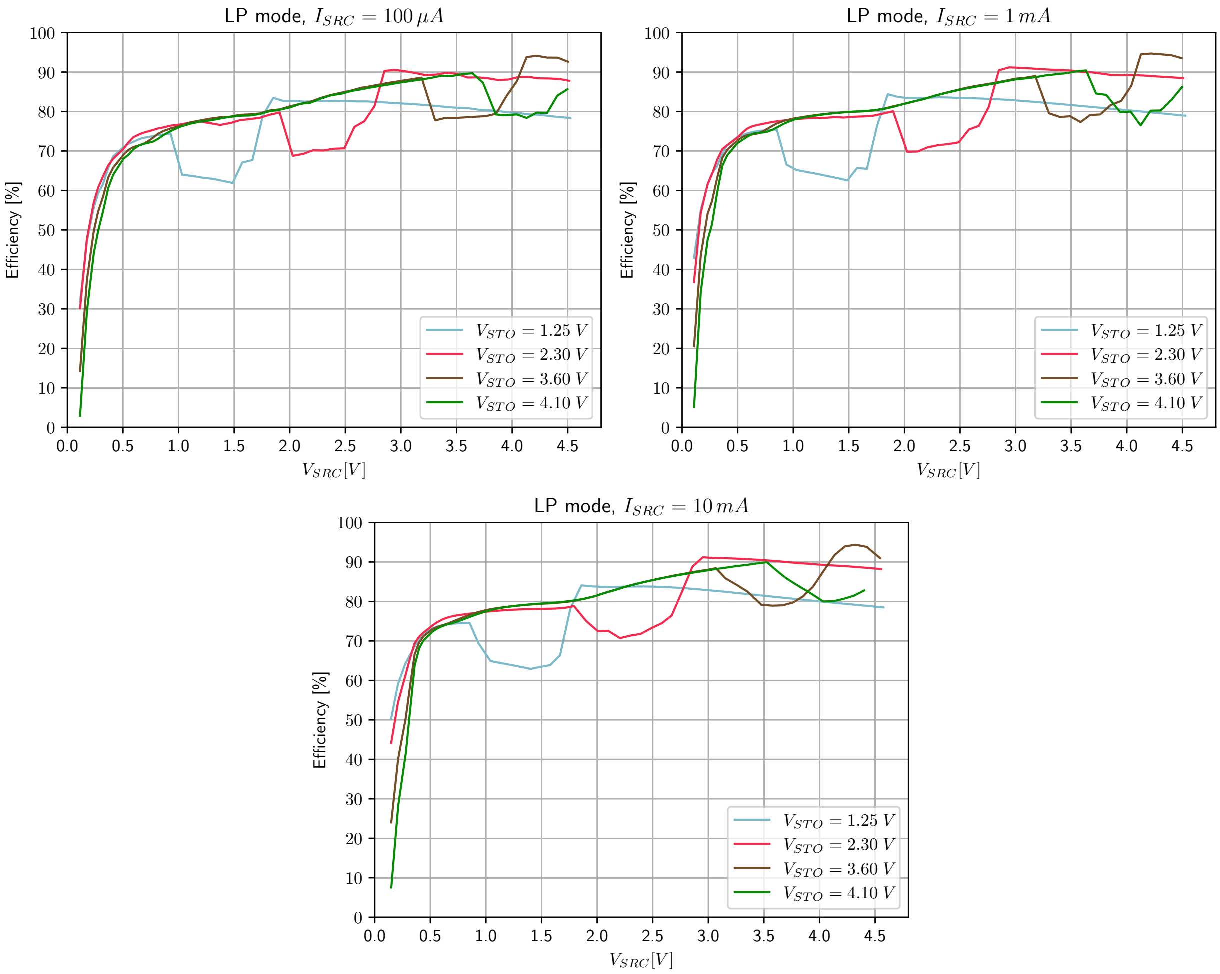

Figure 13: DCDC Efficiency from SRC to STO for 1 mA and 10 mA in Low Power Mode

12.2. DCDC Conversion Efficiency From SRC to STO in High Power Mode

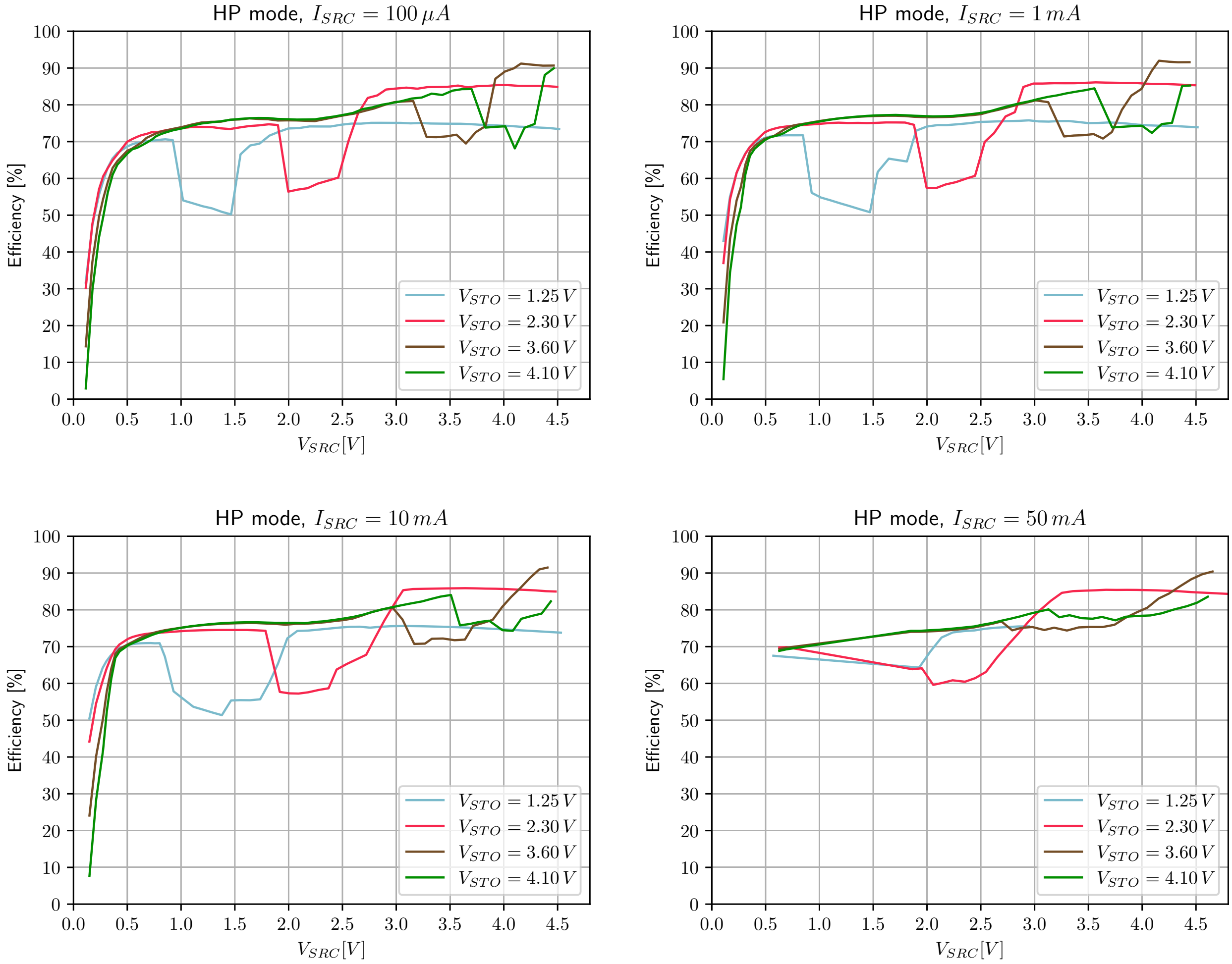

Figure 14: DCDC Efficiency from SRC to STO for 10 mA and 50 mA in High Power Mode

13. Schematic

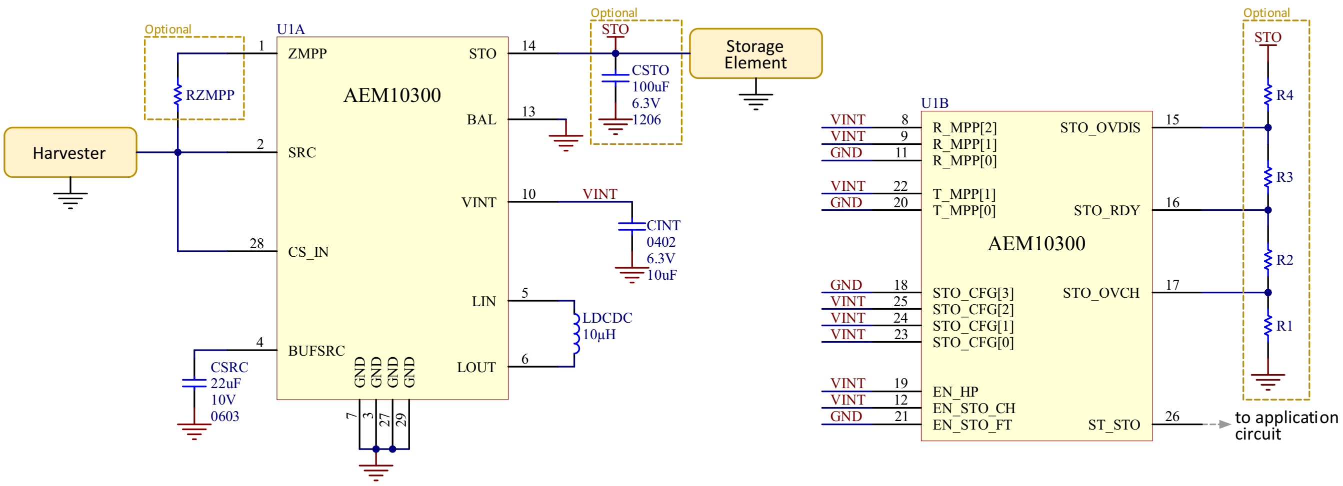

Figure 15: Schematic Example

Designator	Description	Quantity	Manufacturer	Link
U1	AEM10300 - Symbol QFN 28-pin	1	e-peas	order at sales@e-peas.com
L_{DCDC}	Power inductor 10 µH - 1.76A	1	Murata	DFE252010F-100M
C_{INT}	Ceramic Cap 10 µF, 6.3V, 20%, X5R 0402	1	Murata	GRM155R60J106ME15
C_{SRC}	Ceramic Cap 22 µF, 10V, 20%, X5R 0603	1	Murata	GRM188R61A226ME15D
C_{STO} (optional)	Ceramic Cap 100 µF, 6.3V, 20%, X5R 1206	1	TDK	C3216X5R1A107M160AC

Table 11: Minimal Bill of Materials

14. Layout

14.1. Guidelines

Good layout practices are mandatory in order to obtain good stability and best efficiency with the AEM10300. It also allows for minimizing electromagnetic interferences generated by the AEM10300 DCDC converter.

The following list, while not exhaustive, shows the main attention points when routing a PCB with the AEM10300:

- The switching nodes (LIN and LOUT) must be kept as short as possible, with minimal track resistance and minimal track capacitance. Low resistance is obtained by keeping track length as short as possible and track width as large as possible between L_{DCDC} and the AEM10300 pins. Minimal capacitance is obtained by keeping distance between LIN/LOUT and other signals. We recommend removing the ground plane, the power plane and the bottom layer ground pour under L_{DCDC} footprint, as well as adding distance between LIN/LOUT and the top ground pour, as shown on Figure 16.
- The DCDC decoupling capacitors (C_{SRC} - C_{STO}) must be placed as close as possible to the AEM10300, with direct connection and minimum track resistance for the corresponding power nodes (BUFSRC and STO).
- The GND return path between the DCDC decoupling capacitors (C_{SRC} - C_{STO}) and the AEM10300 thermal pad, which is the AEM10300 main GND connection, must be as direct and short as possible. This is preferably done on the top layer when possible, otherwise by internal/bottom plane, using low resistance vias to decrease layer-to-layer connection resistance.
- The external DC power connections (SRC and STO) must be connected to the AEM10300 with low resistance tracks.
- Connection between VINT and C_{INT} must be moderately short for AEM10300 stability, even though this pins does not carry large currents. Same for connection between C_{INT} to GND.
- If used, ZMPP must be connected to the AEM10300 with a low resistance track, according to the expected SRC power.
- The BAL pin connection track must be able to handle at least 40 mA.
- The custom mode setting pins STO_OVDIS, STO_RDY and STO_OVCH are high impedance analog inputs typically connected to a resistive divider with high resistor values, making those three nodes prone to pickup noise. Thus it is recommended to keep those as short as possible and as far as possible to noise sources such as DCDC switching nodes.
- The configuration pins and the status pins have minimal layout restrictions. CS_IN maximum current is below 1 mA, so its layout restrictions are minimal as well.

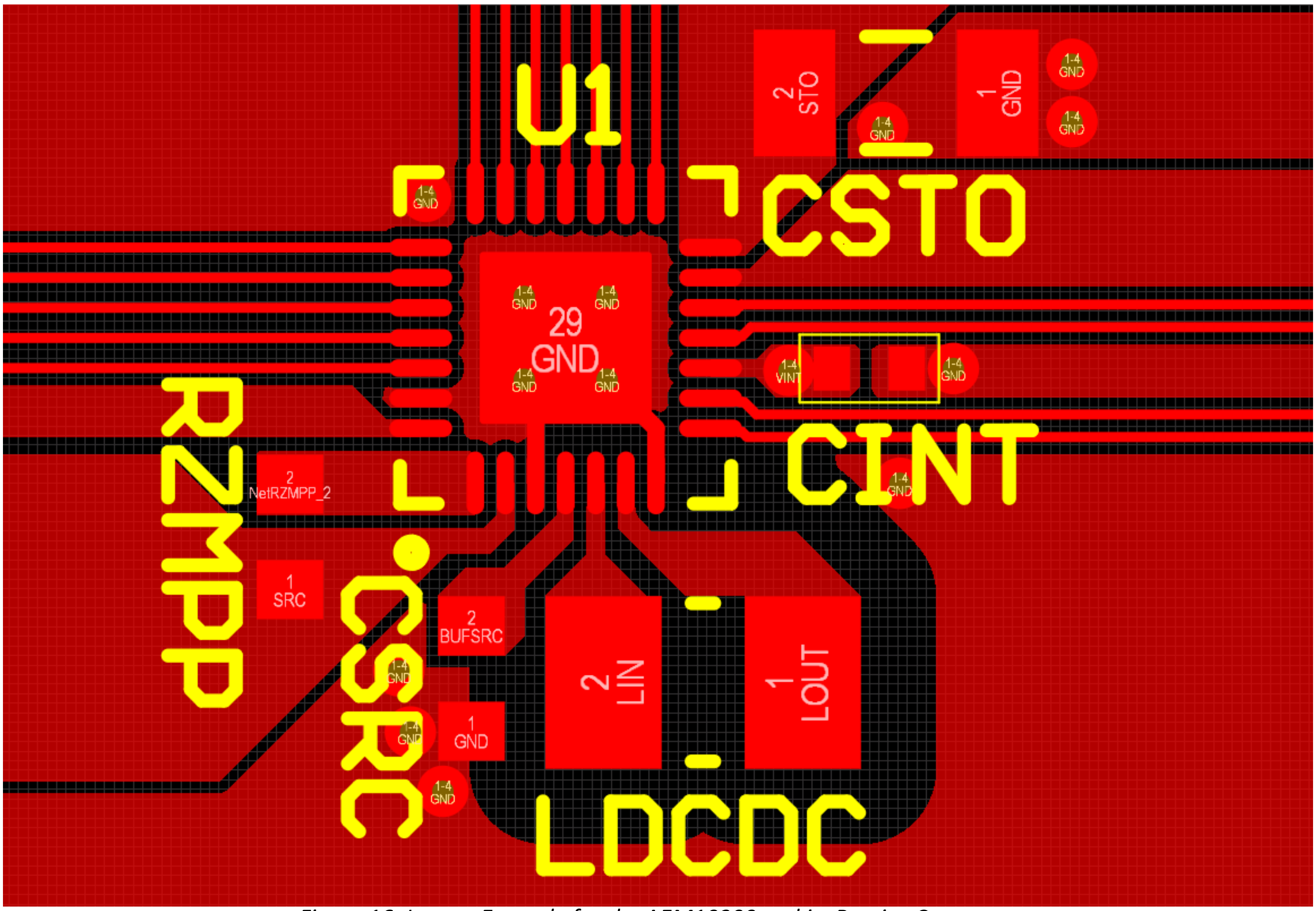

Figure 16: Layout Example for the AEM10300 and its Passive Components

NOTE: schematic, symbol and footprint for the e-peas component can be ordered by contacting e-peas support team at support@e-peas.com

15. Package Information

15.1. Plastic Quad Flatpack No-Lead (QFN 28-pin 4x4mm)

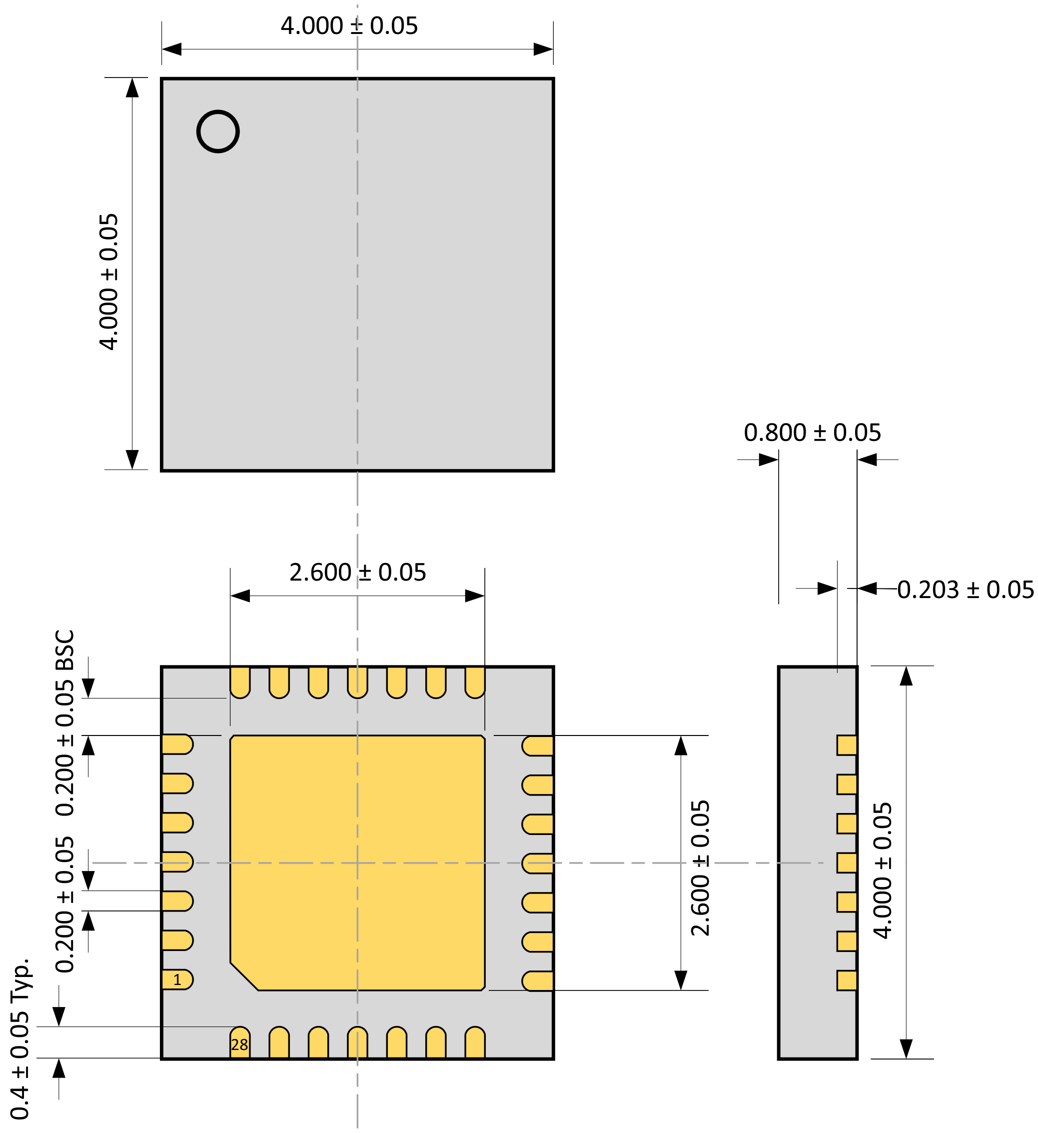

Figure 17: QFN 28-pin 4x4mm Drawing (All Dimensions in mm)

15.2. Board Layout

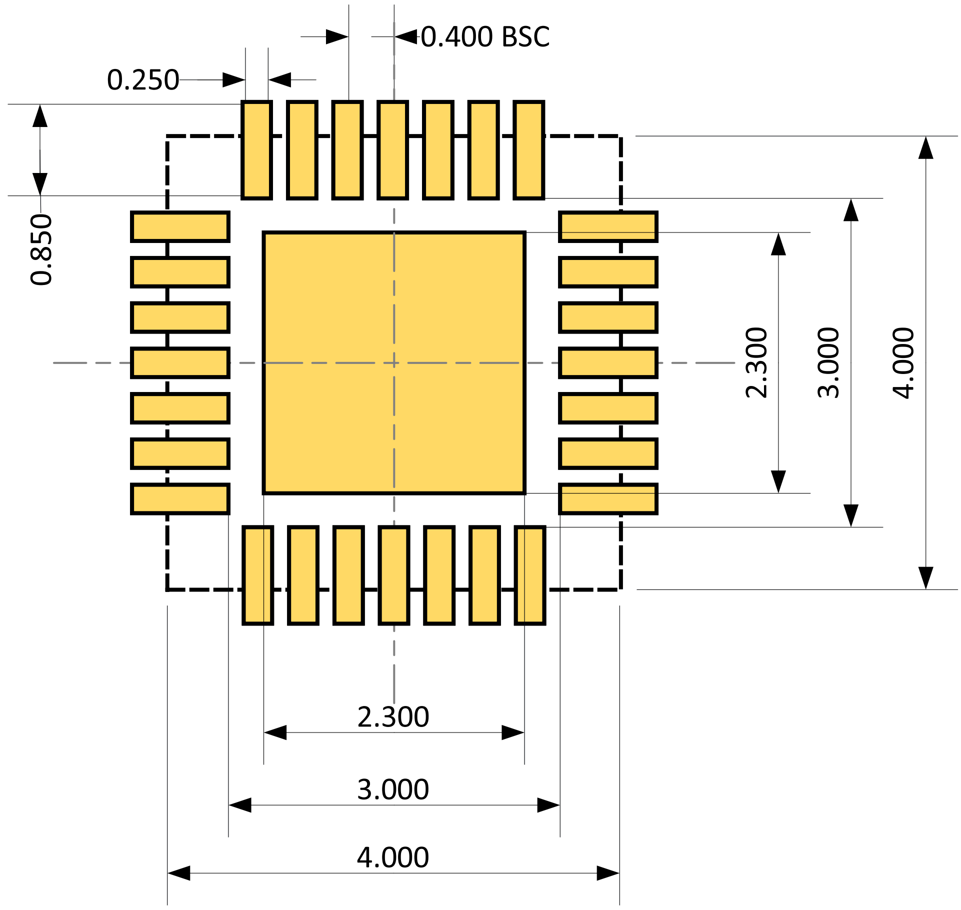

Figure 18: Recommended Board Layout (All Dimensions in mm)

16. Revision History

Revision	Date	Description
0.0	January, 2021	Creation of the document. Preliminary version.
1.0	June, 2021	First version of the document
1.1	August, 2021	Minor modifications
1.2	March, 2023	- Various aesthetic improvements. - Explanations about BAL circuit. - Added EN_STO_FT in Configuration Pins table - Section with precisions about the use of CS_IN. - Fixed state machine graph. - Fixed footprint dimensions - New “behavior” oscilloscope graphs with improved description. - Moved various states description sections as sub-sections of a global section. - Supply State description: explanation about SRC being set to high impedance when all nodes are fully charged. - Updated "Typical use" of storage element vs STO_CFG[3:0] configuration. - Replaced "asserted/de-asserted" by "HIGH/LOW". - Changed CSRC from 15µF/0402 to 22µF/0603. - Updated "Recommended Operation Conditions" with minimum capacitor values including derating and tolerances.
1.3	November, 2023	- Updated efficiency graphs. - Created section for pinout. - Updated schematics with new symbol. - Digital levels High/Low: replaced 0/1 notation by L/H. - Fixed example circuits errors. - Fixed typos and aesthetic issues. - Added layout guidelines with clearer layout examples.
1.4	February, 2024	Fixed wrong HIGH level of ST_STO in “Power and Status Pins” table.

Table 12: Revision History