

Highly Versatile, Regulated Single-Output, Buck-Boost Ambient Energy Manager For Up to 7-cell Solar Panels

Feature

Ultra-low power start-up

- Cold start from 275 mV input voltage and 3 μ W input power (typical).

Very efficient energy extraction

- Open-circuit voltage sensing for Maximum Power Point Tracking (MPPT).
- Selectable open-circuit voltage ratios from 60% to 90% or fixed impedance.
- Programmable MPPT sensing period.
- MPPT voltage operation range from 100 mV to 4.5 V.

Adaptive and smart energy management

- DCDC switches automatically between boost, buck-boost and buck operation, according to input and output voltages, to maximize energy transfer.
- DCDC automatically handles multiple inputs and outputs:
 - Keeps the internal supply and the load voltages regulated while storing the excess of energy in the storage element.
 - The storage element can be used as an input to keep the load and internal voltages regulated when no energy is available on the source.

Load supply voltage

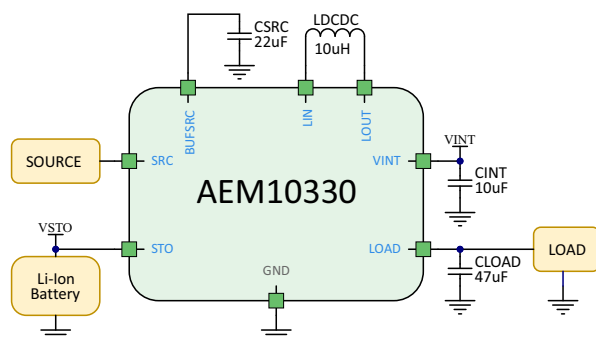
- Selectable load voltage from 1.2 V to 3.3 V.
- Current drive capability: 30 mA in low power mode, 60 mA in high power mode.

Battery protection features

- Selectable over-charge and over-discharge protection for any type of rechargeable battery or (super-)capacitor.
- Fast super-capacitor charging.
- Dual cell super-capacitor balancing circuit.

Smallest footprint, smallest BOM

- Only four external components are required.
- One 10 μ H inductor.
- Three capacitors: one 10 μ F, one 22 μ F and one at least 40 μ F.



Description

The AEM10330 is an integrated energy management circuit that extracts DC power from an ambient energy harvesting source to simultaneously supply an application and store energy in a storage element. The AEM10330 allows to extend battery lifetime and ultimately eliminates the primary energy storage element in a large range of applications.

Thanks to its Maximum Power Point Tracking system, the AEM10330 extracts the maximum energy available from the source. It integrates an ultra-low power DCDC converter which operates with input voltages ranging from 100 mV to 4.5 V.

At start-up, user can choose between charging the storage element first to accumulate energy before the application circuit starts, or charge the load decoupling capacitor first to start the application circuit faster.

With its unique cold start circuit, the AEM10330 can start harvesting with an input voltage as low as 275 mV and from an input power of 3 μ W. The preset protection levels determine the storage element voltages protection thresholds to avoid over-charging and over-discharging the storage element and thus avoiding damaging it. Those are set through configuration pins. Moreover, custom threshold voltages can be obtained at the expense of a few configuration resistors.

The load voltage can be selected to cover most application needs, with a maximum available load current of 60 mA.

The chip integrates all active elements for powering a typical wireless sensor. Only three capacitors and one inductor are required.

Applications

Asset Tracking/Monitoring	Industrial applications
Retail ESL/Smart sensors	Aftermarket automotive
Smart home/Building	

Device Information

Part Number	Package	Body size [mm]
10AEM10330J0000	QFN 40-pin	5x5mm

Evaluation Board

Part Number
2AAEM10330J0010

Table of Contents

1. Introduction	6
2. Pin Configuration and Functions	7
3. Absolute Maximum Ratings	9
4. Thermal Resistance	9
5. Typical Electrical Characteristics at 25 °C	10
6. Recommended Operation Conditions	11
7. Functional Block Diagram	12
8. Theory of Operation	13
8.1. DCDC Converter	13
8.2. Cold-Start Circuit	13
8.3. AEM10330 States Description	14
8.4. Maximum Power Point Tracking	15
8.5. Balancing for Dual-Cell Supercapacitor	16
9. System Configuration	17
9.1. High Power / Low Power Mode	17
9.2. Storage Element Configuration	17
9.3. Load Configuration	19
9.4. Custom Mode Configuration	19
9.5. Disable Storage Element Charging	20
9.6. MPPT Configuration	21
9.7. ZMPP Configuration	21
9.8. Source to Storage Element Feed-Through	21
9.9. External Components	22
10. Typical Application Circuits	23
10.1. Example Circuit 1	23
10.2. Example Circuit 2	24
11. Circuit Behavior	26
11.1. Wake-up state, Start state and Supply state	26
11.2. Supply state, Shutdown state and Reset state	27
12. Performance Data	28
12.1. DCDC Conversion Efficiency From SRC to STO in Low Power Mode	28
12.2. DCDC Conversion Efficiency From SRC to STO in High Power Mode	29
12.3. DCDC Conversion Efficiency From STO to LOAD in Low Power Mode	30
12.4. DCDC Conversion Efficiency From STO to LOAD in High Power Mode	31
12.5. Quiescent Current	32
13. Schematic	33
14. Layout	34
14.1. Guidelines	34
-	35
15. Package Information	36
15.1. Plastic Quad Flatpack No-Lead (QFN 40-pin 5x5mm)	36
15.2. Board Layout	37

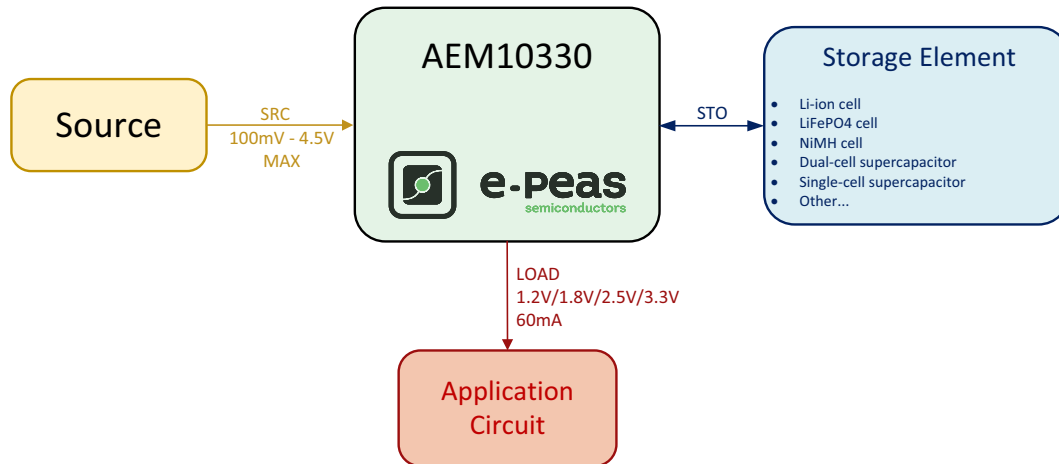
16. Revision History 38

List of Figures

Figure 1: Simplified Schematic View	6
Figure 2: Pinout Diagram QFN 40-pin	7
Figure 3: Functional Block Diagram	12
Figure 4: Simplified Schematic View of the AEM10330	13
Figure 5: Diagram of the AEM10330 States	14
Figure 6: Maximum LOAD Current Depending on V_{STO} and on V_{LOAD}	17
Figure 7: Custom Mode Settings	19
Figure 8: R_{ZMPP} Connection to the AEM10330	21
Figure 9: Typical Application Circuit 1	23
Figure 10: Typical Application Circuit 2	24
Figure 11: Wake-up state, Start state and Supply state	26
Figure 12: Supply State, Shutdown state and Reset state	27
Figure 13: DCDC Efficiency from SRC to STO for 1 mA and 10 mA in Low Power Mode	28
Figure 14: DCDC Efficiency from SRC to STO for 10 mA and 50 mA in High Power Mode	29
Figure 15: DCDC Efficiency from STO to LOAD in Low Power Mode	30
Figure 16: DCDC Efficiency from STO to LOAD in High Power Mode	31
Figure 17: Quiescent Current	32
Figure 18: Schematic Example	33
Figure 19: Layout Example for the AEM10330 and its Passive Components	35
Figure 20: QFN 40-pin 5x5mm Drawing (All Dimensions in mm)	36
Figure 21: Recommended Board Layout for QFN40 package (All Dimensions in mm)	37

List of Tables

Table 1: Power and Status Pins	7
Table 2: Configuration and Ground Pins	8
Table 3: Absolute Maximum Ratings	9
Table 4: Thermal Resistance	9
Table 5: Typical Electrical Characteristics	10
Table 6: Recommended Operation Conditions	11
Table 7: DCDC Converter Modes	13
Table 8: Storage Element Configuration Pins	18
Table 9: Load Configuration Pins	19
Table 10: MPP Ratio Configuration Pins	21
Table 11: MPP Timing Configuration Pins	21
Table 12: Minimal Bill of Materials	33
Table 13: Revision History	38



1. Introduction

Figure 1: Simplified Schematic View

The AEM10330 is a full-featured energy efficient power management circuit able to harvest energy from an energy source (connected to **SRC**) to supply an application circuit (connected to **LOAD**) and use any excess of energy to charge a storage element (connected to **STO**). This is done with a minimal bill of material: only capacitors and one inductor are needed for a basic setup.

The heart of the AEM10330 is a regulated switching DCDC converter with high power conversion efficiency.

At first start-up, as soon as a required cold-start voltage of 275 mV and a sparse amount of power of at least 3 μ W is available at the source, the AEM10330 coldstarts. After the cold start, the AEM extracts the power available from the source if the working input voltage is at least 100 mV.

Through four configuration pins (**STO_CFG[3:0]**), the user can select a specific operating mode out of 15 modes that cover most application requirements without any dedicated external component. Those operating modes define the protection levels of the storage element. If none of those 15 modes fit the user's storage element, a custom mode is also available to allow the user to define a mode with custom specifications.

Status pins **ST_STO**, **ST_STO_RDY** and **ST_STO_OVDIS** provide information about the voltage levels of the storage element. **ST_STO** is HIGH when the voltage of the storage element V_{STO} is above V_{CHRDY} and is reset when the voltage drops below V_{OVDIS} . **ST_STO_RDY** is HIGH when V_{STO} is above V_{CHRDY} , and reset when V_{STO} drops below V_{CHRDY} . **ST_STO_OVDIS** is HIGH when V_{STO} drops below V_{OVDIS} and reset when V_{STO} is above V_{OVDIS} . Status pin **ST_LOAD** is HIGH when the load voltage V_{LOAD} rises above $V_{LOAD,TYP}$, and is reset when V_{LOAD} drops below $V_{LOAD,MIN}$.

The Maximum Power Point (MPP) ratio is configurable thanks to three configuration pins (**R_MPP[2:0]**) and ensures an optimum biasing of the harvester to maximize power extraction. Depending on the harvester, it is possible to adapt the timings of the MPP evaluations with the two configuration pins (**T_MPP[1:0]**) that sets the periodicity and the duration of the MPP evaluation.

Once started, if at any time the load requires more power than can be harvested from the energy source, the AEM10330 automatically uses the storage element to keep the load supplied.

The AEM10330's DCDC converter can work in two modes: **LOW POWER MODE** and **HIGH POWER MODE**, each one of these being optimized for a power range on **SRC** and **LOAD**.

The charging of the storage element can be prevented by pulling **EN_STO_CH** to GND, typically to protect the storage element if the temperature is too low/high to safely charge it.

The AEM10330 also implements a **SLEEP STATE**, which reduces the quiescent current to avoid wasting the energy stored on the storage element when **EN_SLEEP** is HIGH.

At start-up, user can choose to prioritize starting the application circuit connected on **LOAD**, or charging the storage element connected on **STO**. This is set by the **STO_PRIO** pin.



2. Pin Configuration and Functions

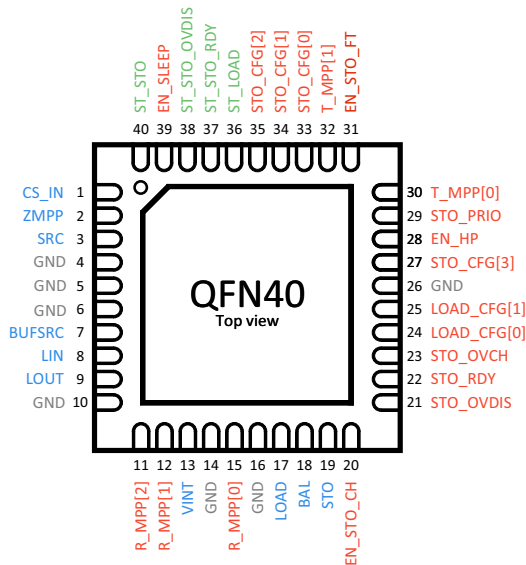


Figure 2: Pinout Diagram QFN 40-pin

NAME	PIN NUMBER	FUNCTION		
Power Pins				
CS_IN	1	Input for the eternal cold start circuit.		
ZMPP	2	Used for the configuration of the ZMPP (optional). Must be left floating if not used.		
SRC	3	Connection to the harvested energy source.		
BUFSRC	7	Connection to an external capacitor buffering the DCDC converter input.		
LIN	8	DCDC inductance connection.		
LOUT	9	DCDC inductance connection.		
VINT	13	Internal voltage supply.		
LOAD	17	Output voltage to supply on application load.		
BAL	18	Connection to mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.		
STO	19	Connection to the energy storage element - battery or (super-)capacitor. Cannot be left floating. Must be connected to a minimum capacitance of 100 μF or to a rechargeable battery.		
Status Pins				
ST_LOAD	36	Logic Output	HIGH: V_{LOAD}	HIGH when the LOAD voltage V_{LOAD} rises above the V_{LOAD,TYP} threshold. LOW when V_{LOAD} drops below V_{LOAD,MIN} threshold.
ST_STO_RDY	37	Logic Output	HIGH: V_{LOAD}	HIGH when V_{STO} is above V_{CHRDY} . LOW when V_{STO} drops below V_{CHRDY} .
ST_STO_OVDIS	38	Logic Output	HIGH: V_{LOAD}	HIGH when the AEM10330 state is SHUTDOWN STATE . LOW when in any other state.
ST_STO	40	Logic Output	HIGH: V_{STO}	HIGH when the storage device voltage V_{STO} rises above V_{CHRDY} threshold. LOW when V_{STO} drops below the V_{OVDIS} threshold.

Table 1: Power and Status Pins



NAME	PIN NUMBER	HIGH LEVEL	FLOATING STATE	FUNCTION
Configuration Pins				
R_MPP[0]	15	V _{VINT}	HIGH	Used for the configuration of the MPP ratio. Read as HIGH when left floating.
R_MPP[1]	12			
R_MPP[2]	11			
T_MPP[0]	30	V _{VINT}	HIGH	Used for the configuration of the MPP timings. Read as HIGH when left floating.
T_MPP[1]	32			
LOAD_CFG[0]	24	V _{VINT}	HIGH	Used for the configuration of LOAD output voltage V _{LOAD} . Read as HIGH when left floating.
LOAD_CFG[1]	25			
STO_CFG[0]	33	V _{VINT}	HIGH	Used for the configuration of the threshold voltages for the energy storage element V _{OVDIS} , V _{CHRDY} and V _{OVCH} . Read as HIGH when left floating.
STO_CFG[1]	34			
STO_CFG[2]	35			
STO_CFG[3]	27			
STO_PRIO	29	V _{VINT}	HIGH	- Pulled up to VINT or floating: storage device (STO) has highest priority at start-up - Pulled down to GND: load (LOAD) has highest priority at start-up
STO_OVCH	23	Used for the configuration of the threshold voltages (V _{OVDIS} , V _{CHRDY} and V _{OVCH}) for the energy storage element when STO_CFG[3:0] are set to custom mode (optional). Must be left floating if not used.		
STO_RDY	22			
STO_OVDIS	21			
EN_SLEEP	39	V _{LOAD}	Cannot be left floating	- Pulled up to LOAD: SLEEP STATE enabled - Pulled down to GND: SLEEP STATE disabled
EN_STO_FT	31	V _{VINT}	HIGH	- Pulled up to VINT or floating: allows charges flowing directly from SRC to STO when SRC is above 5V. - Pulled down to GND: normal operation.
EN_STO_CH	20	V _{LOAD}	HIGH	- Pulled up to LOAD or floating: enables the charging of the battery - Pulled down to GND: disables the charging of the battery
EN_HP	28	V _{VINT}	HIGH	- Pulled up to VINT or floating: HIGH POWER MODE enabled - Pulled down to GND: HIGH POWER MODE disabled
Other				
GND	4, 5, 6, 10, 14, 16, 26	Ground connection, best possible connection to PCB ground plane.		
	Exposed pad			

Table 2: Configuration and Ground Pins

3. Absolute Maximum Ratings

Parameter	Value
Voltage on LOAD , STO , SRC , BUFSRC , LIN , LOUT , ZMPP , BAL , CS_IN , EN_SLEEP , EN_STO_CH	-0.3 V to 5.5 V
Voltage on VINT , T_MPP[1:0] , R_MPP[2:0] , LOAD_CFG[1:0] , STO_CFG[3:0] , STO_PRIO , STO_OVCH , STO_OVDIS , STO_RDY , EN_HP	-0.3 V to 2.75 V
Operating junction temperature	-40 °C to 125 °C
Storage temperature	-65 °C to 150 °C
ESD HBM voltage	> 2000 V
ESD CDM voltage	> 500 V

Table 3: Absolute Maximum Ratings

4. Thermal Resistance

Package	θ_{JA}	θ_{JC}	Unit
QFN 40-pin	TBD	TBD	°C/W

Table 4: Thermal Resistance

ESD CAUTION



ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE

These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality



5. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Conversion						
P _{SRC,CS}	Source power required for cold start	V _{STO} > V _{chrdy}		3		μW
		V _{STO} < V _{chrdy}		6		μW
V _{SRC}	Input voltage of the energy source	During cold start		0.275	4.5	V
		After cold start	0.1		4.5	V
R _{ZMPP}	MPPT ratio	See Table 10	60, 65, 70, 75, 80, 85 or 90, depending on R_MPP[2:0] configuration			%
Timing						
T _{MPP,EVAL}	Duration of a MPP evaluation		50% of Table 11		200% of Table 11	ms
T _{MPP,PERIOD}	Time between two MPP evaluations		50% of Table 11		200% of Table 11	s
Storage element						
V _{OVCH}	Maximum voltage accepted on the storage element before disabling its charging	see Table 8	Depends on STO_CFG[3:0] configuration			V
V _{CHRDY}	Minimum voltage required on the storage element before asserting the ST_STO					V
V _{OVDIS}	Minimum voltage accepted on the storage element before entering into SHUTDOWN STATE					V
Load Output Voltage						
I _{LOAD,MAX}	LOAD current drive capability	V _{LOAD} = 1.8V V _{STO} > 1.6V HP_EN = H		60		mA
		V _{LOAD} = 2.5V V _{STO} > 1.6V HP_EN = H		60		
		V _{LOAD} = 3.3V V _{STO} > 1.8V HP_EN = H		60		
V _{LOAD}	Output voltage	see Table 9	Depends on LOAD_CFG[1:0] configuration			V
Internal supply & Quiescent Current						
V _{VINT}	Internal voltage supply			2.2		V
I _Q	Quiescent current on STO	V _{STO} = 3.7V V _{LOAD} = 2.5V EN_SLEEP = L EN_HP = L		875		nA
Symbol	Logic Level		LOW		HIGH	
Logic output pins						
ST_STO	Logic output levels on the status STO pin		GND		V _{STO}	
ST_LOAD	Logic output levels on the status LOAD pin		GND		V _{LOAD}	
ST_STO_RDY	Logic output levels on the status STO_READY pin		GND		V _{LOAD}	
ST_STO_OVDIS	Logic output levels on the status STO_OVDIS pin		GND		V _{LOAD}	

Table 5: Typical Electrical Characteristics

6. Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
External Components					
L _{DCDC}	Inductor of the DCDC converter		10		μH
C _{SRC}	Capacitor decoupling the SRC terminal	13 ¹	22		μF
C _{INT}	Capacitor decoupling the VINT terminal	5 ¹	10		μF
C _{LOAD}	Capacitor decoupling the LOAD terminal	13 ¹	47		μF
C _{STO}	Optional - Capacitor on STO if no storage element is connected (see Section 9.9.1)	100 ¹			μF
R _{ZMPP}	Optional - Used for the configuration of the ZMPP tracking function	10	Section 9.7	100K	Ω
STO_OVCH	Configuration of V _{OVCH} in custom mode	1	Section 9.4	100	MΩ
STO_OVDIS	Configuration of V _{OVDIS} in custom mode				
STO_RDY	Configuration of V _{CHRDY} in custom mode				
Symbol	Logic Level	LOW		HIGH	
Logic input pins					
R_MPP[2:0]	Configuration pins for the MPP evaluation	GND		VINT	
T_MPP[1:0]	Configuration pins for the MPP timing	GND		VINT	
LOAD_CFG[1:0]	Configuration pins for the LOAD voltage	GND		VINT	
STO_CFG[3:0]	Configuration pins for the STO voltage	GND		VINT	
STO_PRIO	Configuration pin for the controller	GND		VINT	
EN_STO_FT	Configuration pin for the controller	GND		VINT	
EN_SLEEP	Configuration pin for the controller	GND		LOAD	
EN_STO_CH	Configuration pin for the controller	GND		LOAD	
EN_HP	Configuration pin for the controller	GND		VINT	

Table 6: Recommended Operation Conditions

1. Consider all component tolerance and deratings. Typically, DC-bias derating has a major impact on capacitance on ceramic capacitors.

7. Functional Block Diagram

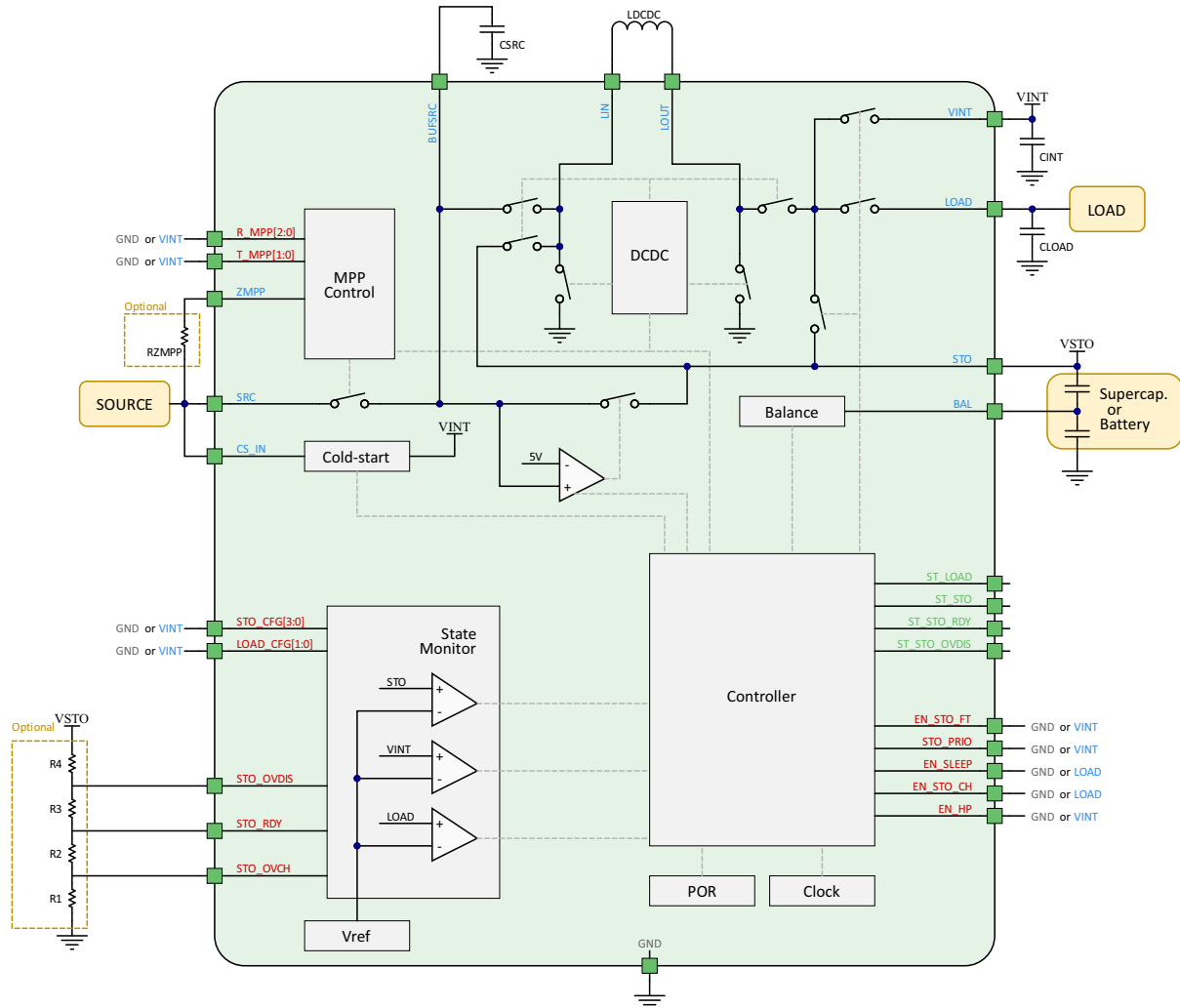


Figure 3: Functional Block Diagram

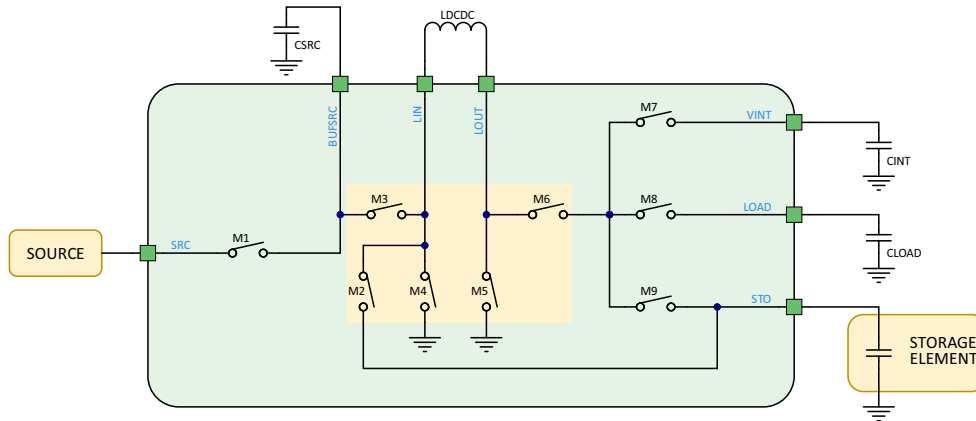


Figure 4: Simplified Schematic View of the AEM10330

8. Theory of Operation

8.1. DCDC Converter

The DCDC converter converts the voltage available at **BUFSRC** or at **STO** to a level suitable for charging the storage element **STO** or to regulate the **LOAD** and the internal supply **VINT**. The switching transistors of the DCDC converter are M2 or M3, M4, M5 and M6. Thanks to M7, M8 and M9, the controller selects between **LOAD**, **STO** and **VINT** respectively as the converter output. M1 selects the source as main input of energy. The internal supply **VINT** is regulated with priority over **LOAD**. **STO** is selected as an output only when neither **VINT** nor **LOAD** needs to be supplied. The converter has two possible inputs: **BUFSRC** or **STO**. **BUFSRC** is used by default as an input via M3. If the energy available on **SRC** is not sufficient to maintain the **LOAD** or **VINT** voltage, for instance because of a sudden current peak on **LOAD**, the converter uses **STO** instead as an input via M2 to keep **LOAD** and **VINT** regulated.

The reactive power component of this converter is the external inductor L_{DCDC} . Periodically, the MPP control circuit disconnects the source from the **BUFSRC** pin with the transistor M1 in order to let the harvester on **SRC** rise to its open-circuit voltage V_{OC} and measure it. This is done to define the optimal voltage level V_{MPP} , which is determined by applying the MPP ratio on V_{OC} . **BUFSRC** is decoupled by the capacitor C_{SRC} which smooths the voltage against the current pulses pulled by the DCDC converter. The storage element is connected to the **STO** pin.

Depending on its input voltage and its output voltage, the DCDC converter will work as a boost converter, a buck converter or a buck-boost converter. The maximum power that can be harvested and supplied to the output **LOAD** depends on the power mode (**HIGH POWER MODE** or **LOW POWER MODE**), which is configured through the **EN_HP** pin (see Section 9.1).

DCDC Converter Mode	Input Voltage / Output Voltage
Boost	$V_{IN} < V_{OUT} - 250 \text{ mV}$
Buck	$V_{IN} > V_{OUT} + 250 \text{ mV}$
Buck - Boost	$V_{OUT} - 250 \text{ mV} < V_{IN} < V_{OUT} + 250 \text{ mV}$

Table 7: DCDC Converter Modes

8.2. Cold-Start Circuit

The AEM10330 is able to coldstart if the voltage on **CS_IN** is above 0.275 V. The minimum available power is:

- 3 μW if V_{STO} is above V_{CHRDY} .
- 6 μW if V_{STO} is below V_{CHRDY} .

CS_IN is typically connected to **SRC** to allow the AEM10330 to coldstart from the energy available on the harvester. Nevertheless, any other energy source can be connected to **CS_IN** as long as it meets the electrical specifications constraints described in Sections 5 and 6.

8.3. AEM10330 States Description

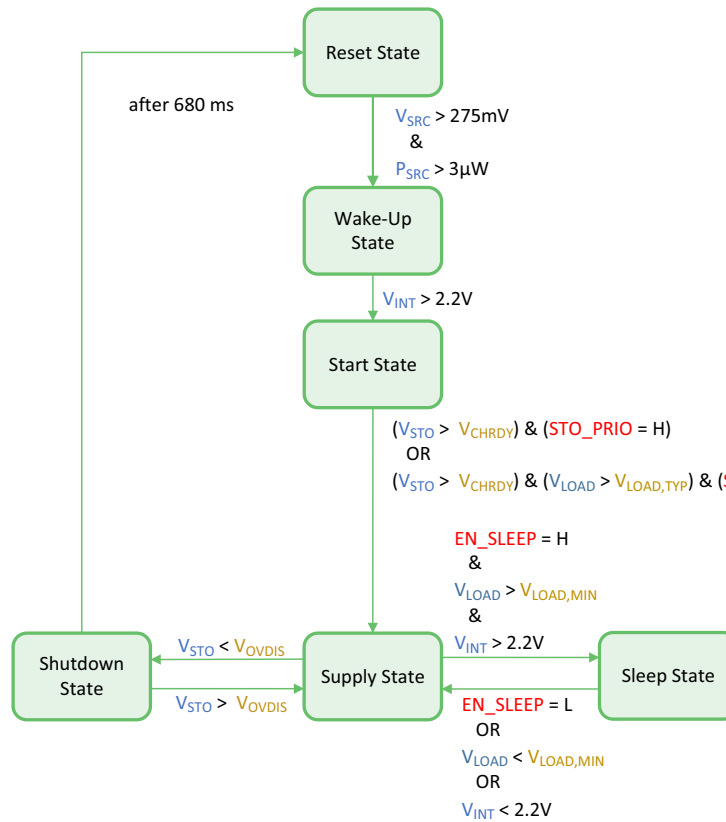


Figure 5: Diagram of the AEM10330 States

8.3.1. Reset, Wake Up and Start States

The **RESET STATE** is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold start voltage of 275 mV and a sparse amount of power of just 3 µW become available on **CS_IN** (usually connected to **SRC**), the AEM10330 switches to **WAKE-UP STATE**, and energy is extracted from **SRC** to make **V_{VINT}** rise to 2.2 V. When **V_{VINT}** reaches those 2.2 V, the AEM10330 switches to **START STATE**. In **START STATE**, two scenarios are possible: in the first scenario, **STO_Prio** is HIGH, the storage element connected to **STO** has the priority on the one connected to **LOAD**. In the second scenario, **STO_Prio** is reset and the **LOAD** has the priority.

When the AEM10330 is in **RESET STATE**, **WAKE-UP STATE** or **START STATE**, the DCDC converter's input is always **BUFSRC**: **STO** is never used as input. This guarantees that the storage element is not used until a minimum amount of energy has been stored in it.

8.3.1.1. Storage Element Priority

This paragraph covers the AEM10330 behavior when **STO_Prio** is pulled up to **V_{VINT}**, so that the storage element connected on **STO** has priority over **LOAD**.

Supercapacitor as a Storage Element

If the storage element is a supercapacitor, it may be fully discharged at first and thus need to be charged from 0 V. The DCDC converter charges **STO** from the input source (**SRC**). When **V_{STO}** reaches **V_{CHRDY}**, the circuit enters **SUPPLY STATE**.

Battery as a Storage Element

If the storage element is a battery, but its voltage is lower than **V_{CHRDY}**, then the storage element needs to be charged first until it reaches **V_{CHRDY}**. Once **V_{STO}** reaches **V_{CHRDY}**, or if the battery was initially charged above **V_{CHRDY}**, the circuit enters **SUPPLY STATE**.

8.3.1.2. Load Priority

If **STO_Prio** is connected to GND, the AEM charges first the **LOAD** to $V_{LOAD,MAX}$ (see Table 9) using energy from the source (**SRC**). This allows to first supply the application circuit connected to **LOAD**. If the storage element was initially charged above V_{CHRDY} , the circuit enters **SUPPLY STATE** as soon as **LOAD** reaches $V_{LOAD,TYP}$. If the storage element is a supercapacitor or a battery which voltage is lower than V_{CHRDY} , the AEM keeps regulating **LOAD** between $V_{LOAD,MAX}$ and $V_{LOAD,TYP}$. Meanwhile, any excess charges on the source is used to charge the storage element until it reaches V_{CHRDY} . Once V_{STO} exceeds V_{CHRDY} , the circuit enters into **SUPPLY STATE**.

This configuration is useful when a large storage element is connected to **STO** and a smaller one is connected to **LOAD**: the application starts as soon as C_{LOAD} is charged and does not have to wait for the large storage element on **STO** to be charged.

8.3.2. Supply State

In **SUPPLY STATE**, four scenarios are possible:

- There is enough power provided by the source (**SRC**) to keep V_{LOAD} near $V_{LOAD,TYP}$ with a small hysteresis and V_{VINT} at 2.2 V. The excessive power is used to charge the storage element on **STO**. In that case, the circuit remains in **SUPPLY STATE**. If **STO** is fully charged, **LOAD** will be maintained at $V_{LOAD,MAX}$ instead of $V_{LOAD,TYP}$. If all nodes are fully charged, the DCDC converter is disabled to prevent over-charging the storage element, and the **SRC** pin is set to high impedance.
- If the circuit connected to **LOAD** consumes more energy than the energy that the AEM10330 is able to extract from the source, the **LOAD** circuit will be supplied by the storage element connected to the **STO** terminal. In this case, the circuit stays in **SUPPLY STATE**.
- Due to a lack of power from the source, V_{STO} falls below V_{OVDIS} . In this case, the circuit enters **SHUTDOWN STATE** as explained in Section 8.3.3.
- If **EN_SLEEP** is HIGH and conditions (shown on Figure 5) on V_{LOAD} and V_{VINT} are satisfied, the AEM enters **SLEEP STATE** (see section 8.3.4).

8.3.3. Shutdown State

If the storage element gets depleted ($V_{STO} < V_{OVDIS}$), the AEM10330 goes to **SHUTDOWN STATE**. As long as the AEM10330 is in this state, the **ST_STO_OVDIS** is HIGH. In **SHUTDOWN STATE**, if V_{STO} recovers within 680 ms, the AEM10330 goes back to **SUPPLY STATE**. This prevents false detection of the storage element being empty because of a **LOAD** current peak.

8.3.4. Sleep State

SLEEP STATE reduces the AEM10330 quiescent current by disabling the DCDC converter and by reducing the controller clock frequency. If V_{VINT} or V_{LOAD} fall below their regulation value, the AEM10330 temporarily exits **SLEEP STATE** to wake up the DCDC converter and supply **VINT** or **LOAD**. Exiting **SLEEP STATE** and waking up the DCDC converter takes up to 1 ms. Depending on the expected **LOAD** current, C_{LOAD} value must be adapted to act as an energy buffer during the 1 ms required to wake up the DCDC converter. Therefore, this state may be enabled when **LOAD** current is small, and be disabled if a high **LOAD** current is expected. As the DCDC is disabled, no energy is harvested from **SRC** while in **SLEEP STATE**, so that the storage element connected to **STO** is no longer charged. **LOAD** and **VINT** are the only nodes that are still supplied and regulated when the AEM10330 is in **SLEEP STATE**. This mode is useful to limit the current drawn on **STO** when the application circuit has detected that the power available on **SRC** is so low that it wouldn't compensate the AEM10330 internal circuit power consumption (see Table 5).

The AEM10330 enters **SLEEP STATE** if all the following conditions are satisfied:

- **EN_SLEEP** pin pulled up to **LOAD** (H)
- $V_{VINT} > 2.2 \text{ V}$
- $V_{LOAD} > V_{LOAD,TYP}$

The AEM10330 leaves **SLEEP STATE** and switches back to **SUPPLY STATE** if one of the following conditions is satisfied:

- **EN_SLEEP** pin pulled down to GND (L)
- $V_{VINT} < 2.2 \text{ V}$
- $V_{LOAD} < V_{LOAD,TYP}$

The AEM10330 will then stay in **SUPPLY STATE** until the **SLEEP STATE** conditions are all satisfied again.

8.4. Maximum Power Point Tracking

During **SUPPLY STATE**, **SHUTDOWN STATE** and **START STATE**, the voltage on **SRC** is regulated by an internal Maximum Power Point Tracking (MPPT) module. The MPPT module evaluates V_{MPP} , the voltage at which the source provides the highest possible power, as a given fraction of the open-circuit voltage of the source V_{OC} . This ratio is set by the **R_MPP[2:0]**

terminals according to Table 10. The sampling period and duration are set according to Table 11 by the **T_MPP[1:0]** terminals. The AEM10330 supports any V_{MPP} levels in the range from 100 mV to 4.5 V. It offers a choice of seven values for the V_{MPP} / V_{OC} fraction. It can also match the input impedance of the DCDC converter with an impedance connected to the **ZMPP** terminal as explained in section 9.7.

8.5. Balancing for Dual-Cell Supercapacitor

The balancing circuit allows the user to balance the internal voltage of the dual-cell supercapacitor connected to **STO** in order to avoid damaging the supercapacitor because of excessive voltage on one cell.

If **BAL** is connected to **GND**, the balancing circuit is disabled. This configuration must be used if a battery, a capacitor or a single-cell supercapacitor is connected on **STO**.

If **BAL** is connected to the node between both cells of a supercapacitor, the balancing circuit compensates for any mismatch of the two cells that could lead to the over-charge of one of two cells. The balancing circuit ensures that **BAL** remains close to $V_{STO} / 2$. This configuration must be used if a dual-cell supercapacitor is connected to **STO**, and that this supercapacitor requires cells balancing.

The balancing circuit works as follows, with V_{BAL} the voltage on the **BAL** pin:

- $V_{BAL} > \frac{V_{STO}}{2}$: the AEM10330 enables a switch between **BAL** and **GND** to discharge the bottom supercapacitor cell to **GND** (up to 20 mA).
- $V_{BAL} < \frac{V_{STO}}{2}$: the AEM10330 enables a switch between **STO** and **BAL** to discharge the top supercapacitor cell to the bottom supercapacitor cell (up to 20 mA).

NOTE: the balancing feature is optimized for supercapacitors, for use with other storage elements (batteries, etc.), please contact e-peas support.

9. System Configuration

9.1. High Power / Low Power Mode

When **EN_HP** is pulled to **VINT**, the DCDC converter is configured to **HIGH POWER MODE**. This allows higher currents to be extracted from the DCDC converter input (**SRC** or **STO**) to the DCDC converter output (**LOAD** or **STO**). Figure 6 shows the maximum current that the DCDC converter can supply to **LOAD**, depending on the storage voltage **V_{STO}**, for every available load voltage **V_{LOAD}**, for both **HIGH POWER MODE** and **LOW POWER MODE**.

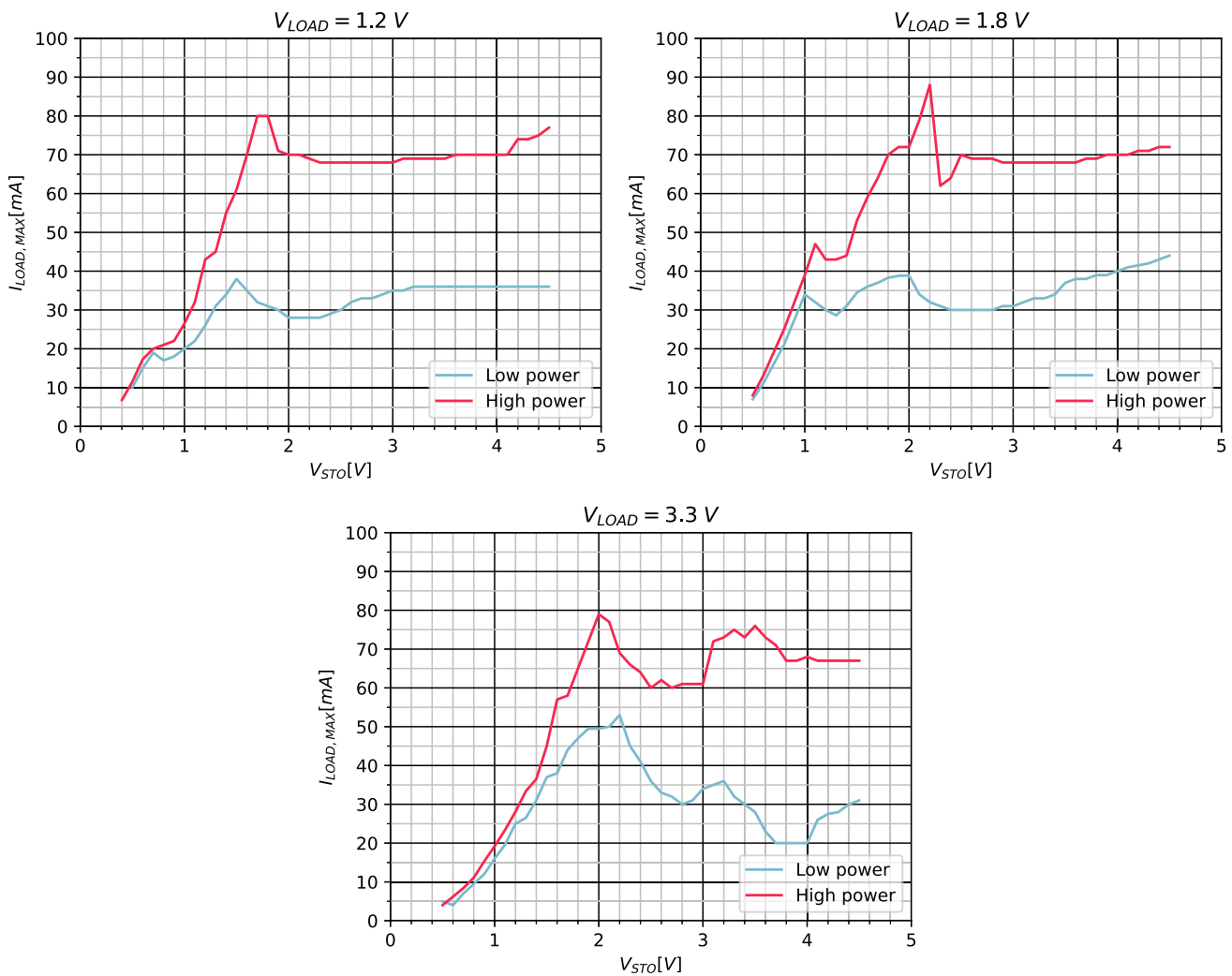


Figure 6: Maximum LOAD Current Depending on V_{STO} and on V_{LOAD}

9.2. Storage Element Configuration

Through four configuration pins (**STO_CFG[3:0]**), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 8. The three threshold levels are defined as:

- **V_{OVCH}**: maximum voltage accepted on the storage element before disabling its charging.
- **V_{CHRDY}**: minimum voltage required on the storage element before starting to supply the **LOAD** (if **STO_Prio** is HIGH) and entering supply state after start-up.

- V_{OVDIS} : minimum voltage accepted on the storage element before considering the storage element as depleted, thus setting ST_STO LOW.

A large-size storage element is not mandatory on STO :

- If the harvested energy source is permanently available and covers the application needs or

- If the application does not need to store energy when the harvested energy source is not available

The storage element may then be replaced by an external capacitor C_{STO} with a minimum value of 100 μF .

CAUTION: running the AEM10330 without this 100 μF minimum capacitance on STO will permanently damage the circuit.

Configuration pins				Storage element threshold voltages			Typical use
$STO_CFG[3:0]$				V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
L	L	L	L	3.00 V	3.50 V	4.05 V	LiCoO ₂ battery, Li-Po battery, Lithium Titanate (3.8 V) battery (long life).
L	L	L	H	2.80 V	3.10 V	3.60 V	LiFePO ₄ battery, Lithium capacitor (LiC).
L	L	H	L	1.85 V	2.40 V	2.70 V	Dual-cell NiMH battery, Lithium-Titanate (2.4V) battery.
L	L	H	H	0.20 V	1.00 V	4.65 V	Dual-cell supercapacitor.
L	H	L	L	0.20 V	1.00 V	2.60 V	Single-cell supercapacitor.
L	H	L	H	1.00 V	1.20 V	2.95 V	Single-cell supercapacitor.
L	H	H	L	1.85 V	2.30 V	2.60 V	Lithium-Titanate battery (2.4V).
L	H	H	H	Custom Mode (single-cell NiMH battery, LiC, etc.) ¹ .			
H	L	L	L	1.10 V	1.25 V	1.50 V	Ni-Cd single-cell battery.
H	L	L	H	2.20 V	2.50 V	3.00 V	Ni-Cd dual-cell battery.
H	L	H	L	1.45 V	2.00 V	4.65 V	Dual-cell supercapacitor.
H	L	H	H	1.00 V	1.20 V	2.60 V	Single-cell supercapacitor.
H	H	L	L	2.00 V	2.30 V	2.60 V	Solid State battery.
H	H	L	H	3.00 V	3.50 V	4.35 V	LiCoO ₂ battery, Li-Po battery, Lithium Titanate (3.8 V) battery.
H	H	H	L	2.60 V	2.70 V	4.00 V	Tadiran TLI.
H	H	H	H	2.60 V	3.50 V	3.90 V	Tadiran HLC.

Table 8: Storage Element Configuration Pins

1. An example of a single-cell NiMH batteries optimized custom mode setting can be found at Section 10.2.

9.3. Load Configuration

The **LOAD** output voltage V_{LOAD} can be configured thanks to the **LOAD_CFG[1:0]** configuration pins covering most application cases (see Table 9). V_{LOAD} is regulated to $V_{LOAD,TYP}$. However, if V_{LOAD} falls below $V_{LOAD,MID}$, the controller forces **STO** as an input of the DCDC converter to supply **LOAD**.

When the AEM10330 is in **SUPPLY STATE**:

- $V_{LOAD} < V_{LOAD,MID}$: the AEM10330 charges C_{LOAD} by transferring the energy available on the storage element **STO** (if V_{STO} is above V_{OVDIS}), even if energy is available on **SRC**.
- $V_{LOAD,MID} < V_{LOAD} < V_{LOAD,MAX}$:
 - If energy is available on **SRC**, the AEM10330 uses it to charge C_{LOAD} .
 - If no energy is available on **SRC**, the AEM10330 uses the energy available on **STO** to charge C_{LOAD} .

- $V_{LOAD,TYP}$ is the typical average voltage to be expected on the **LOAD** pin.
- **ST_LOAD** reflects V_{LOAD} , with an hysteresis between $V_{LOAD,MIN}$ and $V_{LOAD,TYP}$:
 - **ST_LOAD** is HIGH when $V_{LOAD} > V_{LOAD,TYP}$.
 - **ST_LOAD** is LOW when $V_{LOAD} < V_{LOAD,MIN}$.
- As a reminder, the order of priority in which the nodes are recharged is as follows:
 - **VINT** always has the highest priority, as it is mandatory to keep the AEM10330 internal circuit supplied.
 - **LOAD** has the second highest priority, to keep the application circuit supplied.
 - **STO** has the lowest priority, as the storage element is used to store the excessive energy from **SRC**.

Configuration pins		LOAD output voltage			
LOAD_CFG[1:0]		$V_{LOAD,MIN}$	$V_{LOAD,MID}$	$V_{LOAD,TYP}$	$V_{LOAD,MAX}$
L	L	3.15 V	3.23 V	3.28 V	3.34 V
L	H	2.35 V	2.47 V	2.50 V	2.53 V
H	L	1.64 V	1.75 V	1.79 V	1.82 V
H	H	1.14 V	1.16 V	1.20 V	1.23 V

Table 9: Load Configuration Pins

9.4. Custom Mode Configuration

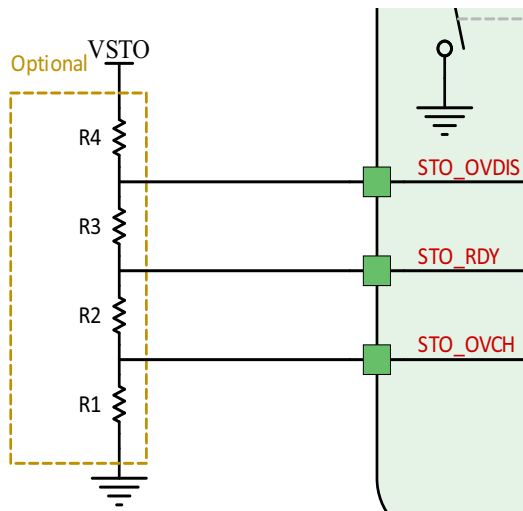


Figure 7: Custom Mode Settings

When **STO_CFG[3:0] = LHHH**, the custom mode is selected and all four configuration resistors must be wired as shown in Figure 7.

V_{OVCH} , V_{CHRDY} and V_{OVDIS} are defined thanks to R_1 , R_2 , R_3 and R_4 , which can be determined within the following constraints:

- $R_T = R_1 + R_2 + R_3 + R_4$
- $1M\Omega \leq R_T \leq 100M\Omega$
- $R_1 = R_T \cdot \frac{1V}{V_{OVCH}}$
- $R_2 = R_T \cdot \left(\frac{1V}{V_{CHRDY}} - \frac{1V}{V_{OVCH}} \right)$
- $R_3 = R_T \cdot \left(\frac{1V}{V_{OVDIS}} - \frac{1V}{V_{CHRDY}} \right)$
- $R_4 = R_T \cdot \left(1 - \frac{1V}{V_{OVDIS}} \right)$

The resistors should have high values to make the additional power consumption negligible. Moreover, the following constraints must be respected to ensure the functionality of the chip:

- $V_{CHRDY} + 0.05V \leq V_{OVCH} \leq 4.5V$
- $V_{OVDIS} + 0.05V \leq V_{CHRDY} \leq V_{OVCH} - 0.05V$
- $1V \leq V_{OVDIS}$



9.5. Disable Storage Element Charging

Pulling down **EN_STO_CH** pin to **GND** disables the charging of the storage element connected to **STO** from **SRC**. This can be done for example to protect the storage element when the system detects that the environment temperature is too low or too high to safely charge the storage element.

While **EN_STO_CH** is pulled down, **VINT** and **LOAD** can still be supplied either from **SRC** or from **STO**.

To enable charging the storage element on **STO**, **EN_STO_CH** must be pulled up to **LOAD** or left floating (pin is pulled up internally).

Please note that **STO** will still be charged to **V_{CHRDY}** during the **START STATE**

9.6. MPPT Configuration

The MPPT module is configured through the following pins:

- **R_MPP[2:0]** allows for configuring the V_{MPP} / V_{OC} tracking ratio, that has to be chosen according to the characteristics of the source. Please note that if the selected mode is **ZMPP**, an external resistor must be added to the circuit as explained in Section 9.7.
- **T_MPP[1:0]** allows for configuring the duration of an MPP evaluation and the time between two MPP evaluations.

Configuration pins			MPPT ratio
R_MPP[2:0]			V_{MPP} / V_{OC}
L	L	L	60%
L	L	H	65%
L	H	L	70%
L	H	H	75%
H	L	L	80%
H	L	H	85%
H	H	L	90%
H	H	H	ZMPP

Table 10: MPP Ratio Configuration Pins

Configuration pins		MPPT timing	
T_MPP[1:0]		Sampling duration	Sampling period
L	L	5.19 ms	280 ms
L	H	70.8 ms	4.5 s
H	L	280 ms	17.9 s
H	H	1.12 s	71.7 s

Table 11: MPP Timing Configuration Pins

9.7. ZMPP Configuration

Instead of working at a ratio of the open-circuit voltage, the AEM10330 can regulate the input impedance of the DCDC converter so that it matches a constant impedance R_{ZMPP} connected to the **ZMPP** pin. In this case, the AEM10330 regulates V_{SRC} at a voltage that is the product of the **ZMPP** resistance R_{ZMPP} and the current available at the **SRC** input.

$$- 10 \Omega \leq R_{ZMPP} \leq 100 \text{ k}\Omega$$

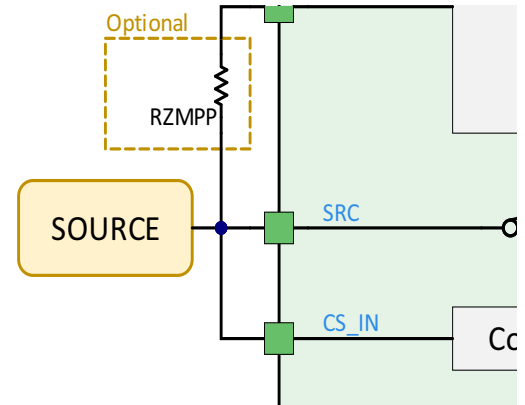


Figure 8: R_{ZMPP} Connection to the AEM10330

9.8. Source to Storage Element Feed-Through

When the harvester connected to **SRC** delivers a high amount of power, the AEM might not be able to pull enough current to regulate V_{SRC} to the MPP voltage. The voltage on **SRC** thus increases, eventually above 5V. To maximize the energy extracted in that case, the AEM30330 can be configured to create a direct feed-through current path from **SRC** to **STO** when V_{SRC} is above 5V. This is measured when the AEM is pulling current from the source (not during an MPP evaluation).

If the MPPT module detects that V_{SRC} is higher than 4 V and **EN_STO_FT** is set, the **SRC** is monitored. From that moment, if the AEM10330 detects that V_{SRC} rises above 5 V and if the storage element is not fully charged, the switch between the **SRC** and **STO** pins is closed until V_{SRC} drops below 5 V or until the storage element is fully charged.

This feature is enabled by pulling up **EN_STO_FT** pin to **VINT**. However, it is disabled if the storage element is fully charged, or when a MPP evaluation is occurring. Therefore the circuit must still be protected from any overshoot voltage on **SRC** above 5.5 V, for instance by a zener diode.

9.9. External Components

Refer to Figure 18 to have an illustration of the external components wiring.

9.9.1. Storage Element Information

The energy storage element of the AEM10330 can be a rechargeable battery, a supercapacitor or a capacitor. The size of the storage element must be determined so that its voltage does not fall below V_{OVDIS} even during current peaks pulled by the application circuit connected to **LOAD**. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to decouple the battery with a capacitor.

If the application expects a disconnection of the battery (e.g. because of a user removable connector), the PCB should include a capacitor C_{STO} of at least 100 μF connected between **STO** and **GND**. The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the whole subsystem.

9.9.2. External Inductor Information

The AEM10330 operates with one standard miniature inductor. L_{DCDC} must sustain a peak current of at least 1 A and a switching frequency of at least 10 MHz. Low equivalent series resistance (ESR) favors the power conversion efficiency of the DCDC converter. The recommended value is 10 μH .

9.9.3. External Capacitors Information

9.9.3.1. C_{SRC}

This capacitor acts as an energy buffer at the input of the DCDC converter. It prevents large voltage fluctuations when the DCDC converter is switching. The recommended nominal value is 22 μF .

9.9.3.2. C_{INT}

This capacitor acts as an energy buffer for the internal voltage supply. The recommended nominal value is 10 μF .

9.9.3.3. C_{LOAD}

This capacitor acts as an energy buffer for **LOAD**. It also reduces the voltage ripple induced by the current pulses inherent to the switched behavior of the converter. The recommended value is at least 13 μF (considering derating and tolerance).

10. Typical Application Circuits

10.1. Example Circuit 1

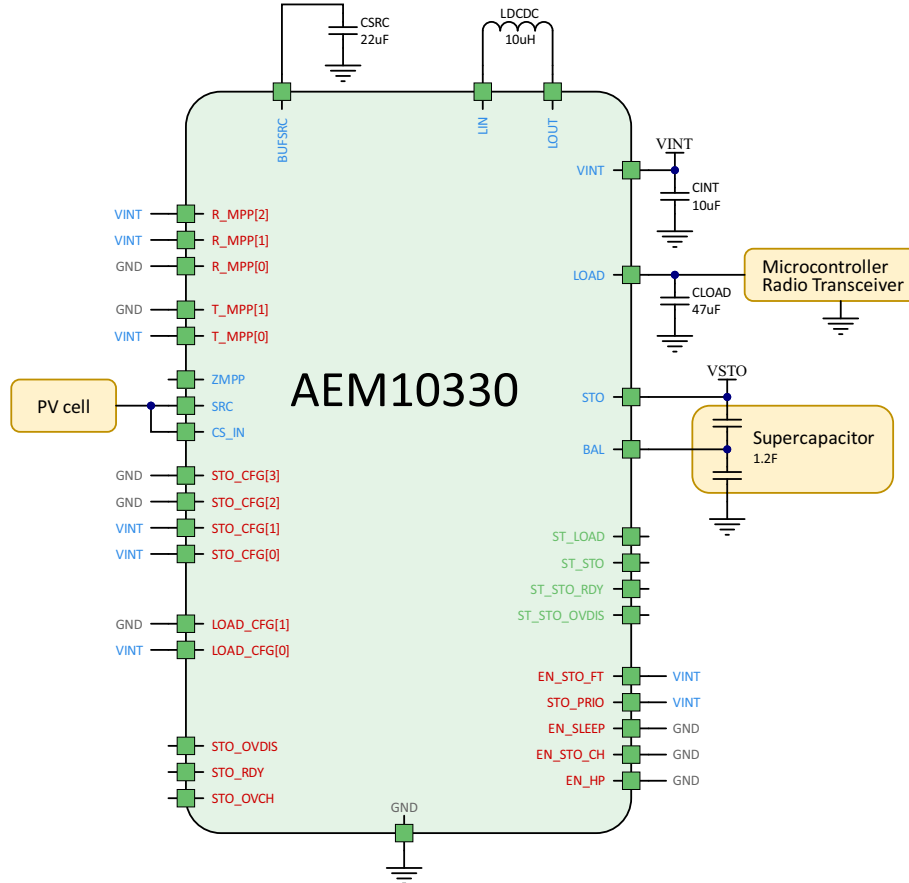


Figure 9: Typical Application Circuit 1

The circuit is an example of a system with solar energy harvesting. It uses a pre-defined operating mode that uses standard components, and a supercapacitor as energy storage.

- Energy source: PV cell.
- **R_MPP[2:0]** = HHL: the MPP tracker ratio is set to 90%.
- **T_MPP[1:0]** = LH: the MPP sampling period is 4.5 s and the MPP sampling duration is 70.8 ms.
- **STO_CFG[3:0]** = LLHH: the storage element is a dual-cell supercapacitor, with:
 - $V_{OVCH} = 4.65\text{ V}$
 - $V_{CHRDY} = 1.00\text{ V}$
 - $V_{OVDIS} = 0.20\text{ V}$
- The balancing pin of the dual-cell supercapacitor is connected to **BAL**.
- **LOAD_CFG[1:0]** = LH: the microcontroller and the radio transceiver are supplied by the **LOAD** terminal, which is regulated at $V_{LOAD} = 2.50\text{ V}$.
- **STO_Prio** is connected to **VINT**: at start-up **STO** will be charged and before **LOAD**.
- **EN_SLEEP** is connected to **GND**: the AEM10330 will never switch to **SLEEP STATE**.
- **EN_STO_CH** is connected to **VINT**: the charging of the storage element on **STO** is enabled.
- **EN_HP** is connected to **GND**: the DCDC converter is in **LOW POWER MODE**.
- **EN_STO_FT** is connected to **VINT**: **SRC** to **STO** feed-through is enabled when V_{SRC} is above 5 V.

10.2. Example Circuit 2

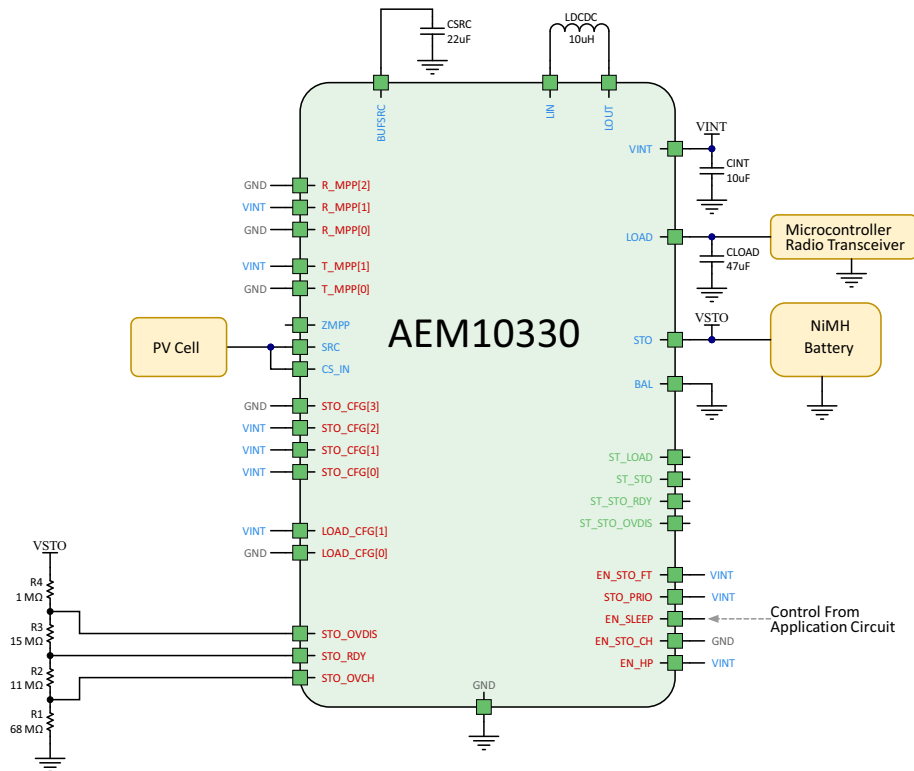


Figure 10: Typical Application Circuit 2

The circuit is an example of a system with solar energy harvesting. It uses a rechargeable NiMH battery as storage element. The voltage thresholds are set by the custom mode.

- Energy source: PV cell.
- **R_MPP[2:0]** = LHL: the MPP ratio is set to 70%.
- **T_MPP[1:0]** = HL: the MPP sampling period is 17.9 s and the MPP sampling duration is 280 ms.
- **STO_CFG[3:0]** = LHHH: the storage element is a NiMH rechargeable battery, used with custom mode:
 - $V_{OVDIS} = 1.00 \text{ V}$
 - $V_{CHRDY} = 1.20 \text{ V}$
 - $V_{OVCH} = 1.40 \text{ V}$
- Custom mode resistor divider calculations (values have been chosen to match E24 series value):
 - $R_T = 95 \text{ M}\Omega$
 - $R_1 = R_T \cdot \frac{1 \text{ V}}{V_{OVCH}} \approx 68 \text{ M}\Omega$
 - $R_2 = R_T \cdot \left(\frac{1 \text{ V}}{V_{CHRDY}} - \frac{1 \text{ V}}{V_{OVCH}} \right) \approx 11 \text{ M}\Omega$

$$R_3 = R_T \cdot \left(\frac{1 \text{ V}}{V_{OVDIS}} - \frac{1 \text{ V}}{V_{CHRDY}} \right) \approx 15 \text{ M}\Omega$$

$$R_4 = R_T \cdot \left(1 - \frac{1 \text{ V}}{V_{OVDIS}} \right) \approx 1 \text{ M}\Omega$$

- **BAL** is not used (not a dual-cell storage element) so it is connected to GND.
- **LOAD_CFG[1:0]** = HL: the micro-controller and the radio transceiver are supplied by the **LOAD** terminal, which is regulated at $V_{LOAD} = 1.79 \text{ V}$.
- **STO_PRI0** is connected to **VINT**: at start-up **STO** will be charged and before **LOAD**.
- **EN_SLEEP** is controlled by the application circuit, typically by a microcontroller GPIO output.
- **EN_STO_CH** is connected to **LOAD**: the charging of the storage element present on **STO** is enabled.
- **EN_HP** is connected to **VINT**: the DCDC converter is in **HIGH POWER MODE**.
- **EN_STO_FT** is connected to **VINT**: **SRC** to **STO** feed-through is enabled when V_{SRC} is above 5 V.



NOTE: for LiC (Lithium-ion Capacitor) storage elements, or others that would not be covered by `STO_CFG[3:0]` presets, please apply the same equations as in the above example to determine custom mode resistors values. E24 series values for typical storage elements can be found in the AEM10330 Configuration Tool spreadsheet, to be downloaded on e-peas website.

11. Circuit Behavior

11.1. Wake-up state, Start state and Supply state

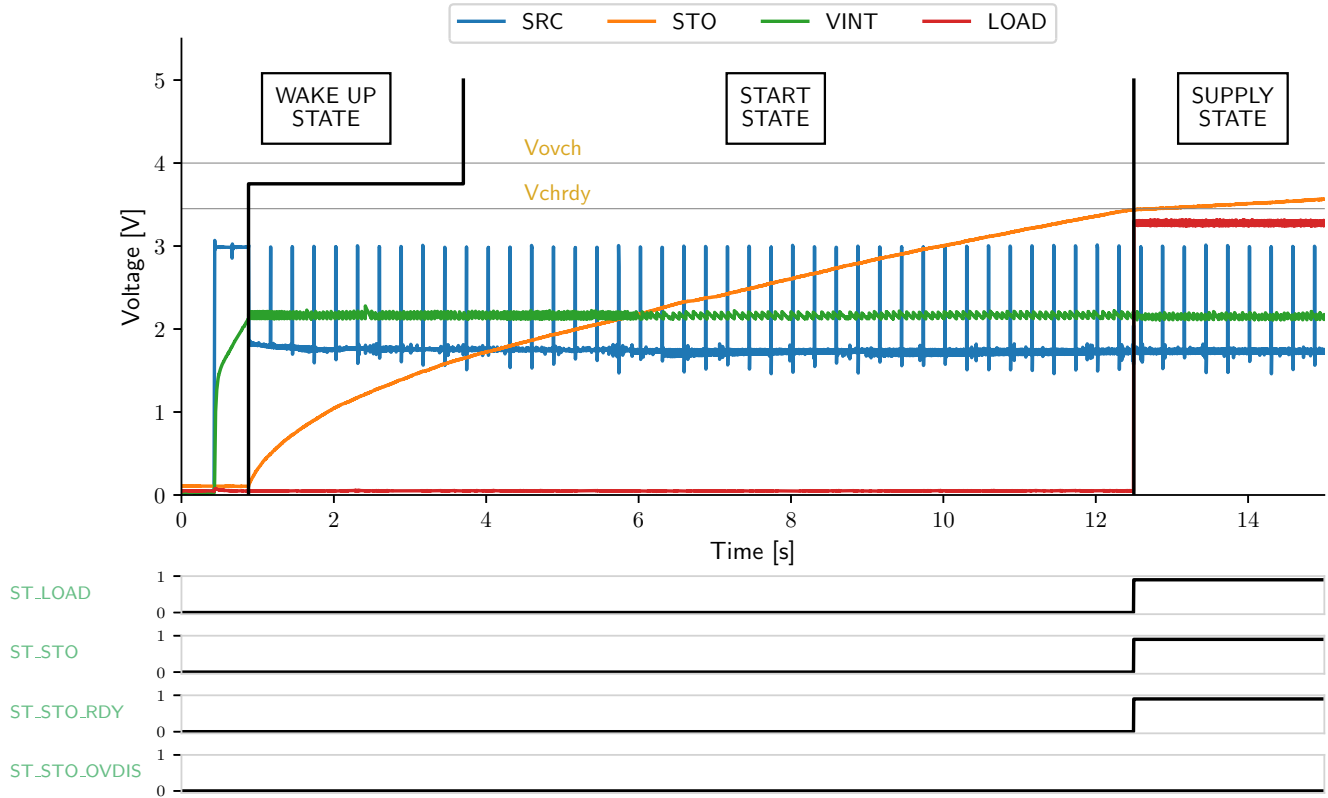


Figure 11: Wake-up state, Start state and Supply state

- **STO_CFG[3:0]** = LLLL
 - V_{OVDIS} = 3.00 V
 - V_{CHRDY} = 3.50 V
 - V_{OVCH} = 4.05 V
- **R_MPP[2:0]** = LLL (60%)
- **T_MPP[1:0]** = LL (5.19 ms / 280 ms)
- C_{STO} = 10 mF
- **SRC**: 5 mA current source with 3 V voltage compliance
- **LOAD_CFG[1:0]** = LL ($V_{LOAD,TYP}$ = 3.28 V)
- **EN_HP** = H (high power mode)
- **EN_STO_CH** = H (storage element charge enabled)
- **STO_PRIO** = H (storage element charged in priority after startup)
- **EN_SLEEP** = L (sleep mode disabled)

11.2. Supply state, Shutdown state and Reset state

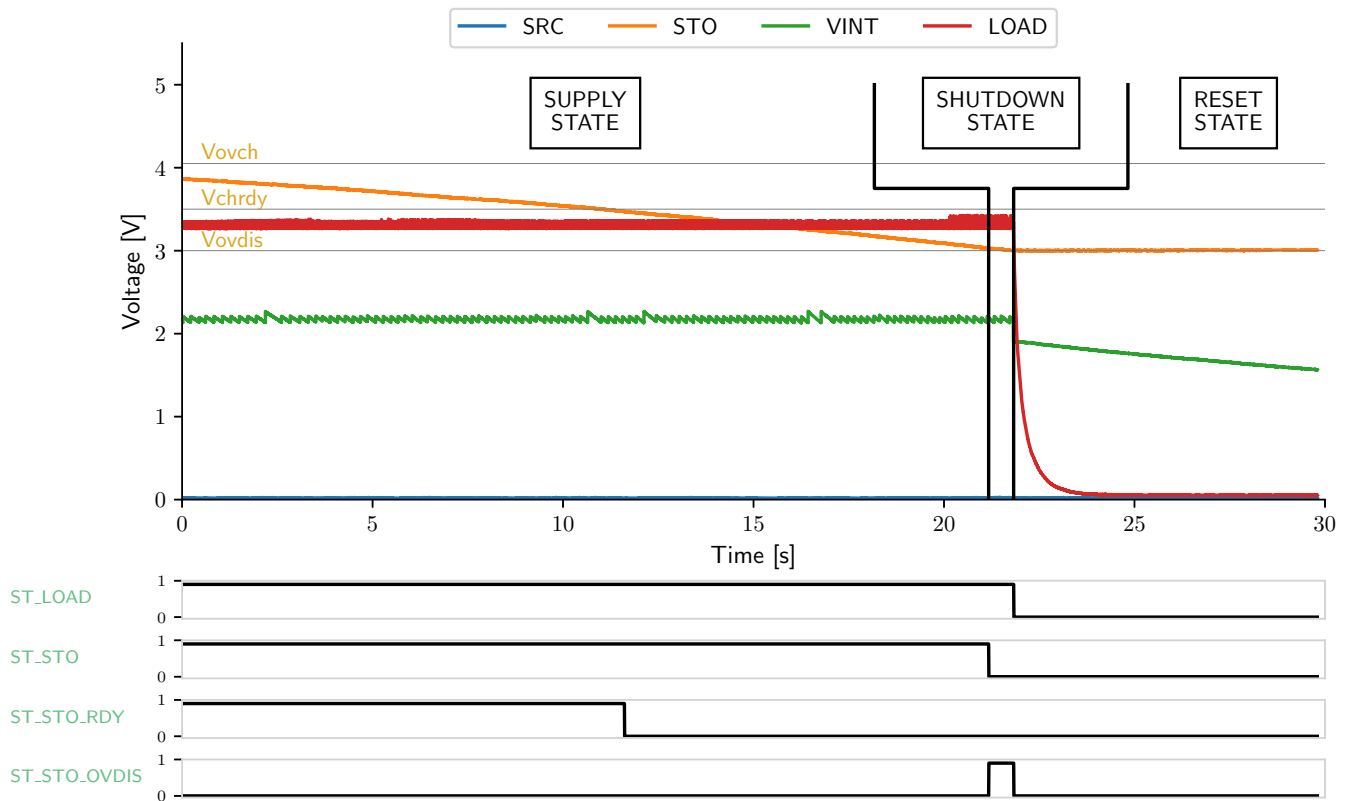


Figure 12: Supply State, Shutdown state and Reset state

- **STO_CFG[3:0]** = LLLL
 - V_{OVDIS} = 3.00 V
 - V_{CHRDY} = 3.50 V
 - V_{OVCH} = 4.05 V
- **LOAD_CFG[1:0]** = LL ($V_{LOAD,TYP}$ = 3.28 V)
- **R_MPP[2:0]** = LLL (60%)
- **T_MPP[1:0]** = LL (5.19 ms / 280 ms)
- C_{STO} = 10 mF
- **SRC**: left floating force the storage element on **STO** to discharge
- **EN_HP** = H (high power mode)
- **STO_Prio** = H (storage element charged in priority after startup)
- **EN_STO_CH** = H (storage element charge enabled)
- **EN_SLEEP** = L (sleep mode disabled)
- 10 k Ω connected between **LOAD** and GND

12. Performance Data

12.1. DCDC Conversion Efficiency From SRC to STO in Low Power Mode

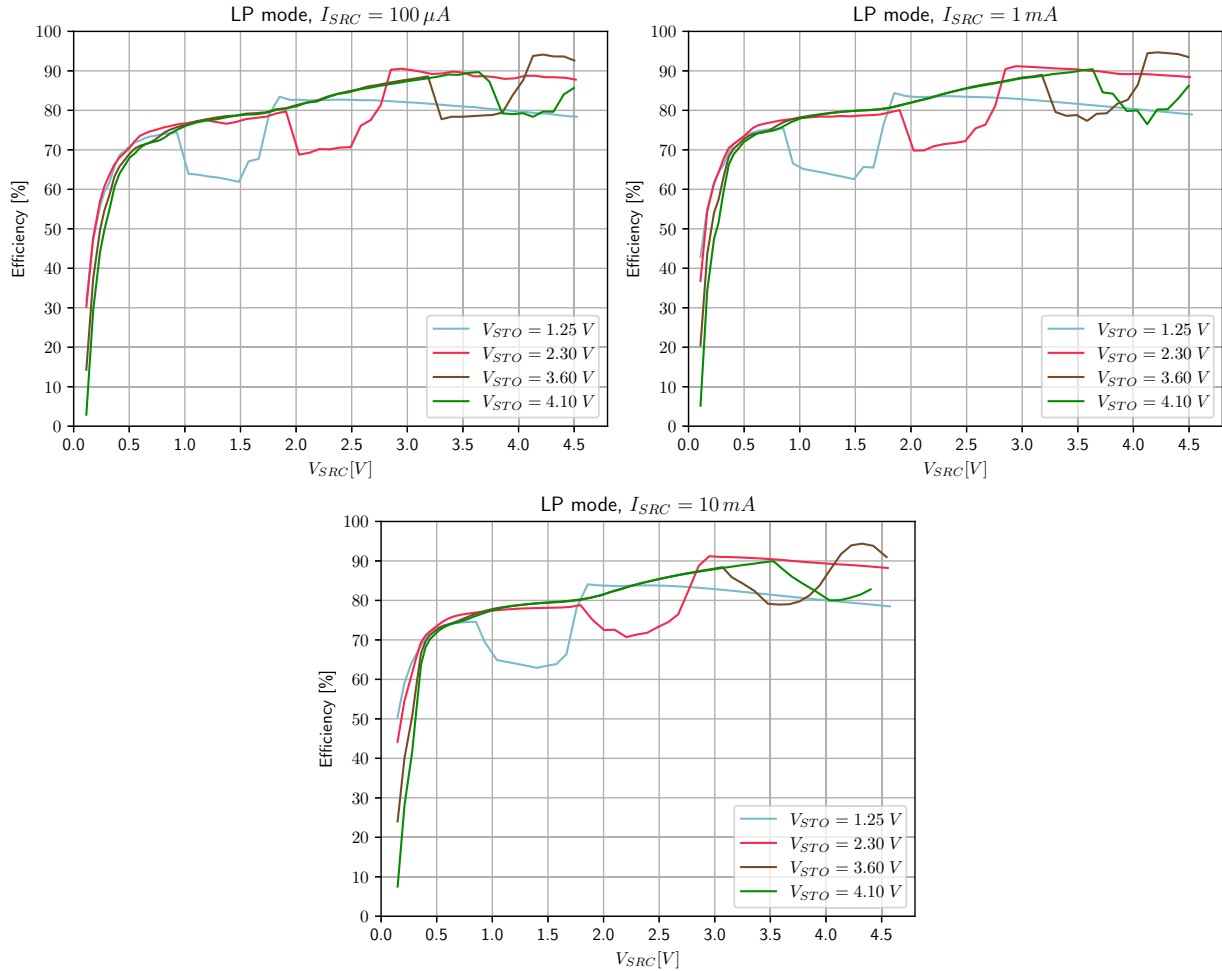


Figure 13: DCDC Efficiency from SRC to STO for 1 mA and 10 mA in Low Power Mode

12.2. DCDC Conversion Efficiency From SRC to STO in High Power Mode

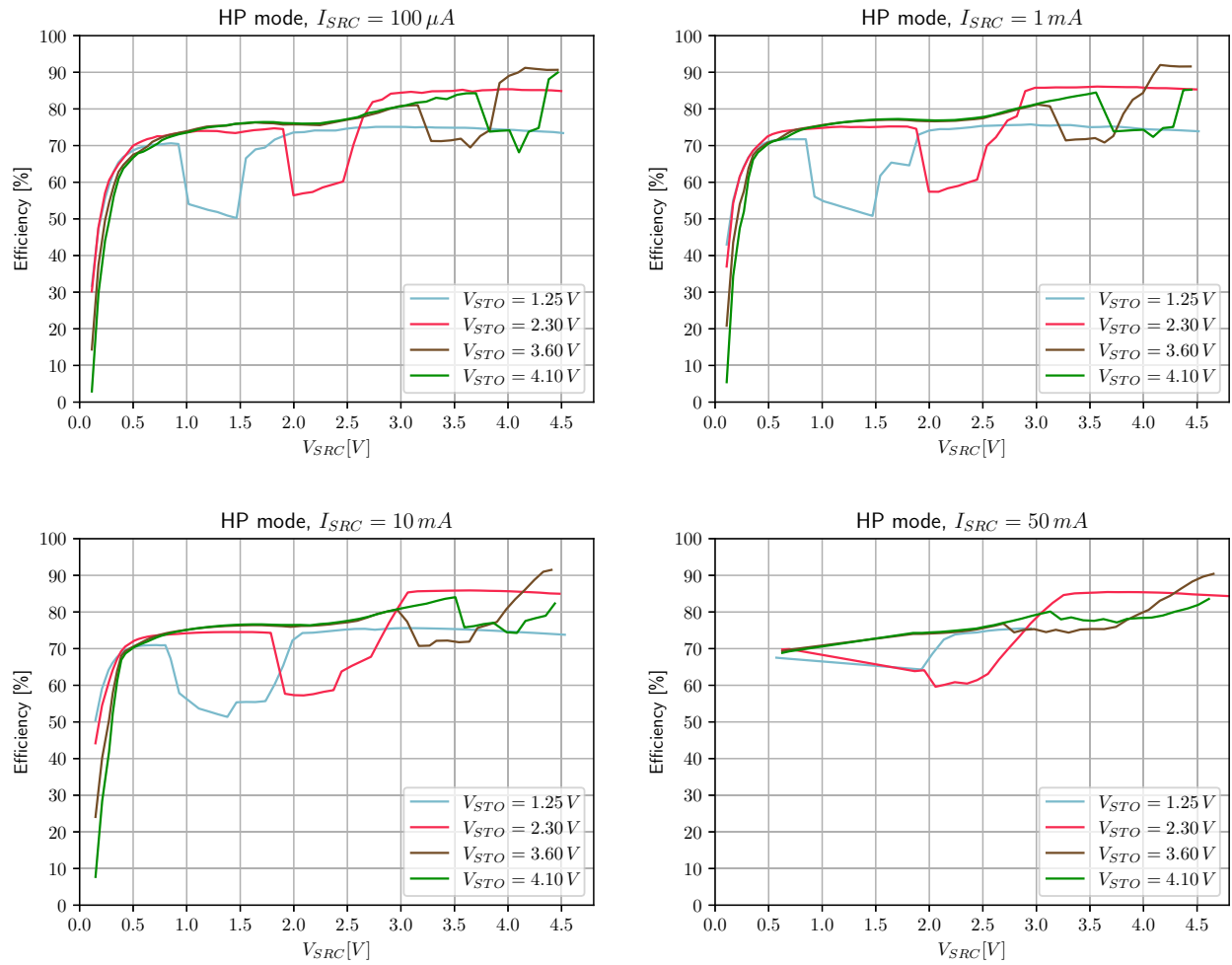


Figure 14: DCDC Efficiency from SRC to STO for 10 mA and 50 mA in High Power Mode

12.3. DCDC Conversion Efficiency From STO to LOAD in Low Power Mode

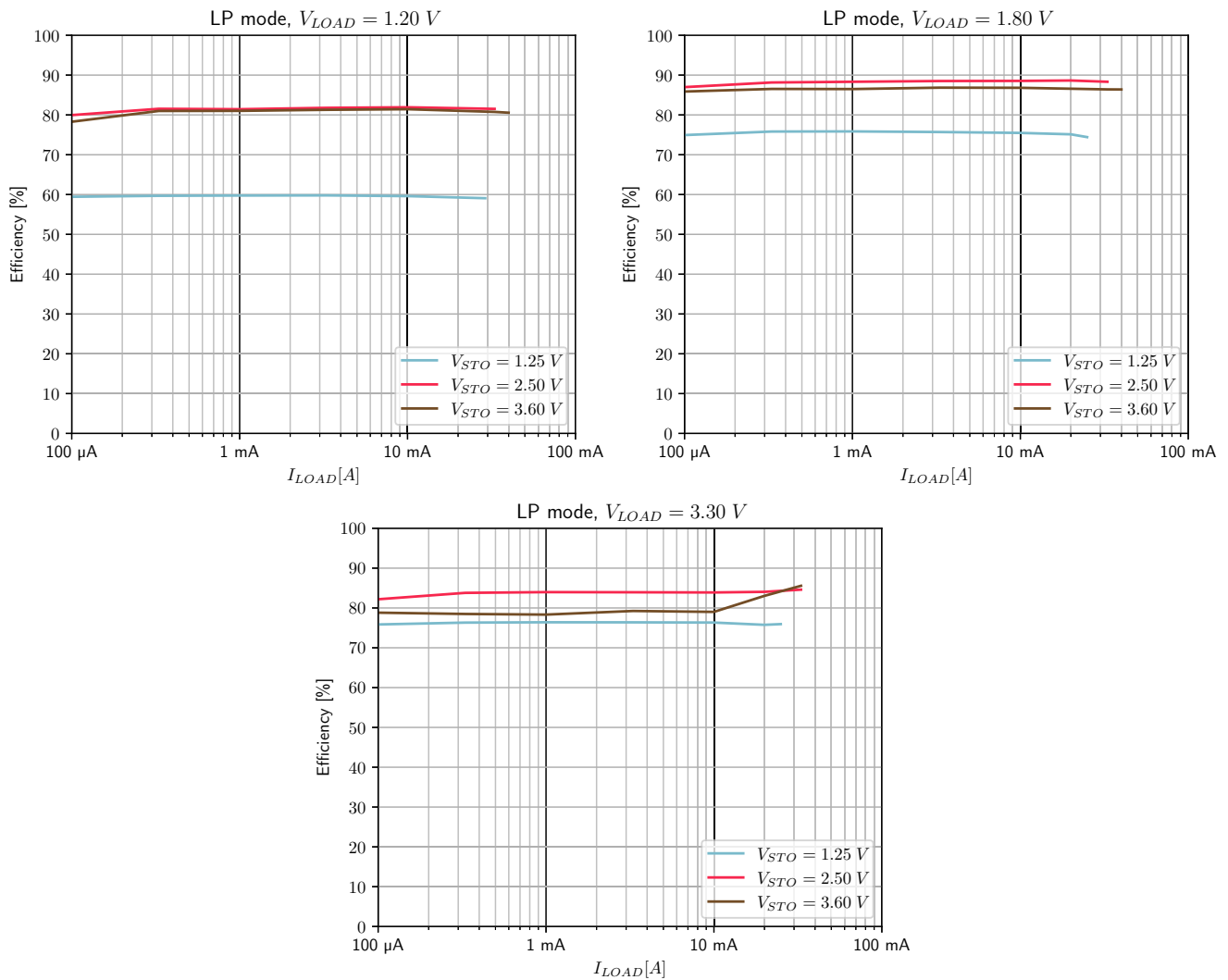


Figure 15: DCDC Efficiency from STO to LOAD in Low Power Mode

12.4. DCDC Conversion Efficiency From STO to LOAD in High Power Mode

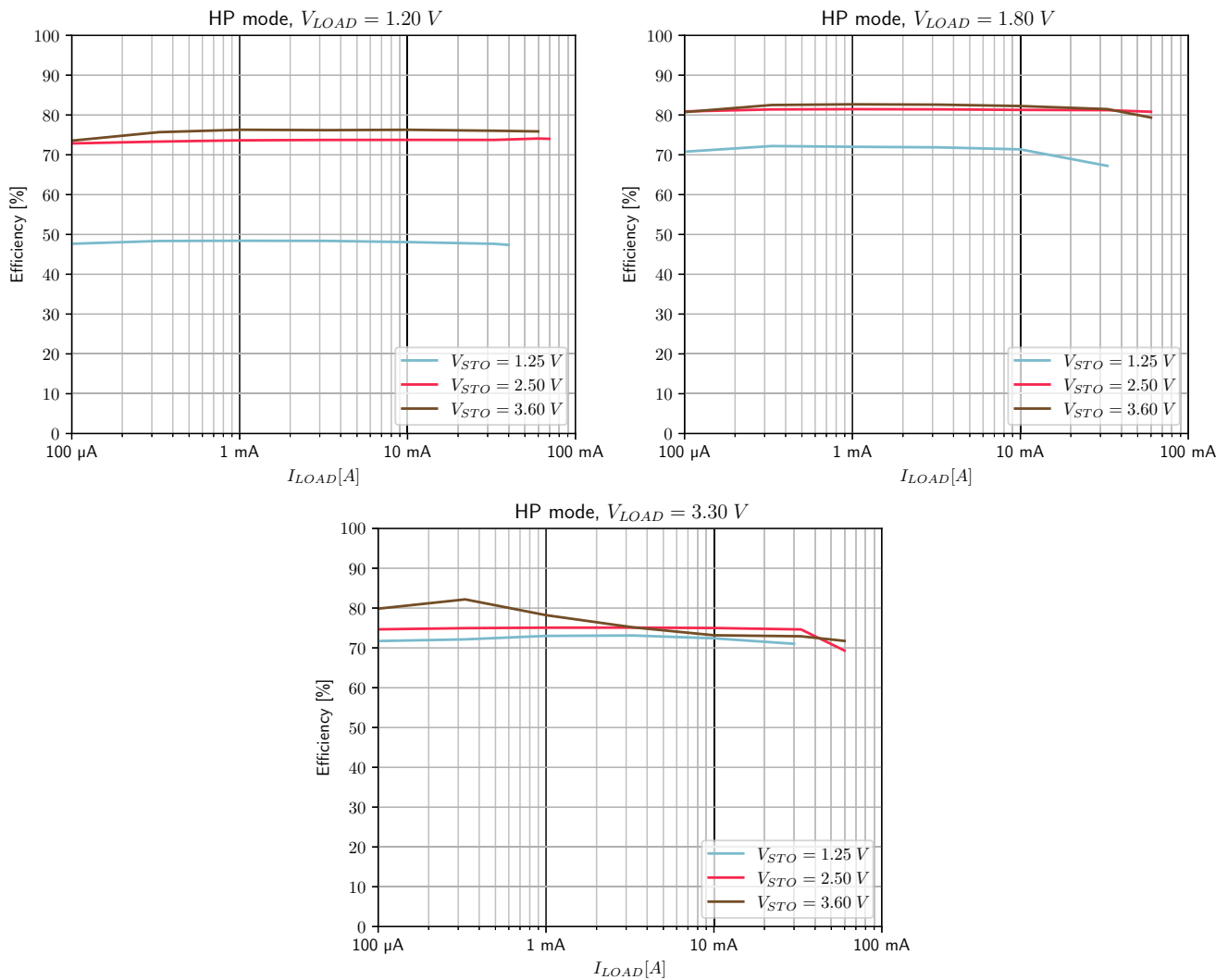


Figure 16: DCDC Efficiency from STO to LOAD in High Power Mode



12.5. Quiescent Current

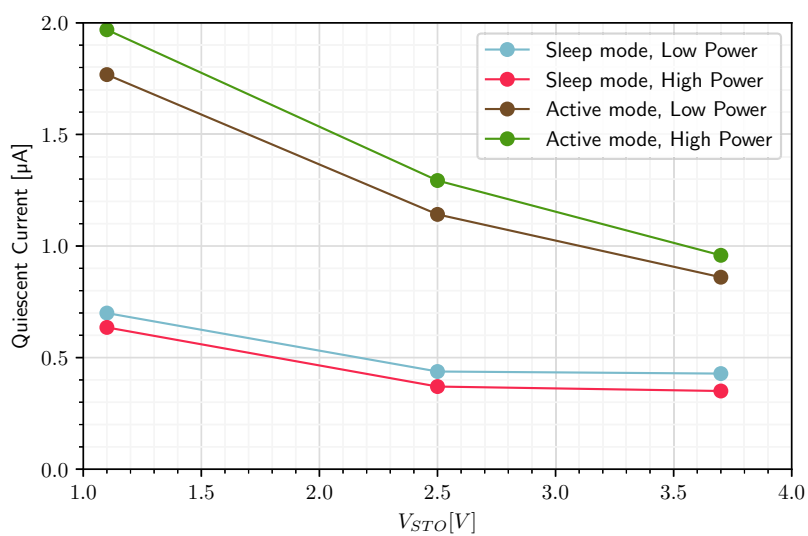


Figure 17: Quiescent Current



13. Schematic

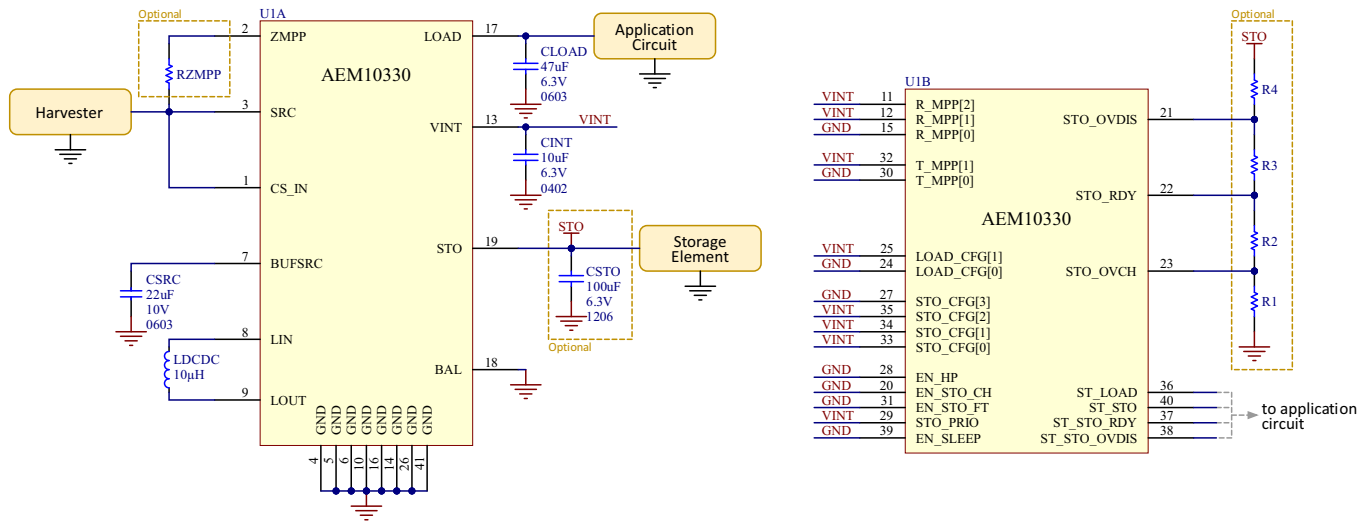


Figure 18: Schematic Example

Designator	Description	Quantity	Manufacturer	Link
U1	AEM10330 - Symbol QFN 40-pin	1	e-peas	order at sales@e-peas.com
L_{DCDC}	Power inductor 10 μ H - 1.76A	1	Murata	DFE252010F-100M
C_{LOAD}	Ceramic Cap 47 μ F, 6.3V, 20%, X5R 0603	1	Murata	GRM188R60J476ME15
C_{INT}	Ceramic Cap 10 μ F, 6.3V, 20%, X5R 0402	1	Murata	GRM155R60J106ME15
C_{SRC}	Ceramic Cap 22 μ F, 10V, 20%, X5R 0603	1	Murata	GRM188R61A226ME15D
C_{STO} (optional)	Ceramic Cap 100 μ F, 6.3V, 20%, X5R 1206	1	TDK	C3216X5R1A107M160AC

Table 12: Minimal Bill of Materials

14. Layout

14.1. Guidelines

Good layout practices are mandatory in order to obtain good stability and best efficiency with the AEM10330. It also allows for minimizing electromagnetic interferences generated by the AEM10330 DCDC converter.

The following list, while not exhaustive, shows the main attention points when routing a PCB with the AEM10330:

- The switching nodes (LIN and LOUT) must be kept as short as possible, with minimal track resistance and minimal track capacitance. Low resistance is obtained by keeping track length as short as possible and track width as large as possible between L_{DCDC} and the AEM10330 pins. Minimal capacitance is obtained by keeping distance between LIN/LOUT and other signals. We recommend removing the ground plane, the power plane and the bottom layer ground pour under L_{DCDC} footprint, as well as adding distance between LIN/LOUT and the top ground pour, as shown on Figure 19.
- The DCDC decoupling capacitors (C_{SRC} - C_{LOAD} - C_{STO}) must be placed as close as possible to the AEM10330, with direct connection and minimum track resistance for the corresponding power nodes (BUFSRC, LOAD and STO).
- The GND return path between the DCDC decoupling capacitors (C_{SRC} - C_{LOAD} - C_{STO}) and the AEM10330 thermal pad, which is the AEM10330 main GND connection, must be as direct and short as possible. This is preferably done on the top layer when possible, otherwise by internal/bottom plane, using low resistance vias to decrease layer-to-layer connection resistance.
- The external DC power connections (SRC, LOAD and STO) must be connected to the AEM10330 with low resistance tracks.
- Connection between VINT and C_{INT} must be moderately short for AEM10330 stability, even though this pins does not carry large currents. Same for connection between C_{INT} to GND.
- If used, ZMPP must be connected to the AEM10330 with a low resistance track, according to the expected SRC power.
- The BAL pin connection track must be able to handle at least 40 mA.
- The custom mode setting pins STO_OVDIS, STO_RDY and STO_OVCH are high impedance analog inputs typically connected to a resistive divider with high resistor values, making those three nodes prone to pickup noise. Thus it is recommended to keep those as short as possible and as far as possible to noise sources such as DCDC switching nodes.
- The configuration pins and the status pins have minimal layout restrictions. CS_IN maximum current is below 1 mA, so its layout restrictions are minimal as well.

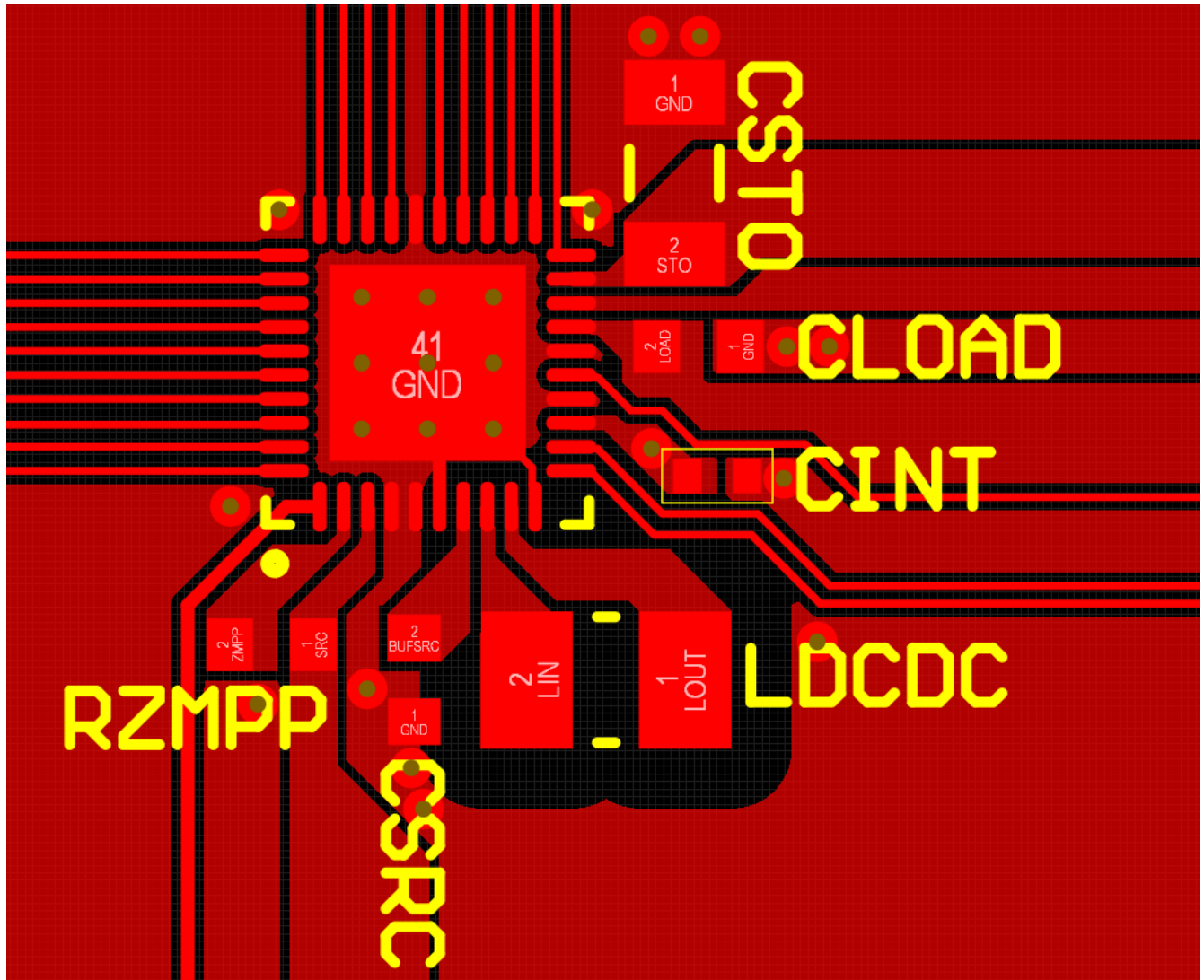
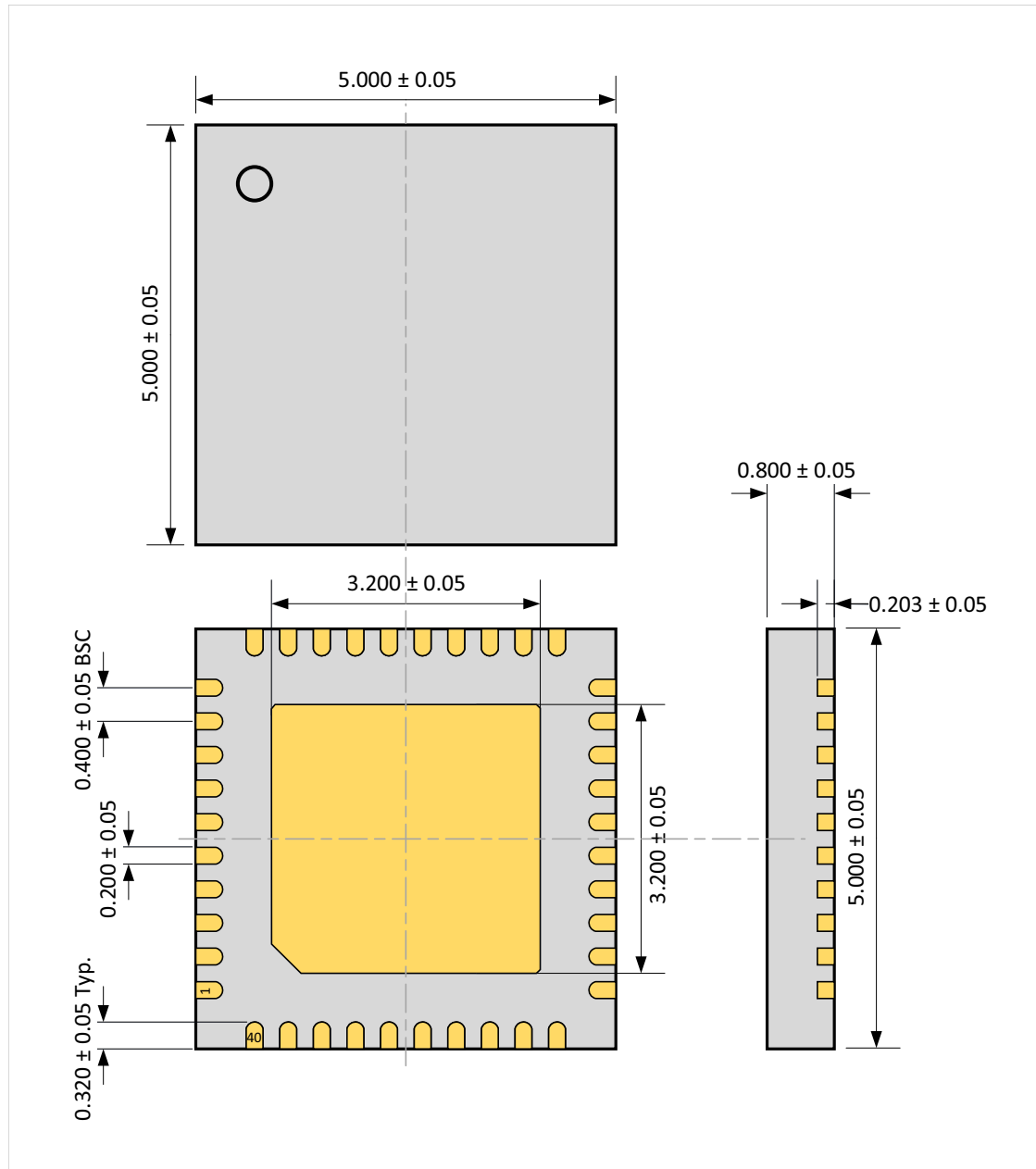


Figure 19: Layout Example for the AEM10330 and its Passive Components

NOTE: schematic, symbol and footprint for the e-peas component can be ordered by contacting e-peas support team at support@e-peas.com

15. Package Information

15.1. Plastic Quad Flatpack No-Lead (QFN 40-pin 5x5mm)



15.2. Board Layout

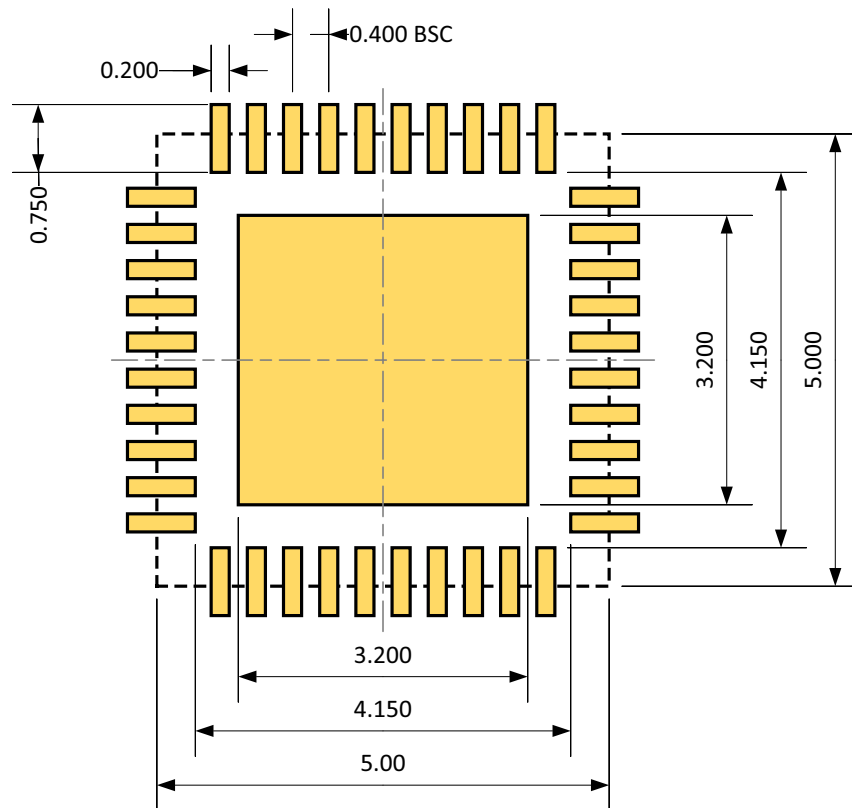


Figure 21: Recommended Board Layout for QFN40 package (All Dimensions in mm)

16. Revision History

Revision	Date	Description
0.0	January, 2021	Creation of the document. Preliminary version.
1.0	June, 2021	First version of the document
1.1	August, 2021	Minor modifications
1.2	March, 2023	- Various aesthetic improvements. - Explanations about BAL circuit. - Section with precisions about the use of CS_IN. - Removed LOAD_CFG[2] and related configurations. - New "behavior" oscilloscope graphs with improved description. - Moved various states description sections as sub-sections of a global section. - Supply State description: explanation about SRC being set to high impedance when all nodes are fully charged. - Updated "Typical use" of storage element vs STO_CFG[3:0] configuration. - Replaced "asserted/de-asserted" by "HIGH/LOW". - Changed CSRC from 15μF/0402 to 22μF/0603. - Updated "Recommended Operation Conditions" with minimum capacitor values including derating and tolerances. - Removed wrong dimension from package dimensions figure.
1.3	November, 2023	- Updated efficiency graphs. - Created section for pinout. - Updated schematics with new symbol. - Digital levels High/Low: replaced 0/1 notation by L/H. - Fixed example circuits errors. - Fixed typos and aesthetic issues. - Added layout guidelines with clearer layout examples.
1.4	February, 2024	Fixed wrong HIGH level of ST_STO in "Power and Status Pins" table.

Table 13: Revision History

Mouser Electronics

Authorized Distributor

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