Analog Reinvented

SABRE9602Q
SABRE Headphone Driver with Output Switch

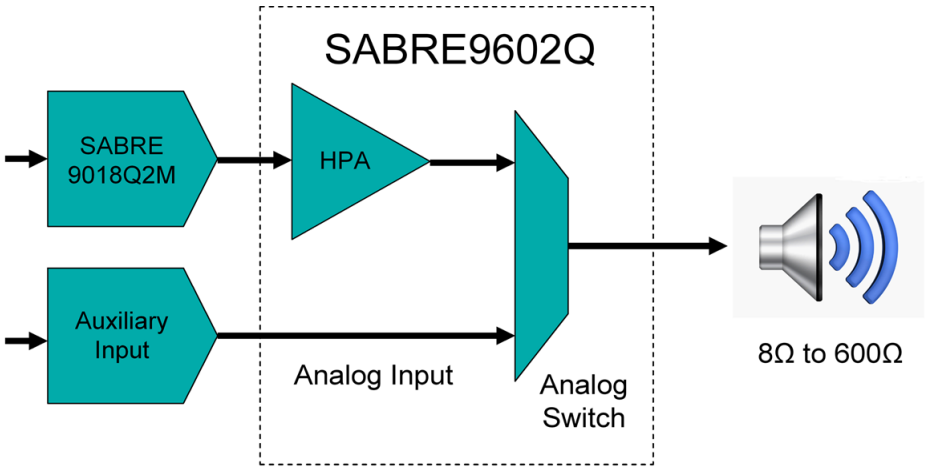
The ***SABRE9602Q Headphone Driver and Output Switch*** is the industry's highest performance, standalone headphone driver targeted for audiophile-grade portable applications such as mobile phones, tablets and digital music players.

The ***SABRE9602Q Headphone Driver and Switch*** delivers +122dB SNR and –123dB THD, a new benchmark in standalone headphone driver performance that will satisfy the most demanding audio enthusiasts.

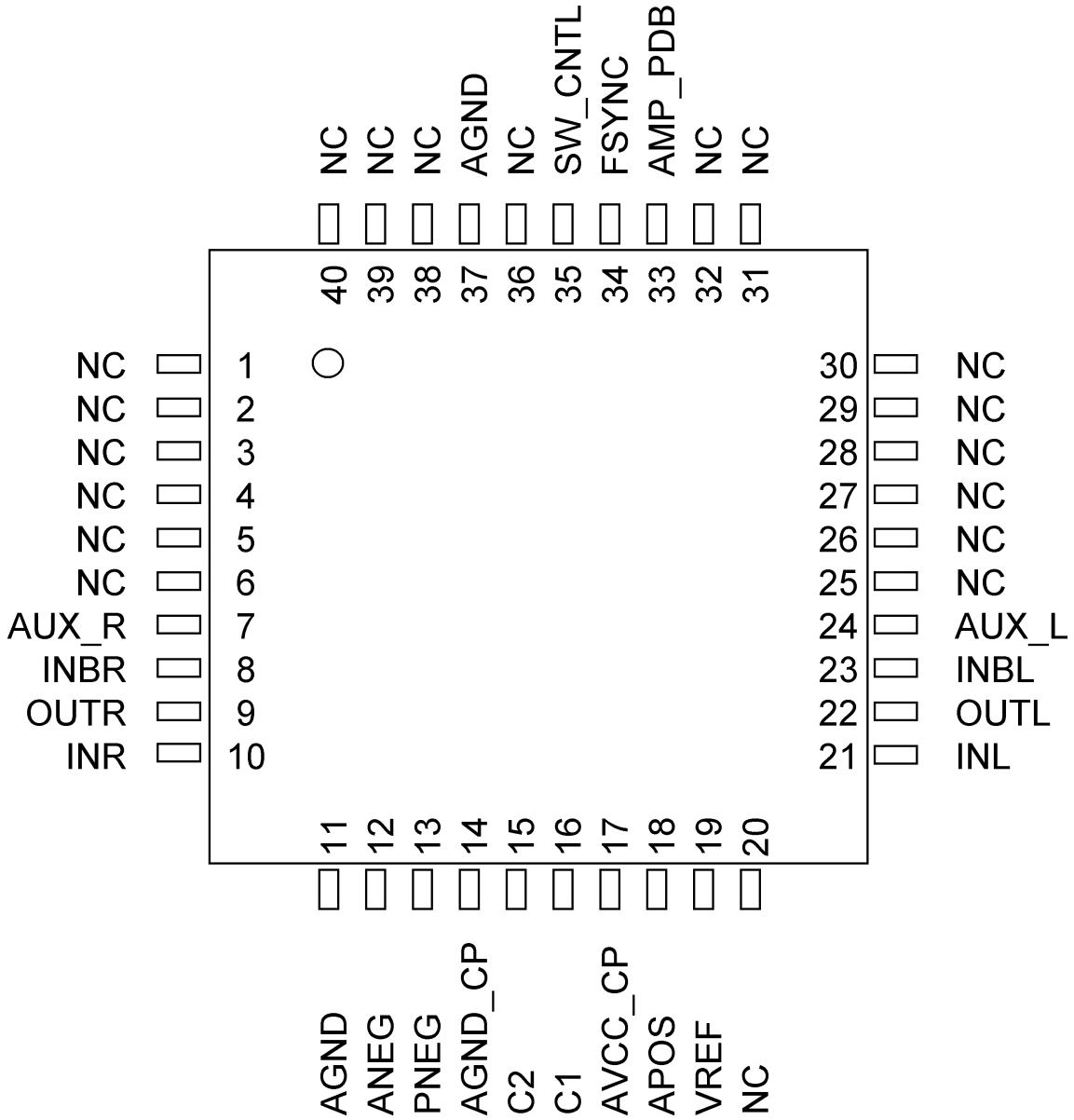
The ***SABRE9602Q Headphone Driver and Switch*** is available in a 40-pin, 5mm x 5mm QFN package.

Like ESS' high-quality SABRE^{32} Reference DACs, the ***SABRE9602Q Headphone Driver and Switch*** sets the standard for HD Audio performance with **SABRE SOUND^{TM}** quality for today's most demanding audio applications.

FEATURE	DESCRIPTION
Unmatched performance ○ +122dB SNR ○ –123dB THD, 2Vrms into 100kΩ ○ –117dB THD+N, 2Vrms into 600Ω load ○ –102dB THD+N, 49mW into 32Ω load	○ Industry's highest performance audio headphone or line-out driver for mobile applications ○ Delivers SABRE SOUND^{TM} quality all the way to the headphones
Ground-referenced output	○ Eliminates large blocking capacitors
Pop-noise suppression	○ Powers up and down without any clicks or pops
Charge pump for negative supply	○ Single AVCC operation simplifies power supply
40-QFN package, 5mm x 5mm	○ Minimizes PCB footprint
7mA / < 5μA, quiescent / standby current	○ Maximizes battery life



PIN LAYOUT


NC 1
NC 2
NC 3
NC 4
NC 5
NC 6
AUX_R 7
INBR 8
OUTR 9
INR 10
30 NC
29 NC
28 NC
27 NC
26 NC
25 NC
24 AUX_L
23 INBL
22 OUTL
21 INL
40 NC
39 NC
38 NC
37 AGND
36 NC
35 SW_CNTL
34 FSYNC
33 AMP_PDB
32 NC
31 NC
11 AGND
12 ANEG
13 PNEG
14 AGND_CP
15 C2
16 C1
17 AVCC_CP
18 APOS
19 VREF
20 NC

PIN DESCRIPTIONS

Pin	Name	I/O	Description
1 to 6	NC	–	No internal connection. May be connected to Analog Ground plane if desired
7	AUX_R	I	Auxiliary Analog Input to the Headphone Switch (Right Channel)
8	INBR	I	Differential Negative Analog Input (Right Channel)
9	OUTR	O	Headphone Amplifier Right Channel Output
10	INR	I	Differential Positive Analog Input (Right Channel)
11	AGND	Ground	Analog Ground
12	ANEG	Power	Negative Amplifier Supply Input. Connect to PNEG when the internal charge pump is being used, and connect a 22μF minimum hold capacitor to ground. Increasing the hold capacitor value will improve supply regulation but increases start-up time.
13	PNEG	Power	Negative Charge Pump Output. Connect to ANEG when the internal charge pump is being used, and connect a 22μF minimum hold capacitor to ground. Increasing the hold capacitor value will improve supply regulation but increases start-up time. PNEG is left open when an external –3.3V supply is used.
14	AGND_CP	Ground	Analog Ground for the Charge Pump
15	C2	–	Negative Analog Flying Capacitor. Connect a 4.7μF, low-ESR ceramic capacitor between C1 & C2
16	C1	–	Positive Analog Flying Capacitor. Connect a 4.7μF, low-ESR ceramic capacitor between C1 & C2
17	AVCC_CP	Power	Analog Power for the Charge Pump
18	APOS	Power	Positive Supply for Headphone Amplifiers. Decouple with a 22μF minimum, low-ESR ceramic capacitor to ground
19	VREF	–	Reference Voltage. A 4.7μF X7R dielectric, ceramic capacitor must be connected between pin 19 and AGND, see Figure 2. The capacitor controls power up and power down of the AUX input switch and the value specified ensures click-less operation
20	NC	–	No internal connection. May be connected to Analog Ground plane if desired
21	INL	I	Differential Positive Analog Input (Left Channel)
22	OUTL	O	Analog Left Channel Output
23	INBL	I	Differential Negative Analog Input (Left Channel)
24	AUX_L	I	Auxiliary Analog Input to the Headphone Switch (Left Channel)
25 to 32	NC	–	No internal connection. May be connected to Analog Ground plane if desired
33	AMP_PDB	I	Active-low Power Down (High for normal operation)
34	FSYNC	I/O	Oscillator drive signal. FSYNC can be used to synchronize multiple devices together using the same charge-pump frequency. Charge pump internal frequency is typically 120kHz with a 0-3.3V amplitude.
35	SW_CNTL	I	Control Input for the Headphone Output Switch. Active-low for HPA signal.
36	NC	–	No internal connection. May be connected to Analog Ground plane if desired
37	AGND	Ground	Analog Ground
38 to 40	NC	–	No internal connection. May be connected to Analog Ground plane if desired
–	PAD	Ground	Exposed pad. Connect to Analog Ground plane for heatsinking

FUNCTIONAL DESCRIPTION

The SABRE9602Q has a pair of CMOS FET input amplifiers that exhibit a total A-weighted SNR of better than 122dB when driving 2Vrms into a 600Ω load. The SABRE9602 has an open-loop gain in excess of 120dB which together with the input stage linearity is the key to its unparalleled –123dB distortion performance. Please note that the amplifier distortion performance far exceeds that of typical external passive components. Therefore, to achieve the THD performance specified for the SABRE9602Q, ensure that the external resistors have a very low, voltage coefficient of resistance, e.g. thin film resistors. Close tolerance ±0.1% thin-film resistors are recommended for all gain-defining components.

Charge Pump

The SABRE9602Q features a low-noise charge pump. The 120kHz switching frequency is above the audio band and, thus, does not interfere with audio signals. The switches are controlled by turn-on and turn-off transistors in a particular sequence that minimizes pops and clicks. The IC requires a 4.7μF minimum flying capacitor between pins C1 and C2 and a 22μF minimum hold capacitor from PNEG to AGND_CP. The chip's FSYNC pin offers three connection options: capacitance may be added from FSYNC to ground to slow down the oscillator (100kHz minimum), a logic signal can drive the FSYNC pin to set a fixed frequency, or the FSYNC pins of several SABRE9602Q chips may be connected together to force them to run synchronously. When driving the FSYNC pin from an external oscillator, the frequency should be in the range 450kHz to 2.5MHz. The charge pump's internal switching rate is actually at FSYNC/4 so it is easy to interfere with the audio band with only modest changes in the FSYNC frequency.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range select capacitors with a minimum X5R dielectric, the X7R dielectric is preferred. The charge pump can be disabled by grounding FSYNC which reduces quiescent current from the +3.3V supply. Disabling the charge pump is recommended when using an external –3.3V supply connected to ANEG.

Flying Capacitor (C4, see Figure 2)

The value of the flying capacitor (C4, connected across pins C1 and C2) affects the charge pump's load regulation and output resistance. A capacitance value (C4) that is too small reduces the current drive capability, which leads to a loss of output voltage. Increasing the value of C4 improves load regulation and reduces the charge-pump output resistance to an extent. With a 4.7μF flying capacitor, the on-resistance of the switches dominates. Use a low-ESR ceramic or electrolytic capacitor for C4. If an electrolytic capacitor is used the correct polarity must be observed, see Figure 2. The flying capacitor C4 can be eliminated when an external –3.3V supply is used & the internal oscillator is disabled by grounding the FSYNC pin.

Hold Capacitor (C2, see Figure 2)

The value of the hold capacitor C2 (connected between ANEG/PNEG and ground) and its Equivalent Series Resistance (ESR) directly affects the ripple voltage at PNEG. Use a low-ESR 22μF minimum capacitor for C2 and also choose the correct voltage rating. C2 can be a ceramic or electrolytic capacitor, if an electrolytic capacitor is used, the correct polarity must be observed, see Figure 2. Increasing the value of the hold capacitor will improve regulation but will increase start-up time.

Amplifier Gain

The recommended gain setting for SABRE9602Q is 0dB (Unity Gain). The feedback resistors R2 and R10 of Figure 2 should match the output impedance of the DAC or other signal source. For example, when working with the ES901xK2M, only the feedback resistors, R2 and R10, are required. The recommend value in this configuration is 806Ω which gives the best DNR.

Compensation Components (see Figure 2)

For optimum performance, the following capacitors should be included in all configurations of the SABRE9602Q. C1 and C6 control the bandwidth of the SABRE9602Q, along with the matching networks C3 and C5. These compensation capacitors should have a low temperature coefficient of capacitance, NP0/C0G types are recommended.

Driving a Low-Impedance Load

In order to drive a load of 32Ω or less it may be necessary to use an external –3.3V supply depending on the load's power requirements. When using an eternal negative supply, it is advisable to disable the internal charge pump by connecting FSYNC (pin 34) to analog ground. PNEG (pin 13) is left open, and the external –3.3V supply is connected to ANEG with a 22μF (minimum) decoupling capacitor (C2). Please check the polarity on C2. To prevent clicks/pops at startup and shutdown the +3.3V and –3.3V supplies should be sequenced. The +3.3V must be ON and stay ON before connecting or disconnecting the –3.3V external supply.

Short-Circuit Protection (see Figure 2)

To protect the SABRE9602Q under short-circuit conditions 4.7Ω resistors should be placed in series with each output, OUTL and OUTR, but the resistors should be inside the feedback loop.

Output Switch

The headphone output is selected by an ultra-low THD analog switch that connects either to the HD audio headphone amplifier or to an alternate audio source (inputs AUX_L and AUX_R). The auxiliary input may be a voice or lo-fi music signal in a cell phone application. The ultra-low ON-resistance analog switch introduces minimal THD whether it's set to the built-in SABRE headphone amplifier or the alternate source. The switch control input SW_CNTL (pin 35) is active-low, connecting the headphone amplifier to the headphones when grounded. The auxiliary inputs are enabled when the SW_CNTL input is high and the headphone amplifier is shut down by pulling the AMP_PDB pin low. If the AMP_PDB pin is high, the SW_CNTL pin has no affect. A capacitor, C7 in Figure 2, connected between VREF (pin 19) and AGND controls the power up and power down of the output switch. The value specified for C7 ensures click-less operation of the switch.

SABRE9602Q Block Diagram

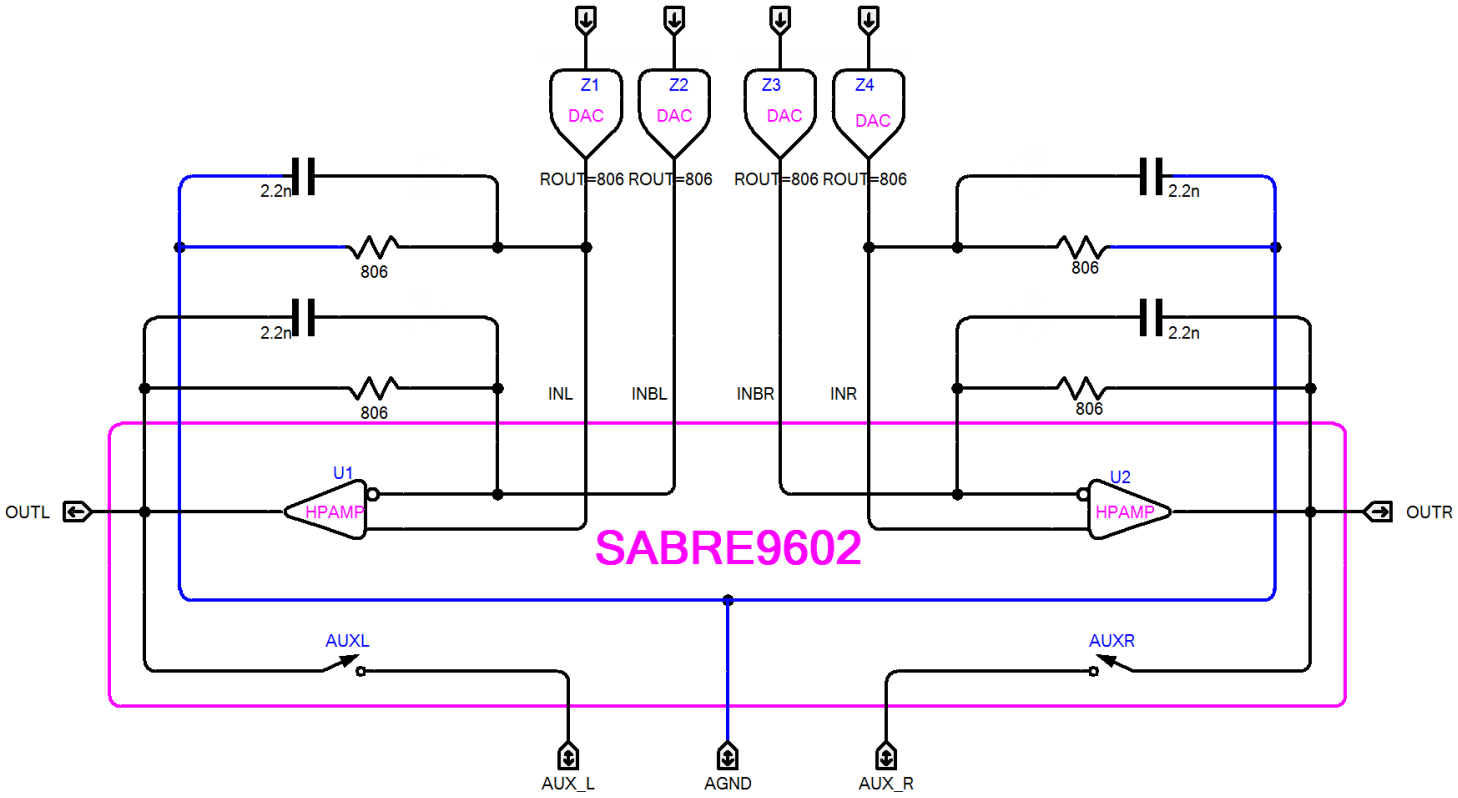


Figure 1. Block Diagram of the SABRE9602Q plus external Gain Setting and Compensation Components.

APPLICATION DIAGRAM

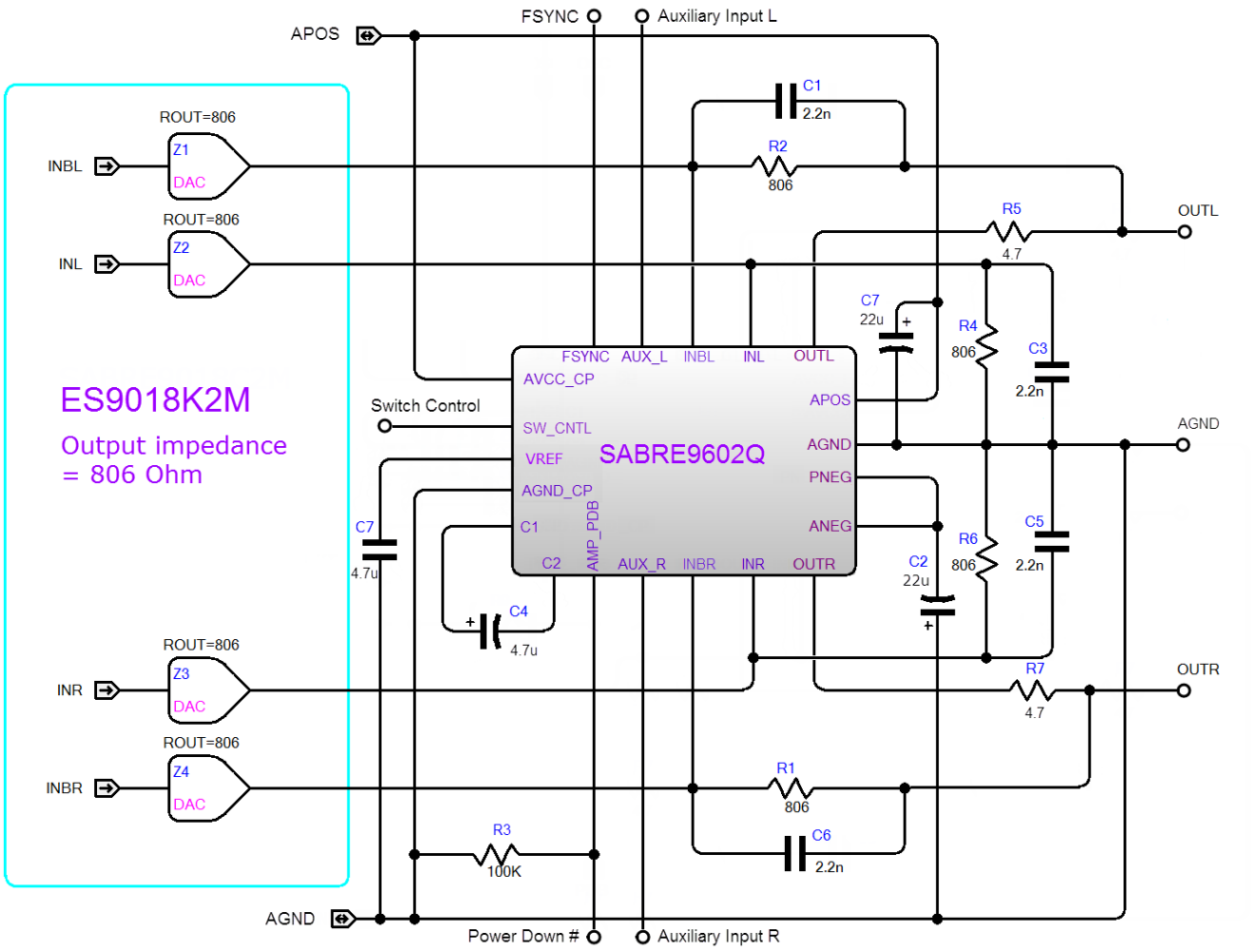


Figure 2. Simplified SABRE9602Q Application Circuit.

APPLICATION DIAGRAM

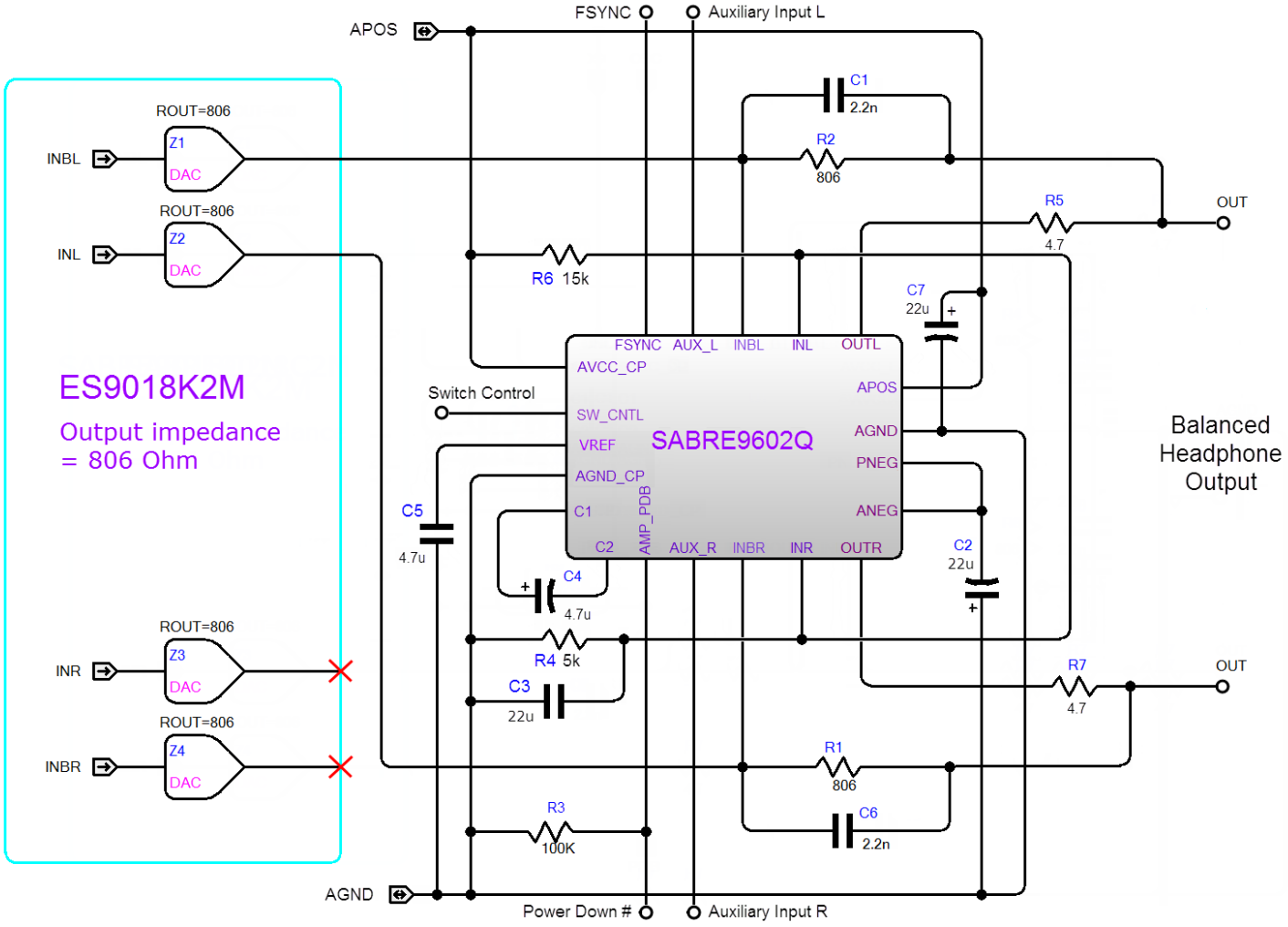


Figure 3. SABRE9602Q configured to drive Balanced Headphones (single channel).

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Storage temperature	–65°C to +105°C
Voltage range for digital input pins	–0.3V to AVCC+ 0.3V
ESD Protection Human Body Model (HBM) Machine Model (MM)	 2000V 200V

WARNING: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature Range	T_A	–20°C to +70°C

Power Supply	Symbol	Voltage	Quiescent Current (Note 1)	Standby Current (Note 2)
Analog power supply voltage	AVCC_CP APOS	+3.3V ± 5%	7mA typical	300µA typical
Analog power supply voltage (Headphone amplifier disabled)	AVCC_CP APOS	+3.3V ± 5%	300µA typical (AUX input enabled)	< 5µA (AUX input disabled)
Power Supply		**Load Resistance**	**Supply Current (Note 3)**	**Output Voltage (Note 4)**
Analog supply current at +3.3V	I_{SY}	32Ω	50mA typical	800mVrms @ 1kHz

Notes

1) Input idling, output unloaded, internal oscillator, all external supply voltages at nominal center values
2) AMP_PDB held low, AUX inputs active
3) Supply current is with both outputs loaded and driven at 800mVrms
4) 800mVrms sine wave across 32Ω load produces a 20mW output

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Minimum	Maximum	Unit
VIH	High-level input voltage	1.4		V
VIL	Low-level input voltage		0.4	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current	I_B	INL, INBL, INR, INBR inputs	–1.0	0.1	+1.0	nA
Output Offset Voltage	V_{OS}	OUTL to AGND & OUTR to AGND, no input signal	–2.0	0.1	+2.0	mV

ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

T_A = 25ºC, AVCC_CP = APOS = +3.3V, 1kHz signal, C2 = 22µF, C4 = 4.7µF, ANEG = PNEG (Figure 2 configuration)

1. SNR / DNR: A-weighted over 20Hz-20kHz in averaging mode
2. THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	VOUT = 2.0Vrms, A-weighted, RL = 600Ω		122		dB
Total Harmonic Distortion	THD	VOUT = 2.0Vrms, RL = 100kΩ		–123		dB
Total Harmonic Distortion plus Noise	THD+N	VOUT = 2.0Vrms, RL = 600Ω		–117		dB
		POUT = 49mW into 32Ω load		–102		dB
External FSYNC range	FSYNC	FSYNC pin is driven by an external oscillator	450		2500	kHz
Power Supply Rejection	PSR	fin = 217Hz, 200mVp-p ripple		–89		dB
		fin = 1kHz, 200mVp-p ripple		–89		dB
		fin = 10kHz, 200mVp-p ripple		–82		dB
AUXILIARY ANALOG INPUTS						
Input Voltage		Ground referenced			1.0	Vrms

Test Conditions (unless otherwise stated)

T_A = 25ºC, AVCC_CP = APOS = +3.3V, 1kHz signal, C2 = 22µF, C4 = 4.7µF, FSYNC pin grounded, ANEG = –3.3V external supply

1. SNR / DNR: A-weighted over 20Hz-20kHz in averaging mode
2. THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	VOUT = 2.0Vrms, A-weighted, RL = 600Ω		122		dB
Total Harmonic Distortion plus Noise	THD+N	POUT = 49mW into 32Ω load		–102		dB
		1.3Vrms into 16Ω load		–106		dB
		1.0Vrms into 8Ω load		–102		dB

TYPICAL PERFORMANCE CURVES

The following typical performance curves are generated using ESS' evaluation board as shown in Figure 11. The internal charge pump is used to supply the negative rail. Measurements are taken using an Audio Precision Audio Analyzer. Note that all measurements in the graphs include errors due to the test equipment plus those of the ES9018K2M DAC on the evaluation board. Although these errors are very low, they are significant when measuring a state-of-the-art headphone amplifier like the SABRE9602Q. Therefore the parametric values shown in the characteristic curves are slightly degraded compared to the values in the tables as the latter are calculated from measurements in near-ideal conditions.

TYPICAL PERFORMANCE CURVES

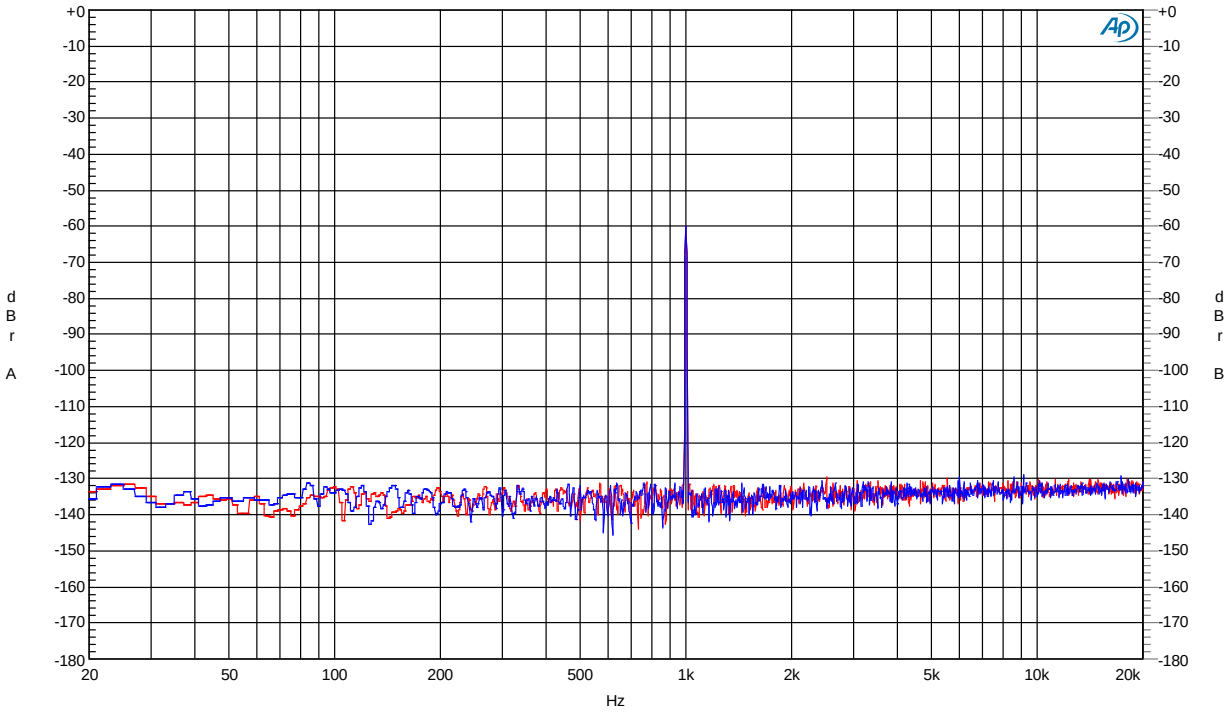


Figure 4. DNR FFT, 1kHz @ –60dB, Single-Ended, 32Ω Load

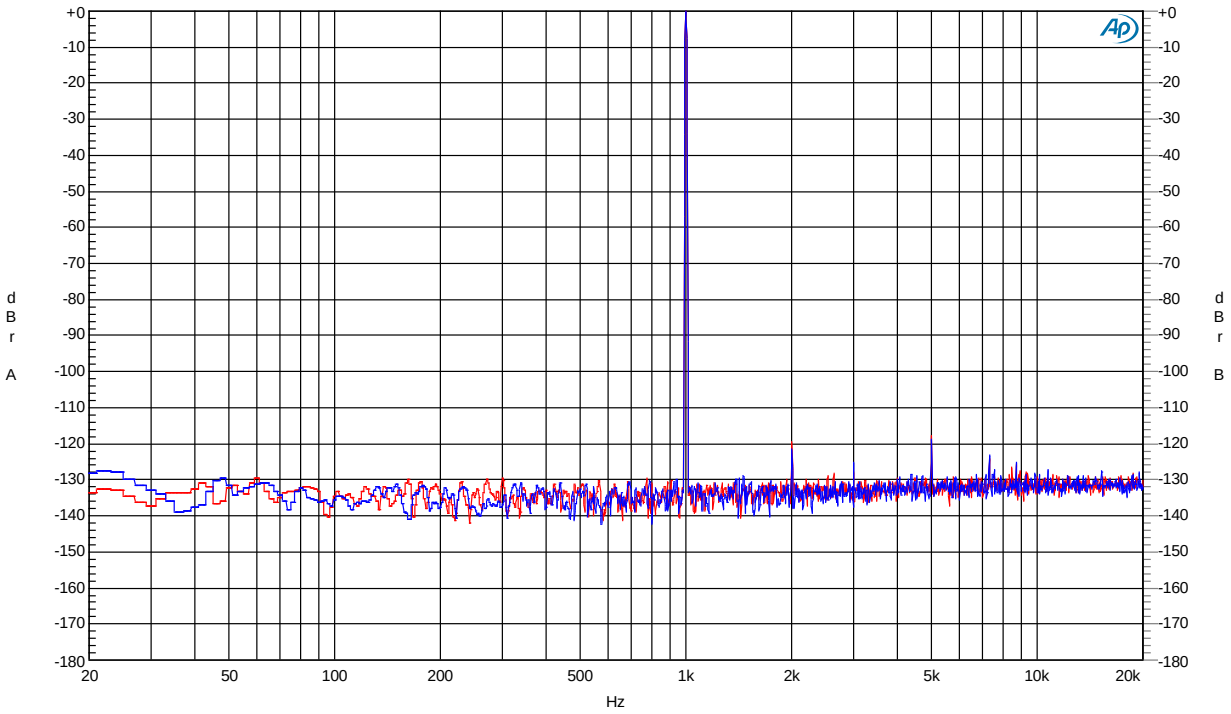


Figure 5. THD+N FFT, 1kHz @ –6dB, Single-Ended, 32Ω Load

TYPICAL PERFORMANCE CURVES

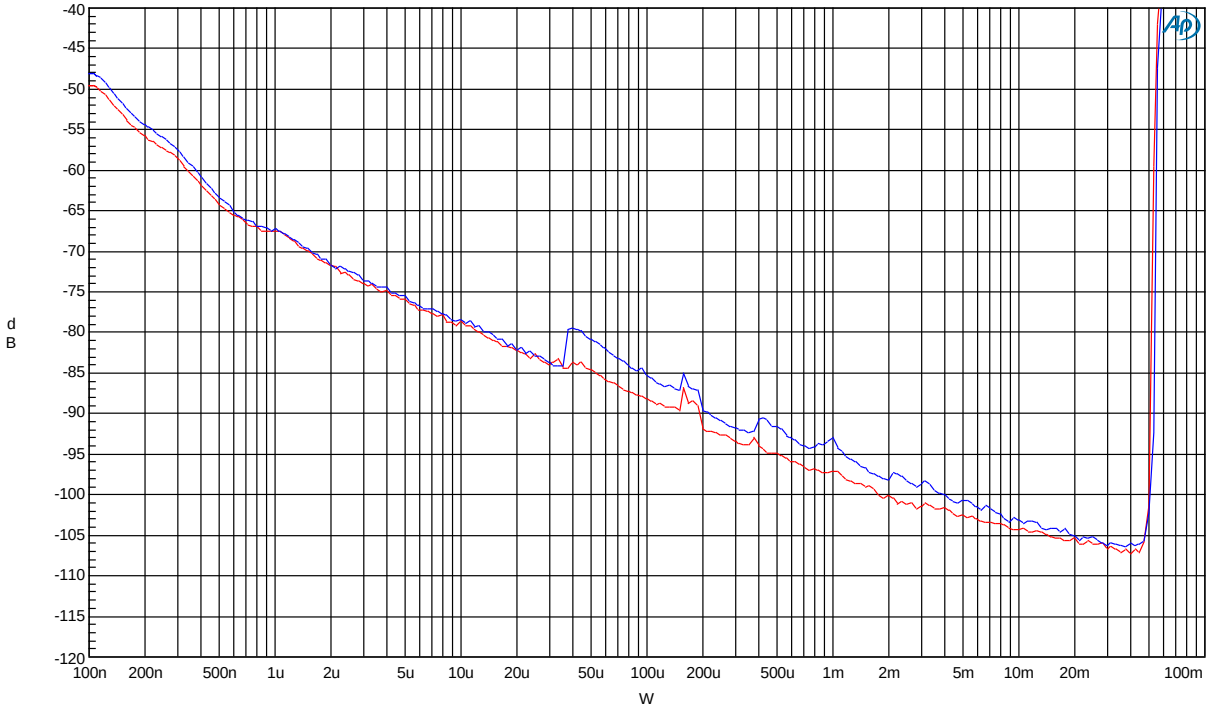


Figure 6. THD+N Unweighted vs. Output Power, Dual Channel Drive, Single Ended, 32Ω Load

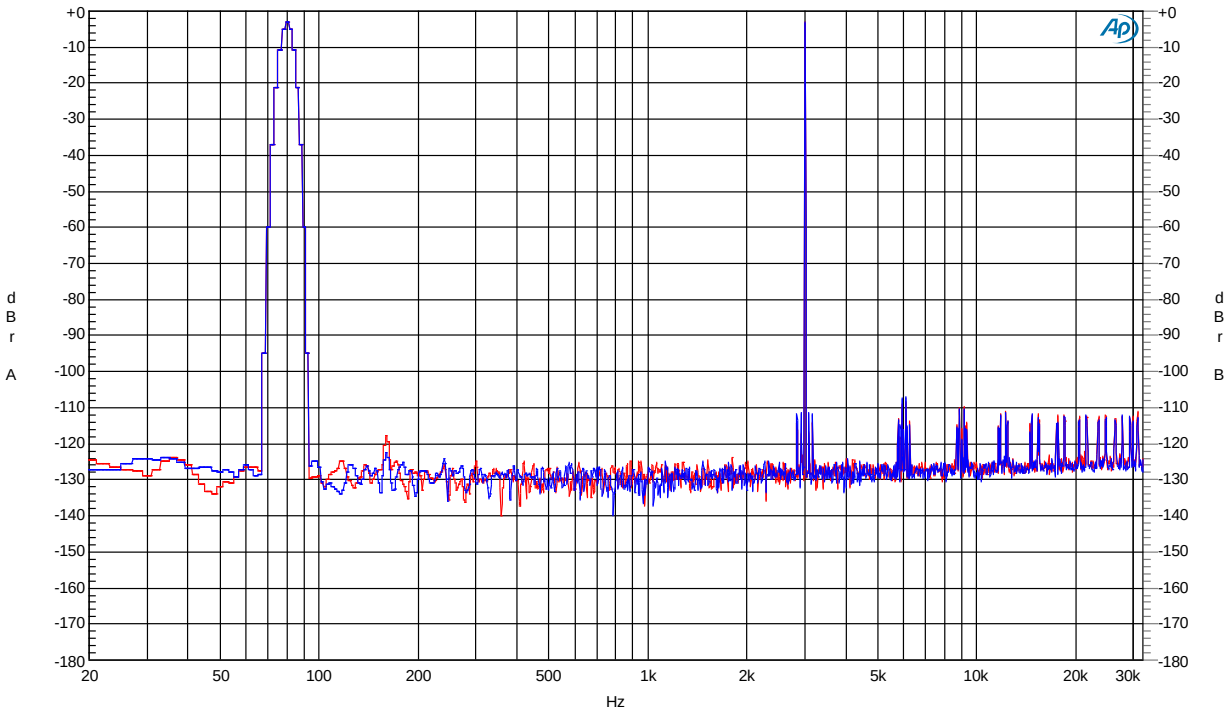


Figure 7. IMD FFT, 3kHz & 80Hz @ SMPTE 1:1, Single Ended, 32Ω Load

TYPICAL PERFORMANCE CURVES

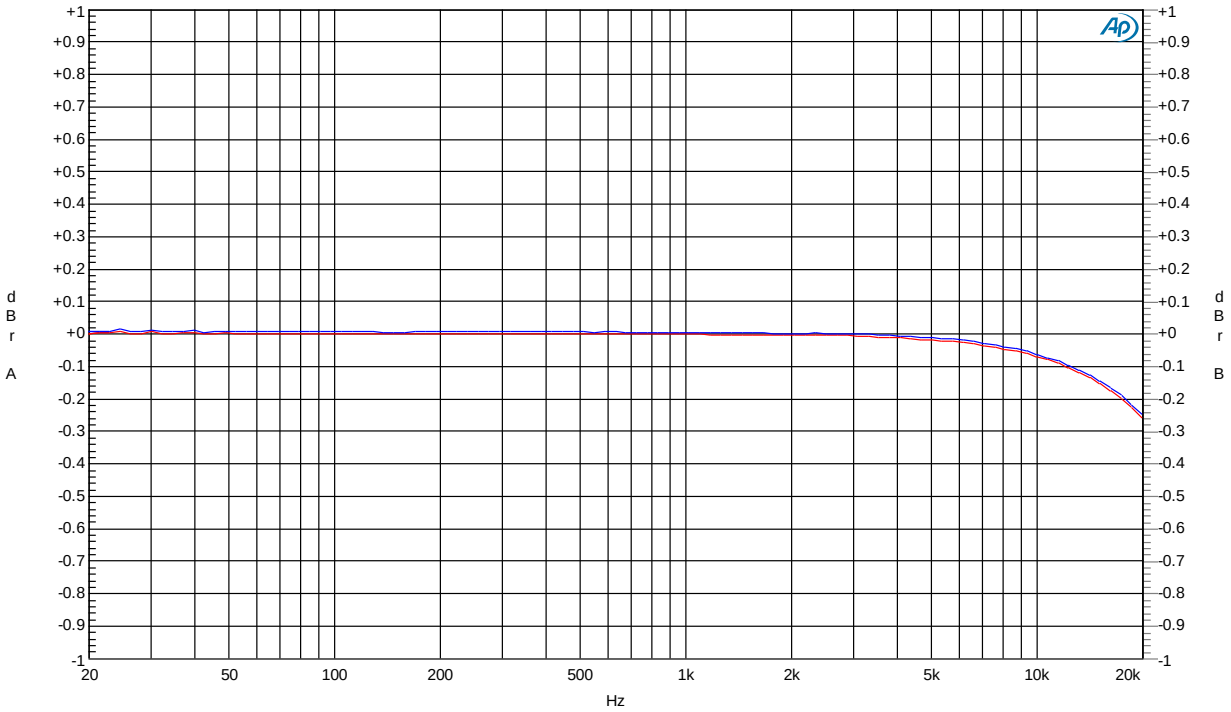


Figure 8. Frequency Response, 20Hz to 22kHz @ 0dB, Log Scale, Single Ended, 32Ω Load

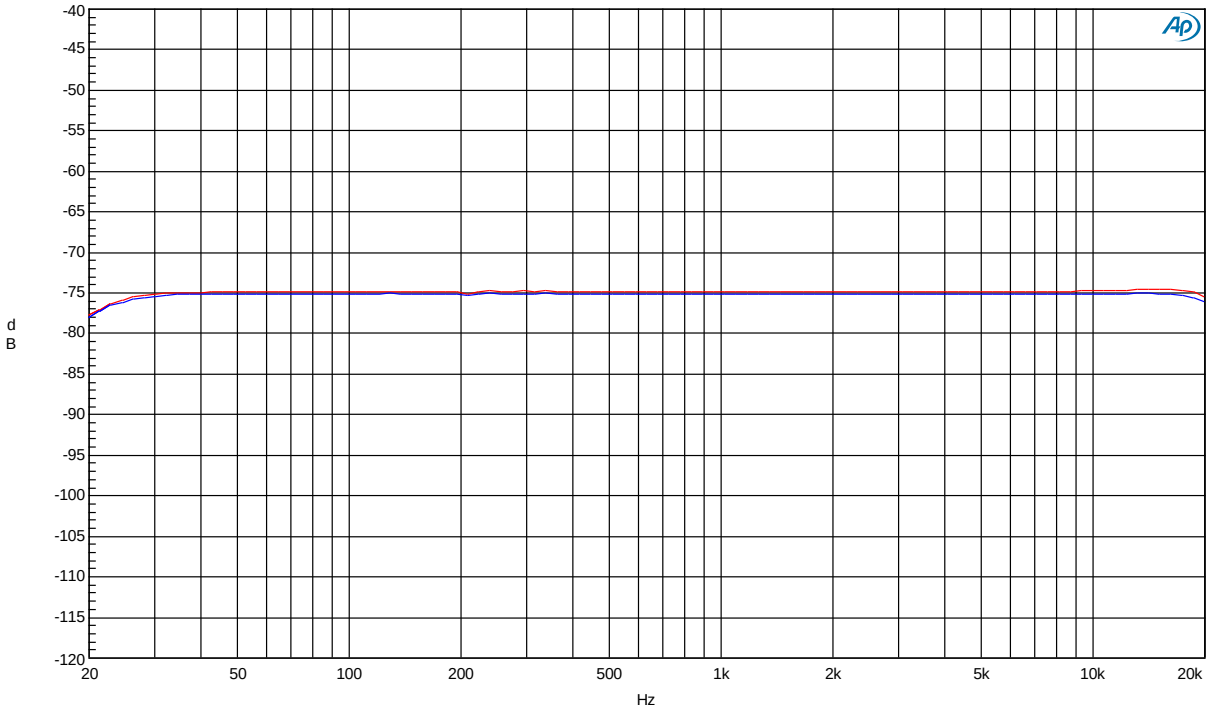


Figure 9. Crosstalk vs. Frequency, Single Ended, 32Ω Load

TYPICAL PERFORMANCE CURVES

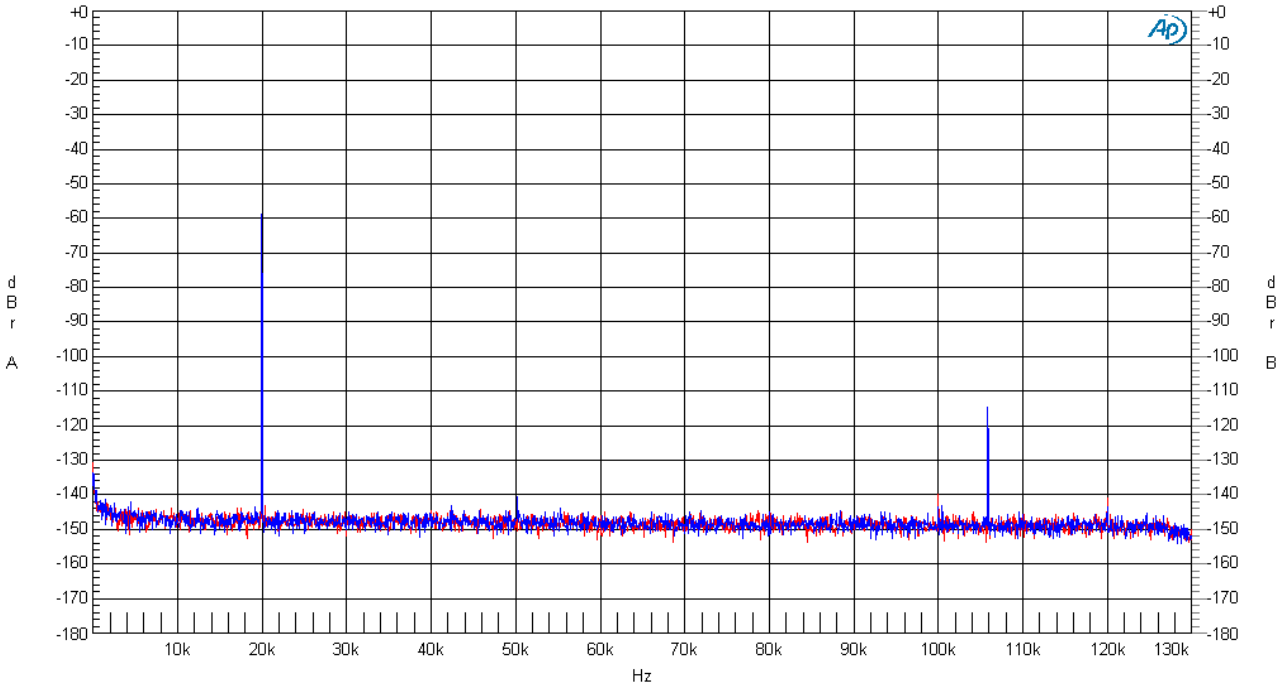


Figure 10. Wideband FFT, 20kHz @ –60dB, Single Ended, 32Ω Load

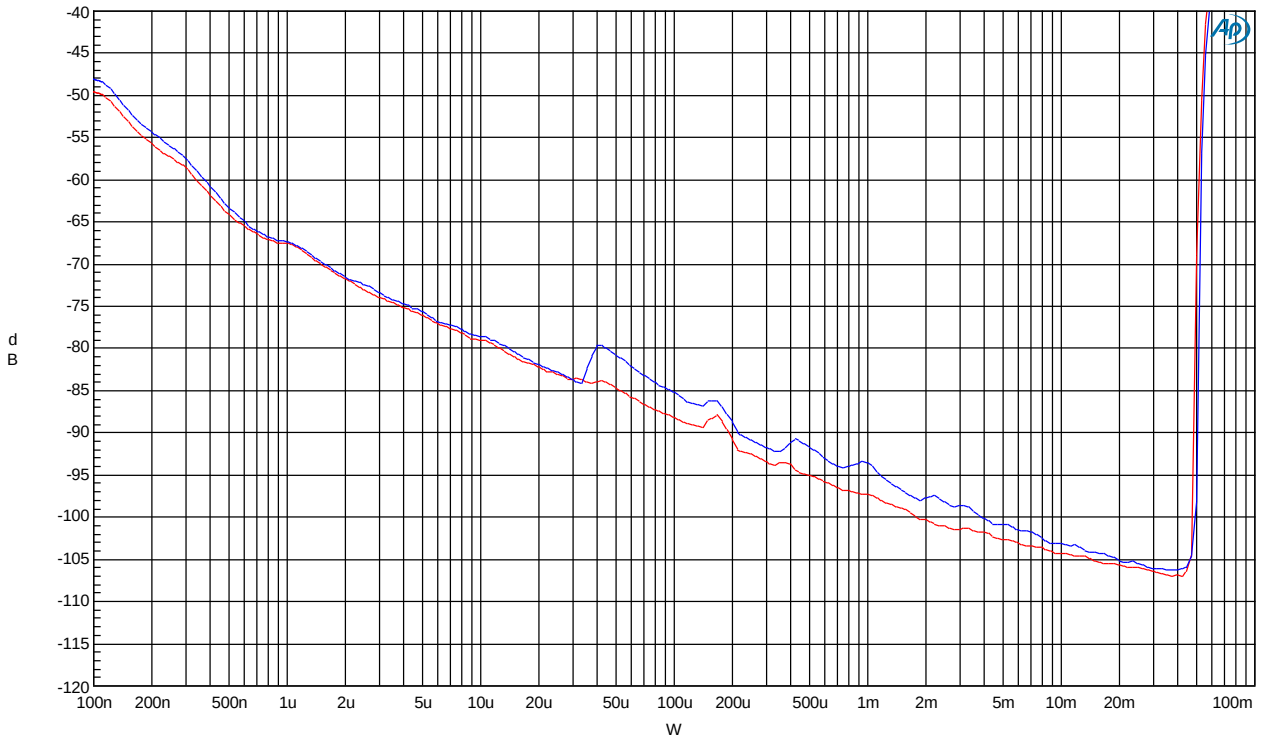


Figure 11. THD+N Unweighted vs. Output Power, Dual Channel Drive, Single Ended, 16Ω Load, external –3.3V supply

SABRE9602Q Headphone Driver with Output Switch

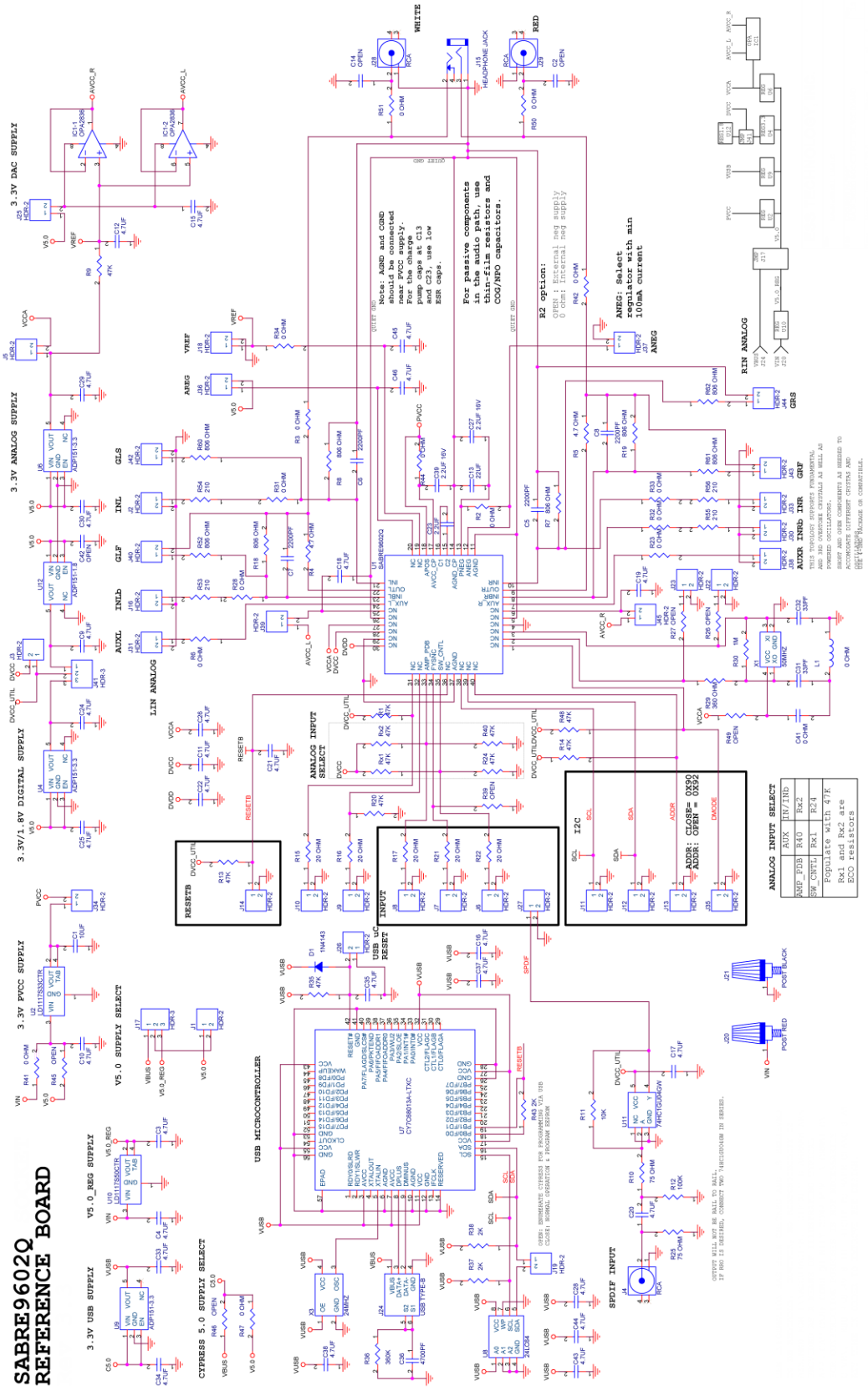
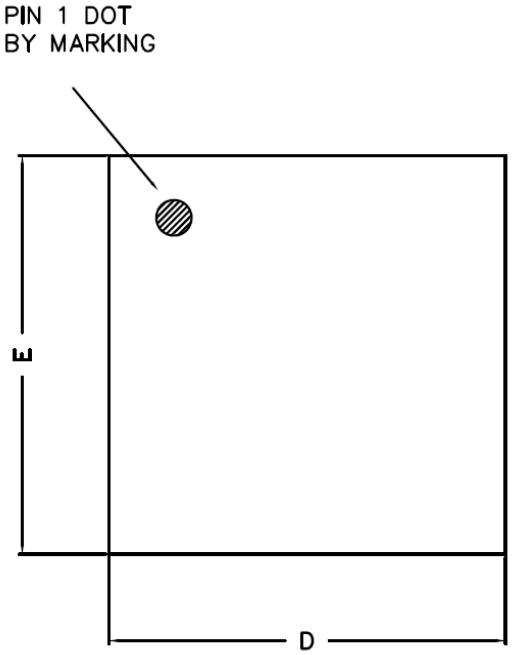
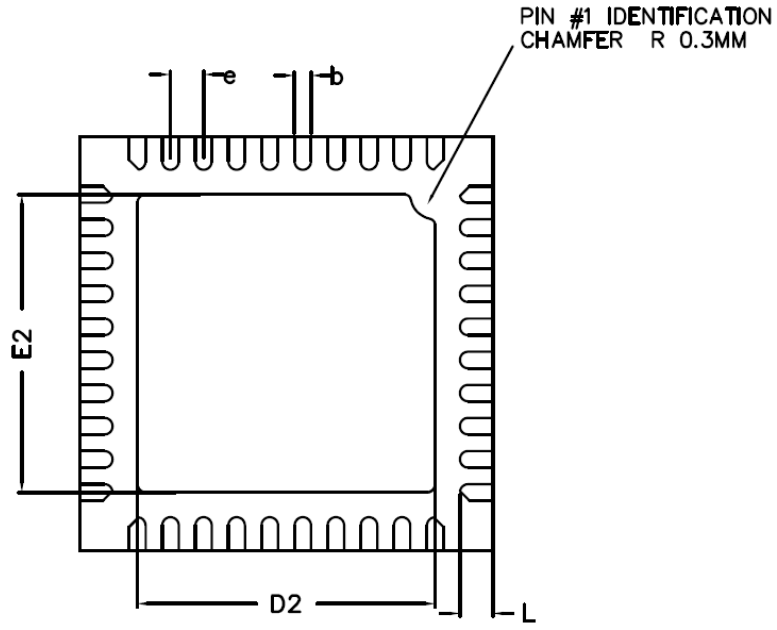


Figure 12. SABRE9602Q Reference Design

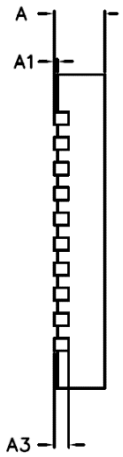
40-Pin QFN Mechanical Dimensions



Top View



Bottom View

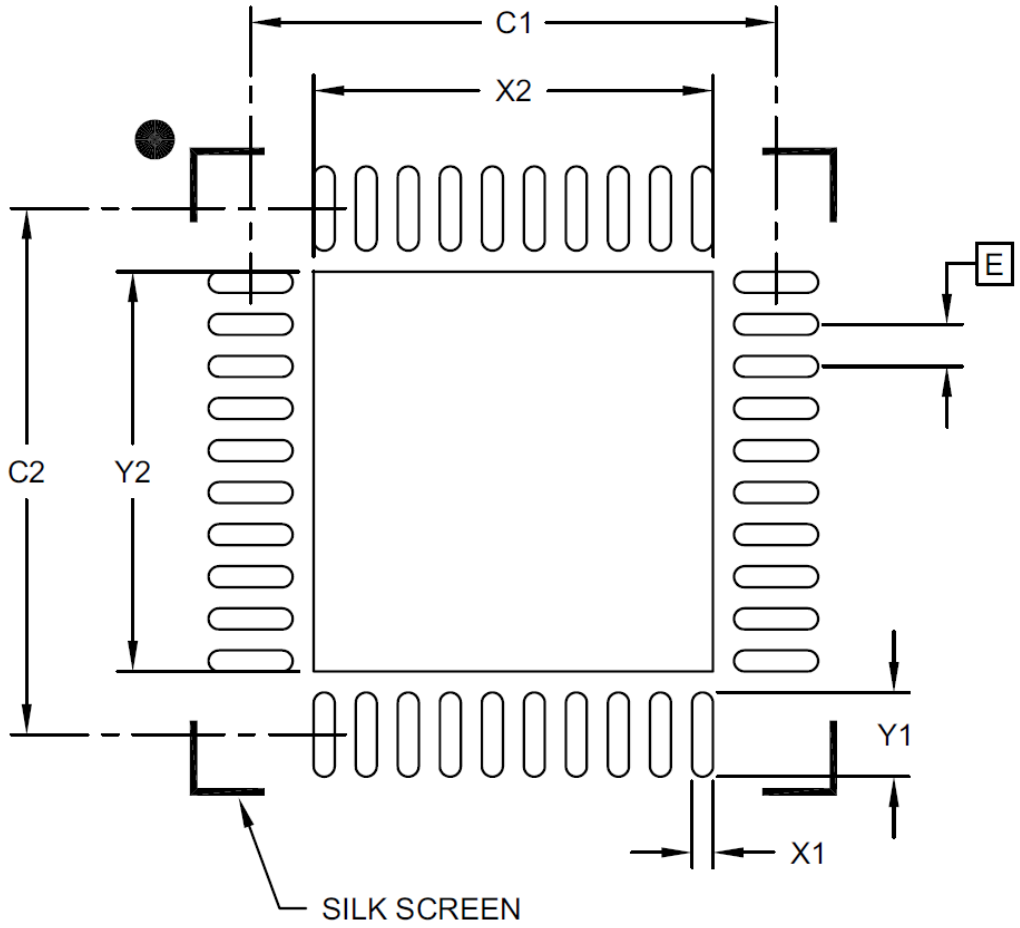


Side View

COMMON DIMENSIONS (mm)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.2 REF.		
D	4.95	5.00	5.05
E	4.95	5.00	5.05
b	0.15	0.20	0.25
L	0.30	0.40	0.50
D2	3.45	3.60	3.70
E2	3.45	3.60	3.70
e	0.4 BSC		

Table 1. Package Dimensions

Example 40-Pin QFN Land Pattern



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.80

Notes:

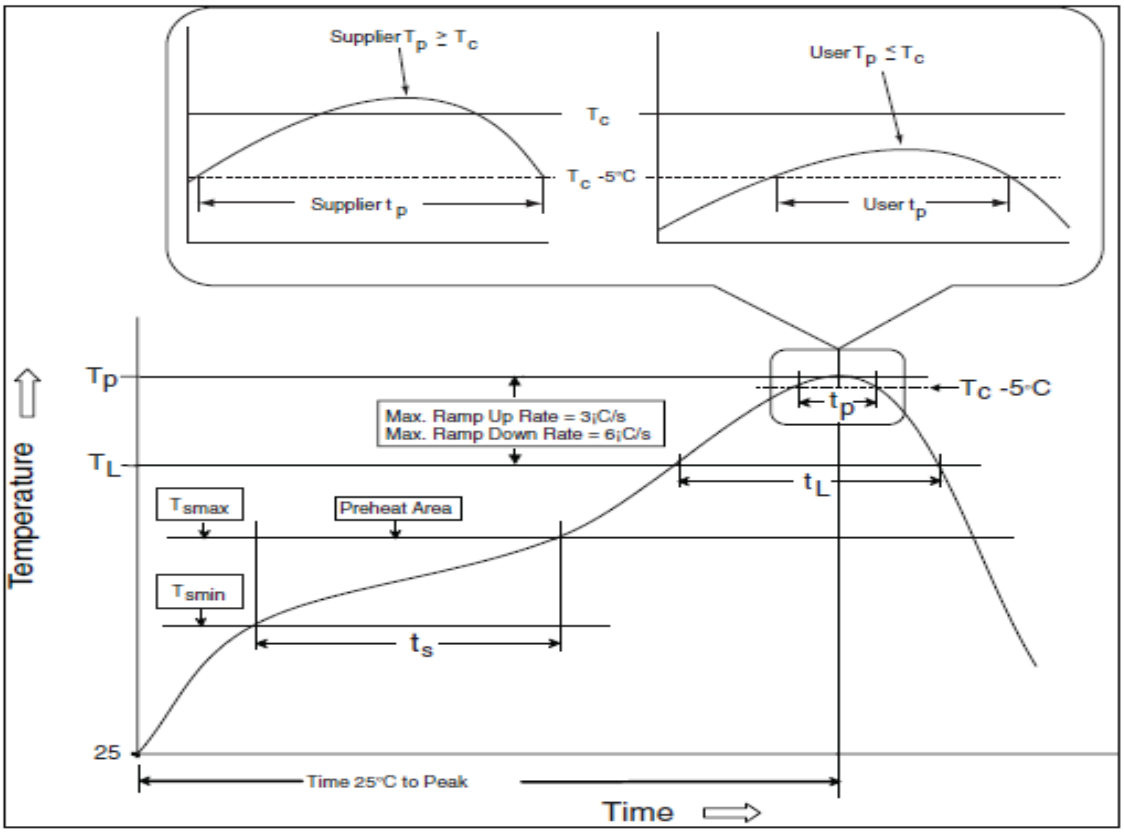
1. All dimensions are in millimeters unless specified otherwise.
2. Thermal vias should be 0.3mm to 0.33mm in diameter, with the barrel plated to 1oz copper.
3. For maximum solder mask in the corners, round the inner corners of each row.
4. For applications where solder loss through vias is a concern, plugging or tenting of the vias should be used. The solder mask diameter for each via should be 0.1mm larger than the via diameter.

Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10°C to 20°C.
The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.
Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)



Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual Soldering:
Allowed up to 2 times with maximum temperature of 350 degrees no longer than 3 seconds.

Table RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	6°C / second max.
Time 25°C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.
For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Table RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

ORDERING INFORMATION

Part Number	Description	Package
SABRE9602Q	Sabre Headphone Driver with Output Switch	40-pin QFN

The letter Q identifies the package type QFN.

Revision History

Rev.	Date	Notes
0.1	August 15, 2014	Initial release
0.2	August 27, 2014	Pin 19 changed from NC to VREF. Tables & circuits updated to show pin 19 connection
0.3	September 16, 2014	Updated Figure 1 block diagram. Added V_{OS} & I_B specifications
0.4	November 10, 2014	Updated cover page specifications and application circuit. Added specifications under Analog Performance.
0.5	November 20, 2014	Corrected error in maximum output power ratings.
0.6	December 12, 2014	Updated specifications for quiescent current and shutdown current.
0.7	December 18, 2014	Added THD specification. Updated Block Diagram and Application Diagram.
0.8	January 28, 2015	Added typical performance graphs.
0.9	February 20, 2015	Added maximum input voltage specification for the Auxiliary Inputs.
1.0	February 26, 2015	Added circuit, Figure 3, to drive balanced headphones.
1.1	March 26, 2015	Updated ESS' mailing address and phone number. Added THD+N and PSR values to the Analog Performance table.
1.2	April 28, 2015	Added information on switching to the AUX inputs with SW_CNTL
1.3	June 12, 2015	Standby current changed from 300μA to < 5μA.
1.31	October 1, 2015	Corrected value of R6 on the differential headphone application circuit
1.4	March 14, 2016	Added recommended frequency range for FSYNC when an external oscillator is used
1.5	November 28, 2017	Remove ESS logo from pin diagram

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ESS Technology:

SABRE9602Q