Analog Reinvented

SABRE HiFi

ES9018JPA
32-bit Stereo Low Power Audio DAC
Datasheet

The ***ES9018JPA Professional Audio DAC*** is a high-performance 32-bit, 2-channel audio D/A converter targeted for audiophile-grade, as well as professional applications such as recording systems, mixer consoles and digital audio workstations.

Using the critically acclaimed ESS patented 32-bit HyperStream™ DAC architecture and Time Domain Jitter Eliminator, the ***ES9018JPA Professional Audio DAC*** delivers a DNR of up to 126dB and THD+N of –116dB, a performance level that will satisfy the most demanding audio enthusiasts.

The ***ES9018JPA Professional Audio DAC*** 32-bit HyperStream™ architecture can handle up to 32-bit, 384kHz PCM data via I^2S, as well as mono mode for highest performance applications. Both synchronous and asynchronous sample rate conversion modes are supported.

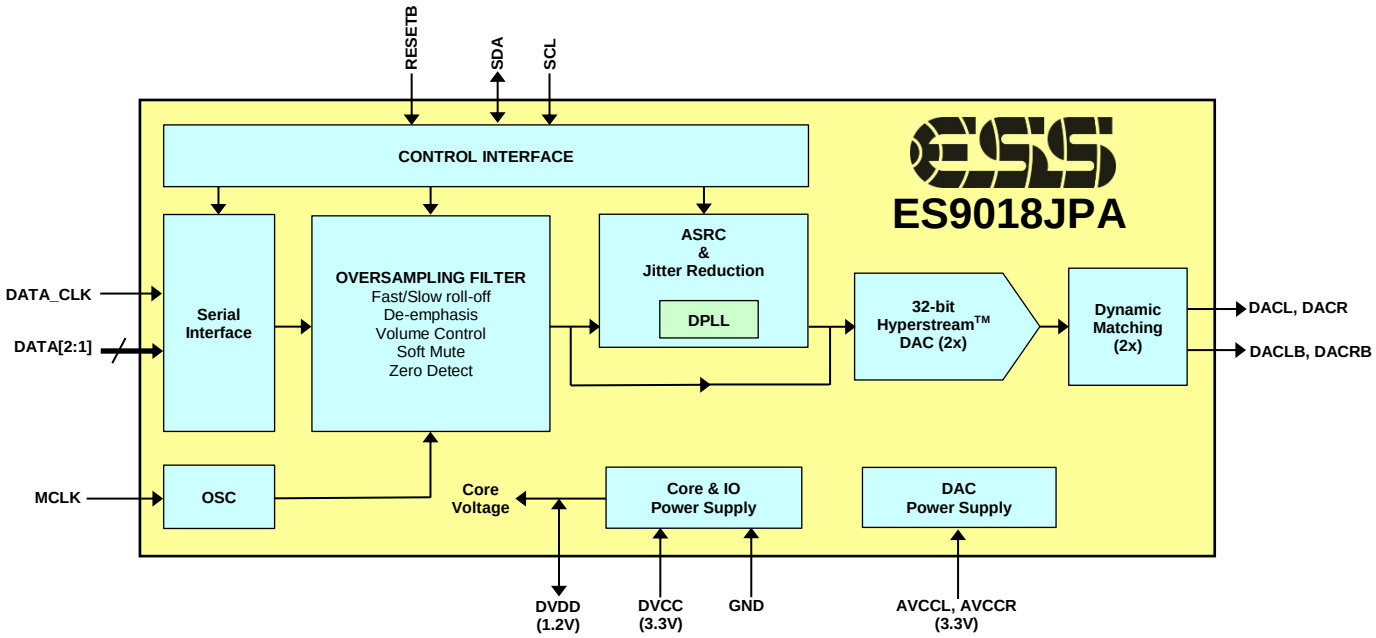
The ***ES9018JPA Professional Audio DAC*** comes in 28-TSSOP package and typically consumes 80mW in normal operating mode.

FEATURE	DESCRIPTION
Patented 32-bit HyperStream™ DAC ○ +123dB DNR & –112dB THD+N (Stereo) ○ +126dB DNR & -116dB THD+N (Mono)	○ Industry's highest performance 32-bit mobile audio DAC with unprecedented dynamic range and ultra-low distortion ○ Supports both synchronous and asynchronous sample rate converter modes
Patented Time Domain Jitter Eliminator	○ Unmatched audio clarity free from input clock jitter
64-bit accumulator and 32-bit processing	○ Distortion free signal processing
Integrated DSP Functions	○ Click-free soft mute and volume control ○ Programmable Zero detect ○ De-emphasis for 32kHz, 44.1kHz, and 48kHz sampling
Customizable output configuration	○ Mono or stereo output in current or voltage mode based on performance criterion
I^2C control	○ Allows software control of DAC features
28-TSSOP package	○ Minimizes PCB footprint
76mW typical operating power < 1mW standby power	○ Low power design
Versatile digital input	○ Supports PCM I^2S, LJ 16-32-bit inputs
Customizable filter characteristics	○ User-programmable filter allowing custom roll-off response ○ By-passable oversampling filter

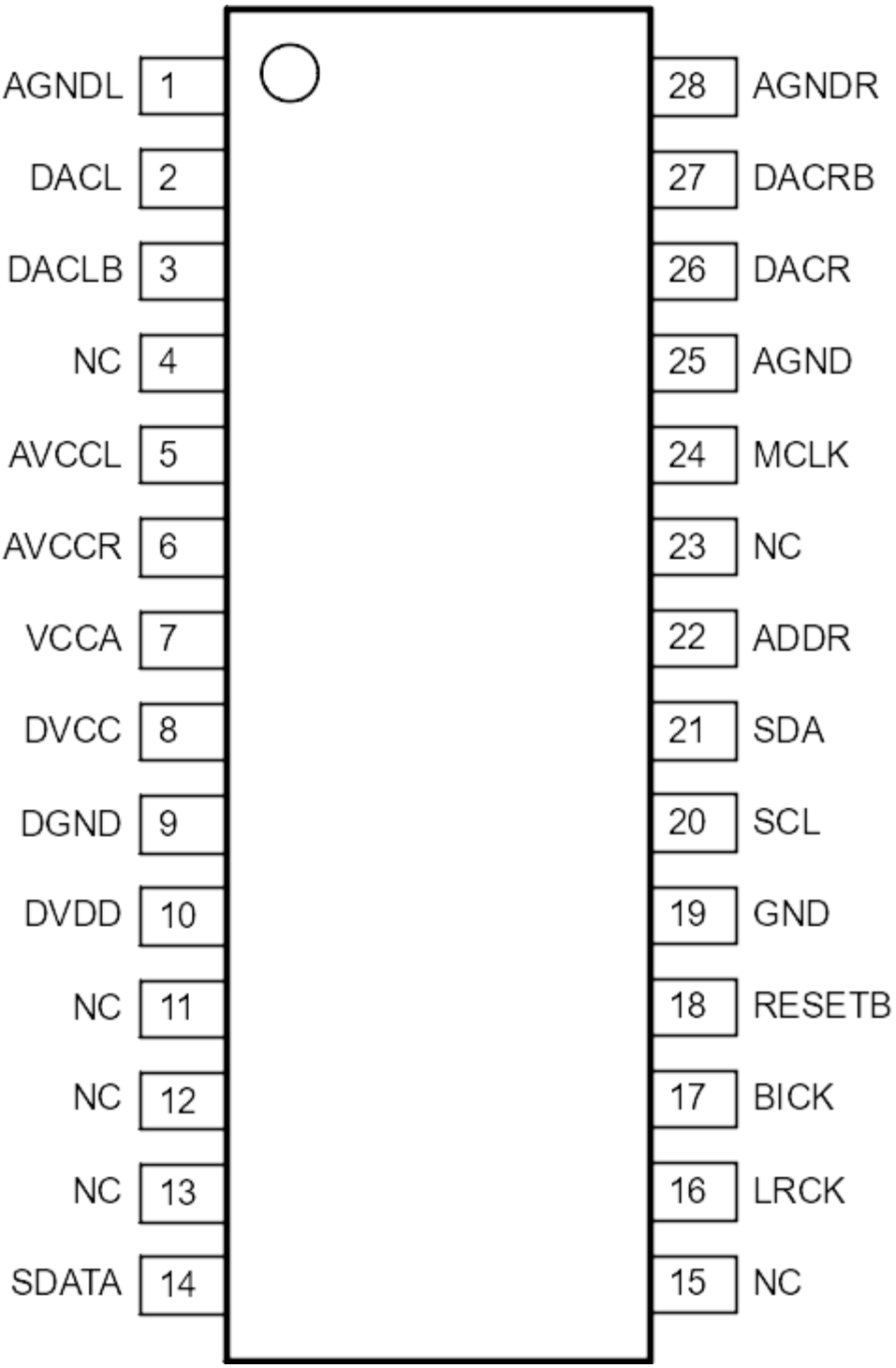
APPLICATIONS

- Professional audio recording systems
- Mixing consoles
- Digital audio workstation

FUNCTIONAL BLOCK DIAGRAM



PIN LAYOUT


AGNDL 1
DACL 2
DACLB 3
NC 4
AVCCL 5
AVCCR 6
VCCA 7
DVCC 8
DGND 9
DVDD 10
NC 11
NC 12
NC 13
SDATA 14
28 AGNDR
27 DACRB
26 DACR
25 AGND
24 MCLK
23 NC
22 ADDR
21 SDA
20 SCL
19 GND
18 RESETB
17 BICK
16 LRCK
15 NC

PIN DESCRIPTIONS

Pin	Name	Pin Type	Reset State	Pin Description
1	AGNDL	Ground	Ground	Analog Ground
2	DACL	AO	Driven to ground	Differential Positive Analog Output Left
3	DACLB	AO	Driven to ground	Differential Negative Analog Output Left
4	N.C.	-	-	No internal connection. Pin may be grounded if desired.
5	AVCCL	Power	Power	Analog AVCC for Left Channel
6	AVCCR	Power	Power	Analog AVCC for Right Channel
7	VCCA	Power	Power	Analog +3.3V for OSC
8	DVCC	Power	Power	Digital I/O Voltage, +3.3V
9	DGND	Ground	Ground	Digital Ground.
10	DVDD	Power	Power	Digital Core Voltage, +1.2V
11	N.C.	-	-	No internal connection. Pin may be grounded if desired.
12	N.C.	-	-	No internal connection. Pin may be grounded if desired.
13	N.C.	-	-	No internal connection. Pin may be grounded if desired.
14	SDATA	I	Tri-stated	PCM Data CH1/CH2
15	N.C.	-	-	No internal connection. Pin may be grounded if desired.
16	LRCK	I	Tri-stated	Input for PCM Frame Clock
17	BICK	I	Tri-stated	Input for PCM Bit Clock
18	RESETB	I	Tri-stated	Master Reset / Power Down (active low)
19	DGND	Ground	Ground	Digital Ground
20	SCL	I	Tri-stated	I^2C Serial Clock Input
21	SDA	I/O	Tri-stated	I^2C Serial Data Input / Output
22	ADDR	I	Tri-stated	I^2C Address Select
23	N.C.	-	-	No internal connection. Pin may be grounded if desired.
24	MCLK	AI	Floating	Master Clock Input
25	AGND	Ground	Ground	Analog Ground
26	DACR	AO	Driven to ground	Differential Positive Analog Output Right
27	DACRB	AO	Driven to ground	Differential Negative Analog Output Right
28	AGND_R	Ground	Ground	Analog Ground

Notes:

- There are 6 N.C. (No Connect) pins. If desired, these pins can be connected to ground on the PCB to strengthen the otherwise isolated pin pads. Alternatively, the N.C. pins can be used to route signals to simplify PCB layout.

FUNCTIONAL DESCRIPTION

NOTATATIONS for Sampling Rates

Mode	fs (target sample rate)	FSR (raw sample rate)
Serial (PCM) Normal Mode	Frame Clock Rate	Frame Clock Rate
Serial (PCM) OSF Bypass Mode	Frame Clock Rate / 8	Frame Clock Rate

PCM Pin Connections

Notes:
MCLK clock must be > 192 x FSR when using PCM input (normal mode), or 128 x FSR (synchronous MCLK).
MCLK clock must be > 24 x FSR when using PCM input (OSF bypass mode).

Pin Name	Description
LRCK	Frame clock
SDATA	2-channel PCM serial data
BICK	Bit clock for PCM audio format

FEATURE DESCRIPTIONS

Soft Mute

When Mute is asserted the output signal will ramp to the -∞ level. When Mute is reset the attenuation level will ramp back up to the previous level set by the volume control register. Asserting Mute will not change the value of the volume control register. The ramp rate is 0.0078125 x fs / $2^{(vol\_rate-5)}$ dB/s.

Automute

During an automute condition the ramping of the volume of each DAC to -∞ can now be programmatically enabled or disabled. In PCM serial mode, “AUTOMUTE” will become active once the audio data is continuously below the threshold set by <Register Automute_lev>, for a length of time defined by 2096896 / (<Register#4> x 64 x fs) Seconds.

Volume Control

Each output channel has its own attenuation circuit. The attenuation for each channel is controlled independently. Each channel can be attenuated from 0dB to –127dB in 0.5dB steps.
Each 0.5dB step transition takes up to 64 intermediate levels, depending on the vol_rate register setting. The result being that the level changes are done using small enough steps so that no switching noise occurs during the transition of the volume control. When a new volume level is set, the attenuation circuit will ramp softly to the new level.

Master Trim

The master trim sets the 0dB reference level for the volume control of each DAC. The master trim is programmable via registers 17-20 and is a 32bit signed number. Therefore, it should never exceed’32'h7FFFFFFF (as this is full-scale signed).

All Mono Mode

An all mono mode is supported where all DACs are driven from the same source. This can be useful for high-end audio applications. The source data for all DACs can be programmatically configured to be either CH1 or CH2.

De-emphasis

The de-emphasis feature is included for audio data that has utilized the 50/15μs pre-emphasis for noise reduction. There are three de-emphasis filters, one for 32kHz, one for 44.1kHz, and one for 48kHz.

Master Clock (MCLK)

A system clock is required for proper operation of the digital filters and modulation circuitry. See p.30, Note 2 for the maximum MCLK frequencies supported. The minimum system clock frequency must also be satisfied:

Data Type	Minimum MCLK Frequency	Note
Serial Normal Mode	MCLK > 192 x FSR, FSR ≤ 384kHz or MCLK = 128 x FSR (synchronous MCLK) with FSR ≤ 384kHz	The maximum FSR frequency is further limited by the maximum MCLK frequencies supported as shown p.24
Serial OSF Bypass Mode	MCLK > 24 x FSR, FSR ≤ 1.536MHz	

Data Clock

DATA_CLOCK must be (2 x i2s_length) x FSR.

Built-in Digital Filters

Three digital filters (fast roll-off, slow roll-off filters and minimum phase filter) are included for PCM data. See 'PCM Filter Characteristics' for more information.

Standby Mode

For lowest power consumption, the followings should be performed to enter stand-by mode:

- Set the soft_start bit in register 14 to 1'b0 to ramp the DAC outputs (DACL, DACLB, DACR, DACRB) to ground.
- RESETB pin should be brought to low digital level to:
  - Shut off the DACs, and Oscillator.
  - Force digital I/O pins (BICK, LRCK, SDA) into tri-state mode
  - Reset all registers to default states
- If MCLK is supplied externally, it should be stopped at logic low level
- DVDD should be shut down during standby.

To resume from standby mode, bring RESETB to high digital level and reinitialize all registers.

Programmable FIR filter

A two stage interpolating FIR design is used. The interpolating FIR filter is generated using MATLAB, and can then be downloaded using a custom C code.

Example Source Code for Loading a Filter

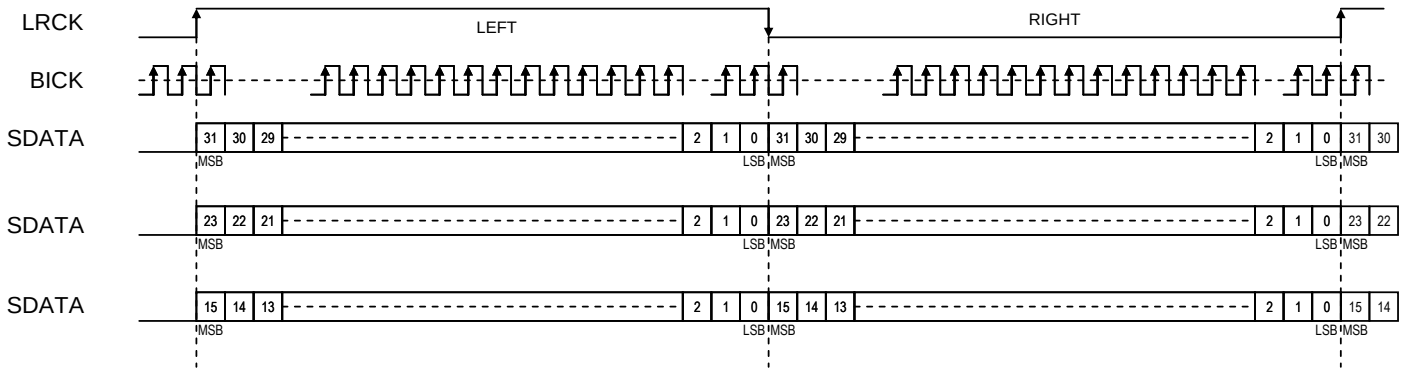
```
// only accept 128 or 16 coefficients
// Note:  The coefficients must be quantized to 24 bits for this method!
// Note:  Stage 1 consists of 128 values (0-127 being the coefficients)
// Note:  Stage 2 consists of 16 values (0-13 being the coefficients, 14-15 are zeros)
// Note:  Stage 2 is symmetric about coefficient 13.  See the example filters for more information.
byte reg26 = (byte)(coeffs.Count == 128 ? 0 : 128);
for (int i = 0; i < coeffs.Count; i++)
{
    // stage 1 contains 128 coefficients, while stage 2 contains 16 coefficients
    registers.WriteRegister(26, (byte)(reg26 + i));

    // write the coefficient data
    registers.WriteRegister(27, (byte)(coeffs[i] & 0xff));
    registers.WriteRegister(28, (byte)((coeffs[i] >> 8) & 0xff));
    registers.WriteRegister(29, (byte)((coeffs[i] >> 16) & 0xff));

    registers.WriteRegister(30, 0x02);   // set the write enable bit
}
// disable the write enable bit when’we're done
registers.WriteRegister(30, (byte)(setEvenBit ? 0x04 : 0x00));
```

OSF Bypass

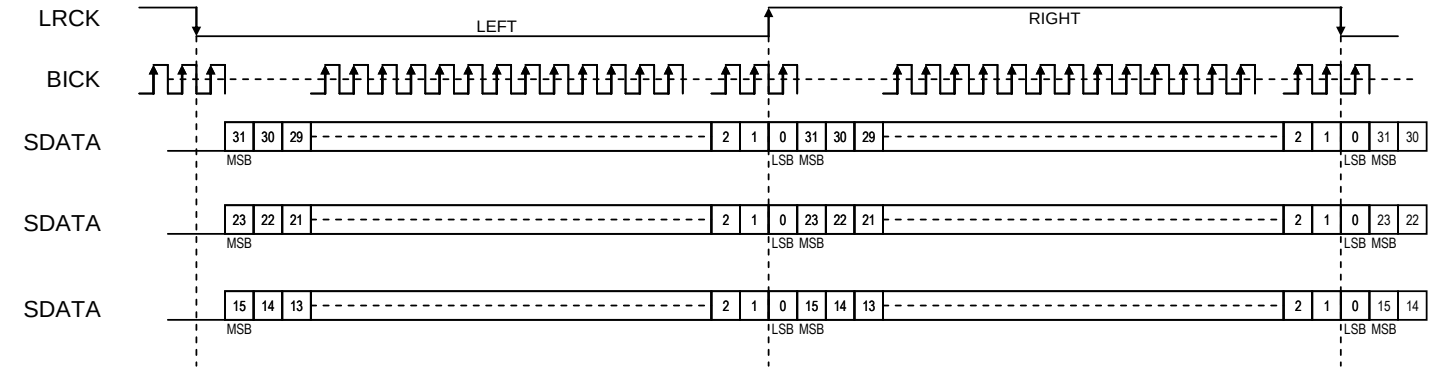
The oversampling FIR filter can be bypassed, sourcing data directly into the IIR filter. ESS recommends using 8 x FSR as the input. For example, an external signal at 44.1kHz can be oversampled externally to 8 x 44.1kHz = 352.8kHz and then applied to the serial decoder in either I^2S or LJ format. The maximum sample rate that can be applied is 1.536MHz (8 x 192kHz).

Audio Interface Formats

Several interface formats are provided so that direct connection to common audio processors is possible. The available formats are shown in the following diagrams. The audio interface format can be set by programming the registers.



LEFT JUSTIFIED FORMAT



I2S FORMAT

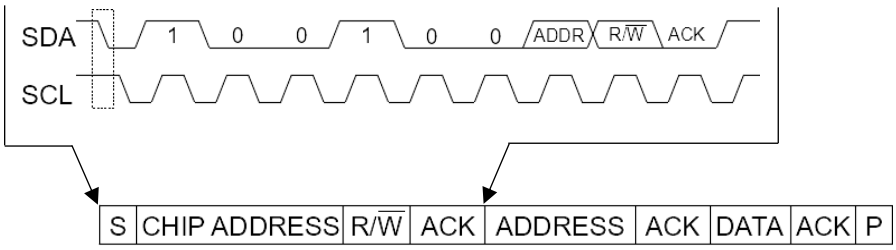
Notes: for Left-Justified and I²S formats, the following number of BICKs is present per (left plus right) frame:

- 16-bit mode: 32 BICKs
- 24-bit mode: 48 BICKs
- 32-bit mode: 64 BICKs

SERIAL CONTROL INTERFACE

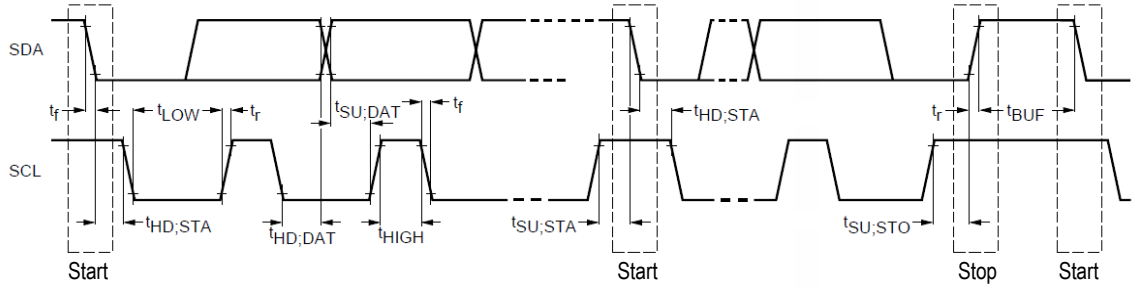
The registers inside the chip are programmed via an I²C interface. The diagram below shows the timing for this interface. The chip address can be set to 2 different settings via the "ADDR" pin. The table below summarizes this.

ADDR	CHIP ADDRESS
0	0x90
1	0x92



Notes:

1. The "ADDR" pin is used to create the CHIP ADDRESS. (0x90, 0x92)
2. The first byte after the chip address is the "ADDRESS" this is the register address.
3. The second byte after the CHIP ADDRESS is the "DATA" this is the data to be programmed into the register at the previous "ADDRESS".



Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
START condition hold time	$t_{HD,STA}$	4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of SCL	t_{HIGH}	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU,STA}$	4.7	-	0.6	-	µs
SDA hold time from SCL falling	$t_{HD,DAT}$	0.3	-	0.3	-	µs
SDA setup time from SCL rising	$t_{SU,DAT}$	250	-	100	-	ns
Rise time of SDA and SCL	t_r	-	1000		300	ns
Fall time of SDA and SCL	t_f	-	300		300	ns
STOP condition setup time	$t_{SU,STO}$	4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF

REGISTER MAP

Address (Dec/Hex)	Register	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Read/Write									
0 / 0x00	SYSTEM SETTINGS	OSC_DRV				RESERVED			SOFT_RESET
1 / 0x01	INPUT CONFIGURATION	I2S_LENGTH		I2S_MODE		RESERVED		RESERVED	
2 / 0x02	RESERVED	RESERVED							
3 / 0x03	RESERVED	RESERVED							
4 / 0x04	AUTOMUTE _TIME	AUTOMUTE_TIME							
5 / 0x05	AUTOMUTE LEVEL	AUTOMUTE_ LOOPBACK	AUTOMUTE_LEVEL						
6 / 0x06	SOFT VOLUME CONTROL 3 & DE-EMPHASIS	RESERVED	DEEMPH _BYPASS	DEEMPH_SEL		RESERVED	VOL_RATE		
7 / 0x07	GENERAL SETTINGS	RESERVED	FILTER_SHAPE		RESERVED			MUTE	
8 / 0x08	RESERVED	RESERVED							
9 / 0x09	RESERVED	RESERVED							
10 / 0x0A	RESERVED	RESERVED							
11 / 0x0B	CHANNEL MAPPING	RESERVED	RESERVED			CH2_ANALOG _SWAP	CH1_ANALOG _SWAP	CH2_SEL	CH1_SEL
12 / 0x0C	RESERVED	RESERVED							
13 / 0x0D	RESERVED	RESERVED							
14 / 0x0E	SOFT START SETTINGS	SOFT_START	SOFT_START _ON_LOCK	MUTE_ON _LOCK	SOFT_START_TIME				
15 / 0x0F	VOLUME 1	VOLUME 1							
16 / 0x10	VOLUME 2	VOLUME 2							
17 / 0x11	MASTER TRIM	MASTER_TRIM							
18 / 0x12									
19 / 0x13									
20 / 0x14									
21 / 0x15	IIR & OSF BYPASS	RESERVED					BYPASS_IIR	RESERVED	BYPASS_OSF
22 / 0x16	RESERVED	RESERVED							
23 / 0x17	RESERVED	RESERVED							
24 / 0x18	RESERVED	RESERVED							
25 / 0x19	RESERVED	RESERVED							
26 / 0x1A	PROGRAMMABLE FILTER ADDRESS	PROG_COEFF _STAGE	PROG_COEFF_ADDR						
27 / 0x1B	PROGRAMMABLE FILTER COEFFICIENT	PROG_COEFF							
28 / 0x1C									
29 / 0x1D									
30 / 0x1E	PROGRAMMABLE FILTER CONTROL	RESERVED					EVEN_STAGE2 _COEFF	PROG_ COEFF_WE	PROG_ COEFF_EN
Read Only									
64 / 0x40	CHIP STATUS	RESERVED			CHIP_ID			AUTOMUTE _STATUS	LOCK_STATUS

REGISTER SETTINGS

Register #0: System Settings

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	osc_drv				reserved *			soft_reset
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
[7:4]	osc_drv	Oscillator drive specifies the bias current to the oscillator pad. • 4'b0000: full bias (default) • 4'b1000: 3/4 bias • 4'b1100: 1/2 bias • 4'b1110: 1/4 bias • 4'b1111: shut down the oscillator • Other settings: reserved It is recommended to use the default setting.
[3:1]	reserved *	
[0]	soft_reset	1'b1 resets chip 1'b0 is normal operation (default)

* All Reserved Bits in Register #0 must be set to the indicated logic level to ensure correct device operation.

Register #1: Input Configuration

8 bit, Read-Write Register, Default = 0x8C

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	i2s_length		i2s_mode		reserved		reserved	
Default	1	0	0	0	1	1	0	0

Bit	Mnemonic	Description
[7:6]	i2s_length	2'd0 = 16bit 2'd1 = 24bit 2'd2 or 2'd3 = 32bit (default)
[5:4]	i2s_mode	2'd0 = I²S (default) 2'd1 = LJ mode 2'd2 = I²S 2'd3 = LJ mode
[3:2]	reserved *	Must be set to 2'b11 for normal operation
[1:0]	reserved *	must be set to 2'b00 for normal operation

* All Reserved Bits in Register #1 must be set to the indicated logic level to ensure correct device operation.

Register #2: Reserved

8 bit, Read-Write Register, Default = 0x18

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	Reserved							
Default	0	0	0	1	1	0	0	0

Register #3: Reserved

8 bit, Read-Write Register, Default = 0x10

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	Reserved							
Default	0	0	0	1	0	0	0	0

Register #4: Soft Volume Control 1 (Automute Time)

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	automute_time							
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
[7:0]	automute_time	Default o' 8'd0 (Automute Disabled) Time in Seconds = 2096896 / (automute_time x DATA_CLK) with DATA_CLK in Hz

Register #5: Soft Volume Control 2 (Automute Level)

8 bit, Read-Write Register, Default = 0x68

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	automute_loopback	automute_level						
Default	0	1	1	0	1	0	0	0

Bit	Mnemonic	Description
[7]	automute_loopback	1'b0 disables automute_loopback (default) 1'b1 ramps to -infinity on automute
[6:0]	automute_level	The level (in 1dB increments) of the automute, default of 7'd104

Register #6: Soft Volume Control 3 and De-emphasis

8 bit, Read-Write Register, Default = 0x4A

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved	deemph_bypass	deemph_sel		reserved *	vol_rate		
Default	0	1	0	0	1	0	1	0

Bit	Mnemonic	Description
[7]	reserved *	Must be set to 1’b0 for normal operation
[6]	deemph_bypass	1'b0 enables de-emphasis filters 1'b1 disabled de-emphasis filters (default)
[5:4]	deemph_sel	2’b00 = 32kHz (default) 2’b01 = 44.1kHz 2’b10 = 48kHz 2’b11 = RESERVED
[3]	reserved	Must be left as 1'b1 for normal operation
[2:0]	vol_rate	3'd2 by default Sets the volume ramp rate to 0.0078125 x fs / $2^{(vol\_rate-5)}$ dB/s

* All Reserved Bits in Register #6 must be set to the indicated logic level to ensure correct device operation.

Register #7: General Settings

8 bit, Read-Write Register, Default = 0x80

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *	filter_shape		reserved *			mute	
Default	1	0	0	0	0	0	0	0

Bit	Mnemonic	Description
[7]	reserved *	Must be set to 1’b1 for normal operation
[6:5]	filter_shape	2’d0 = fast rolloff (default) 2’d1 = slow rolloff 2’d2 = minimum phase 2'd3 = reserved
[4:2]	reserved *	Must be set to 3’b000 for normal operation
[1:0]	mute	This is a soft mute, which uses the ramping volume control. mute[0] • 1’b0: Channel 1 (default of left channel) unmuted (default) • 1’b1: Channel 1 (default of left channel) muted mute[1] • 1’b0: Channel 2 (default of right channel) unmuted (default) • 1’b1: Channel 2 (default of right channel) muted

* All Reserved Bits in Register #7 must be set to the indicated logic level to ensure correct device operation.

Register #8: Reserved

8 bit, Read-Write Register, Default = 0x10

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *							
Default	0	0	0	1	0	0	0	0

* All Reserved Bits in Register #8 must be set to the indicated logic level to ensure correct device operation.

Register #9: Reserved

8 bit, Read-Write Register, Default = 0x0

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *							
Default	0	0	0	0	0	0	0	0

* All Reserved Bits in Register #9 must be set to the indicated logic level to ensure correct device operation.

Register #10: Reserved

8 bit, Read-Write Register, Default = 0x15

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *							
Default	0	0	0	1	0	1	0	1

* All Reserved Bits in Register #10 must be set to the indicated logic level to ensure correct device operation.

Register #11: Channel Mapping

8 bit, Read-Write Register, Default = 0x02

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *				ch2_analog_swap	ch1_analog_swap	ch2_sel	ch1_sel
Default	0	0	0	0	0	0	1	0

Bit	Mnemonic	Description
[7:4]	reserved *	Must be set to 3'b000 for normal operation
[3]	ch2_analog_swap	1'b0 = normal operation (default) 1'b1 = swap dac and dacb
[2]	ch1_analog_swap	1'b0 = normal operation (default) 1'b1 = swap dac and dacb
[1]	ch2_sel	1'b0 = left 1'b1 = right (default)
[0]	ch1_sel	1'b0 = left (default) 1'b1 = right

Left and Right channels can be reversed using Register #11.

* All Reserved Bits in Register #11 must be set to the indicated logic level to ensure correct device operation.

Register #12: Reserved

8 bit, Read-Write Register, Default = 0x15

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved							
Default	0	1	0	1	1	0	1	0

* All Reserved Bits in Register #12 must be set to the indicated logic level to ensure correct device operation.

Register #13: Reserved

8 bit, Read-Write Register, Default = 0x40

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *							
Default	0	1	0	0	0	0	0	0

* All Reserved Bits in Register #13 must be set to the indicated logic level to ensure correct device operation.

Register #14: Soft Start Settings

8 bit, Read-Write Register, Default = 0x8A

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	soft_start	soft_start_on_lock	mute_on_lock	soft_start_time				
Default	1	0	0	0	1	0	1	0

Bit	Mnemonic	Description
[7]	soft_start	1'b0: Ramp the output stream to ground 1'b1: Normal operation (default) – ramp the output stream to ½ x AVCC_L/R
[6]	soft_start_on_lock	1'b0: Do not force output low when lock is lost (default) 1'b1: Force output low when lock is lost
[5]	mute_on_lock	1'b0: Do not force a mute when lock is lost (default) 1'b1: Force a mute when lock is lost
[4:0]	soft_start_time	Time for soft start ramp = 4096 x $2^{(soft\_start\_time+1)}$ / MCLK seconds (where MCLK is measured in Hz). The valid range of soft-start_time is from 0 to 20.

Register #15: Volume 1 (usually selected for the Left Channel, but can be reversed using Register #11)

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	volume1							
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
[7:0]	volume1	Default to 8'd0 0dB to –127.5dB in 0.5dB steps

Register #16: Volume 2 (usually selected for the Right Channel, but can be reversed using Register #11)

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	volume2							
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
[7:0]	volume2	Default to 8'd0 0dB to –127.5dB in 0.5dB steps

Register #20-17: Master Trim

32 bit, Read-Write Register, Default = 32'h7fffffff. Reg 20 are the MSB's, Reg 17 are the LSBs.

Bits	[31:0]
Mnemonic	master_trim
Default	32'h7fffffff

This is a 32 bit value that sets the 0dB level for all volume controls. This is a signed number, so it should never exceed 32'h7fffffff (which is $2^{31} - 1$).

Register #21: IIR and OSF Bypass

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *					bypass_iir	reserved *	bypass_osf
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
[7:3]	reserved *	Must be set to 5'b00000 for normal operation
[2]	bypass_iir	1'b0 = Use the IIR filter (default) 1'b1 = Bypass the IIR filter.
[1]	reserved *	Must be set to 1'b1 for normal operation
[0]	bypass_osf	1'b0 = Use the interpolating 8x FIR filter (default) 1'b1 = Bypass the interpolating 8x FIR filter. Note: Bypassing the interpolating filter requires that the input data be oversampled at 8x fs by an external oversampling filter.

* All Reserved Bits in Register #21 must be set to the indicated logic level to ensure correct device operation.

Register #22: Reserved

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *							
Default	0	0	0	0	0	0	0	0

* All Reserved Bits in Register #22 must be set to the indicated logic level to ensure correct device operation.

Register #23: Reserved

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *							
Default	0	0	0	0	0	0	0	0

* All Reserved Bits in Register #23 must be set to the indicated logic level to ensure correct device operation.

Register #24: Reserved

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *							
Default	0	0	0	0	0	0	0	0

* All Reserved Bits in Register #24 must be set to the indicated logic level to ensure correct device operation.

Register #25: Reserved

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved *							
Default	0	0	0	0	0	0	0	0

* All Reserved Bits in Register #25 must be set to the indicated logic level to ensure correct device operation.

Register #26: Programmable Filter Address

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6:0]						
Mnemonic	prog_coeff_stage	prog_coeff_addr						
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
[7]	prog_coeff_stage	Selects which stage of the filter to write. 1'b0 = Stage 1 of the oversampling filter (128 coefficients). 1'b1 = Stage 2 of the oversampling filter (16 coefficients)
[6:0]	prog_coeff_addr	Selects the coefficient address when writing custom coefficients for the oversampling filter.

Register #29-27: Programmable Filter Coefficient

8 bit, Read-Write Register, Default = 0x000000

Bits	[23:0]
Mnemonic	prog_coeff
Default	24'd0

Bit	Mnemonic	Description
[23:0]	prog_coeff	A 24-bit filter coefficient that will be written to address 'prog_coeff_addr'.

Register #30: Programmable Filter Control

8 bit, Read-Write Register, Default = 0x00

Bits	[7:3]	[2]	[1]	[0]
Mnemonic	reserved *	even_stage2_coeff	prog_coeff_we	prog_coeff_en
Default	0 0 0 0 0	0	0	0

Bit	Mnemonic	Description
[7:3]	reserved *	
[2]	even_stage2_coeff	Sets the type of symmetry of the stage 2 programmable filter. 1'b0 = Uses a sine symmetric filter (27 coefficients). 1'b1 = Uses a cosine symmetric filter (28 coefficients).
[1]	prog_coeff_we	1'b0 = Disable writing to the custom filter coefficients. 1'b1 = Enable writing to the custom filter coefficients. Note: When set to 1'b1 the custom filter will be bypassed regardless of the state of register 21[0].
[0]	prog_coeff_en	1'b0 = Use one of the built-in oversampling filters. 1'b1 = Use the custom oversampling filter. Note: The custom filter is not programmed to anything on reset, valid coefficients must be written to the filter before enabling.

* All Reserved Bits in Register #30 must be set to the indicated logic level to ensure correct device operation.

Notes: even_stage2_coeff sets the type of symmetry used by the second stage filter. The actual RAM is 16 coefficients, but only the first 14 coefficients are used when applying the oversampling filter. The first 14 coefficients are mirrored using either sine or cosine symmetry, resulting in a filter length of either 27 or 28 taps. This means that the second stage RAM should only contain half of the impulse response of the second stage filter, and the impulse peak value will be contained in the 14th coefficient. Also note that, due to the symmetry of the filter, only linear phase filters may be used in the second stage.

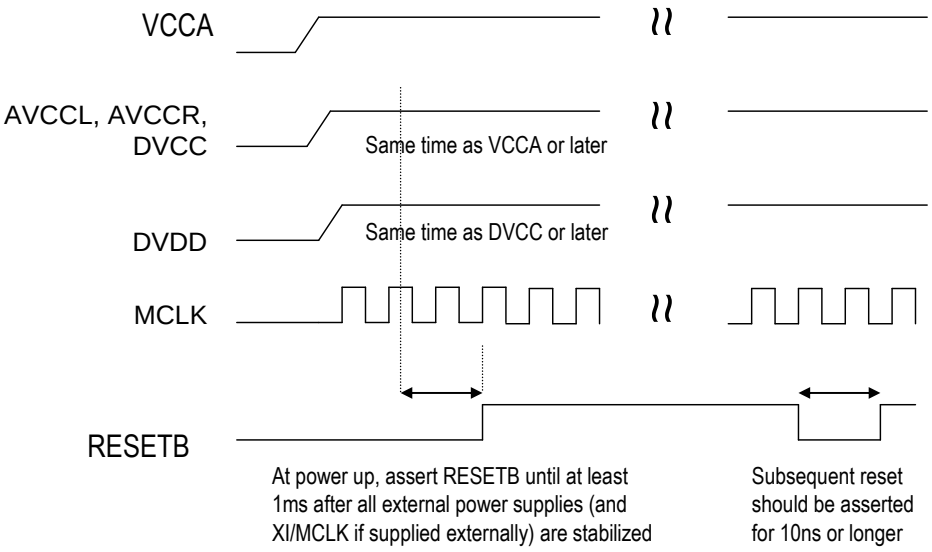
Register #64: Chip Status

8 bit, Read-Only Register

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	reserved			chip_id			automute_status	lock_status

Bit	Mnemonic	Description
[7:5]	reserved	
[4:2]	chip_id	3'd0 => ES9018JPA
[1]	automute_status	1'b0 => Automute condition is inactive. 1'b1 => Automute condition is active.
[0]	lock_status	1'b0 => The Jitter Eliminator is not locked to an incoming signal. 1'b1 => The Jitter Eliminator is locked to an incoming signal.

RECOMMENDED POWER-UP SEQUENCE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Positive Supply Voltage (DVCC, VCCA, AVCCL, AVCCR)	+4.7V with respect to GND
Positive Supply Voltage (DVDD)	+1.8V with respect to GND
DAC Output voltage Range (DACL, DACR, DACLB, DACRB)	GND < Vout < AVCC
Storage temperature Range	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage Range for Digital Input pins	–0.3V to DVCC+ 0.3V
ESD Protection Human Body Model (HBM) Machine Model (MM)	 2000V 200V

WARNING: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	–20°C to +70°C

Power Supply		Voltage	Current nominal (Note 1)	Current standby (Notes 1, 2)
Digital Power Supply Voltage	DVCC	+3.3V ± 5%	14.2mA	0mA
Digital Core Supply Voltage	DVDD	+1.2V ± 5% +1.2V ± 5% (Note 3)	TBD 50mA	0mA
Analog Core Supply Voltage	VCCA	+3.3V ± 5%	0.8mA	0mA
Analog Power Supply Voltage	AVCCL AVCCR	+3.3V ± 5%	8.0mA	0mA
Total Power		DVCC = +3.3V	76mW	< 1mW

Notes:

(1) fs = 44.1kHz, external MCLK = 22MHz, I^2S input, DAC output connected to current-to-voltage converter, all external supply voltages at nominal center values

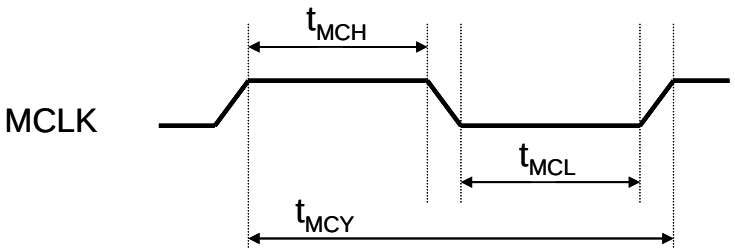
(2) With RESETB held low after setting the soft_start bit in register 14 to 1'b0 to fully ramp the DAC outputs to ground

(3) DVDD current measured at 192kHz sample rate and MCLK = 80MHz.

DC ELECTRICAL CHARACTERISTICS

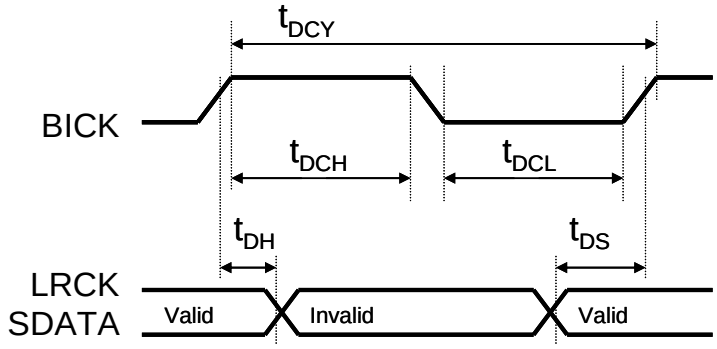
Symbol	Parameter	Minimum	Maximum	Unit	Comments
VIH	High-level input voltage	DVCC/2 + 0.4		V	
VIL	Low-level input voltage		0.4	V	
VOH	High-level output voltage	DVCC – 0.2		V	IOH = 100μA
VOL	Low-level output voltage		0.2	V	IOL = 100μA

MCLK Timing



Parameter	Symbol	Min	Max	Unit
MCLK pulse width high	T_{MCH}	4.5		ns
MCLK pulse width low	T_{MCL}	4.5		ns
MCLK cycle time	T_{MCY}	10		ns
MCLK duty cycle		45:55	55:45	

Audio Interface Timing



Parameter	Symbol	Min	Max	Unit
BICK pulse width high	t_{DCH}	4.5		ns
BICK pulse width low	t_{DCL}	4.5		ns
BICK cycle time	t_{DCY}	10		ns
BICK duty cycle		45:55	55:45	
DATA set-up time to BICK rising edge	t_{DS}	4.1		ns
DATA hold time to BICK rising edge	t_{DH}	2		ns

Notes:

- Audio data on LRCK, SDATA are sampled at the rising edges of BICK and must satisfy the setup and hold time requirements relative to the rising edge of BICK

ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

1. T_A = 25ºC, AVCC = VCCA = DVCC = 3.3V, DVDD = 1.2V, fs = 44.1kHz, MCLK = 27MHz & 32-bit data
2. SNR / DNR: A-weighted over 20Hz-20kHz in averaging mode
   THD+N: un-weighted over 20Hz-20kHz bandwidth

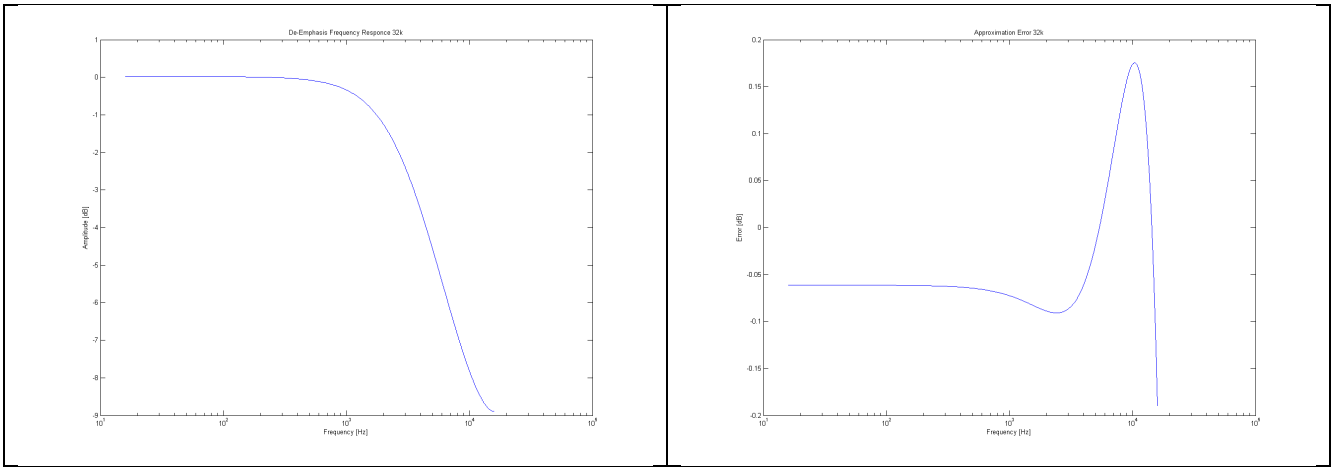
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				32		Bits
MCLK (PCM normal mode)		Note *2	192FSR			Hz
MCLK (PCM OSF bypass mode)			24FSR			
DYNAMIC PERFORMANCE						
DNR (differential current mode)		–60dBFS		123		dB-A
THD+N (differential current mode)		0dBFS		–112		dB
ANALOG OUTPUT						
Differential (+ or –) voltage output range		Full-scale out		3.05 (0.924 x AVCC)		Vp-p
Differential (+ or –) voltage output offset		Bipolar zero out		1.65 (AVCC / 2)		V
Differential (+ or –) current output range (Note *1)		Full-scale out		3.783		mAp-p
Differential (+ or –) current output offset (Note *1)		Bipolar zero out to virtual ground at voltage Vg (V)		2.112 – (1000 x Vg) / 806		mA
Digital Filter Performance						
De-emphasis error					±0.2	dB
Mute Attenuation				127		dB
PCM Filter Characteristics (Sharp Roll Off)						
Pass band		±0.003dB			0.454fs	Hz
		–3dB			0.49fs	Hz
Stop band		< –115dB	0.546fs			Hz
Group Delay				35 / fs		s
PCM Filter Characteristics (Slow Roll Off)						
Pass band		±0.05dB			0.308fs	Hz
		–3dB			0.454fs	Hz
Stop band		< –100dB	0.814fs			Hz
Group Delay				6.25 / fs		s
PCM Filter Characteristics (Minimum Phase)						
Pass band		±0.003dB			0.454fs	Hz
		–3dB			0.49fs	Hz
Stop band		< –115dB	0.546fs			Hz

Notes

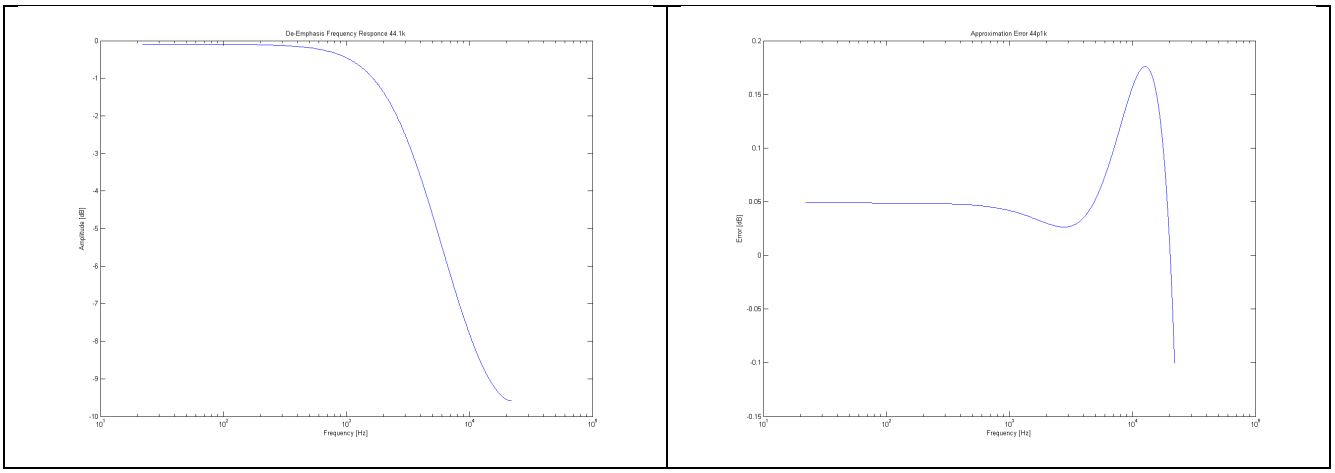
*1. Differential (+ or –) current output is equivalent to a differential (+ or –) voltage source in series with an 806Ω ±11% resistor. The differential (+ or –) voltage source has a peak-to-peak output range of 0.924 x AVCC = 3.05V and an output offset of AVCC / 2 = 1.65V.

*2. Synchronous MCLK at 128 x FSR is also supported.

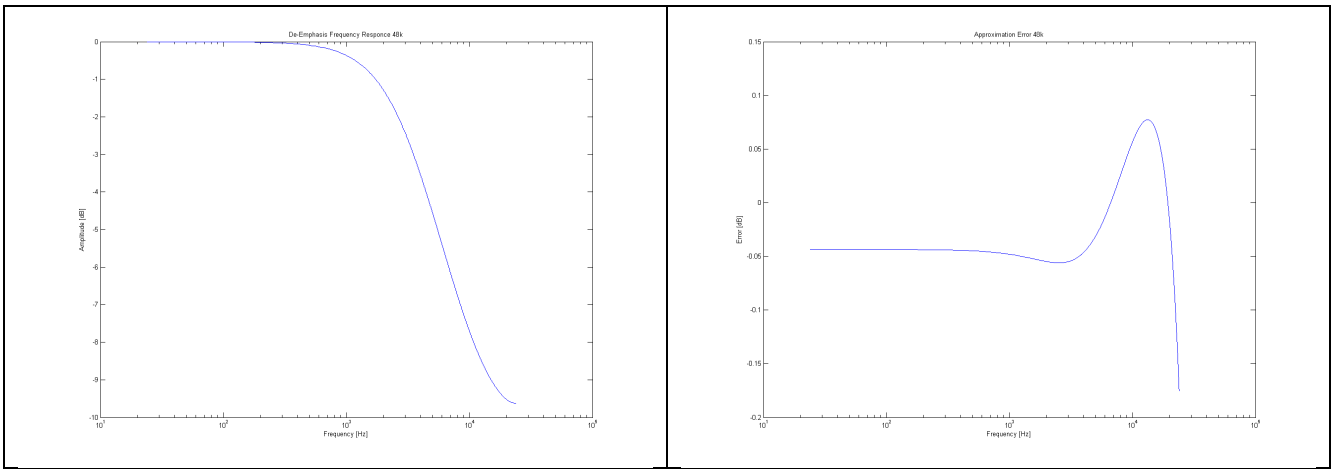
PCM DE-EMPHASIS FILTER RESPONSE (32kHz)



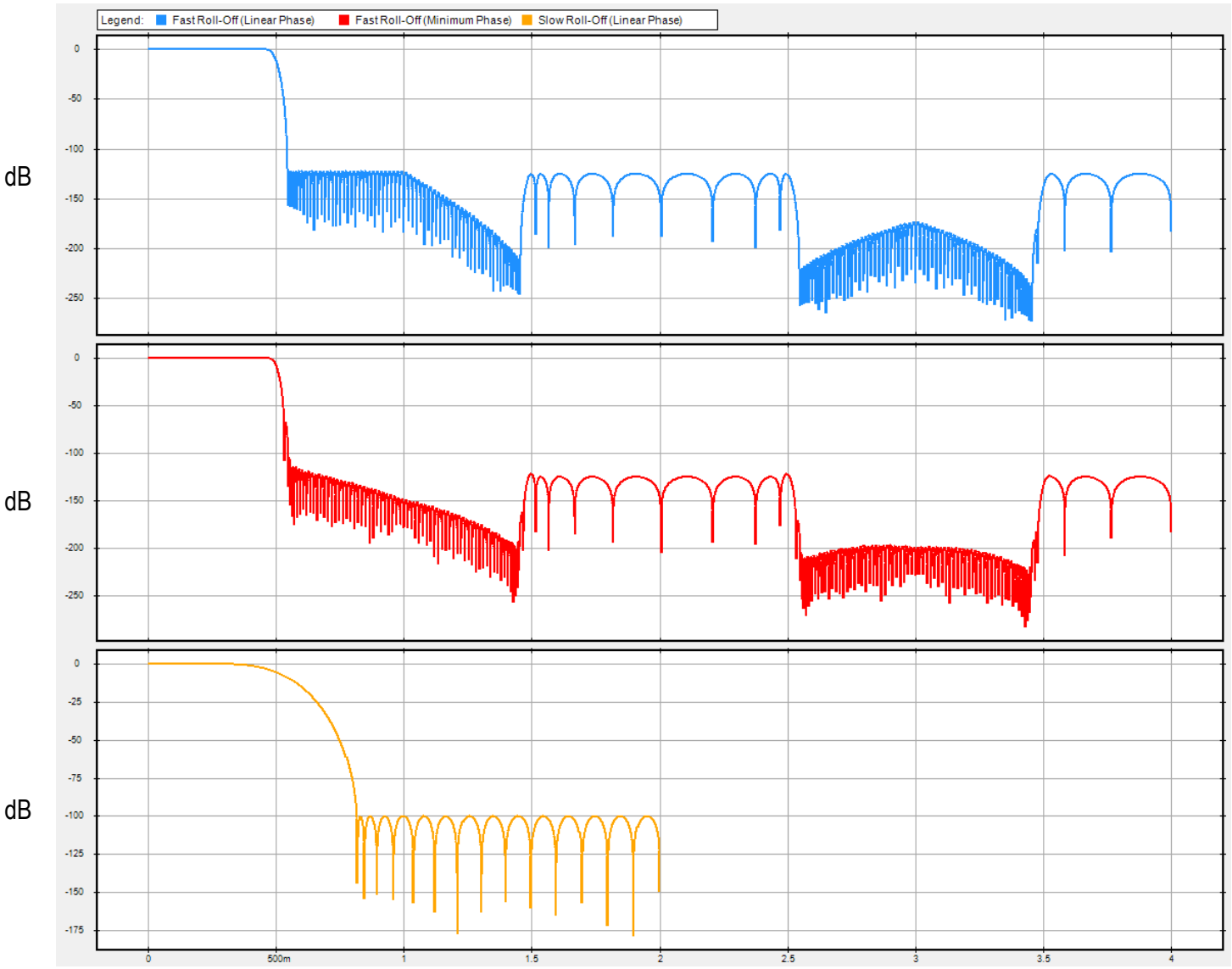
PCM DE-EMPHASIS FILTER RESPONSE (44.1kHz)



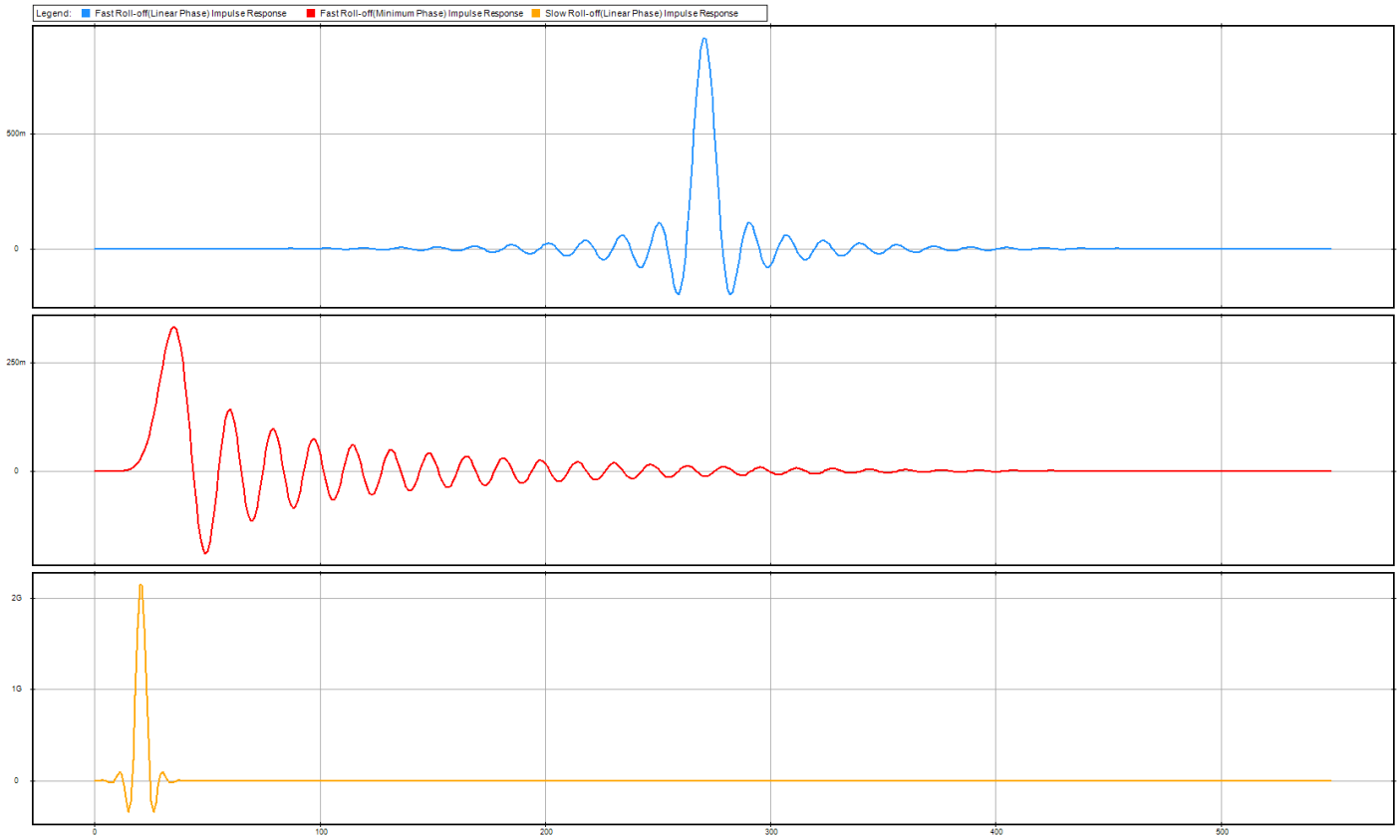
PCM DE-EMPHASIS FILTER RESPONSE (48kHz)



PCM FILTER FREQUENCY RESPONSE

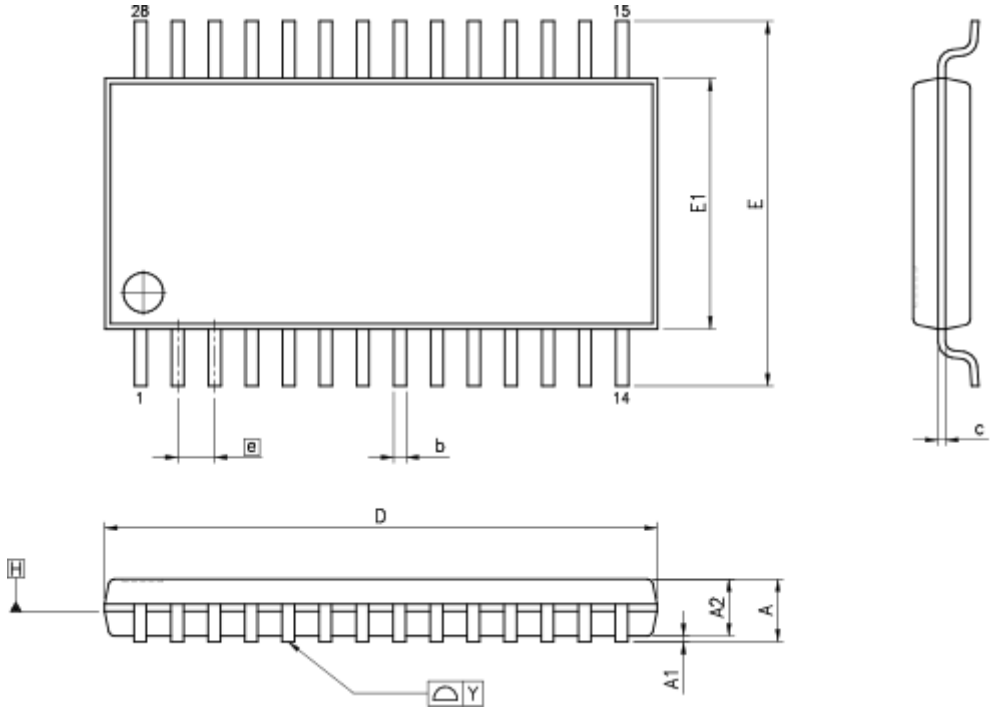


PCM FILTER IMPULSE RESPONSE



Unit: 1/fs (s)

28-Pin TSSOP Mechanical Dimensions



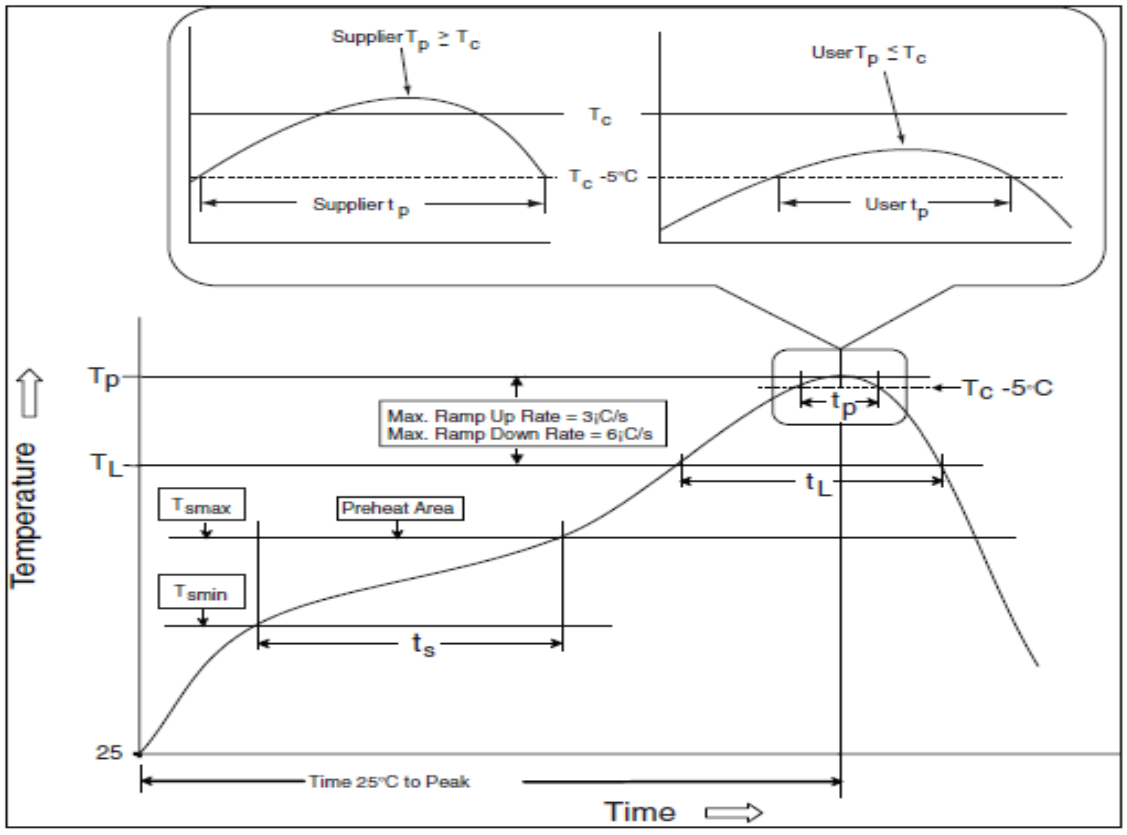
Symbol	Millimeter		
	MIN	NOM	MAX
A			1.2
A1	0.05		0.15
A2	0.80		1.00
A3	0.39	0.44	0.49
b	0.20		0.29
b1	0.19	0.22	0.25
c	0.14		0.18
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		

Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10°C to 20°C.
The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.
Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)



Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual Soldering:
Allowed up to 2 times with maximum temperature of 350 degrees no longer than 3 seconds.

Table RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	6°C / second max.
Time 25°C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within ± 2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.
For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Table RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

ORDERING INFORMATION

Part Number	Description	Package
ES9018JPA	Professional Audio DAC	28-pin TSSOP

Revision History

Rev.	Date	Notes
1.0	July 25, 2017	Initial Release
1.1	November 28, 2017	Removed ESS logo from pin diagram
1.2	November 15, 2018	Removed Advanced Information

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