Analog Reinvented

ES9826
32-bit High performance 2 Channel ADC w/PGA
Product Datasheet

The SABRE® ES9826 is a 32-bit analog-to-digital (A/D) converter targeted for professional audio applications such as recording systems, professional microphones, video conferencing, digital turntables, IP network camera systems, smart speakers, and other consumer applications.

The ES9826 has 2 integrated ADCs which use ESS' patented Hyperstream® IV ADC architecture, and a front-end PGA which delivers unprecedented audio sound quality and specifications, including a DNR of +123dB and a THD+N of -105dB in 2 channel mode with a 2.5kΩ input impedance.

The ES9826 introduces a new optional Auto Ranging Enhancement (ARE) function that broadens the dynamic range of the source material while maintaining audio integrity.

The SABRE ADC supports S/PDIF, I2S/LJ master/slave, and TDM digital output formats. The ES9826 can be controlled by software (I²C/SPI) or hardware mode (HW) to reduce or eliminate programming with external source.

A programmable microphone bias regulator is integrated for reduction of BOM requirements when using analog microphones.

Built-in digital filters with pre-programmed filter coefficients that allow for sound and latency preferences.

The ES9826 has an Ultra-Low Noise Floor Bandwidth of 200kHz. This bandwidth is up to 10 times wider than the competition, enabling higher resolution at higher sample rates.

FEATURE	DESCRIPTION
+123dB DNR per channel (w/ ARE) +115dB DNR per channel (w/o ARE) -105dB THD+N per channel	Unprecedented dynamic range and very low distortion
High Sample Rates	Up to PCM 768kHz through I2S and TDM output
Auto Ranging Enhancement (ARE)	Optional feature for enhancing performance
Customizable filter characteristics	8 presets of digital optimal filters
Programmable gain amplifier (PGA) w/ selectable input impedance	PGA frontend with +0-30dB gain in 3dB steps with 2.5kΩ or 10kΩ input impedance
Programmable microphone bias (MIC Bias)	Integrated programmable microphone bias regulator for BOM reduction costs Stereo PDM digital microphones are also supported
Integrated Analog PLL	Improved low jitter Analog PLL to generate clock and eliminate need for oscillator.
Multiple Output formats available	PCM, TDM, and S/PDIF outputs are available.
I²C, SPI, and Hardware interface control	Configured by microcontroller or other I²C/SPI source, or set mode through Hardware Mode to avoid programming registers.
Ultra-Low Noise Floor Bandwidth	200kHz bandwidth enabling higher resolution at higher sample rates
Integrated low noise ADC reference regulators	Reduced BOM cost, PCB area and improved DNR if required
Low Power Consumption	Simplifies power supply design
Low Pin Count Standardized Packaging	5mm x 5mm, 28 pin QFN

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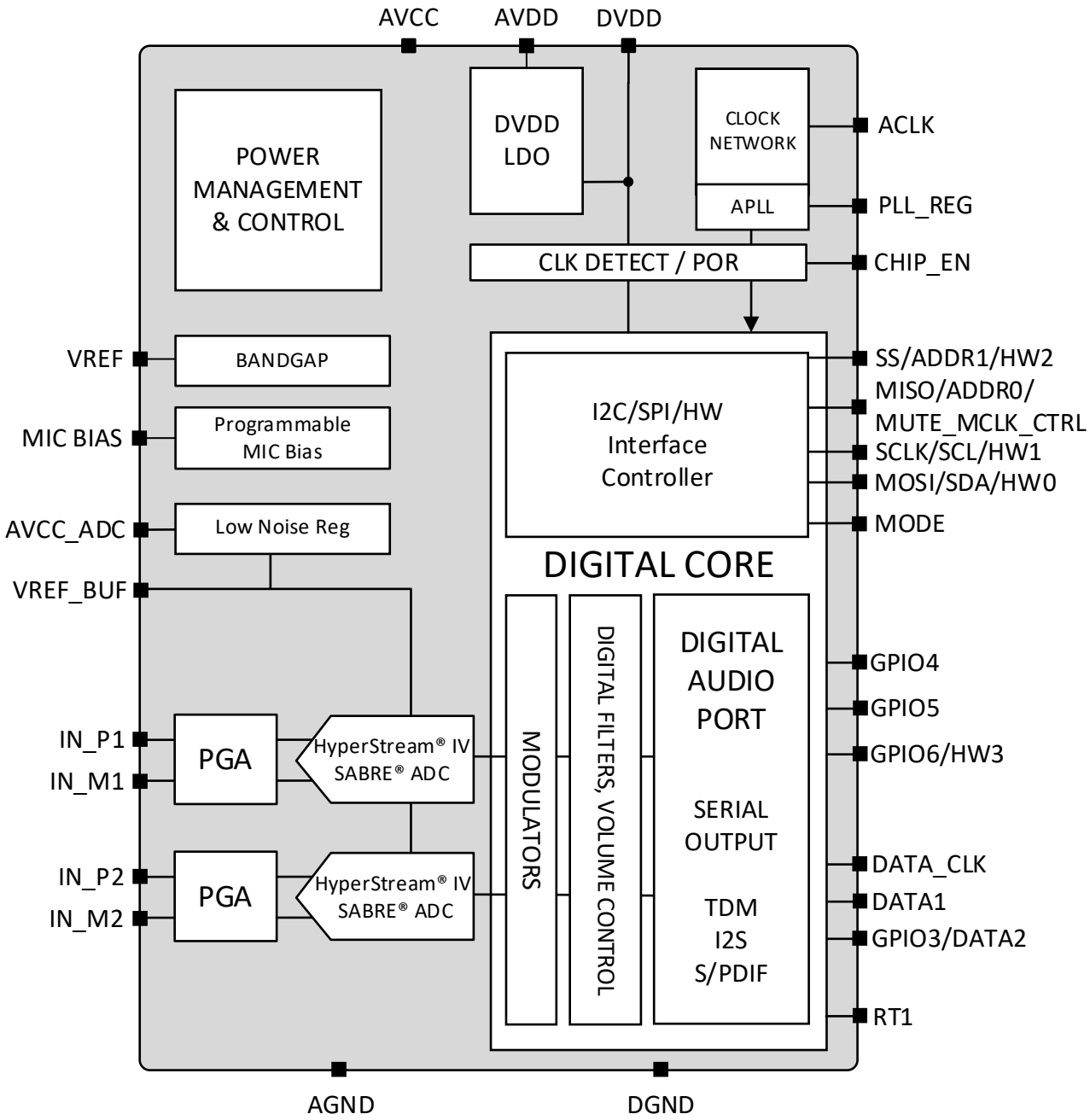


Figure 1 - ES9826 Block Diagram

ES9826 Pinout

28 QFN Pinout

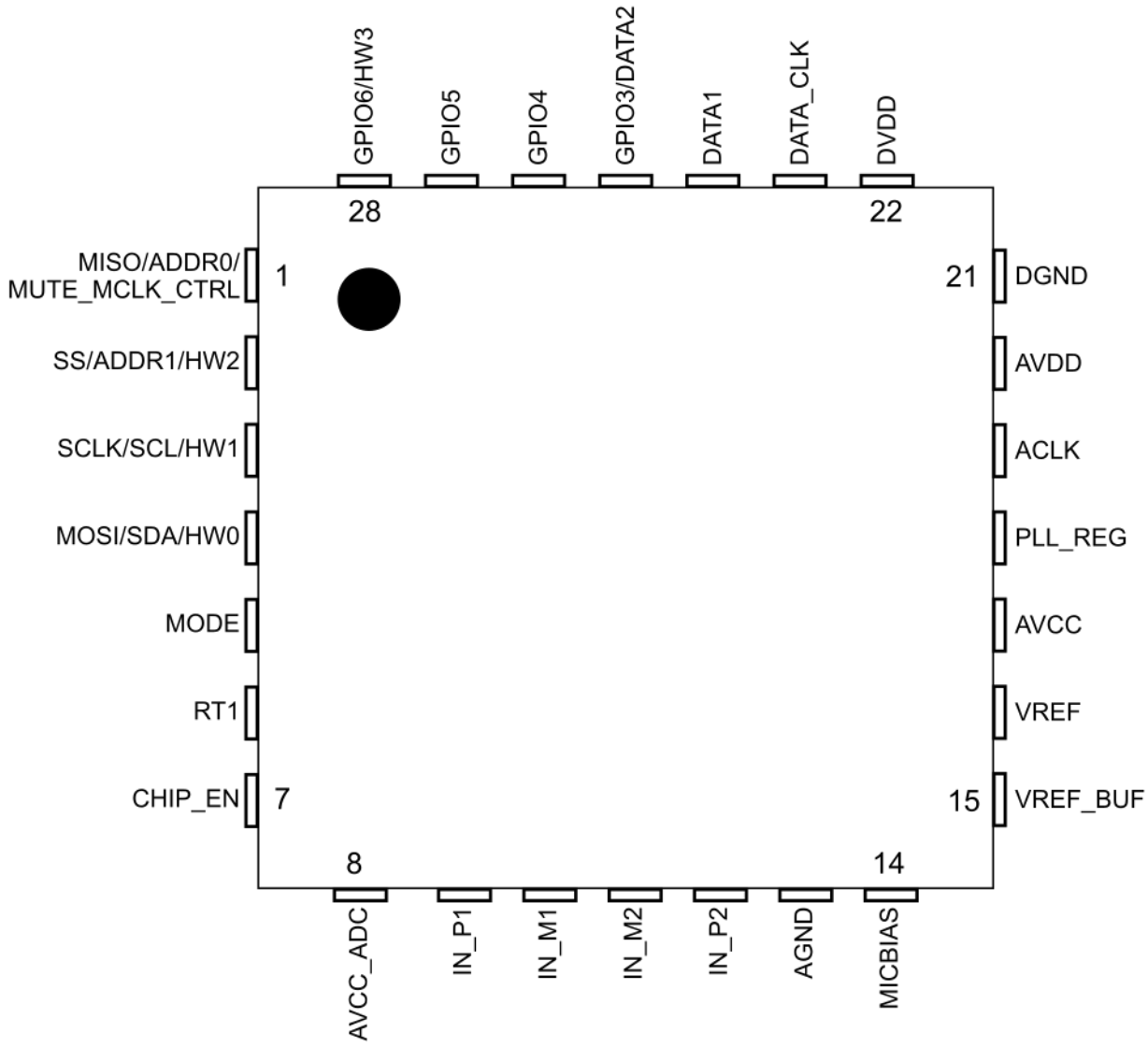


Figure 2. ES9826 Pinout*
(Top View)

*Note: ES9826Q has an exposed pad (pin 29) that should be connected to ground.

28 QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	MISO/ADDR0/ MUTE_MCLK_CTRL	I/O	HiZ	Serial communication for SPI/I²C & HW interface pin, controlled by MODE pin
2	SS/ADDR1/HW2	I/O	HiZ	Serial communication for SPI/I²C & HW2 interface pin, controlled by MODE pin
3	SCLK/SCL/HW1	I/O	HiZ	Serial communication for SPI/I²C & HW1 interface pin, controlled by MODE pin
4	MOSI/SDA/HW0	I/O	HiZ	Serial communication for SPI/I²C & HW0 interface pin, controlled by MODE pin
5	MODE	I/O	HiZ	I²C/SPI Control selection or HW mode
6	RT1	I	HiZ	Reserved. Must be connected to DGND for normal operation.
7	CHIP_EN	I/O	HiZ	Active-high chip enable.
8	AVCC_ADC	Power	Power	ADC reference voltage 3.3V Supply
9	IN_P1	AI	HiZ	ADC Channel 1 differential positive (+) input
10	IN_M1	AI	HiZ	ADC Channel 1 differential negative (-) input
11	IN_M2	AI	HiZ	ADC Channel 2 differential negative (-) input
12	IN_P2	AI	HiZ	ADC Channel 2 differential positive (+) input
13	AGND	Ground	Ground	Analog Ground
14	MIC_BIAS	Power	P/D	Analog microphone bias reference voltage output
15	VREF_BUF	Power	Power	Low Noise reference for on-chip regulator
16	VREF	Power	Power	Low Noise reference for bandgap circuitry
17	AVCC	Power	Power	3.3V Supply
18	PLL_REG	Power	Power	Low Noise reference for PLL regulator
19	ACLK	AI	HiZ	Main Clock Input
20	AVDD	Power	Power	3.3V, I/O Supply
21	DGND	Ground	Ground	Digital Core Ground
22	DVDD	Power	Power	Digital Core Supply. Internally Supplied
23	DATA_CLK	I/O	HiZ	Serial Clock pin
24	DATA1	I/O	HiZ	Serial Frame pin
25	DATA2/GPIO3	I/O	HiZ	Serial Data pin / General GPIO 3
26	GPIO4	I/O	HiZ	General GPIO 4
27	GPIO5	I/O	HiZ	General GPIO 5
28	GPIO6/HW3	I/O	HiZ	General GPIO 6 & HW3 interface pin, controlled by MODE pin
29*	Package PAD	-	-	Not electrically connected, used for heat dissipation

* Note: AO = Analog Output, I = Digital Input, I/O = Digital Input/Output,
**Note: Res. to Ground = Resistor to ground, see calibration resistor section for more information.

Table 1 – ES9826 28 QFN pin list

Configuration Modes

The ES9826 has options for hardware or software modes. They are controlled by the state of the MODE (pin 5):

MODE PIN	Configuration
0	Software mode - I²C interface
Pull Low	Hardware mode (see Hardware Mode Table, Table 9)
Pull High	Hardware mode (see Hardware Mode Table, Table 9)
1	Software mode - SPI interface

Table 2 - Mode pin configuration options

Software Mode

ES9826 supports I²C or SPI serial communication to configure registers.

I²C

- MODE (Pin 5) – '0' – ***GND.***
- Connect per I²C standard.
  - SDA (Pin 4)
  - SCL (Pin 3)
  - ADDR0 (Pin 1)
  - ADDR1 (Pin 2)

I²C Address	I²C Synchronous Address (PLL registers)	ADDR1	ADDR0
0x40	0x48	***GND***	***GND***
0x42	0x4A	***GND***	***AVDD***
0x44	0x4C	***AVDD***	***GND***
0x46	0x4E	***AVDD***	***AVDD***

Table 3 – I2C addresses

SPI

- Mode (Pin 5) – '1' – **AVDD.**
- Connect per SPI standard.
  - MOSI (Pin 4)
  - SCLK (Pin 3)
  - SS (Pin 2)
  - MISO (Pin 1)

SPI command	First byte
PLL	***7***
Write	***3***
Read	***1***

Table 4 - SPI commands

See I²C Slave Interface Timing or SPI Slave Interface for details.

Hardware Mode

The ES9826 hardware modes can be set with external pull-up and/or pull-down resistors. These modes configure the ADC for different output modes and sample rates. Hardware modes also support stereo digital PDM microphones as inputs.

Hardware modes are set with pins:

- MODE (Pin 5)
- HW0 (Pin 4)
- HW1 (Pin 3)
- HW2 (Pin 2)
- HW3/GPIO6 (Pin 28)
- MUTE_MCLK_CTRL (Pin 1)

Design Information

Hardware mode pins must be configured correctly for the desired hardware mode. Some guidelines include the following:

- The HW0 and HW1 pins are always 1/0 and do not require a pull-up or pull-down resistor.
- All HW pins must be set with CHIP_EN low as shown in the Recommended Hardware Mode Setup Sequence

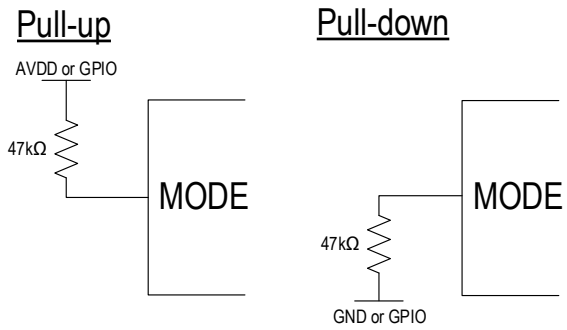


Figure 2 – Example hardware mode pin configurations

Input/Output Mode

In hardware modes #0 - #15, HW3 (Pin 28) sets the input mode between analog inputs through the ADC or digital PDM microphones. Hardware modes #16 - #30 are for TDM LJ slave modes and do not support S/PDIF output, or PDM input. S/PDIF output in hardware mode is only supported with the Master Mode modes #0 - #7

Pin	State	Input	Output
HW3/GPIO6	0	Analog – ADC See table 6.	PCM output
	Pull 0		S/PDIF output
	Pull 1	Digital – PDM See table 7.	S/PDIF output
	1		PCM output

Table 5 - Input modes controlled through HW3 (pin 28)

GPIO Table

In analog input mode, DC blocking can be enabled and/or disabled by setting GPIO5.
In digital PDM input mode, GPIO4 and GPIO5 are the PDM data and PDM_CLK, respectively.
GPIO3/DATA2 is always the digital data output, either in hardware TDM, PCM, or S/PDIF modes.

GPIO #	Input/Output	HW3 State	HW mode function
DATA2/GPIO3	Output	0 / 1	PCM data
		Pull 0 / Pull 1	S/PDIF data
GPIO4	Input	0 / Pull 0	Must connect to Ground
GPIO5	Input	0 / Pull 0	DC Block enable

Table 6 – Analog ADC GPIO functions in Hardware mode

GPIO #	Input/Output	HW3 State	HW mode function
DATA2/GPIO3	Output	0 / 1	PCM data
		Pull 0 / Pull 1	S/PDIF data
GPIO4	Input	Pull 1 / 1	PDM data
GPIO5	Output	Pull 1 / 1	PDM clock

Table 7 – Digital PDM GPIO functions in hardware mode

Mute

Set MUTE_MCLK_CTRL (Pin 1) to mute the output while in Hardware Mode:

HW MUTE Control (Pin 1)	Condition
0	Mute (MCLK 24.576MHz)
1	Unmute (MCLK 24.576MHz)
Pull 0	Mute (MCLK 49.152MHz)
Pull 1	Unmute (MCLK 49.152MHz)

Table 8 – Mute Control for HW mode configuration

Note: If MUTE_MCLK_CTRL (Pin 1) is set incorrectly, then it may seem that the ADC has higher noise than specified.

Hardware Mode Pin Configurations

The following table shows the available hardware modes for the ES9826.

	Description	FS[kHz]	BCK[MHz]	MODE	HW2	HW1	HW0
32-bit PCM Master Modes (Ext MCLK)							
0	I2S or S/PDIF with Ext MCLK	MCLK/128	MCLK/2 (64*FS)	Pull 0	0	0	0
1	I2S or S/PDIF with Ext MCLK	MCLK/256	MCLK/4 (64*FS)	Pull 0	0	0	1
2	I2S or S/PDIF with Ext MCLK	MCLK/512	MCLK/8 (64*FS)	Pull 0	0	1	0
3	I2S or S/PDIF with Ext MCLK	MCLK/1024	MCLK/16 (64*FS)	Pull 0	0	1	1
4	LJ or S/PDIF with Ext MCLK	MCLK/128	MCLK/2 (64*FS)	Pull 0	Pull 0	0	0
5	LJ or S/PDIF with Ext MCLK	MCLK/256	MCLK/4 (64*FS)	Pull 0	Pull 0	0	1
6	LJ or S/PDIF with Ext MCLK	MCLK/512	MCLK/8 (64*FS)	Pull 0	Pull 0	1	0
7	LJ or S/PDIF with Ext MCLK	MCLK/1024	MCLK/16 (64*FS)	Pull 0	Pull 0	1	1
32-bit PCM Slave Modes (PLL or Ext MCLK)							
8	I2S with Ext MCLK, AutoDetect FS	8 ≤ FS ≤ 384	64*FS	Pull 0	Pull 1	0	0
9	I2S with PLL from BCK	48	3.072	Pull 0	Pull 1	0	1
10	I2S with PLL from BCK	96	6.144	Pull 0	Pull 1	1	0
11	I2S with PLL from BCK	192	12.288	Pull 0	Pull 1	1	1
12	LJ with Ext MCLK , AutoDetect FS	8 ≤ FS ≤ 384	64*FS	Pull 0	1	0	0
13	LJ with PLL from BCK	48	3.072	Pull 0	1	0	1
14	LJ with PLL from BCK	96	6.144	Pull 0	1	1	0
15	LJ with PLL from BCK	192	12.288	Pull 0	1	1	1
32-bit TDM LJ Slave Modes, Autodetect FS & CH num							
16	TDM LJ Channel Slots = 1,2	8 ≤ FS ≤ 384	Auto (64FS, 128FS, 256FS, 512FS, 1024FS)	Pull 1	0	0	0
17	TDM LJ Channel Slots = 3,4	8 ≤ FS ≤ 384	Auto (128FS, 256FS, 512FS, 1024FS)	Pull 1	0	0	1
18	TDM LJ Channel Slots = 5,6	8 ≤ FS ≤ 192	Auto (256FS, 512FS, 1024FS)	Pull 1	0	1	0
19	TDM LJ Channel Slots = 7,8	8 ≤ FS ≤ 192	Auto (256FS, 512FS, 1024FS)	Pull 1	0	1	1
20	TDM LJ Channel Slots = 9,10	8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	0	0
21	TDM LJ Channel Slots = 11,12	8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	0	1
22	TDM LJ Channel Slots = 13,14	8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	1	0
23	TDM LJ Channel Slots = 15,16	8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	1	1
16-bit TDM LJ Slave Modes, Autodetect FS & CH num							
24	TDM LJ Channel Slots = 1,2	8 ≤ FS ≤ 384	Auto (32FS, 64FS, 128FS, 256FS, 512FS, 1024FS)	Pull 1	Pull 1	0	0
25	TDM LJ Channel Slots = 3,4	8 ≤ FS ≤ 384	Auto (64FS, 128FS, 256FS, 512FS, 1024FS)	Pull 1	Pull 1	0	1
26	TDM LJ Channel Slots = 5,6	8 ≤ FS ≤ 192	Auto (128FS, 256FS, 512FS, 1024FS)	Pull 1	Pull 1	1	0
27	TDM LJ Channel Slots = 7,8	8 ≤ FS ≤ 192	Auto (128FS, 256FS, 512FS, 1024FS)	Pull 1	Pull 1	1	1
28	TDM LJ Channel Slots = 9,10	8 ≤ FS ≤ 96	Auto (256FS, 512FS, 1024FS)	Pull 1	1	0	0
29	TDM LJ Channel Slots = 11,12	8 ≤ FS ≤ 96	Auto (256FS, 512FS, 1024FS)	Pull 1	1	0	1
30	TDM LJ Channel Slots = 13,14	8 ≤ FS ≤ 96	Auto (256FS, 512FS, 1024FS)	Pull 1	1	1	0
31	TDM LJ Channel Slots = 15,16	8 ≤ FS ≤ 96	Auto (256FS, 512FS, 1024FS)	Pull 1	1	1	1

Table 9 - Hardware mode pin configurations table

Recommended Hardware Mode Setup Sequence

The hardware mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted.

Note: It is recommended that MUTE_CTRL is set low until the HW mode is finalized and after CHIP_EN is asserted, then asserted last.

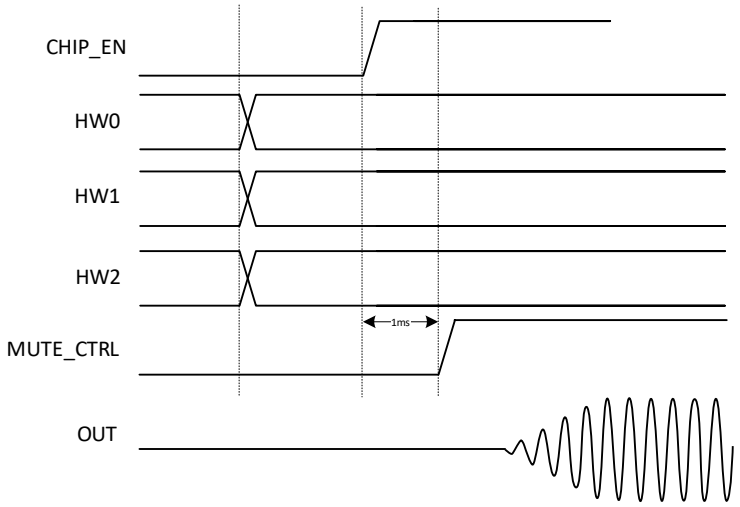
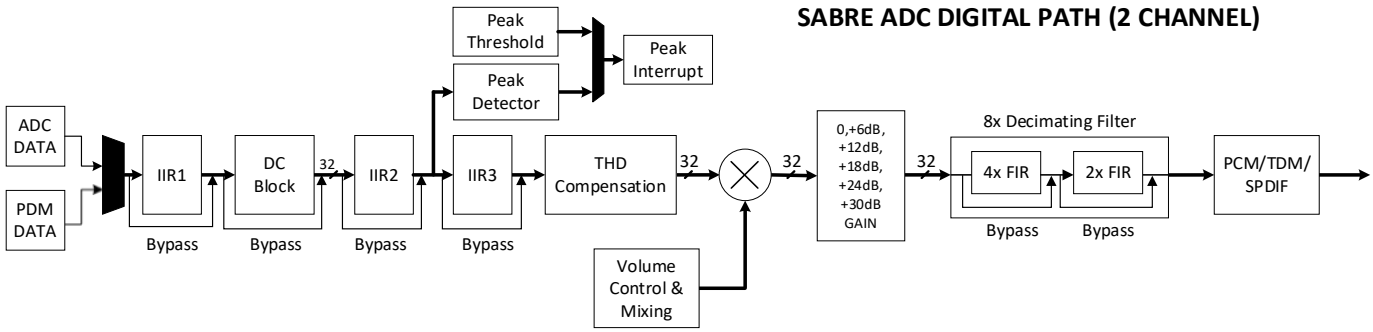


Figure 3 - Hardware mode startup sequence

Digital Features

Digital Signal Path



Volume Control

This volume control is intended for use during audio capture. Each channel can be digitally attenuated from 0dB to –90dB.
The maximum volume 0dB corresponds to CHx_VOLUME – 16'h7FFF.
The minimum volume -90dB corresponds to CHx_VOLUME – 16'h0001.
Muting the ADC output can be accomplished by setting the CHx_VOLUME to zero (16'h0000).

- 16'h8000 (0dB) to 16'hFFFF (-90dB) inverts the phase of the volume.

Channel volumes, by default, are updated as soon as the volume registers are written. The volume control can be updated by VOLUME_RATE by setting the ramp rate.

Volume Control Registers

- Register 46-45: CH1_VOLUME
- Register 48-47: CH2_VOLUME
- Register 49: VOLUME_RATE

Volume control is available for PCM, S/PDIF and TDM formats.

Peak Detect

The peak detector is configurable through software registers. GPIOs can output the peak detection on a per channel basis.

Applicable Registers:

- Register 38: PEAK DETECTOR CONFIG
- Register 39: CH1 PEAK THRESHOLD
- Register 40: CH2 PEAK THRESHOLD
- Register 224: PEAK FLAG READ (flag set if input signal peak level is greater than peak threshold)

- Register 238-237: PEAK CH1 READ (readback level)
- Register 240-239: PEAK CH2 READ (readback level)

8x FIR decimation filter

Select the decimation filter response from 8 pre-programmed filter shapes (Register 59[4:2] FILTER_SHAPE).

For more information on the filter responses, see Digital Filters section.

THD Compensation

The ES9826 has built-in THD compensation to help compensate for system second and third harmonics that may be present on the digital output signal. The compensation is controlled through 4 individual signed 16-bit coefficients.

The following equation displays how the second and third harmonics are affected by the C2 and C3 values:

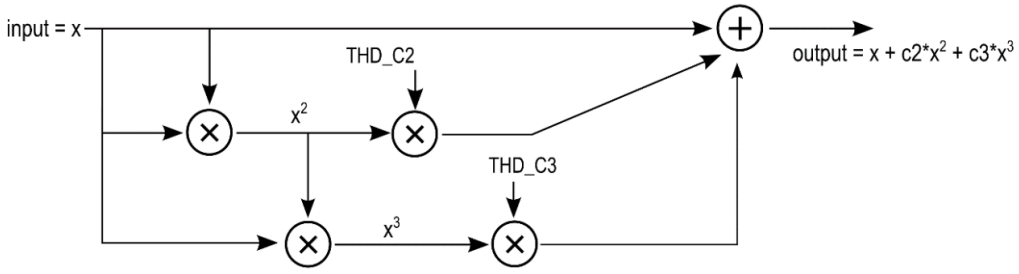


Figure 4 – THD Compensation Block Diagram

For best results, the chosen compensation coefficients should be tuned for each system/device in-situ. For reference, the THD coefficients used on the ESS EVB are C2=0, C3=0, bypassing the THD compensation.

THD Compensation Coefficient Registers

- Registers 51-50: THD_C2_CH1, THD Compensation C2 for Channel 1
- Registers 53-52: THD_C3_CH2, THD Compensation C3 for Channel 1
- Registers 55-54: THD_C2_CH2, THD Compensation C2 for Channel 2
- Registers 57-56: THD_C3_CH2, THD Compensation C3 for Channel 2

Note: Coefficients are 16-bit signed values

Audio Output Formats

The ES9826 supports multiple serial output data formats.

In Hardware mode, see Input/Output mode table to configure the output format. Hardware mode is limited to a single output format. Since S/PDIF and PCM data are both on GPIO3, the user must choose between the two options.

In Software mode, the TDM encoder (used for TDM and PCM) is enabled, and the S/PDIF encoder is disabled by default. In Software mode, both PCM and S/PDIF outputs can be used in parallel since S/PDIF can be mapped to any GPIO.

PCM (I2S, LJ)

Data is packaged as 2 channel slots per data line. Either ADC can be mapped to either the first or second slot of the frame through Registers 7[4:0] & 8[4:0] **TDM_SLOT_SEL_CHx**. Data is latched on the positive edge of BCLK.

Pin Name	Function	Description
DATA_CLK	I2S BCLK	I2S clock (Bit Clock), Master or Slave
DATA1	I2S WS	I2S WS (Word Select/Frame Select), Master or Slave
GPIO3/DATA2	I2S DATA	I2S DATA

Table 10 - PCM pin connections

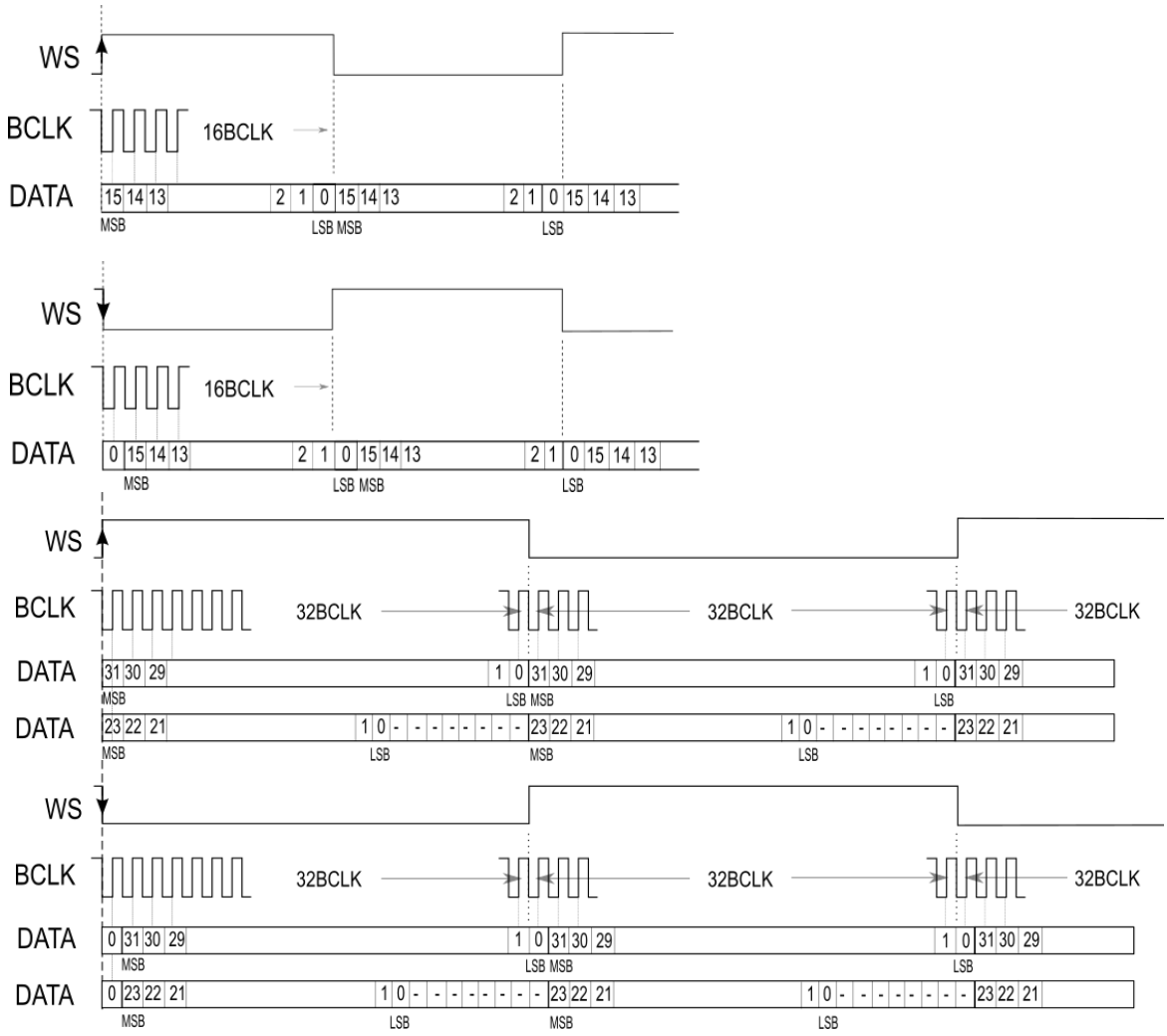


Figure 5 – LJ & I2S Input for 16-bit and 32-bit word widths

TDM (Time-division multiplexing)

The ES9826 supports time-division multiplexing (TDM) format, allowing more than 2 channels (or slots) to be transmitted on each data line, up to a maximum of 32 channels per data line. Typical formats are TDM128 (4chx32bit), TDM256 (8chx32bit), TDM512 (16chx32bit) and TDM1024 (32chx32bit). In this mode, Registers 7[4:0] & 8[4:0] **TDM_SLOT_SEL_CHx** can be used to internally map either ADC to any TDM slot (channel). Data is latched on the positive edge of BCLK.

TDM Pin Connections (default configuration)

Pin Name	Function	Description
DATA_CLK	TDM BCLK	TDM clock, Master or Slave
DATA1	TDM WS	TDM WS (Word Select/Frame Select), Master or Slave
DATA2	TDM DATA	TDM DATA

Table 11 - TDM pin connections

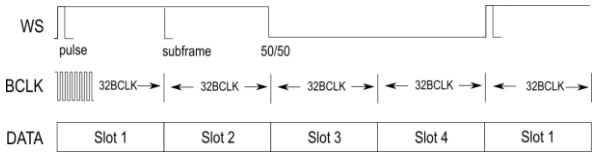


Figure 6 – TDM128 mode

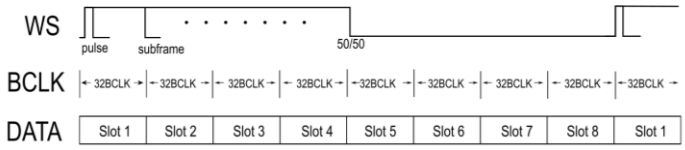


Figure 7 – TDM256 mode

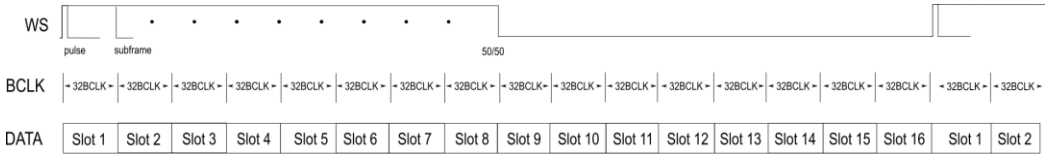


Figure 8 – TDM512 mode

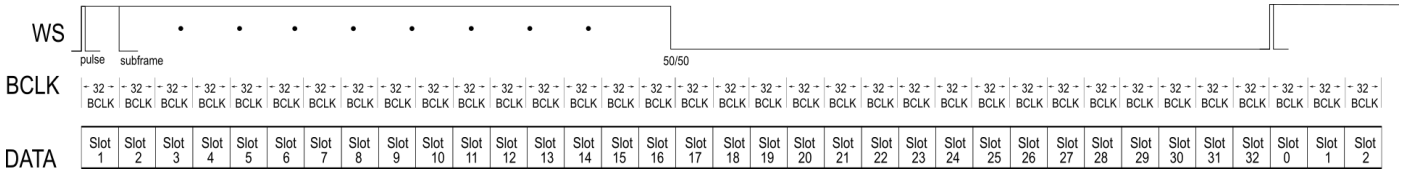


Figure 9 – TDM1024 mode

Multiple ES9826 devices in parallel in TDM mode

In TDM modes, several ES9826 can be used in parallel to increase the number of channels. Each ES9826 can be configured in HW or SW mode to output its data to different slots on the TDM DATA line.
Note: In hardware modes, only Left Justified TDM formats are supported. In software mode, the user can configure it to be I2S TDM format.

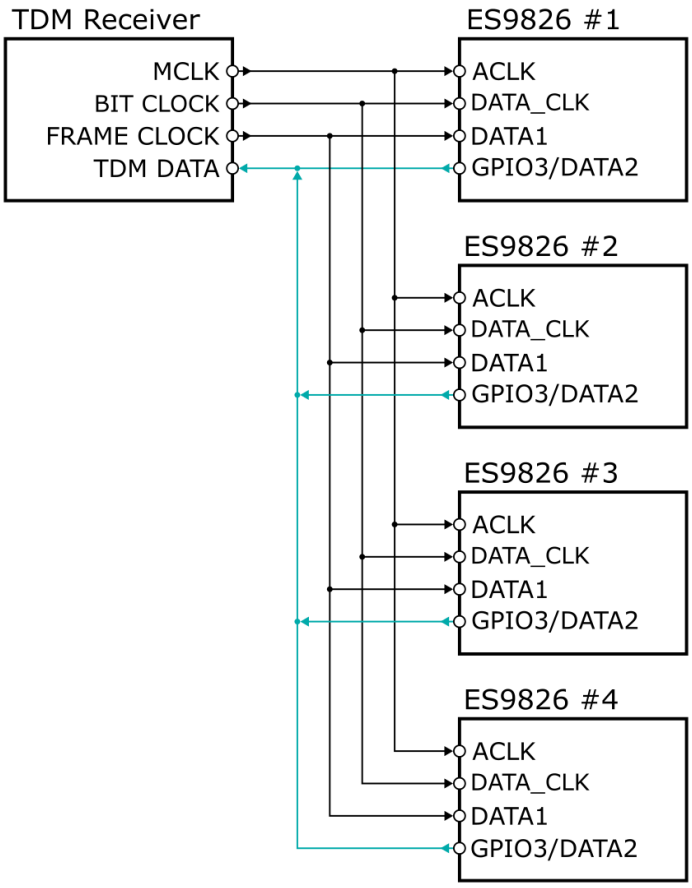


Figure 10 – TDM connection of several ES9826 devices in parallel

Applicable Registers

- Register 5[1] TDM_LJ_MODE set to 1'b1.
- Register 5[2] TDM_VALID_EDGE set to 1'b1.
- Register 5[0] TDM_LENGTH: Sets the width of one data word. 1’b0: 32-bits (default), 1’b1: 16-bits.
- Register 6[4:0] TDM_CH_NUM or using Register 6[7] AUTO_CH_DETECT: Sets the # of TDM slots / frame.
- Register 7[4:0] & Register 8[4:0] TDM_SLOT_SEL_CHx: Sets the TDM slots for each device.

S/PDIF

S/PDIF output is only available in Master Mode. Register 4[0] MASTER_MODE_ENABLE must be set to 1'b1.

Pin Name	Description
GPIO3/DATA2	HW mode requires for GPIO3/DATA2 pin to be the S/PDIF output.
GPIO3 – GPIO6	SW mode allows for any GPIO to be the S/PDIF output.

Table 12 - S/PDIF pin connections

S/PDIF is transmitted over a single signal line using dual phase encoded data, which allows for clock extraction from the data signal line.

GPIO Configuration

GPIOs 3 to 6 have 16 configurable modes set by GPIO#_CFG. The table below shows the available configurations:

GPIO_CFG	Function	Input / Output	GPIO3	GPIO4	GPIO5	GPIO6	Description
4'd0	Analog Shutdown	-	Shutdown				Output shutdown
4'd1	AUX Input	I	N/A	PDM DATA	N/A	N/A	GPIO4 is PDM DATA input.
4'd2	AUX Output	O	PCM DATA	N/A	PDM CLK	N/A	GPIO5 is PDM CLK output in PDM mode. GPIO3 is PCM DATA in PCM mode.
4'd3	RESERVED	O	N/A				
4'd4	RESERVED	O	N/A				
4'd5	CH1 Peak Interrupt	O	CH1 Peak Interrupt				Interrupt status of Ch1 peak detector.
4'd6	CH2 Peak Interrupt	O	CH2 Peak Interrupt				Interrupt status of Ch2 peak detector.
4'd7	OR of all interrupts	O	OR of all unmasked interrupts				OR of ARE and Peak detect interrupts.
4'd8	S/PDIF data stream	O	S/PDIF data stream				S/PDIF output format. Requires ENABLE_SPDIF_ENCODE = 1.
4'd9	PWM Signal	O	PWM signal				PWM output. See PWM Signal for formula.
4'd10	CH1 ARE Interrupt	O	CH1 ARE Interrupt				CH1 ARE interrupt
4'd11	CH2 ARE Interrupt	O	CH2 ARE Interrupt				CH2 ARE interrupt.
4'd12	CLK_IADC	O	CLK_IADC				Front-end decimation path clock. Should ideally be run at 24.576MHz / 22.5792MHz.
4'd13	CLK_ADC (128*FS Hz)	O	CLK_ADC				Back-end decimation path clock. Needs to be run at 128*FS. Note: 64*FS with ENABLE_2X_MODE.
4'd14	Output 0	O	Output 0				Output 0.
4'd15	Output 1	O	Output 1				Output 1.

Table 13 - GPIO Configuration function

Note: If PDM_INPUT_SEL is set, it will automatically output PDM CLK on GPIO5 and expect PDM data input on GPIO4.

Interrupts

Interrupts can be output through GPIOs. By default, interrupts are all masked and require unmasking to connect to GPIOs. To unmask interrupts, use Register 12 – INTERRUPT MASK.

OR of All Interrupts

GPIOx_CFG can be set to a bitwise OR of all unmasked interrupts.

Interrupts that are ORed together:

- INT_MASK_CH2_ARE_ENGAGED
- INT_MASK_CH1_ARE_ENGAGED
- INT_MASK_CH2_PEAK_DET
- INT_MASK_CH1_PEAK_DET
- INT_MASK_CH2_PEAK_LATCH*
- INT_MASK_CH1_PEAK_LATCH*

Note: All interrupts mentioned above will self-clear with the exception of INT_MASK_CHx_PEAK_LATCH*. INT_MASK_CHx_PEAK_LATCH requires Register 19[1:0] INT_CLEAR_CHx_PEAK_LATCH to be toggled to clear the interrupt.

Digital Filters

The ES9826 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 59[4:2] FILTER_SHAPE for configuration).

The pre-programmed filters are:

1. **Minimum phase (default)**
2. Linear phase apodizing fast roll-off
3. Linear phase fast roll-off
4. Linear phase fast roll-off low-ripple
5. Linear phase slow roll-off
6. Minimum phase fast roll-off
7. Minimum phase slow roll-off
8. Minimum phase slow roll-off low dispersion

#	Filter	Description
1	**Minimum phase (default)**	Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection
2	Linear phase apodizing fast roll-off	Full image rejection by fs/2 to avoid any aliasing, with smooth roll-off starting before 20k.
3	Linear phase fast roll-off	Sabre legacy filter, optimized for image rejection @ 0.55 fs
4	Linear phase fast roll-off low-ripple	Sabre legacy filter, optimized for in-band ripple
5	Linear phase slow roll-off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response

6	Minimum phase fast roll-off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55fs
7	Minimum phase slow roll-off	Lowest latency at the cost of image rejection
8	Minimum phase fast roll-off low dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 14 – FIR digital filter properties

Note on Minimum phase filters:

Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

PCM Filter Properties (44.1kHz Sampling)

Minimum phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-82 dB	0.54 x fs			Hz
Group Delay		2.90/fs		9.24/fs	s
Flatness (ripple)	0.0030				dB

Linear phase apodizing fast roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 x fs	Hz
Stop band	-75 dB	0.5 x fs			Hz
Group Delay			33.25/fs		s
Flatness (ripple)	0.0034				dB

Linear phase fast roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-76 dB	0.54 x fs			Hz
Group Delay			32.88/fs		s
Flatness (ripple)	0.0043				dB

Linear phase fast roll-off low ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-73 dB	0.55 x fs			Hz
Group Delay			33.00/fs		s
Flatness (ripple)	0.0040				dB

Linear phase slow roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.50 x fs	Hz
Stop band	-84 dB	0.81 x fs			Hz
Group Delay			5.87/fs		s
Flatness (ripple)	-				dB

Minimum phase fast roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-80 dB	0.54 x fs			Hz
Group Delay		2.95/fs		9.42/fs	s
Flatness (ripple)	0.0038				dB

Minimum phase slow roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 x fs	Hz
Stop band	-90 dB	0.80 x fs			Hz
Group Delay		2.03/fs		2.53/fs	s
Flatness (ripple)	-				dB

Minimum phase slow roll-off low dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 x fs	Hz
Stop band	-90 dB	0.80 x fs			Hz
Group Delay		11.66/fs		11.73/fs	s
Flatness (ripple)	-				dB

Table 15 – PCM Filter Properties

PCM Filter Latency

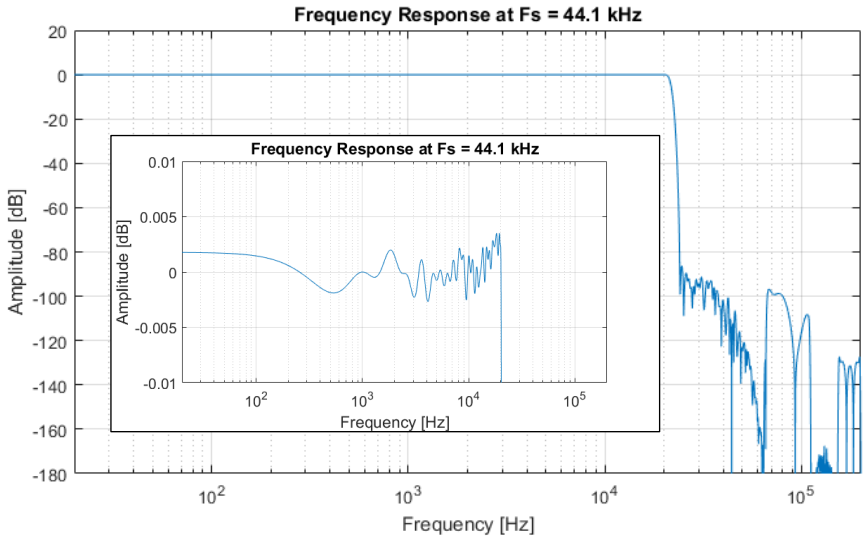
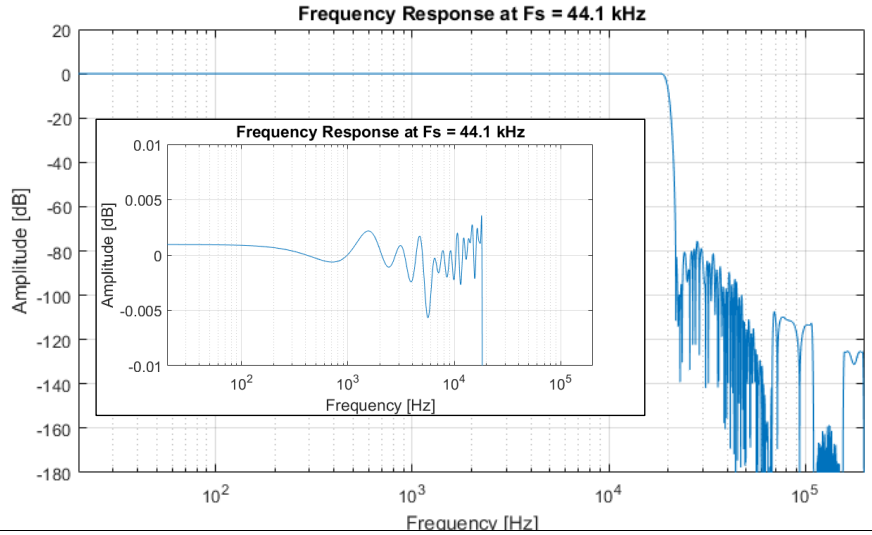
The following table shows the simulated latency of each filter at 44.1kHz sampling rate. The latency was measured at the peak amplitude of the impulse response prior to being down sampled to 1FS. Latency delay will reduce (scale) with sampling rate.

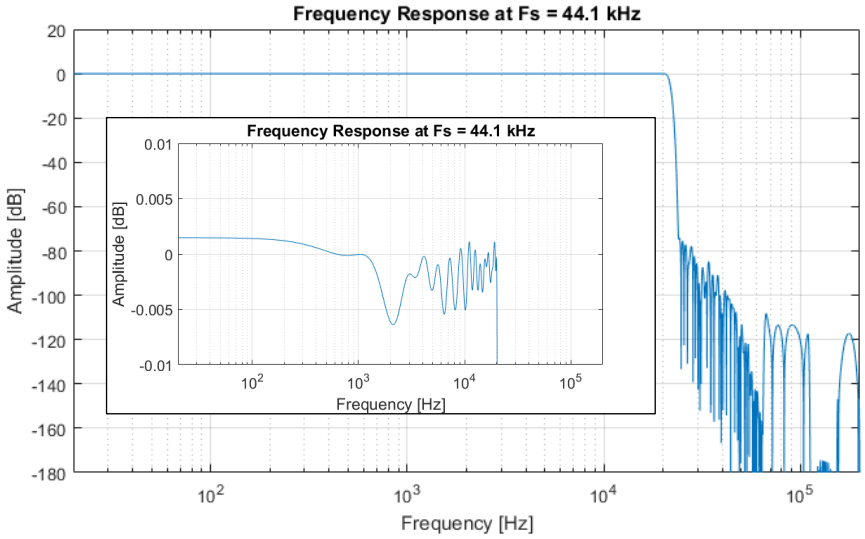
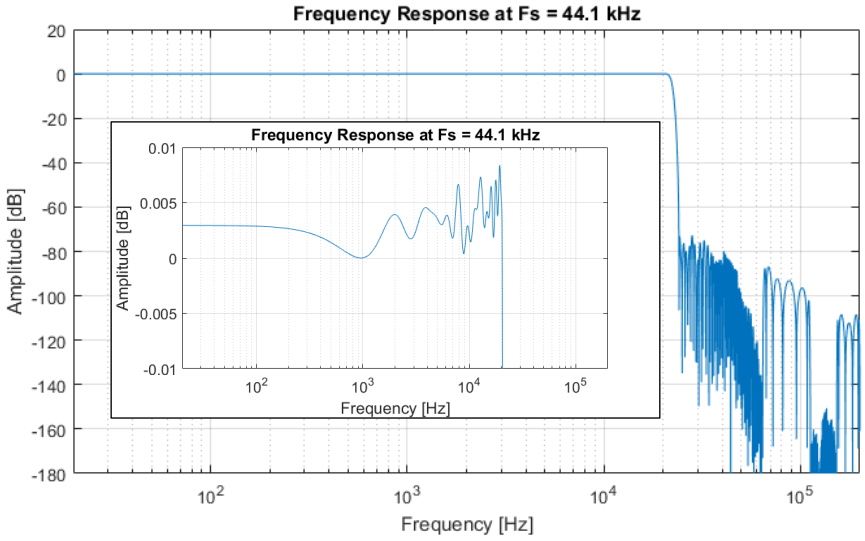
Digital Filter	Delay(us) @ fs=44.1kHz
Minimum phase (default)	156 us
Linear phase apodizing fast roll-off	833 us
Linear phase fast roll-off	836 us
Linear phase fast roll-off low ripple	828 us
Linear phase slow roll-off	213 us
Minimum phase fast roll-off	159 us
Minimum phase slow roll-off	133 us
Minimum phase slow roll-off low dispersion	357 us

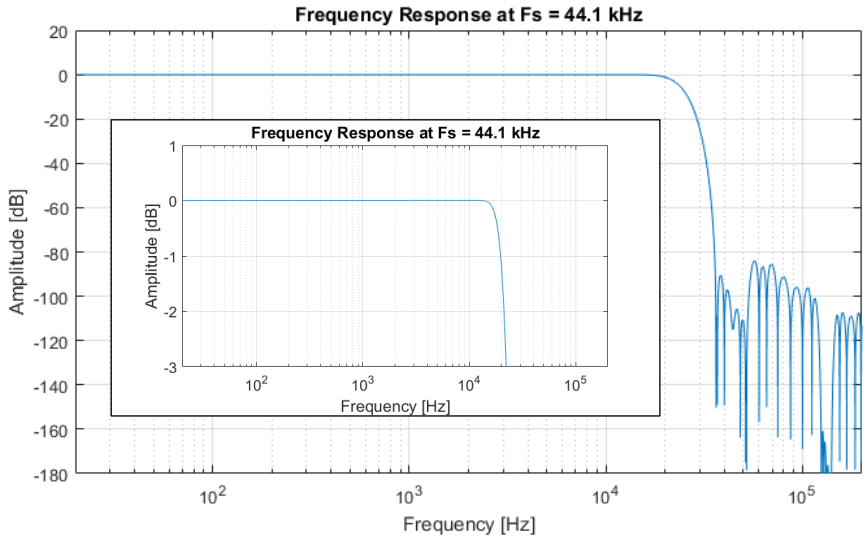
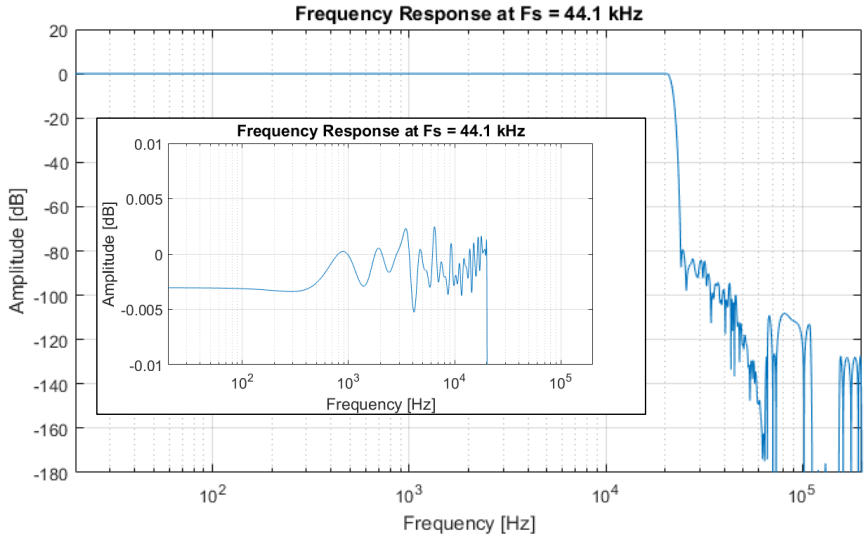
Table 16 - Latency of Pre-Programmed Digital Filters

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum phase	
Linear phase apodizing fast roll-off	

Linear phase fast roll-off	
Linear phase fast roll-off low ripple	

Linear phase slow roll-off	
Minimum phase fast roll-off	

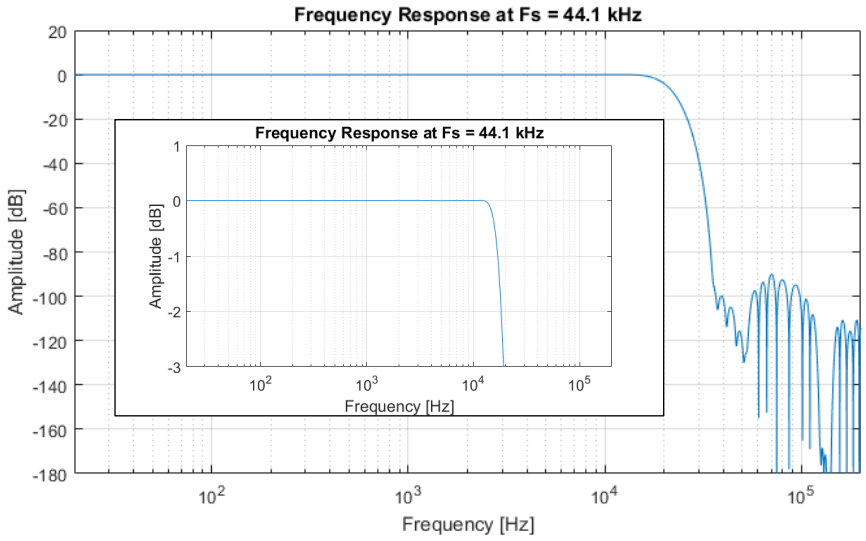
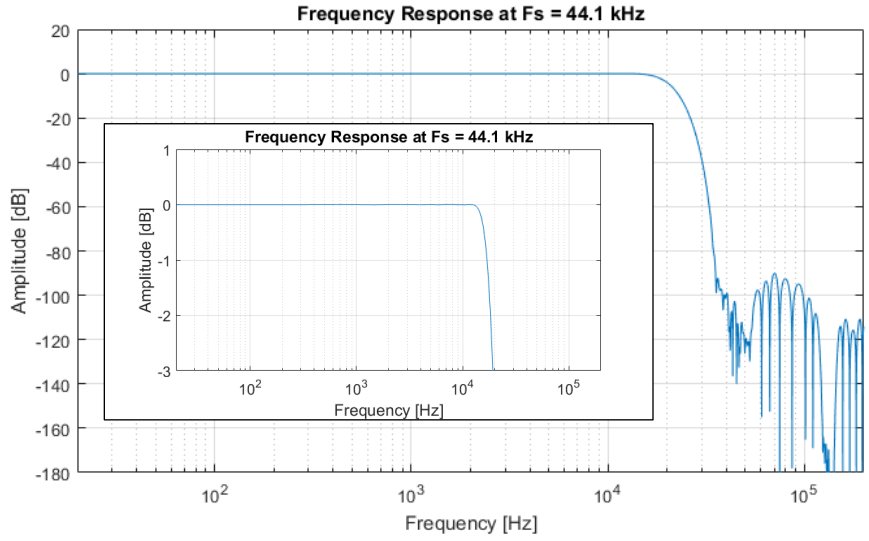
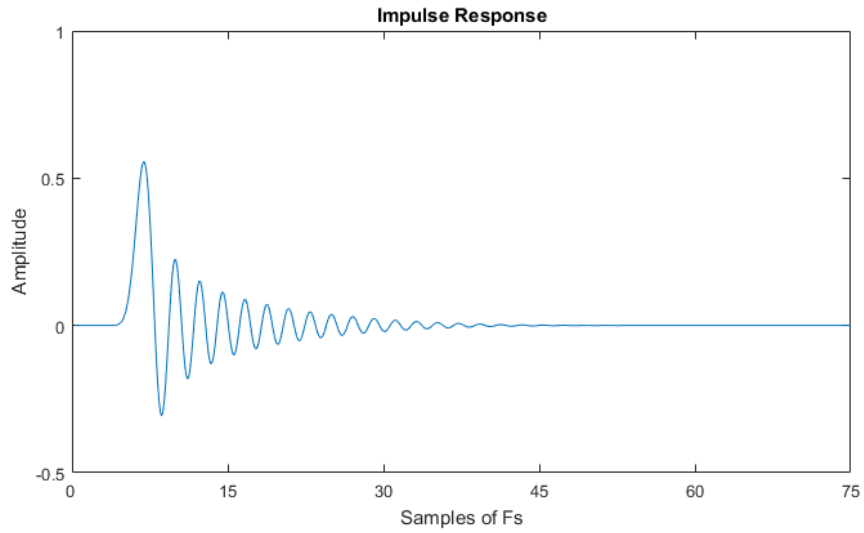
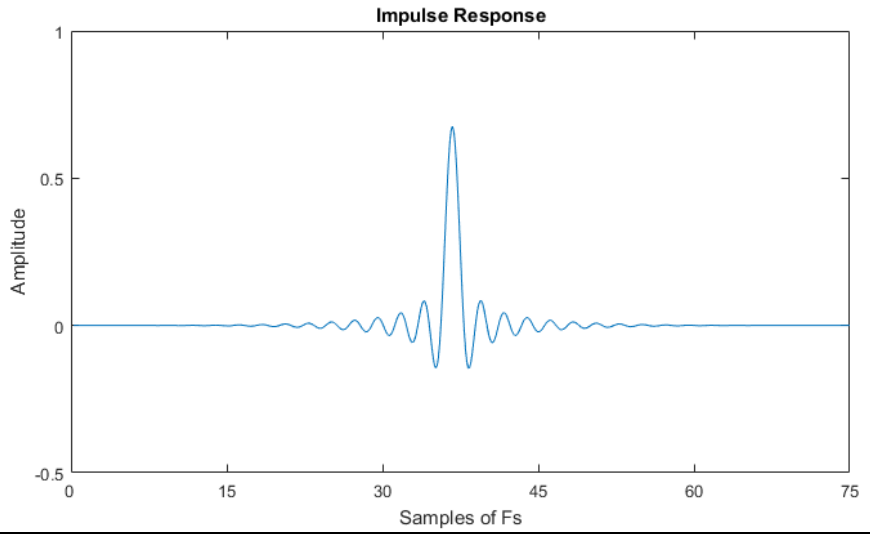
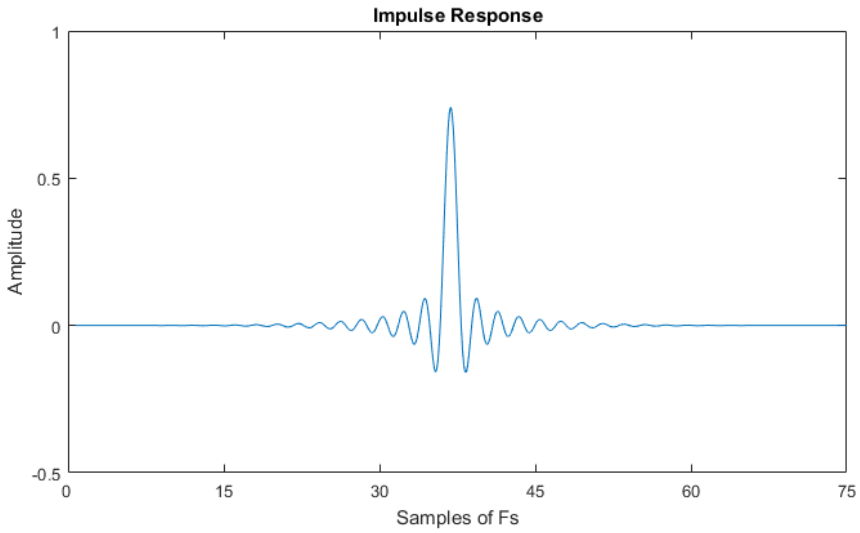
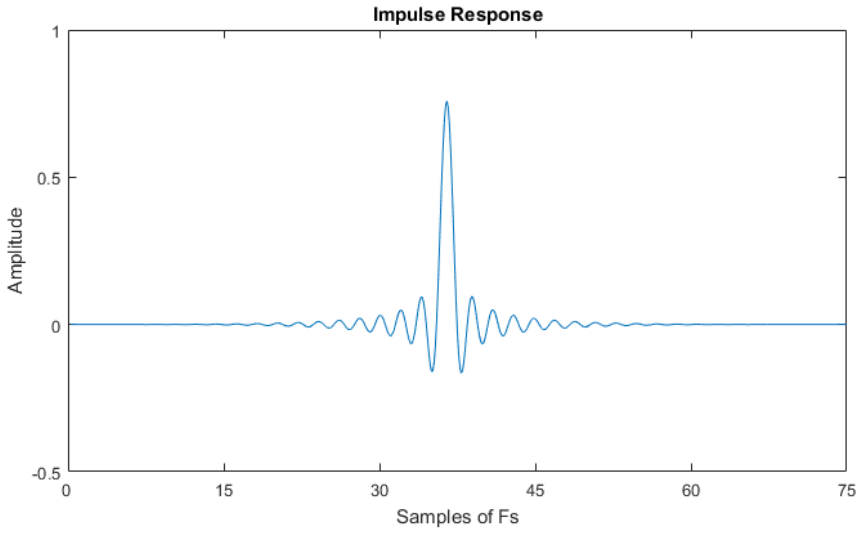
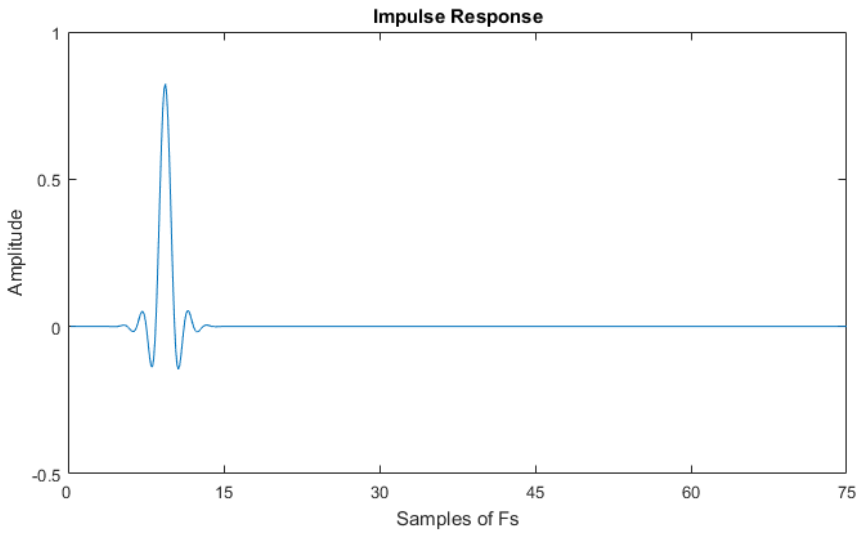
Minimum phase slow roll-off	
Minimum phase slow roll-off low dispersion	

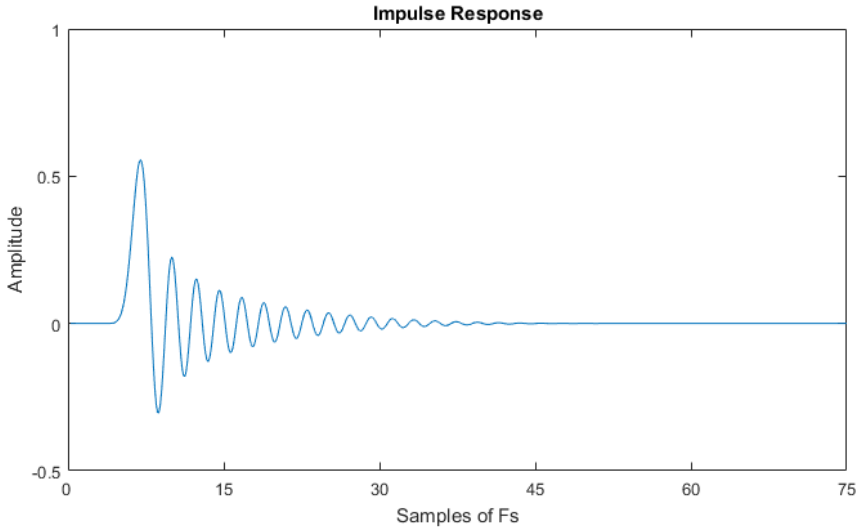
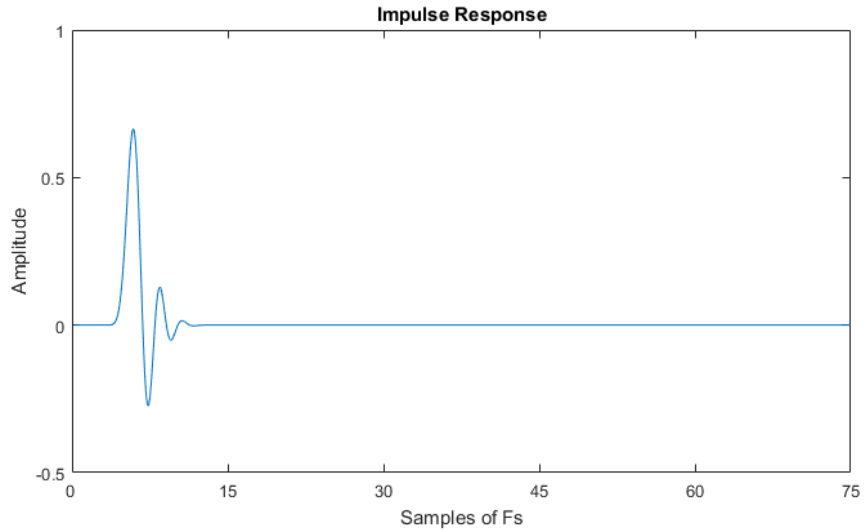
Table 17 – PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. The impulse responses the decimation path uses, prior to the down-sampling to 1FS are reported below.

Filter	Impulse Response
Minimum phase	
Linear phase apodizing fast roll-off	

Linear phase fast roll-off	
Linear phase fast roll-off low ripple	
Linear phase slow roll-off	

Minimum phase fast roll-off	
Minimum phase slow roll-off	

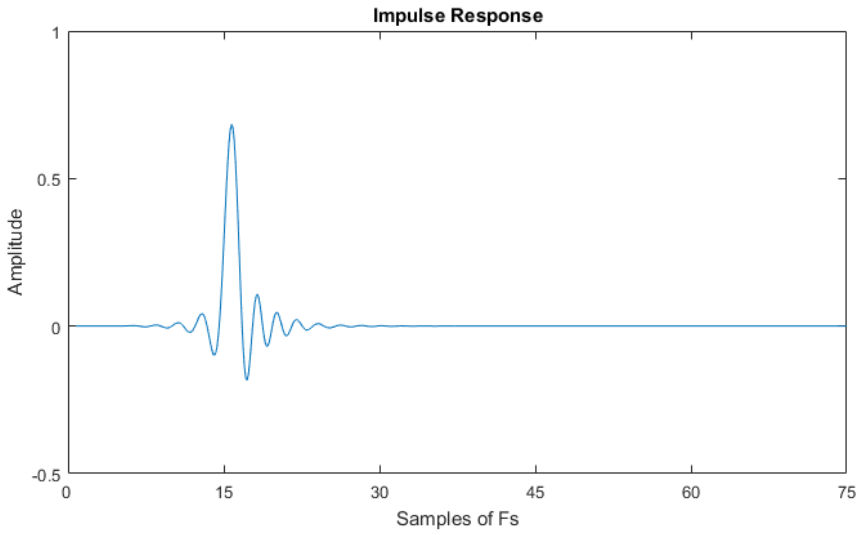
Minimum phase slow roll-off low dispersion	

Table 18 – PCM Filter Impulse Response

PDM input mode

The ES9826 supports stereo digital PDM input microphones both in hardware and software modes. The PDM input goes through the ADC decimation path and can be output as PCM or S/PDIF.

In hardware mode, PDM input mode can be enabled by setting HW3 according to Input/Output Mode.

In software mode, PDM input can be enabled by setting Register 37[4] PDM_INPUT_SEL.

Note: If PDM_INPUT_SEL is set, it will automatically output PDM CLK on GPIO5 and expect PDM data input on GPIO4.

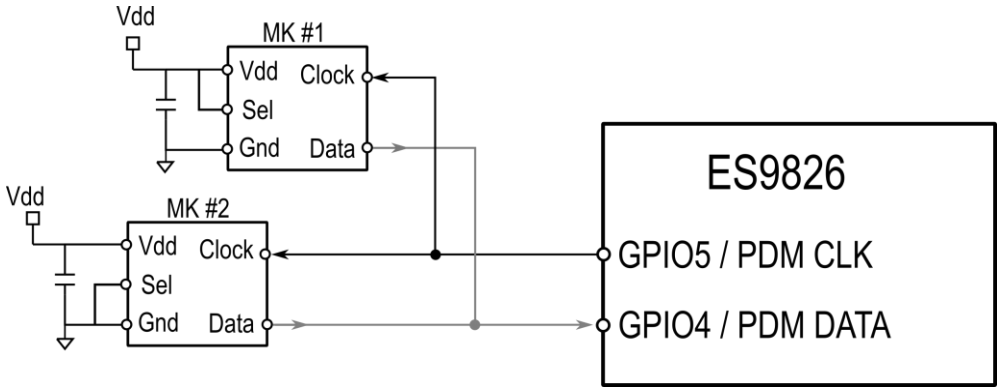


Figure 11 - PDM input mode application diagram with stereo PDM microphones.

PWM Signal

Output a configurable PWM signal. Frequency and duty cycle of PWM signal can be calculated with the following equations:

$$frequency\ [Hz] = \frac{MCLK}{PWM\_FREQ + 1}$$

$$Duty\ Cycle\ [\%] = \left(\frac{PWM\_COUNT}{PWM\_FREQ + 1}\right) \times 100$$

Configured with 8-bit value Register 33: PWM_COUNT and 16-bit value Registers 35-34: PWM_FREQ.

Analog Features

Programmable Gain Amplifier (PGA)

The ES9826 integrates an analog programmable gain amplifier (PGA) with a 0 to +30dB gain in increments of +3dB steps.

Applicable registers:

- Register 62: PGA GAIN CONTROL EN (defaults to 0)
- Register 67: ADC ATTEN SET
- Register 68: PGA GAIN CONTROL
- Register 72: PGA SETTINGS

Auto Ranging Enhancement (ARE)

The ES9826 introduces a new optional Auto Ranging Enhancement (ARE) function that broadens the dynamic range of the source material while maintaining audio integrity.

ARE is available in software mode only. An ARE application note will be available from ESS FAE or distributor.

Clock Selection

The ES9826 requires a 49.152/45.1584MHz or 24.576/22.5792MHz clock. It can be provided from an external high quality clock or it can be configured through the integrated PLL by setting the PLL dividers and enables.

- EN_MCLK_IN – Register 193[0]
  - Enables clock inputs to the digital core
- SEL_MCLK_IN – Register 193[2:1]
  - Selection of the ADC & digital core clock (ACLK/PLL)
- EN_PLL_CLK_IN – Register 193[3]
  - Enables SEL_PLL_IN source input
- SEL_PLL_CLK_IN – Register 193[5:4]
  - Selection of PLL clock source (ACLK or BCK)

Analog Phase Locked Loop (APLL)

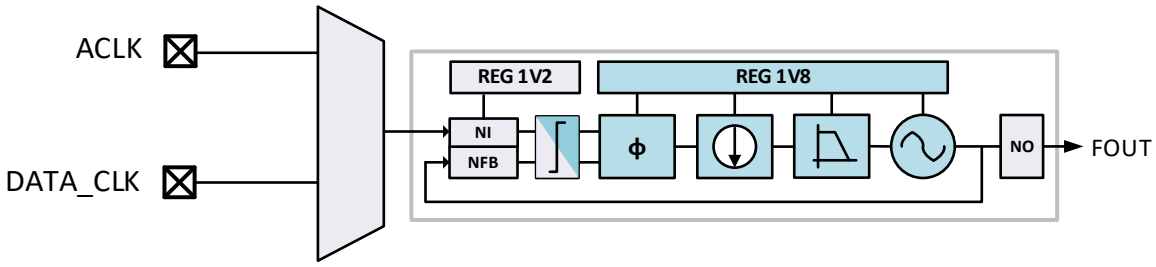


Figure 12 - Functional Block Diagram of ES9826 APLL

The ES9826 has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally. For the application note on the APLL, please ask your FAE or distributor.

For calculation of the PLL frequency output, use the following formulas:

$$F_{ref} = \left(\frac{F_{in}}{N_i}\right) \qquad F_{vco} = \left(\frac{F_{in}}{N_i}\right) * FBDIV \qquad N_{fb} = \frac{2^{25}}{FBDIV} \qquad F_{out} = \left(\frac{F_{in}}{N_i}\right) * \frac{N_{fb}}{N_o}$$

Where:

a. FBDIV is a 24-bit number
b. PLL frequency range requirements:
    a. *Fref* requirement: 2.5MHz < *Fref* < 12 MHz
    b. *Fvco* requirement: 90MHz < *Fvco* < 110MHz
    c. *Fout* requirement: 22.5792/24.576MHz & 45.1584/49.152Mhz
c. Ni = input divider
    - Accessible from Reg 202-200[9:1], **PLL_CLK_IN_DIV**
d. No = output divider
    - Accessible from Reg 202-200[13:10], **PLL_CLK_OUT_DIV**
e. Nfb = feedback divider
    - Accessible from Reg 199-197[23:0], **PLL_CLK_FB_DIV**

Programmable Microphone Regulator (MICBIAS)

ES9826 integrates a low noise programmable regulator intended to power or bias external microphones. MICBIAS is nominally 2.8V but can be programmed from 1.4-2.8V.

In hardware mode, MICBIAS is disabled.

In software mode, MICBIAS can be enabled by setting Register 78[3] - MB PDB to 1'b1. To program MICBIAS to other voltages, first set Register 78[6] - MB VR BYPASS and controlled by Register 78 [2:0] - MB VR SET.

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_ADC • AVCC • AVDD • DVDD	 • +3.6V with respect to Ground • +3.6V with respect to Ground • +3.6V with respect to Ground • +1.4V with respect to Ground
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD (nom) + 0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2kV 500V

Table 19 – Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

I/O Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
High-level input voltage	VIH	(AVDD / 2) + 0.4		V
Low-level input voltage	VIL		0.4	V
High-level output voltage	VOH	AVDD – 0.2		V
Low-level output voltage	VOL		0.2	V

Table 20 – I/O Electrical Characteristics

Recommended Operating Conditions

These are the recommended operating conditions for the ES9826.

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	–20°C to +85°C
AVCC		3.3V
AVCC_ADC		3.3V
AVDD		3.3V
VREF		Internal
VREF_BUF		Internal
DVDD		Internal
Input DC offset		AVCC/2
PLL_REG		Internal

Table 21 – Recommended Operating Conditions

Note: Supplied power is required to be within +/- 5% of the recommended condition.

Power Consumption

Test Conditions (unless otherwise noted)
T_A = 25ºC, AVCC = AVCC_ADC = AVDD = +3.3V, fs = 48kHz, **MCLK = 49.152MHz**, I2S output, with -1dBFS output signal
MCLK of 49.152Mhz will work for all sample rates

Parameter		Min	Typ	Max	Unit
48kHz, FS=MCLK/1024 HW#8	Slave Mode				
AVCC			4.3		mA
AVCC_ADC			10.1		mA
AVDD			10.0		mA
Power Consumption			**80.5**		**mW**
384kHz, FS=MCLK/128 HW#8	Slave Mode				
AVCC			4.3		mA
AVCC_ADC			10.1		mA
AVDD			20.1		mA
Power Consumption			**113.9**		**mW**

Table 22 – 49.152MHz MCLK power consumption

Performance

Test Conditions (unless otherwise noted)
T_A = 25°C, AVCC = AVCC_ADC = AVDD = +3.3V, Fs = 48kHz, MCLK = 49.152MHz, HW #8, 1kHz sine, -1dBFS output, 2.5kΩ input impedance

Measurements were done using ESS ES9826 1v0 Evaluation Board.

Parameter			Min	Typ	Max	Unit
0dBFS Input Voltage (differential)				2.06		Vrms
THD+N Ratio (w/o PLL) @ fs=48kHz, BW=20Hz-20kHz	2 ch mode	-1dBFS output		-105		dB
THD+N Ratio (w/ PLL) @ fs=48kHz, BW=20Hz-20kHz				-104		
DNR A-weighted (w/o PLL, w/ARE)	2 ch mode	-60dBFS output		123		dB
DNR A-weighted (w/o PLL, w/o ARE)				115		
DNR A-weighted (w/ PLL, w/ARE)				122		
DNR A-weighted (w/ PLL, w/o ARE)				114		

Table 23 – Performance test results

Timing Requirements

I²C Slave Interface Timing

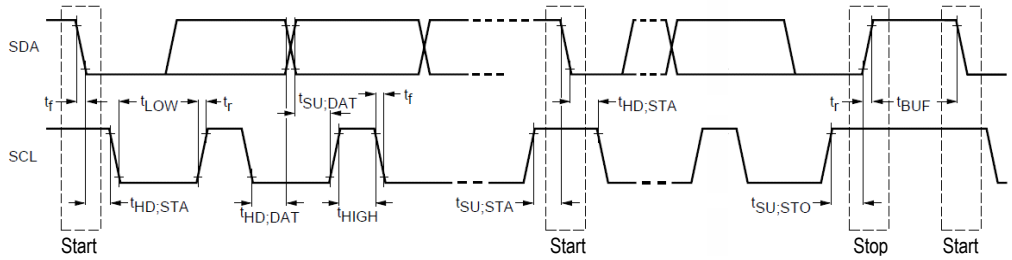


Figure 13 – I²C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 24 – I²C slave interface timing definitions

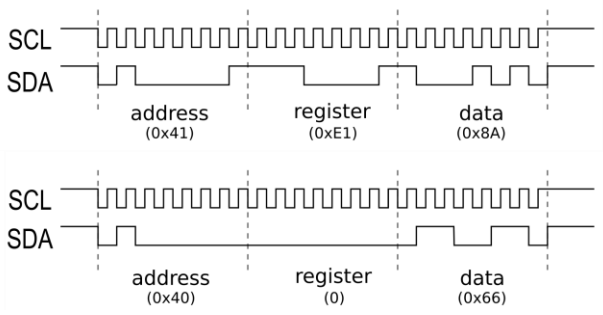


Figure 14 – I²C single byte examples of read and write instructions with I²C

SPI Slave Interface

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data

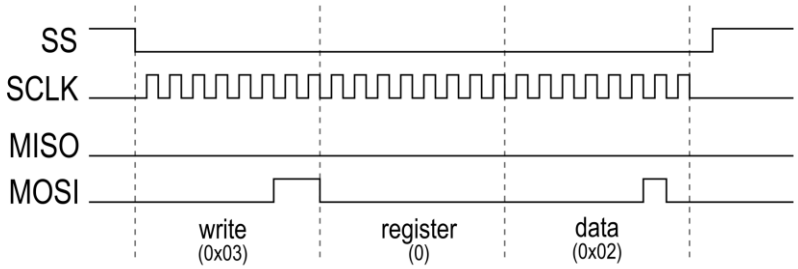


Figure 15 – SPI single byte write

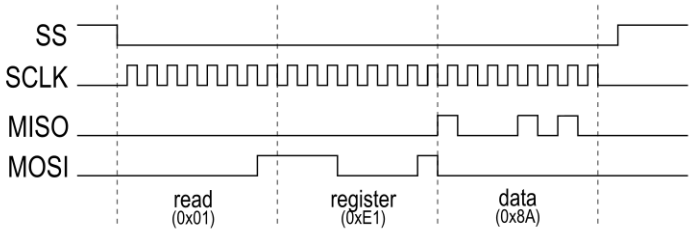


Figure 16 – SPI single byte read

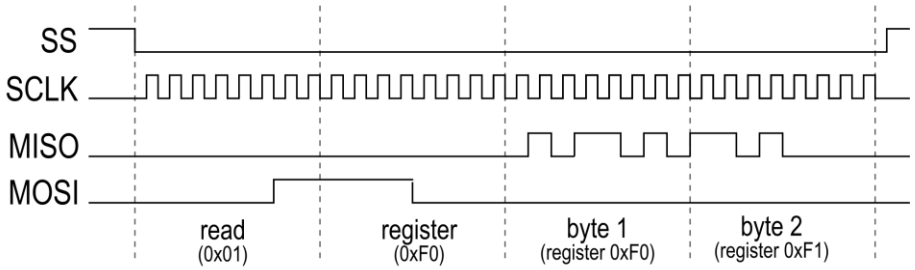


Figure 17 – SPI multi-byte read

Audio Interface Timing

Audio data on DATA1-2 are sampled at the rising edges of DATA_CLK and must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK.

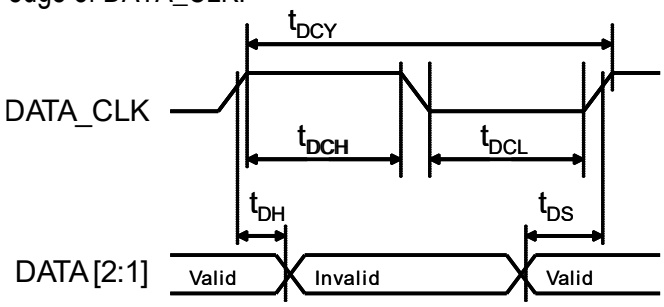


Figure 18 – Audio interface timing

Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	9.0		ns
DATA_CLK pulse width low	t_{DCL}	9.0		ns
DATA_CLK cycle time	t_{DCY}	20		ns
DATA_CLK duty cycle		45:55	55:45	
DATAx set-up time to DATA_CLK rising edge	t_{DS}	4.1		ns
DATAx hold time to DATA_CLK rising edge	t_{DH}	2.0		ns

Table 9 - Audio interface timing definitions

Register Overview

ES9826 features two different register interfaces. There is a standard I²C slave interface, and a synchronous I²C slave interface. The standard I²C slave interface requires a system clock present through ACLK or from the PLL to read and write registers. The synchronous I²C slave interface does not require a system clock, and allows for write-only configuration of the PLL registers to create a system clock from some reference clock (through DATA_CLK, or the ACLK pin).

Standard I²C Slave Interface (Device Address 0x40,0x42,0x44,0x46)

Read/Write Registers

Registers 0 – 80 (0x00 – 0x50) are read/write registers.

Read-only Registers

Register 192 – 206 (0xC0 – 0xCE) are PLL read registers.

Registers 224 – 241 (0xE0 – 0xF1) are read only registers.

Synchronous I²C Slave Interface (Device Address 0x48,0x4A,0x4C,0x4E)

This interface contains Write-only registers. These registers can be written even when there is no system clock present. When CHIP_EN is 0, all peripherals are automatically disabled, and all clocks are stopped.

Write-only Registers

Registers 192 – 206 (0xC0 – 0xCE) are write only registers.

Multi-Byte Registers

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read.

MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYS CONFIG	SOFT_RESET	AUTO_FS_BLOCK_64FS	AUTO_FS_DETECT	ENABLE_64FS_MODE	ENABLE_SPDIF_ENCODE	ENABLE_TDM_ENCODE	ENABLE_ADC	RESERVED
0x01	1	ADC CLOCK CONFIG1	RESERVED	SELECT_ADC_HALF	SELECT_ADC_NUM					
0x02	2	SYNC CONTROL	FORCE_PHASE_ADC_CLK	RESERVED	FORCE_PHASE_CLK_IADC	PHASE_CLK_IADC	AUTO_CLK_IADC_PHASE_SYNC	AUTO_WS_PHASE_SYNC	AUTO_ICG_SYNC	AUTO_FS_CLK_GEN_SYNC
0x03	3	I2S/TDM MASTER CLK CONFIG	MASTER_BCK_DIV							
0x04	4	I2S/TDM MASTER MODE CONFIG	ADC_CLK_DIV2	ADC_CLK_INV	MASTER_FRAME_LENGTH		MASTER_WS_PULSE_MODE	MASTER_BCK_INVERT	MASTER_WS_INVERT	MASTER_MODE_ENABLE
0x05	5	TDM CONFIG1	RESERVED					TDM_VALID_EDGE	TDM_LJ	TDM_LENGTH
0x06	6	TDM CONFIG2	AUTO_CH_DETECT	RESERVED		TDM_CH_NUM				
0x07	7	TDM CH1 SLOT CONFIG	RESERVED		SLAVE_BCK_INVERT	TDM_SLOT_SEL_CH1				
0x08	8	TDM CH2 SLOT CONFIG	RESERVED			TDM_SLOT_SEL_CH2				
0x09 - 0x0B	9 - 11	RESERVED	RESERVED							
0x0C	12	INTERRUPT MASK	INT_MASK_CH2_ARE_ENGAGED	INT_MASK_CH1_ARE_ENGAGED	RESERVED		INT_MASK_CH2_PEAK_DET	INT_MASK_CH1_PEAK_DET	INT_MASK_CH2_PEAK_LATCH	INT_MASK_CH1_PEAK_LATCH
0x0D	13	S/PDIF CONFIG	SPDIF_CS							
0x0E	14		SPDIF_CS							
0x0F	15		SPDIF_CS							
0x10	16		SPDIF_CS							
0x11	17		SPDIF_CS							
0x12	18	RESERVED	RESERVED							
0x13	19	INTERRUPT CLEAR	RESERVED						INT_CLEAR_CH2_PEAK_LATCH	INT_CLEAR_CH1_PEAK_LATCH
0x14	20	RESERVED	RESERVED							
0x15 - 0x18	21 - 24	RESERVED	RESERVED							
0x19	25	VREF CONFIG	RESERVED							ENFCB
0x1A	26	RESERVED	RESERVED							
0x1B	27	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x1C	28	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x1D	29	GPIO CONTROLS 1	RESERVED		GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	RESERVED	
0x1E	30	GPIO CONTROLS 2	GPIO4_WK_EN	GPIO3_WK_EN	RESERVED		GPIO6_SDB	GPIO5_SDB	GPIO4_SDB	GPIO3_SDB
0x1F	31	GPIO CONTROLS 3	INVERT_GPIO6	INVERT_GPIO5	INVERT_GPIO4	INVERT_GPIO3	RESERVED		GPIO6_WK_EN	GPIO5_WK_EN
0x20	32	GPIO READ	RESERVED		GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	RESERVED	
0x21	33	PWM COUNT	PWM_COUNT							
0x22	34	PWM FREQUENCY	PWM_FREQ							
0x23	35		PWM_FREQ							
0x24	36	ADC DATAPATH CONTROL	RESERVED	BYPASS_FIR2X	BYPASS_FIR4X	BYPASS_IIR3	BYPASS_IIR2	BYPASS_IIR1	CH1_AVG	MONO_MODE
0x25	37	DC BLOCKING & PDM INPUT	RESERVED		PDM_PHASE	PDM_INPUT_SEL	DC_BLOCKING_FILTER_CH2	DC_BLOCKING_FILTER_CH1	RESERVED	
0x26	38	PEAK DETECTOR CONFIG	LOCK_PEAK_VALUE	PEAK_DECAY_RATE					EN_PEAK_DETECT_CH2	EN_PEAK_DETECT_CH1
0x27	39	CH1 PEAK THRESHOLD	PEAK_THRESH_CH1							
0x28	40	CH2 PEAK THRESHOLD	PEAK_THRESH_CH2							
0x29 - 0x2C	41 - 44	RESERVED	RESERVED							
0x2D	45	CH1 VOLUME	VOLUME_CH1							
0x2E	46		VOLUME_CH1							
0x2F	47	CH2 VOLUME	VOLUME_CH2							
0x30	48		VOLUME_CH2							
0x31	49	VOLUME RATE	VOLUME_RATE							
0x32	50	THD COMP C2 CH1	THD_C2_CH1							
0x33	51		THD_C2_CH1							
0x34	52	THD COMP C3 CH1	THD_C3_CH1							
0x35	53		THD_C3_CH1							
0x36	54	THD COMP C2 CH2	THD_C2_CH2							
0x37	55		THD_C2_CH2							
0x38	56	THD COMP C3 CH2	THD_C3_CH2							
0x39	57		THD_C3_CH2							
0x3A	58	16-BIT OUTPUT	RESERVED						EN_16BIT_CH2	EN_16BIT_CH1
0x3B	59	FIR FILTER	RESERVED			FILTER_SHAPE			EN_32BIT_CH2	EN_32BIT_CH1
0x3C	60	RESERVED	RESERVED							

0x3D	61	ARE CONTROL	RESERVED						ARE_ENABLE
0x3E	62	PGA GAIN CONTROL EN	PGA_GAIN_CTRL_CH2_EN	PGA_GAIN_CTRL_CH1_EN	RESERVED				
0x3F - 0x42	63 - 66	RESERVED	RESERVED						
0x43	67	ADC ATTEN SET	ADC_ATTEN_SET_CH2				ADC_ATTEN_SET_CH1		
0x44	68	PGA GAIN CONTROL	PGA_GAIN_SET_CH2				PGA_GAIN_SET_CH1		
0x45 - 0x47	69 - 71	RESERVED	RESERVED						
0x48	72	PGA SETTINGS	RESERVED	PGA_RIN_CH2	PGA_RIN_CH1		RESERVED		
0x49	73	DIGITAL GAIN	RESERVED		DIGITAL_GAIN_CH2		RESERVED	DIGITAL_GAIN_CH1	
0x4A	74	MIX GAIN CH1	MIX_GAIN_CH1						
0x4B	75		MIX_GAIN_CH1						
0x4C	76	MIX GAIN CH2	MIX_GAIN_CH2						
0x4D	77		MIX_GAIN_CH2						
0x4E	78	MIC BIAS	RESERVED		MB_VR_BYPB	RESERVED	MB_PDB	MB_VR_SET	
0x4F	79	PDM CLK SELECT	RESERVED		SELECT_PDM_NUM				
0x50	80	RESERVED	RESERVED						
0xC0	192	PLL SOFT RESET	AO_SOFT_RESET	PLL_SOFT_RESET	RESERVED				PLL_CLK_PHASE_INV
0xC1	193	PLL CLOCK SELECT	RESERVED			SEL_PLL_CLK_IN	EN_PLL_CLK_IN	SEL_MCLK_IN	EN_MCLK_IN
0xC2	194	RESERVED	RESERVED						
0xC3	195	PLL VCO & CP CONFIG	RESERVED					VCO_PDB	CP_PDB
0xC4	196	RESERVED	RESERVED						
0xC5	197	PLL FEEDBACK DIV	PLL_CLK_FB_DIV						
0xC6	198		PLL_CLK_FB_DIV						
0xC7	199		PLL_CLK_FB_DIV						
0xC8	200	PLL IN & OUT DIV	PLL_CLK_IN_DIV						PLL_FB_DIV_LOAD
0xC9	201		RESERVED		PLL_CLK_OUT_DIV			PLL_CLK_IN_DIV	
0xCA	202		PLL_REG_PDB		RESERVED				
0xCB	203	PLL RESETB	RESERVED		PLL_DIG_RSTB	RESERVED			
0xCC	204	PLL CONFIG	RESERVED				CLKSMP_PDB	RESERVED	
0xCD - 0xCE	205 - 206	RESERVED	RESERVED						
0xE0	224	PEAK FLAG READ	PEAK_FLAG_CH2	PEAK_FLAG_CH1	RESERVED				
0xE1	225	CHIP ID	CHIP_ID						
0xE2 - 0xE5	226 - 229	RESERVED	RESERVED						
0xE6	230	AUTO FS READ	RATIO_VALID	ADC_HALF_DIV_AUTO	ADC_DIV_AUTO				
0xE7	231	AUTO CH NUM READ	CH2_DC_VALID	CH1_DC_VALID	TDM_VALID	AUTO_CH_NUM			
0xE8	232	GPIO INPUT READ	RESERVED		GPIO6_I_R	GPIO5_I_R	GPIO4_I_R	GPIO3_I_R	RESERVED
0xE9	233	DC CH1	CH1_DC_READ						
0xEA	234		CH1_DC_READ						
0xEB	235	DC CH2	CH2_DC_READ						
0xEC	236		CH2_DC_READ						
0xED	237	PEAK CH1 READ	CH1_PEAK						
0xEE	238		CH1_PEAK						
0xEF	239	PEAK CH2 READ	CH2_PEAK						
0xF0	240		CH2_PEAK						
0xF1	241	ARE READ	RESERVED					ARE_ENGAGED_CH2	ARE_ENGAGED_CH1

Register Listings

Some reserved registers values might be asserted in default mode. This is normal and does not need to be changed.

System Registers

Register 0: SYS CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b1	1'b0	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core and clocked registers (0-80).
[6]	AUTO_FS_BLOCK_64FS	Disable AUTO_FS_DETECT from entering 64FS mode. • 1'b0: 64FS mode allowed (default) • 1'b1: 64FS mode blocked
[5]	AUTO_FS_DETECT	Automatic sample rate (FS) detection. • 1'b0: Disabled, use the values of SELECT_ADC_NUM & SELECT_ADC_HALF to determine FS • 1'b1: Automatically tune the MCLK/CLK_ADC ratio according to detected FS (default)
[4]	ENABLE_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: Disabled (default) • 1'b1: Enabled
[3]	ENABLE_SPDIF_ENCODE	Enables S/PDIF encoding clock. • 1'b0: S/PDIF clock disabled (default) • 1'b1: S/PDIF clock enabled
[2]	ENABLE_TDM_ENCODE	Enables I2S/TDM encoding clock. • 1'b0: I2S/TDM clock disabled • 1'b1: I2S/TDM clock enabled (default)
[1]	ENABLE_ADC	Enables ADC decimation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[0]	RESERVED	NA

Register 1: ADC CLOCK CONFIG1

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd3

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	SELECT_ADC_HALF	Specifies whether to halve the SELECT_ADC_NUM divider. Can only produce half of an odd number divider, SELECT_ADC_NUM must be even. • 1'b0: Disabled (default) • 1'b1: Halve the value of SELECT_ADC_NUM + 1
[5:0]	SELECT_ADC_NUM	Whole number divide value + 1 for CLK_ADC (MCLK/divide_value). • 6'd3: Divide by 4 (default) • 6'dn: Divide by (N + 1)

Register 2: SYNC CONTROL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b1	1'b0	1'b0	1'b1	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	FORCE_PHASE_ADC_CLK	Forces the ADC_CLK phase to use the state of Reg4[6] ADC_CLK_INV. • 1'b0: Automatically determine the best phase. (default) • 1'b1: Use the state of ADC_CLK_INV
[6]	RESERVED	NA
[5]	FORCE_PHASE_CLK_IADC	Sets phase of CLK_IADC with the value of PHASE_CLK_IADC. • 1'b0: Auto phase tuning if AUTO_CLK_IADC_PHASE_SYNC is set • 1'b1: Sets phase by PHASE_CLK_IADC
[4]	PHASE_CLK_IADC	Sets phase of CLK_IADC relative to MCLK when FORCE_PHASE_CLK_IADC is set. Only used when MCLK is faster than CLK_IADC. • 1'b0: Phase 0 (default) • 1'b1: Phase 1
[3]	AUTO_CLK_IADC_PHASE_SYNC	Allows phase of CLK_IADC to be tuned automatically according to ADC input data. Only used when MCLK is faster than CLK_IADC. • 1'b0: CLK_IADC phase tuning disabled • 1'b1: Auto CLK_IADC phase tuning (default)
[2]	AUTO_WS_PHASE_SYNC	Uses WS input from GPIO2 as the sync reference. • 1'b0: WS is not the sync reference • 1'b1: WS is the sync reference
[1]	AUTO_ICG_SYNC	Allows programmable clock dividers to auto sync to the reference. • 1'b0: Auto sync disabled • 1'b1: Auto sync enabled (default)
[0]	AUTO_FS_CLK_GEN_SYNC	Allows FS signals to auto sync to the reference. • 1'b0: Auto sync disabled • 1'b1: Auto sync enabled (default)

Register 3: I2S/TDM MASTER CLK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_BCK_DIV	Master decoding clock divider. Whole number divide value + 1 for CLK_BCK_WS_GEN (MCLK/divide_value).

Register 4: I2S/TDM MASTER MODE CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	2'b00	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC_CLK_DIV2	Sets ADC clock rate. • 1'b0: Full rate (default) • 1'b1: 1/2 rate
[6]	ADC_CLK_INV	Inverts the phase of ADC_CLK. • 1'b0: Non-inverted (default) • 1'b1: Inverted Note: Requires Reg2[7] FORCE_PHASE_ADC_CLK = 1'b1.
[5:4]	MASTER_FRAME_LENGTH	Selects the bit length of the I2S/TDM channels in master mode. • 2'b00: 32-bit (default) • 2'b10: 16-bit • Others: Reserved
[3]	MASTER_WS_PULSE_MODE	When enabled, master WS is a 1 BCK pulse signal instead of a 50% duty cycle signal. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[2]	MASTER_BCK_INVERT	Inverts master BCK. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	MASTER_MODE_ENABLE	Enables I2S/TDM master mode and generates master BCK and master WS. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 5: TDM CONFIG1

Bits	[7:3]	[2]	[1]	[0]
Default	5'b00011	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2]	TDM_VALID_EDGE	Sets which WS edge the frame starts on. • 1'b0: Frame starts on negedge of WS (default) • 1'b1: Frame starts on posedge of WS
[1]	TDM_LJ	Sets left-justified mode. • 1'b0: One BCK period delay (default) • 1'b1: Left-justified
[0]	TDM_LENGTH	Sets the width, in bits, of one data word / subframe. A subframe is a frame divided by the number of channels. • 1'b0: 32-bit (default) • 1'b1: 16-bit

Register 6: TDM CONFIG2

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'b00	5'd1

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Automatically determine the number of TDM channels, from the BCK/WS ratio. • 1'b0: Disabled, use the value of TDM_CH_NUM (default) • 1'b1: Enabled Note: Cannot be set in Master Mode.
[6:5]	RESERVED	NA
[4:0]	TDM_CH_NUM	Sets number of channels in each frame. • 5'd0: 1 channel • 5'd1: 2 channels (default) • 5'd31: 32 channels

Register 7: TDM CH1 SLOT CONFIG

Bits	[7:6]	[5]	[4:0]
Default	2'b00	1'b0	5'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	SLAVE_BCK_INVERT	• 1'b0: Non-inverted (default) • 1'b1: Invert BCK input
[4:0]	TDM_SLOT_SEL_CH1	Selects which TDM channel slot is filled by ADC Ch1 data. • 5'd0: Slot 1 (default) • 5'd1: Slot 2 • 5'd31: Slot 32

Register 8: TDM CH2 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'b000	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:0]	TDM_SLOT_SEL_CH2	Selects which TDM channel slot is filled by ADC Ch2 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 11-9: RESERVED

Register 12: INTERRUPT MASK

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	2'b00	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	INT_MASK_CH2_ARE_ENGAGED	Masks the ARE_ENGAGED_CH2 interrupt. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt enabled
[6]	INT_MASK_CH1_ARE_ENGAGED	Masks the ARE_ENGAGED_CH1 interrupt. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt enabled
[5:4]	RESERVED	NA
[3]	INT_MASK_CH2_PEAK_DET	Masks the PEAK_FLAG interrupt on ADC CH2. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt enabled
[2]	INT_MASK_CH1_PEAK_DET	Masks the PEAK_FLAG interrupt on ADC CH1. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt enabled
[1]	INT_MASK_CH2_PEAK_LATCH	Masks the latched PEAK_FLAG interrupt on ADC CH2. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt enabled
[0]	INT_MASK_CH1_PEAK_LATCH	Masks the latched PEAK_FLAG interrupt on ADC CH1. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt enabled

Register 17-13: S/PDIF CONFIG

Bits	[39:0]
Default	40'd0

Bits	Mnemonic	Description
[39:0]	SPDIF_CS	Configures S/PDIF sub-code bits.

Register 18: RESERVED

Register 19: INTERRUPT CLEAR

Bits	[7:2]	[1]	[0]
Default	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	INT_CLEAR_CH2_PEAK_LATCH	Clears the latched PEAK_FLAG interrupt on ADC CH2. • 1'b0: Interrupt held if asserted (default) • 1'b1: Interrupt cleared
[0]	INT_CLEAR_CH1_PEAK_LATCH	Clears the latched PEAK_FLAG interrupt on ADC CH1. • 1'b0: Interrupt held if asserted (default) • 1'b1: Interrupt cleared

Register 24-20: RESERVED

Register 25: VREF CONFIG

Bits	[7:1]	[0]
Default	7'b0000000	1'b0

Bits	Mnemonic	Description
[7:1]	RESERVED	NA
[0]	ENFCB	Enable the fast charge of the ADC reference voltage. • 1'b0: Fast charge enabled (default) • 1'b1: Fast charge disabled

GPIO Registers

Register 26: RESERVED

Register 27: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd2

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configure GPIO4 function selection. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Aux inputs – input • 4'd2: Aux outputs – output • 4'd3: Reserved • 4'd4: Reserved • 4'd5: CH1 PEAK_FLAG interrupt – output • 4'd6: CH2 PEAK_FLAG interrupt – output • 4'd7: OR of all interrupts – output • 4'd8: S/PDIF data stream – output • 4'd9: PWM Signal – output • 4'd10: CH1 ARE interrupt – output • 4'd11: CH2 ARE interrupt – output • 4'd12: CLK_IADC – output • 4'd13: CLK_ADC – output • 4'd14: Output 0 – output • 4'd15: Output 1 – output
[3:0]	GPIO3_CFG	Configure GPIO3 function selection. • 4'd0: Analog outputs off – shutdown • 4'd1: Aux inputs – input • 4'd2: Aux outputs – output (default) • 4'd3: Reserved • 4'd4: Reserved • 4'd5: CH1 PEAK_FLAG interrupt – output • 4'd6: CH2 PEAK_FLAG interrupt – output • 4'd7: OR of all interrupts – output • 4'd8: S/PDIF data stream – output • 4'd9: PWM Signal – output • 4'd10: CH1 ARE interrupt – output • 4'd11: CH2 ARE interrupt – output • 4'd12: CLK_IADC – output • 4'd13: CLK_ADC – output • 4'd14: Output 0 – output • 4'd15: Output 1 – output

Register 28: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configure GPIO6 function selection. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Aux inputs – input • 4'd2: Aux outputs – output • 4'd3: Reserved • 4'd4: Reserved • 4'd5: CH1 PEAK_FLAG interrupt – output • 4'd6: CH2 PEAK_FLAG interrupt – output • 4'd7: OR of all interrupts – output • 4'd8: S/PDIF data stream – output • 4'd9: PWM Signal – output • 4'd10: CH1 ARE interrupt – output • 4'd11: CH2 ARE interrupt – output • 4'd12: CLK_IADC – output • 4'd13: CLK_ADC – output • 4'd14: Output 0 – output • 4'd15: Output 1 – output
[3:0]	GPIO5_CFG	Configure GPIO5 function selection. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Aux inputs – input • 4'd2: Aux outputs – output • 4'd3: Reserved • 4'd4: Reserved • 4'd5: CH1 PEAK_FLAG interrupt – output • 4'd6: CH2 PEAK_FLAG interrupt – output • 4'd7: OR of all interrupts – output • 4'd8: S/PDIF data stream – output • 4'd9: PWM Signal – output • 4'd10: CH1 ARE interrupt – output • 4'd11: CH2 ARE interrupt – output • 4'd12: CLK_IADC – output • 4'd13: CLK_ADC – output • 4'd14: Output 0 – output • 4'd15: Output 1 – output

Register 29: GPIO CONTROLS 1

Bits	[7:6]	[5]	[4]	[3]	[2]	[1:0]
Default	2'd3	1'b0	1'b0	1'b0	1'b1	2'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	GPIO6_OE	• 1'b0: Tristate GPIO6 output (default) • 1'b1: GPIO6 output enabled
[4]	GPIO5_OE	• 1'b0: Tristate GPIO5 output (default) • 1'b1: GPIO5 output enabled
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 output (default) • 1'b1: GPIO4 output enabled
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 output • 1'b1: GPIO3 output enabled (default)
[1:0]	RESERVED	NA

Register 30: GPIO CONTROLS 2

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	2'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[6]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[5:4]	RESERVED	NA
[3]	GPIO6_SDB	• 1'b0: GPIO6 input disabled (default) • 1'b1: GPIO6 input enabled
[2]	GPIO5_SDB	• 1'b0: GPIO5 input disabled (default) • 1'b1: GPIO5 input enabled
[1]	GPIO4_SDB	• 1'b0: GPIO4 input disabled (default) • 1'b1: GPIO4 input enabled
[0]	GPIO3_SDB	• 1'b0: GPIO3 input disabled (default) • 1'b1: GPIO3 input enabled

Register 31: GPIO CONTROLS 3

Bits	[7]	[6]	[5]	[4]	[3:2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	INVERT_GPIO6	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO6 output
[6]	INVERT_GPIO5	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO5 output
[5]	INVERT_GPIO4	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO4 output
[4]	INVERT_GPIO3	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO3 output
[3:2]	RESERVED	NA
[1]	GPIO6_WK_EN	• 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled
[0]	GPIO5_WK_EN	• 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled

Register 32: GPIO READ

Bits	[7:6]	[5]	[4]	[3]	[2]	[1:0]
Default	2'd0	1'b0	1'b0	1'b0	1'b0	2'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	GPIO6_READ	• 1'b0: GPIO6 readback disabled (default) • 1'b1: Allows readback of GPIO6 input
[4]	GPIO5_READ	• 1'b0: GPIO5 readback disabled (default) • 1'b1: Allows readback of GPIO5 input
[3]	GPIO4_READ	• 1'b0: GPIO4 readback disabled (default) • 1'b1: Allows readback of GPIO4 input
[2]	GPIO3_READ	• 1'b0: GPIO3 readback disabled (default) • 1'b1: Allows readback of GPIO3 input
[1:0]	RESERVED	NA

Register 33: PWM COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM_COUNT	Sets the number of MCLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 35-34: PWM FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM_FREQ	Sets the frequency of the PWM signal in terms of MCLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $$frequency\ [Hz] = \frac{MCLK}{PWM\_FREQ + 1}$$ $$Duty\ Cycle\ [\%] = \left(\frac{PWM\_COUNT}{PWM\_FREQ + 1}\right) \times 100$$

ADC Registers

Register 36: ADC DATAPATH CONTROL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	BYPASS_FIR2X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_2x
[5]	BYPASS_FIR4X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_4x
[4]	BYPASS_IIR3	• 1'b0: Non-bypass (default) • 1'b1: Bypass IIR3
[3]	BYPASS_IIR2	• 1'b0: Non-bypass (default) • 1'b1: Bypass IIR2
[2]	BYPASS_IIR1	• 1'b0: Non-bypass (default) • 1'b1: Bypass IIR1
[1]	CH1_AVG	Sets the CH1 datapath input to an average of both analog inputs, (CH1 + CH2)/2. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	MONO_MODE	Mute CH2 decimation path. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 37: DC BLOCKING & PDM INPUT

Bits	[7:6]	[5]	[4]	[3]	[2]	[1:0]
Default	2'b00	1'b0	1'b0	1'b1	1'b1	2'b11

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	PDM_PHASE	Selects which channel is on which edge of the PDM clock. • 1'b0: CH1 on the rising edge, CH2 on the falling edge (default) • 1'b1: CH2 on the rising edge, CH1 on the falling edge
[4]	PDM_INPUT_SEL	Select between Analog and PDM input stream. • 1'b0: Analog ADC input stream (default) • 1'b1: Enable PDM input stream
[3]	DC_BLOCKING_FILTER_CH2	Enable the CH2 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[2]	DC_BLOCKING_FILTER_CH1	Enable the CH1 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[1:0]	RESERVED	NA

Register 38: PEAK DETECTOR CONFIG

Bits	[7]	[6:2]	[1]	[0]
Default	1'b0	5'd10	1'b0	1'b0

Bits	Mnemonic	Description
[7]	LOCK_PEAK_VALUE	Locks the current peak detector values, for reading back. Values can be read from Reg237-240. • 1'b0: Peak detector value can update (default) • 1'b1: Peak detector value locked
[6:2]	PEAK_DECAY_RATE	Sets the speed at which the peak detector value will decay when greater than the input signal. • 5'd0: Instant decay • 5'd1: Fastest decay • 5'd10: Default value • 5'd22: Slowest decay • Others: Reserved
[1]	EN_PEAK_DETECT_CH2	Enables the ADC CH2 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	EN_PEAK_DETECT_CH1	Enables the ADC CH1 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 39: CH1 PEAK THRESHOLD

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	PEAK_THRESH_CH1	Threshold value to trigger the PEAK_FLAG in the CH1 peak detector. Triggers if the input signal > PEAK_THRESH_CH1. Shift left 1 bit corresponds to -6dB. • 8'h01: -48dB • 8'hFF: 0dB (default)

Register 40: CH2 PEAK THRESHOLD

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	PEAK_THRESH_CH2	Threshold value to trigger the PEAK_FLAG in the CH2 peak detector. Triggers if the input signal > PEAK_THRESH_CH2. Shift left 1 bit corresponds to -6dB. • 8'h01: -48dB • 8'hFF: 0dB (default)

Register 44-42: RESERVED

Register 46-45: CH1 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	VOLUME_CH1	Next desired ADC CH1 signed volume coefficient. Shift right 1 bit corresponds to -6dB. • 16'h7FFF: 0dB (default) • 16'h0001: -90dB • 16'h0000: CH1 muted Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume.

Register 48-47: CH2 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	VOLUME_CH2	Next desired ADC CH2 signed volume coefficient. Shift right 1 bit corresponds to -6dB. • 16'h7FFF: 0dB (default) • 16'h0001: -90dB • 16'h0000: CH2 muted Note: 16'h8000 to 16'hFFFF is the phase inverted version of the volume.

Register 49: VOLUME RATE

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_RATE	Value by which the old coefficient value is incremented/decremented to reach the new coefficient. • 8'h00: Instant ramp rate (default) • 8'h01: Slowest ramp rate • 8'hFF: Fastest ramp rate

Register 51-50: THD COMP C2 CH1

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_C2_CH1	A 16-bit signed coefficient for correcting for the CH1 second harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 53-52: THD COMP C3 CH1

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_C3_CH1	A 16-bit signed coefficient for correcting for the CH1 third harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 55-54: THD COMP C2 CH2

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_C2_CH2	A 16-bit signed coefficient for correcting for the CH2 second harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 57-56: THD COMP C3 CH2

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_C3_CH2	A 16-bit signed coefficient for correcting for the CH2 third harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 58: 16-BIT OUTPUT

Bits	[7:2]	[1]	[0]
Default	6'b100100	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	EN_16BIT_CH2	Sets the bit depth from the CH2 decimation path. • 1'b0: 24-bit output (default) • 1'b1: 16-bit output Note: Has priority over EN_32BIT_CH2
[0]	EN_16BIT_CH1	Sets the bit depth from the CH1 decimation path. • 1'b0: 24-bit output (default) • 1'b1: 16-bit output Note: Has priority over EN_32BIT_CH1

Register 59: FIR FILTER

Bits	[7:5]	[4:2]	[1]	[0]
Default	3'd4	3'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:2]	FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing fast roll-off • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[1]	EN_32BIT_CH2	Sets the bit depth from the CH2 decimation path. • 1'b0: 24-bit output (default) • 1'b1: 32-bit output
[0]	EN_32BIT_CH1	Sets the bit depth from the CH1 decimation path. • 1'b0: 24-bit output (default) • 1'b1: 32-bit output

Register 60: RESERVED

Register 61: ARE CONTROL

Bits	[7:1]	[0]
Default	7'b1101000	1'b0

Bits	Mnemonic	Description
[7:1]	RESERVED	NA
[0]	ARE_ENABLE	Enable Automatic Range Enhancement (ARE). • 1'b0: ARE disabled (default) • 1'b1: ARE enabled **Note: Please consult application note before using ARE_ENABLE.**

Register 62: PGA GAIN CONTROL EN

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd11

Bits	Mnemonic	Description
[7]	PGA_GAIN_CTRL_CH2_EN	Disentangles the PGA gain and ADC attenuation for CH2. • 1'b0: Datapath gain normalization is enabled (default) • 1'b1: Datapath gain normalization is disabled. ADC attenuation is controlled by ADC_ATTEN_SET_CH2. PGA gain is controlled by PGA_GAIN_SET_CH2.
[6]	PGA_GAIN_CTRL_CH1_EN	Disentangles the PGA gain and ADC attenuation for CH1. • 1'b0: Datapath gain normalization is enabled (default) • 1'b1: Datapath gain normalization is disabled. ADC attenuation is controlled by ADC_ATTEN_SET_CH1. PGA gain is controlled by PGA_GAIN_SET_CH1.
[5:0]	RESERVED	NA

Register 66-63: RESERVED

Register 67: ADC ATTEN SET

Bits	[7:4]	[3:0]
Default	4'd10	4'd10

Bits	Mnemonic	Description
[7:4]	ADC_ATTEN_SET_CH2	• If ARE is disabled, ADC_ATTEN_SET_CH2 sets the amount of ADC attenuation (requires PGA_GAIN_CTRL_EN_CH2 = 1). • If ARE is enabled, ADC_ATTEN_SET_CH2 sets the amount of PGA gain when ARE is engaged. Valid from 4'd0 (0dB) to 4'd10 (30dB), 3dB steps. Default is 30dB.
[3:0]	ADC_ATTEN_SET_CH1	• If ARE is disabled, ADC_ATTEN_SET_CH1 sets the amount of ADC attenuation (requires PGA_GAIN_CTRL_EN_CH1 = 1). • If ARE is enabled, ADC_ATTEN_SET_CH1 sets the amount of PGA gain when ARE is engaged. Valid from 4'd0 (0dB) to 4'd10 (30dB), 3dB steps. Default is 30dB.

Register 68: PGA GAIN CONTROL

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	PGA_GAIN_SET_CH2	• If ARE is disabled, PGA_GAIN_SET_CH2 sets the amount of PGA gain (requires PGA_GAIN_CTRL_EN_CH2 = 1). • If ARE is enabled, PGA_GAIN_SET_CH2 controls the PGA gain when ARE is disengaged. Valid from 4'd0 (0dB) to 4'd10 (30dB), 3dB steps. Default is 0dB.
[3:0]	PGA_GAIN_SET_CH1	• If ARE is disabled, PGA_GAIN_SET_CH1 sets the amount of PGA gain (requires PGA_GAIN_CTRL_EN_CH1 = 1). • If ARE is enabled, PGA_GAIN_SET_CH1 controls the PGA gain when ARE is disengaged. Valid from 4'd0 (0dB) to 4'd10 (30dB), 3dB steps. Default is 0dB.

Register 71-69: RESERVED

Register 72: PGA SETTINGS

Bits	[7:6]	[5]	[4]	[3:0]
Default	2'd0	1'b0	1'b0	4'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	PGA_RIN_CH2	CH2 PGA input impedance. • 1'b0: 2.5kΩ (default) • 1'b1: 10kΩ
[4]	PGA_RIN_CH1	CH1 PGA input impedance. • 1'b0: 2.5kΩ (default) • 1'b1: 10kΩ
[3:0]	RESERVED	NA

Register 73: DIGITAL GAIN

Bits	[7]	[6:4]	[3]	[2:0]
Default	1'b0	3'd0	1'b0	3'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:4]	DIGITAL_GAIN_CH2	Digital gain in the ADC CH2 datapath. • 3'd0: +0dB (default) • 3'd1: +6dB • 3'd2: +12dB • 3'd3: +18dB • 3'd4: +24dB • 3'd5: +30dB • Others: Reserved
[3]	RESERVED	NA
[2:0]	DIGITAL_GAIN_CH1	Digital gain in the ADC CH2 datapath. • 3'd0: +0dB (default) • 3'd1: +6dB • 3'd2: +12dB • 3'd3: +18dB • 3'd4: +24dB • 3'd5: +30dB • Others: Reserved

Register 75-74: MIX GAIN CH1

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	MIX_GAIN_CH1	A 16-bit signed number, for the percentage of CH1 mixed into CH2. • 16'h8000: -100% • 16'h0000: Disabled (default) • 16'h7FFF: +100%

Register 77-76: MIX GAIN CH2

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	MIX_GAIN_CH2	A 16-bit signed number, for the percentage of CH2 mixed into CH1. • 16'h8000: -100% • 16'h0000: Disabled (default) • 16'h7FFF: +100%

Register 78: MIC BIAS

Bits	[7]	[6]	[5:4]	[3]	[2:0]
Default	1'b0	1'b0	2'b00	1'b0	3'b010

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	MB_VR_BYPB	Bypass the MICBIAS reference voltage select. • 1'b0: 2.85V, voltage of VREF_BUF (default) • 1'b1: Determined by MB_VR_SET
[5:4]	RESERVED	NA
[3]	MB_PDB	Enables the MICBIAS. • 1'b0: Disabled (default) • 1'b1: Enabled
[2:0]	MB_VR_SET	Set mic bias voltage. • 3'b000: 1.45V • 3'b001: 2.55V • 3'b010: 2.65V (default) • 3'b011: 2.75V • 3'b100: 1.65V • 3'b101: 1.75V • 3'b110: 1.85V • 3'b111: 1.95V

Register 79: PDM CLK SELECT

Bits	[7]	[6:0]
Default	1'b0	7'd3

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:0]	SELECT_PDM_NUM	Whole number divide value + 1 for CLK_PDM (MCLK/divide_value). • 7'd3: Divide by 4 (default) • 7'dn: Divide by (N + 1)

Register 80: RESERVED

PLL Registers

Register 192: PLL SOFT RESET

Bits	[7]	[6]	[5:1]	[0]
Default	1'b0	1'b0	5'd0	1'b0

Bits	Mnemonic	Description
[7]	AO_SOFT_RESET	Performs soft reset to digital core and clocked registers (0-80).
[6]	PLL_SOFT_RESET	Performs soft reset to only the PLL registers (192-206).
[5:1]	RESERVED	NA
[0]	PLL_CLK_PHASE_INV	Inverts the PLL clock output. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 193: PLL CLOCK SELECT

Bits	[7:6]	[5:4]	[3]	[2:1]	[0]
Default	2'b01	2'b10	1'b0	2'b00	1'b1

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	SEL_PLL_CLK_IN	Selects PLL input clock source when EN_PLL_CLK_IN is set. • 2'b00: ACLK • 2'b10: BCK (default) • Others: Reserved
[3]	EN_PLL_CLK_IN	Allows SEL_PLL_CLK_IN to select PLL input clock source. • 1'b0: Disabled (default) • 1'b1: Enabled
[2:1]	SEL_MCLK_IN	Selects digital core and ADC clock source when EN_MCLK_IN is set. • 2'b00: ACLK • 2'b10: PLL_CLK • Others: Reserved
[0]	EN_MCLK_IN	Enables clock inputs to the digital core. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 194: RESERVED

Register 195: PLL VCO & CP CONFIG

Bits	[7:2]	[1]	[0]
Default	6'b011111	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	VCO_PDB	Enables/disables the PLL voltage-controlled oscillator (VCO). • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	CP_PDB	Enables/disables the PLL charge pump. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 196: RESERVED

Register 199-197: PLL FEEDBACK DIV

Bits	[23:0]
Default	24'h100000

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider (Nfb). • 24'h000000: Reserved • 24'h100000: Default • 24'hn: Divide by 2^25/n

Register 202-200: PLL IN & OUT DIV

Bits	[23:22]	[21:14]	[13:10]	[9:1]	[0]
Default	2'b00	8'd1	4'd3	9'd0	1'b1

Bits	Mnemonic	Description
[23:22]	PLL_REG_PDB	Power down the PLL regulators. • 2'b00: Disables the PLL regulators (default) • 2'b11: Enables the PLL regulators (Normal Operation) Note: Other options are invalid.
[21:14]	RESERVED	NA
[13:10]	PLL_CLK_OUT_DIV	Sets the PLL clock output divider (No). • 4'dn: Divide by (n + 1).
[9:1]	PLL_CLK_IN_DIV	Sets the PLL clock input divider (Ni). • 9'dn: Divide by (n + 1).
[0]	PLL_FB_DIV_LOAD	Write 1'b1 then write 1'b0 to load PLL_CLK_FB_DIV.

Register 203: PLL RESETB

Bits	[7:6]	[5]	[4:0]
Default	2'b00	1'b0	5'b01010

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	PLL_DIG_RSTB	Resets the Digital core of the PLL. • 1'b0: PLL core reset (default) • 1'b1: PLL core active
[4:0]	RESERVED	NA

Register 204: PLL CONFIG

Bits	[7:3]	[2]	[1:0]
Default	5'b00001	1'b0	2'b00

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2]	CLKSMP_PDB	Power Down the PLL circuitry. • 1'b0: PLL Block disabled (default) • 1'b1: PLL Block enabled
[1:0]	RESERVED	NA

Register 206-205: RESERVED

Readback Registers

Register 224: PEAK FLAG READ

Bits	[7]	[6]	[5:0]
Default	-	-	-

Bits	Mnemonic	Description
[7]	PEAK_FLAG_CH2	ADC CH2 latched peak detector flag. • 1'b0: CH2 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH2 input signal > PEAK_THRESH_CH2 Note: Requires reg19[1] INT_CLEAR_CH2_PEAK_LATCH to clear flag.
[6]	PEAK_FLAG_CH1	ADC CH1 latched peak detector flag. • 1'b0: CH1 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH1 input signal > PEAK_THRESH_CH2 Note: Requires reg19[0] INT_CLEAR_CH1_PEAK_LATCH to clear flag.
[5:0]	RESERVED	NA

Register 225: CHIP ID

Bits	[7:0]
Default	8'h8A

Bits	Mnemonic	Description
[7:0]	CHIP_ID	Chip ID

Register 229-227: RESERVED

Register 230: AUTO FS READ

Bits	[7]	[6]	[5:0]
Default	-	-	-

Bits	Mnemonic	Description
[7]	RATIO_VALID	Validity of the MCLK/CLK_ADC ratio. $\left(\frac{\mathrm{N}+1}{\mathrm{M}}\right) * 128$ MCLK periods in a WS frame. • 1'b0: Invalid ratio • 1'b1: Valid ratio
[6]	ADC_HALF_DIV_AUTO	Result (M) of the automatic sample rate detect (reg0[5] AUTO_FS_DETECT) logic. • 1'b0: CLK_ADC is an integer multiple of MCLK, M = 1. • 1'b1: CLK_ADC is a N*0.5 multiple of MCLK, M = 2.
[5:0]	ADC_DIV_AUTO	Result (N) of the automatic sample rate detect (reg0[5] AUTO_FS_DETECT) logic. $FS\ [Hz] = \frac{M * MCLK}{(N+1) * 128}$

Register 231: AUTO CH NUM READ

Bits	[7]	[6]	[5]	[4:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	CH2_DC_VALID	Validity of the CH2 DC value. • 1'b0: Invalid • 1'b1: Valid
[6]	CH1_DC_VALID	Validity of the CH1 DC value. • 1'b0: Invalid • 1'b1: Valid
[5]	TDM_VALID	TDM valid flag • 1'b0: Invalid • 1'b1: Valid
[4:0]	AUTO_CH_NUM	Result of the automatic TDM channel logic. Note: Requires reg6[7] AUTO_CH_DETECT to enable functionality.

Register 232: GPIO INPUT READ

Bits	[7:6]	[5]	[4]	[3]	[2]	[1:0]
Default	-	-	-	-	-	-

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	GPIO6_I_R	GPIO6 input readback.
[4]	GPIO5_I_R	GPIO5 input readback.
[3]	GPIO4_I_R	GPIO4 input readback.
[2]	GPIO3_I_R	GPIO3 input readback.
[1:0]	RESERVED	NA

Register 234-233: DC CH1

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	CH1_DC_READ	Channel 1 DC value readback. $DC\_Offset\,[D] = \frac{CH1\_DC\_READ\ <<\ 11}{2^{31} - 1}$

Register 236-235: DC CH2

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	CH2_DC_READ	Channel 2 DC value readback. $DC\_Offset\,[D] = \frac{CH2\_DC\_READ\ <<\ 11}{2^{31} - 1}$

Register 238-237: PEAK CH1 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	CH1_PEAK	Channel 1 peak detector value readback. Note: Requires reg38[0] EN_PEAK_DETECT_CH1 to enable functionality.

Register 240-239: PEAK CH2 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	CH2_PEAK	Channel 2 peak detector value readback. Note: Requires reg38[1] EN_PEAK_DETECT_CH2 to enable functionality.

Register 241: ARE READ

Bits	[7:2]	[1]	[0]
Default	-	-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	ARE_ENGAGED_CH2	CH2 ARE is engaged. • 1'b0: ARE not engaged on channel 2 • 1'b1: ARE engaged on channel 2
[0]	ARE_ENGAGED_CH1	CH1 ARE is engaged. • 1'b0: ARE not engaged on channel 1 • 1'b1: ARE engaged on channel 1

ES9826 Reference Schematics

These schematics are for evaluation reference only.

Hardware (HW) mode

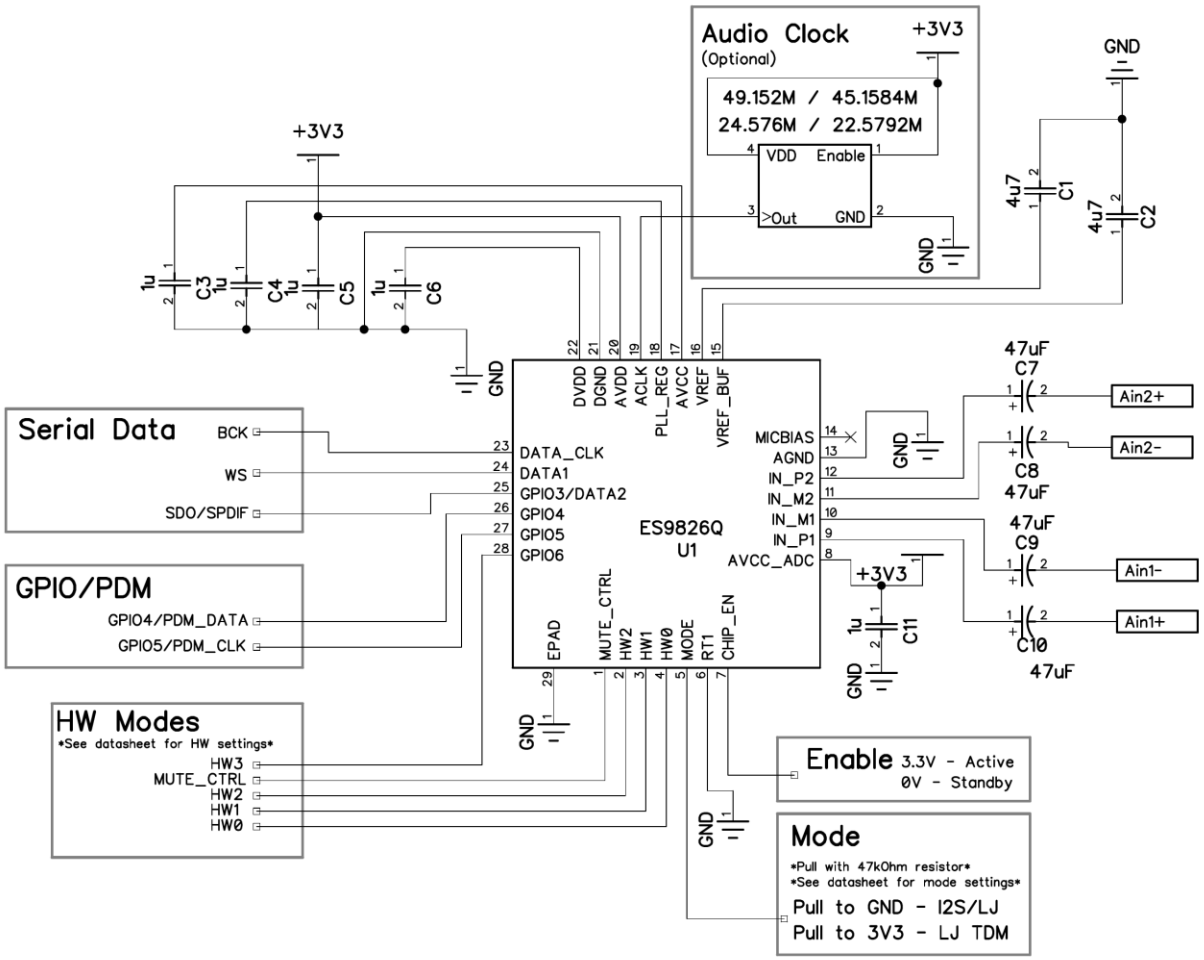


Figure 19 – Hardware (HW) mode reference schematic for ES9826Q

Note: ES9826Q has an exposed pad (EPAD, pin 29) and should be connected to ground.

Software (SW) mode

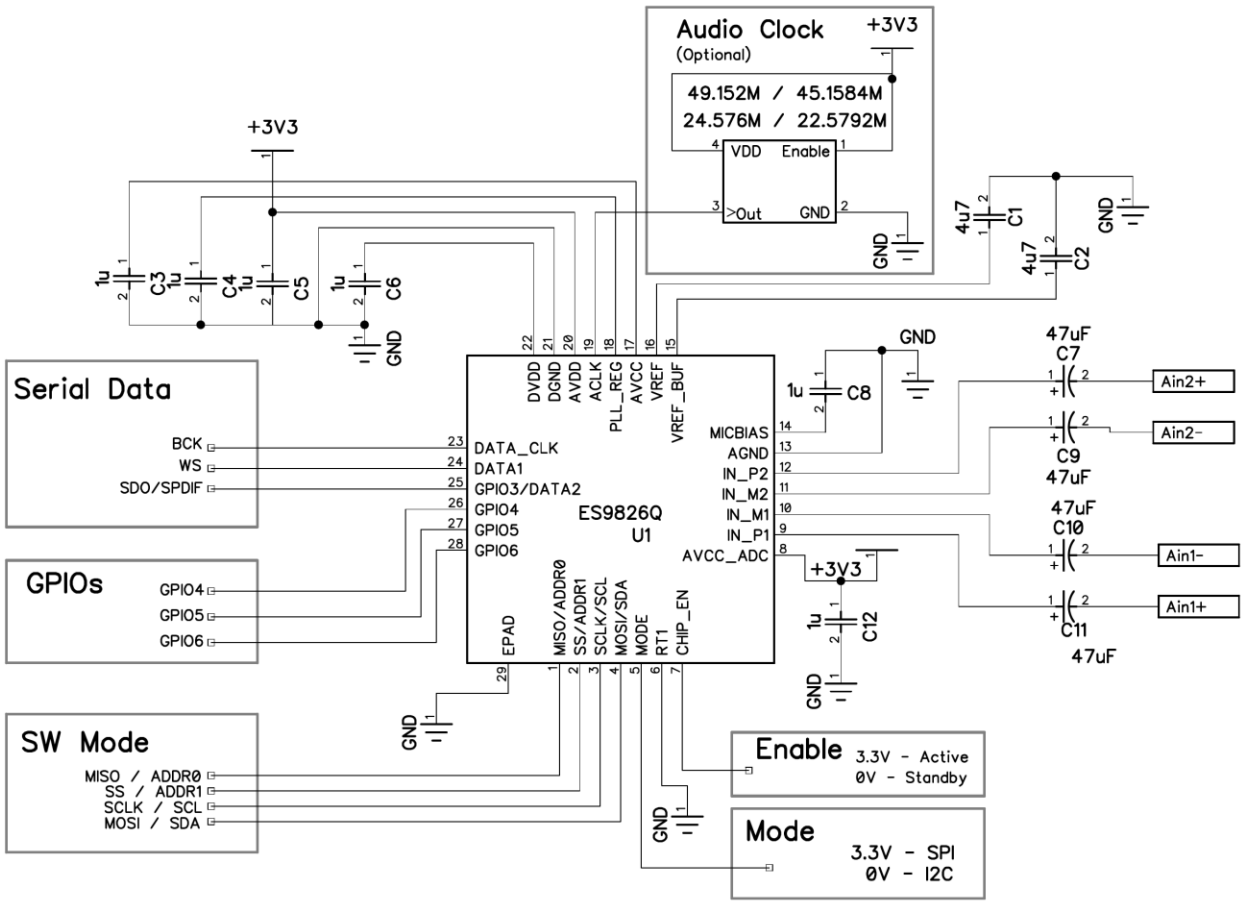
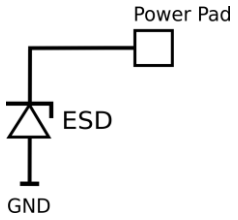
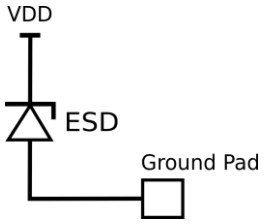
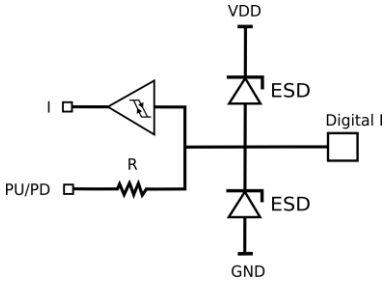
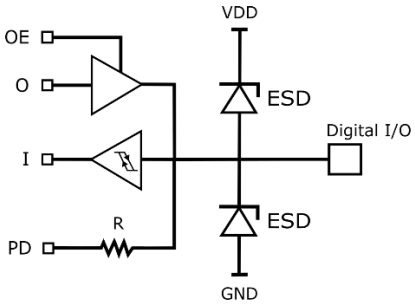


Figure 20 – Software mode reference schematic for ES9826Q

Note: ES9826Q has an exposed pad (EPAD, pin 29) and should be connected to ground.

Internal Pad Circuitry

Pin	Type	Pin Name	Equivalent Circuit
AVCC_ADC AVDD AVCC	Power	8 20 17	
AGND DGND	Ground	13 21	
CHIP_EN	Reset	7	
MISO/ADDR0/MUTE_MCLK_CTRL SCLK/SCL/HW1 MOSI/SDA/HW0 MODE GPIO6/HW3 GPIO5 GPIO4 DATA2/GPIO3 DATA1 DATA_CLK SS/ADDR1/HW2 ACLK	Digital I/O	1 3 4 5 28 27 26 25 24 23 2 19	

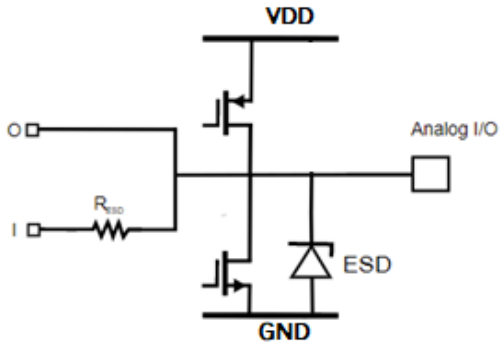
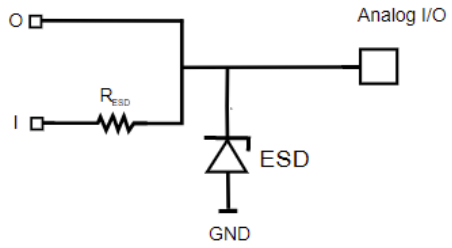
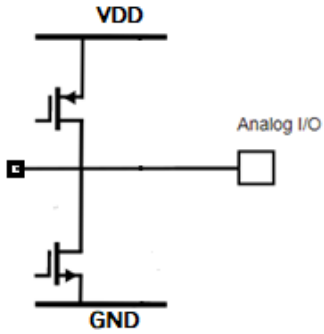
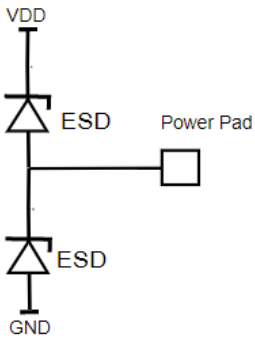
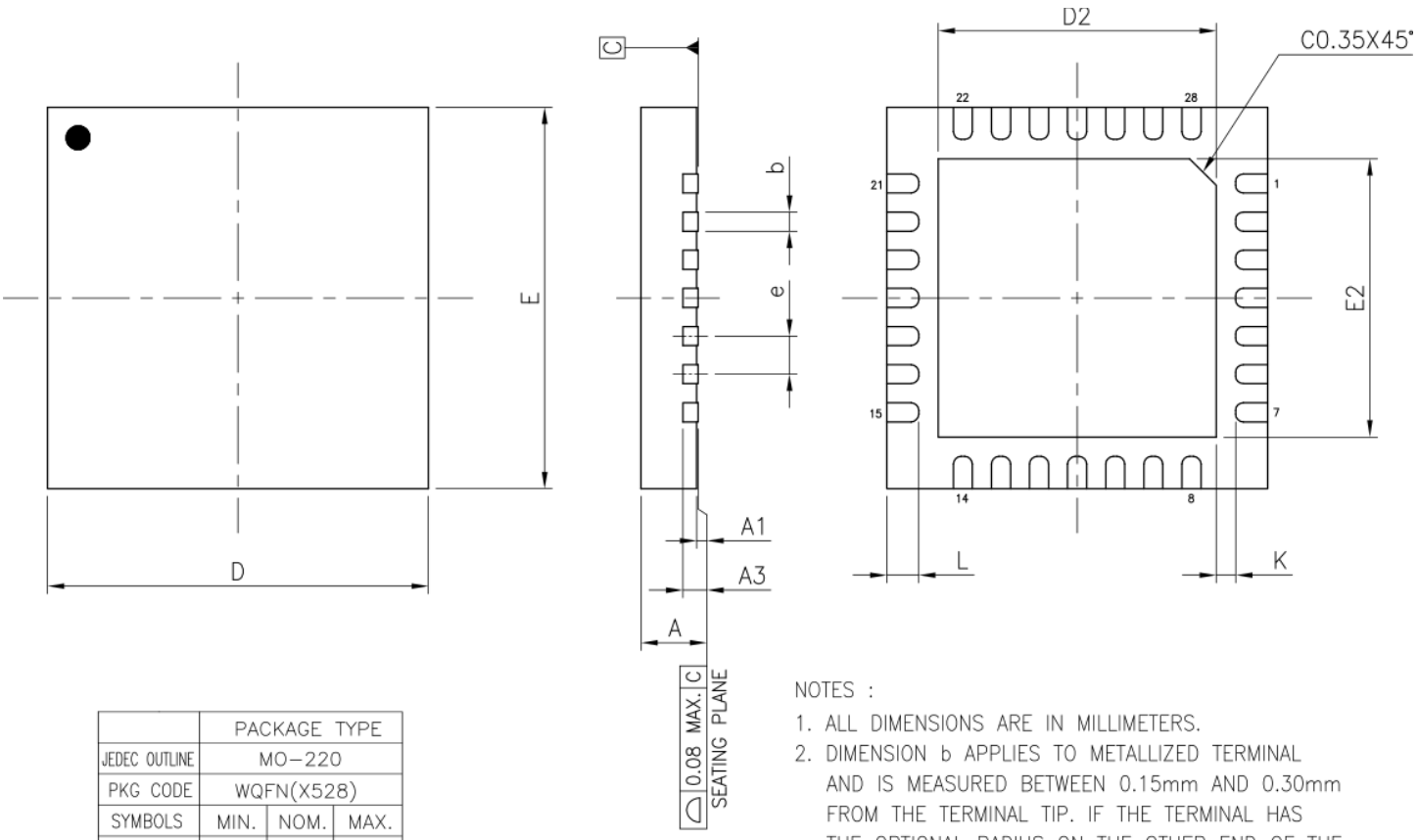
VREF VREF_BUF MICBIAS	Analog_IO_ 2XVDD	16 15 14	
PLL_REG	Analog I/O	18	
IN_P1 IN_P2 IN_M1 IN_M2	Analog I/O ADC	9 12 10 11	
DVDD	I/O Power	22	

Table 25 – Internal Pad Circuitry

28 QFN Package Dimensions



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X528)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
K	0.20	—	—

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
138X138 MIL	3.20	3.25	3.30	3.20	3.25	3.30	0.50	0.55	0.60	V	X	W(V)HHD-1

Figure 21 – ES9826Q 28 QFN package dimensions

28 QFN Top View Marking

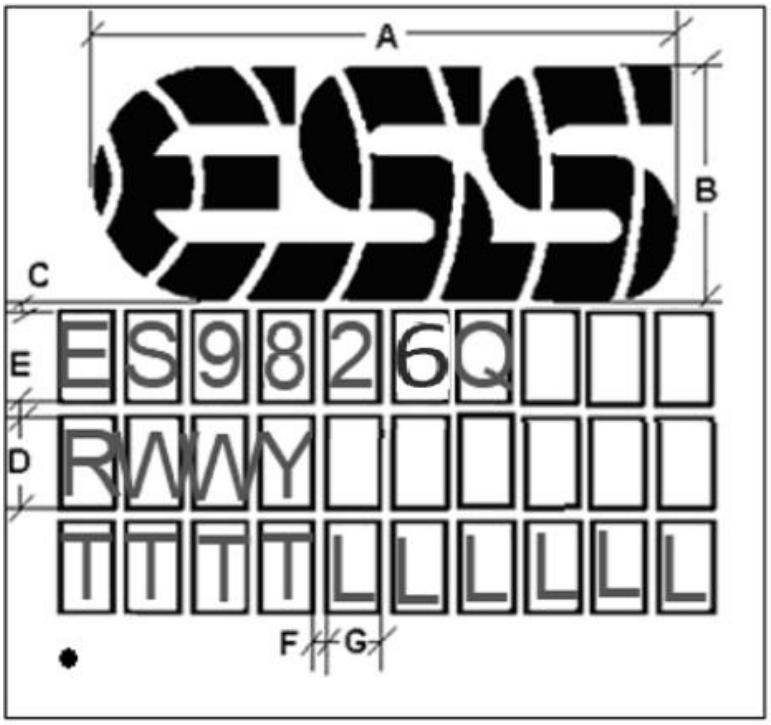


Figure 22 – ES9826Q Marking

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
28 QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

T	*Tracking number*
W	*Work week*
Y	*Last digit of year*
L	*Lot number*
R	*Silicon Revision*

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider. The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process – Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

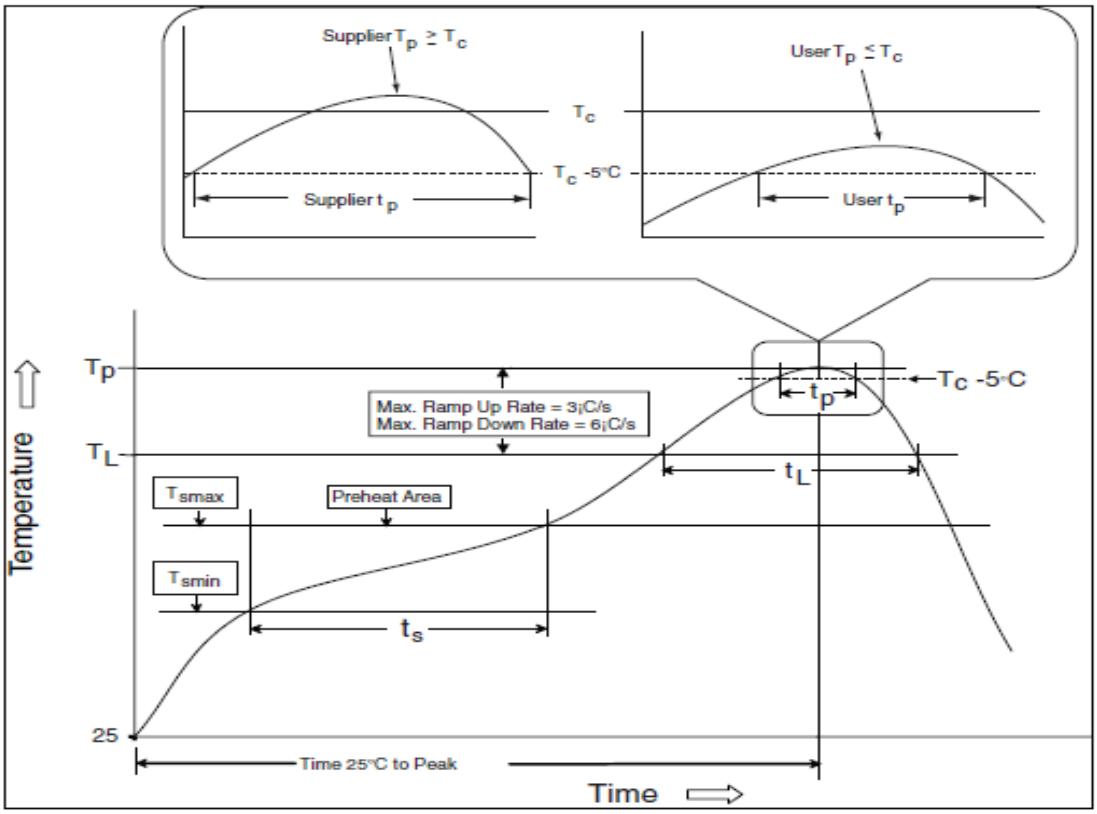


Figure 23 – IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 26 – RPC-1 Classification reflow profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 27 – RPC-2 Pb free classification temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9826Q	SABRE 32-bit 2 Channel ADC with built in PGA, MicBias, APLL, and multiple output formats	5mm x 5mm 28 QFN

Revision History

Current Version 0.1.2

Rev.	Date	Notes
0.1.2	April, 2023	Initial release

Mouser Electronics

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ES9826Q