ES9603Q
SABRE Headphone Driver with Programmable Current

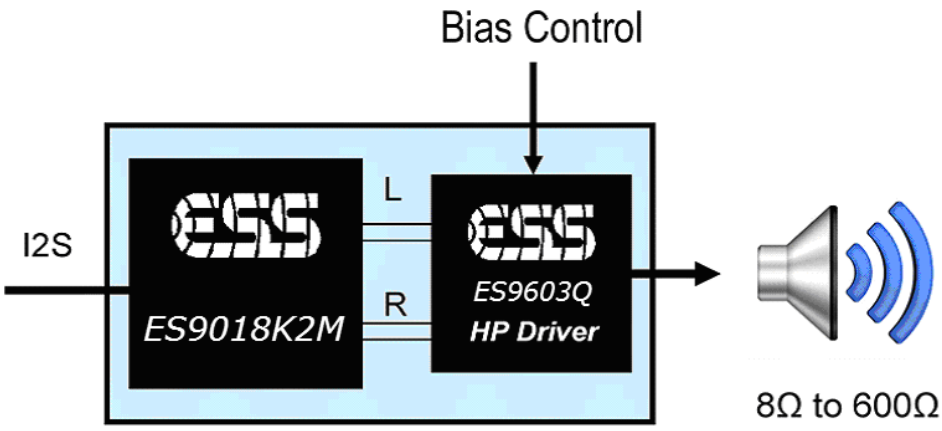
The ***ES9603Q Headphone Driver with Programmable Current*** is the industry's highest performance, standalone headphone driver targeted for audiophile-grade portable applications such as mobile phones, tablets and digital music players.

The ***ES9603Q Headphone Driver with Programmable Current*** delivers 122dB SNR and –123dB THD, a new benchmark in standalone headphone driver performance that will satisfy the most demanding audio enthusiasts.

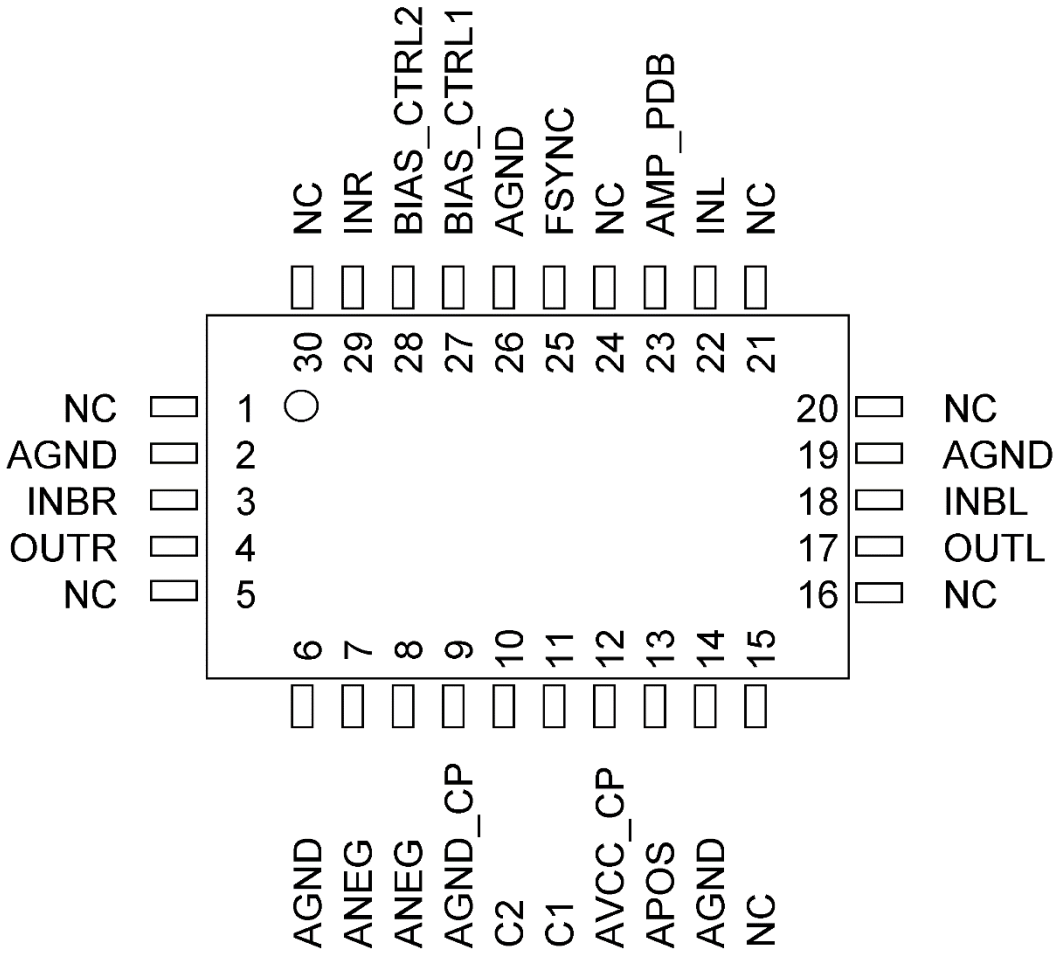
The ***ES9603Q Headphone Driver with Programmable Current*** allows the user to program the quiescent current and optimize the THD+N performance to match the listener's preferences.

Like ESS' high-quality SABRE[32] Reference DACs, the ***ES9603Q Headphone Driver with Programmable Current*** sets the standard for HD Audio performance with **SABRE SOUND™** quality for today's most demanding audio applications.

FEATURE	DESCRIPTION
Unmatched performance ○ +122dB SNR ○ –123dB THD, 2Vrms into 100kΩ load ○ –117dB THD+N, 2Vrms into 600Ω load	○ Industry's highest performance audio headphone or line-out driver for mobile applications ○ Delivers SABRE SOUND™ quality all the way to the headphones
Ground-referenced output	○ Eliminates large blocking capacitors
Pop-noise suppression	○ Powers up and down without any clicks or pops
Charge pump for negative supply	○ Single AVCC operation simplifies power supply
30-pin QFN	○ Minimizes PCB footprint
7mA / < 5μA, Normal power / standby mode	○ Maximizes battery life
Programmable performance ○ Lowest Power –98dB THD+N into 32Ω ○ Normal Power –106dB THD+N into 32Ω ○ Best Performance –112dB THD+N into 32Ω	○ Performance to match the listener's preferences



PIN LAYOUT



Top View

PIN DESCRIPTIONS

Pin	Name	I/O	Description
1	NC	–	No internal connection. May be connected to Analog Ground plane if desired
2	AGND	I	Analog Ground
3	INBR	I	Differential Negative Analog Input (Right Channel)
4	OUTR	O	Headphone Amplifier Right Channel Output
5	NC	–	No internal connection. May be connected to Analog Ground plane if desired
6	AGND	Ground	Analog Ground
7,8	ANEG	Power	Negative Amplifier Supply Input. Connect a 22μF minimum hold capacitor from ANEG to analog ground. Increasing the hold capacitor value will improve supply regulation but increases start-up time.
9	AGND_CP	Ground	Analog Ground for the Charge Pump
10	C2	–	Negative Analog Flying Capacitor. Connect a 4.7μF, low-ESR ceramic capacitor between C1 & C2
11	C1	–	Positive Analog Flying Capacitor. Connect a 4.7μF, low-ESR ceramic capacitor between C1 & C2
12	AVCC_CP	Power	Analog Power for the Charge Pump
13	APOS	Power	Positive Supply for Headphone Amplifiers. Decouple with a 22μF minimum, low-ESR ceramic capacitor to ground
14	AGND	–	Analog Ground
15, 16	NC	–	No internal connection. May be connected to Analog Ground plane if desired
17	OUTL	O	Analog Left Channel Output
18	INBL	I	Differential Negative Analog Input (Left Channel)
19	AGND	–	Analog Ground
20, 21	NC	–	No internal connection. May be connected to Analog Ground plane if desired
22	INL	I	Differential Positive Analog Input (Left Channel)
23	AMP_PDB	I	Active-low Power Down (High for normal operation)
24	NC	–	No internal connection. May be connected to Analog Ground plane if desired
25	FSYNC	I/O	Oscillator drive signal. FSYNC can be used to synchronize multiple devices together using the same charge-pump frequency. Typically 120kHz, 0-3.3V.
26	AGND	Ground	Analog Ground
27	BIAS_CTRL1	I	Bias control input 1
28	BIAS_CTRL2	I	Bias control input 2
29	INR	I	Differential Positive Analog Input (Right Channel)
30	NC	–	No internal connection. May be connected to Analog Ground plane if desired
–	PAD	Ground	Exposed pad. Connect to Analog Ground plane for heatsinking

FUNCTIONAL DESCRIPTION

The ES9603Q has a pair of CMOS FET input amplifiers that exhibit a total A-weighted SNR of better than 123dB when driving 2Vrms into a 600Ω load. The ES9603Q has an open-loop gain well in excess of 120dB which together with the input stage's excellent linearity is the key to its unparalleled –123dB distortion performance (normal power). Please note that the amplifier distortion performance far exceeds that of typical external passive components. Therefore, to achieve the THD performance specified for the ES9603Q, ensure that the external resistors have a very low, voltage coefficient of resistance, e.g. thin film resistors. Tight tolerance (0.1%) thin-film resistors are recommended for all gain-defining components.

Charge Pump

The ES9603Q features a low-noise charge pump. The 120kHz switching frequency is above the audio band and, thus, does not interfere with audio signals. The switches are controlled by turn-on and turn-off transistors that operate in a particular sequence that minimizes pops and clicks. The IC requires a 4.7μF minimum flying capacitor between pins 15 and 16 and a 22μF minimum hold capacitor from pins 12/13 to pin 11. The chip's FSYNC pin offers three connection options; capacitance may be added from FSYNC to ground to slow down the oscillator (100kHz minimum), a logic signal can drive the FSYNC pin to set a fixed frequency, or the FSYNC pins of several ES9603Q chips may be connected together to force them to run synchronously.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range select capacitors with a minimum X5R dielectric, the X7R dielectric is preferred. The charge pump can be disabled by grounding FSYNC which reduces quiescent current from the +3.3V supply. Disabling the charge pump is recommended when using an external –3.3V supply connected to ANEG.

Flying Capacitor (C4, see Figure 2)

The value of the flying capacitor (C4, connected across pins 15 and 16) affects the charge pump's load regulation and output resistance. A capacitance value (C4) that is too small reduces the current drive capability, which leads to a loss of output voltage. Increasing the value of C4 improves load regulation and reduces the charge-pump output resistance to an extent. The value of the flying capacitor also affects power-on "pop" and the larger the capacitor the larger the pop. The minimum value of flying capacitor is 1μF which provides the lowest switch-on pop and is the lowest capacitor value that should be used.

With a 4.7μF flying capacitor, the on-resistance of the switches dominates. Use a low-ESR ceramic or electrolytic capacitor for C4. If an electrolytic capacitor is used the correct polarity must be observed, see Figure 2.

Hold Capacitor (C2, see Figure 2)

The value of the hold capacitor C2 (connected between ANEG and ground) and its Equivalent Series Resistance (ESR) directly affects the ripple voltage at ANEG. Use a low-ESR 22μF minimum capacitor for C2 and also choose the correct voltage rating. C2 can be a ceramic or electrolytic capacitor, if an electrolytic capacitor is used, the correct polarity must be observed, see Figure 2. Increasing the value of the hold capacitor will improve regulation but will increase start-up time.

Amplifier Gain

The recommended gain setting for ES9603Q is 0dB (Unity Gain). The feedback resistors R1 and R2 of Figure 2 should match the output impedance of the DAC or other signal source. For example, when working with the ES901xK2M the recommend values of R1, R2, R4, and R6 are all 806Ω which gives the best DNR.

Compensation Components (see Figure 2)

For optimum performance, the following capacitors should be included in all configurations of the ES9603Q. C1 and C6 control the bandwidth of the ES9603Q, along with the matching networks C3 and C5. These compensation capacitors should have a low temperature coefficient of capacitance, NP0/C0G types are required.

Short-Circuit Protection (see Figure 2)

To protect the ES9603Q under short-circuit conditions 4.7Ω resistors should be placed in series with each output, OUTL and OUTR.

Programming the Quiescent Current

There are two pins provided for programming the quiescent current of the ES9603Q which in turn modifies the THD+N performance of the headphone amplifier. The programming pins are BIAS_CTRL1 and BIAS_CTRL2 and these set three different performance levels listed in the table below.

			External -3.3V Supply		Internal Negative CP supply	
Description	**BIAS_CTRL1**	**BIAS_CTRL2**	**THD+N (32Ω)**	**Quiescent Current**	**THD+N (32Ω)**	**Quiescent Current**
Low Power	Low	Low	-98 dB	63 uA	-95 dB	2.6 mA
Normal Power	Low	High	-106 dB	1.25 mA	-103 dB	4.3 mA
Best Performance	High	High	-112 dB	3 mA	-110 dB	8.3 mA
AMP_PDB set high (active)				10 uA		8 uA

Performance measured with Apx555 using full scale signal.

ES9603Q Block Diagram

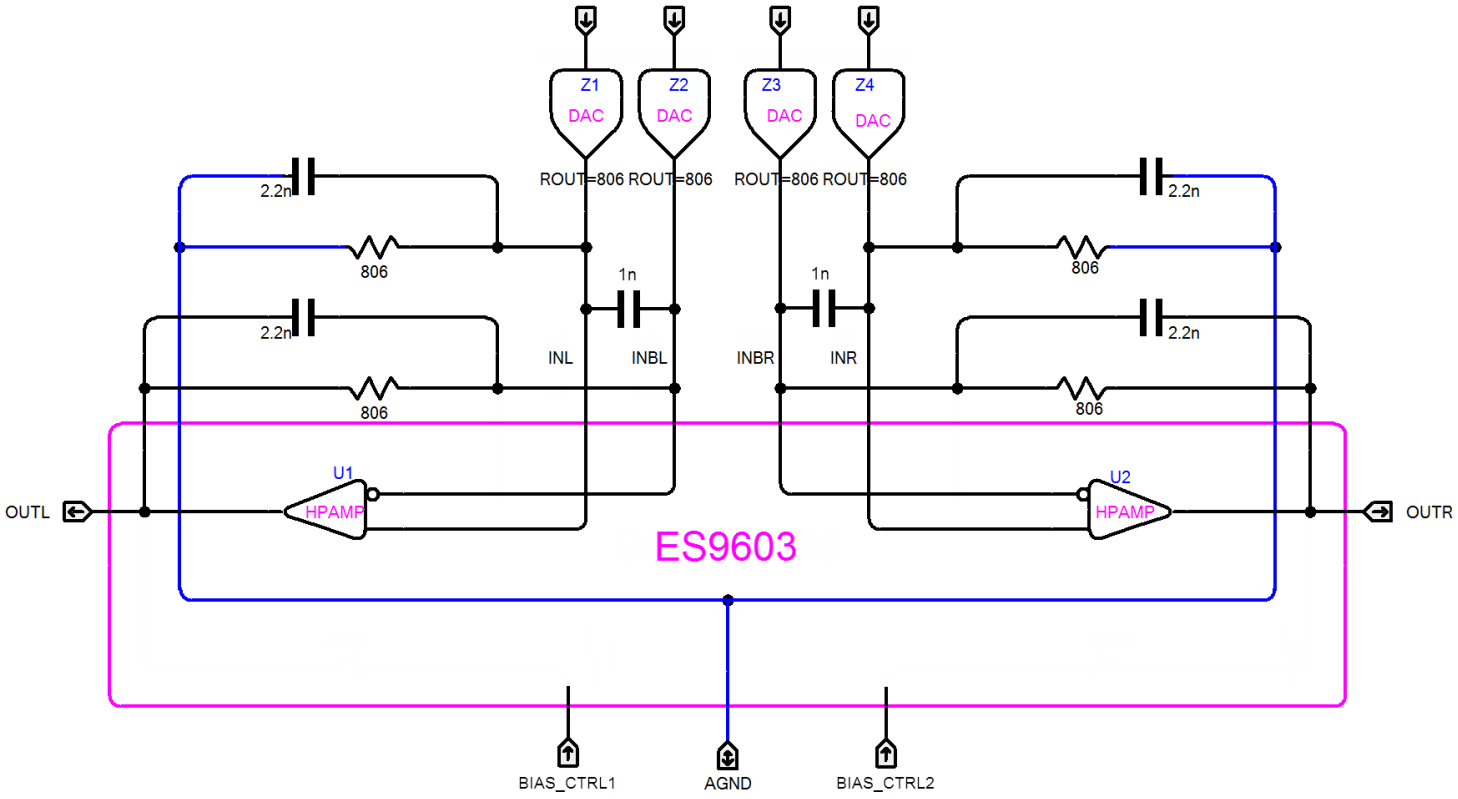


Figure 1. Block Diagram of the ES9603Q plus external Gain Setting and Compensation Components.

APPLICATION DIAGRAM

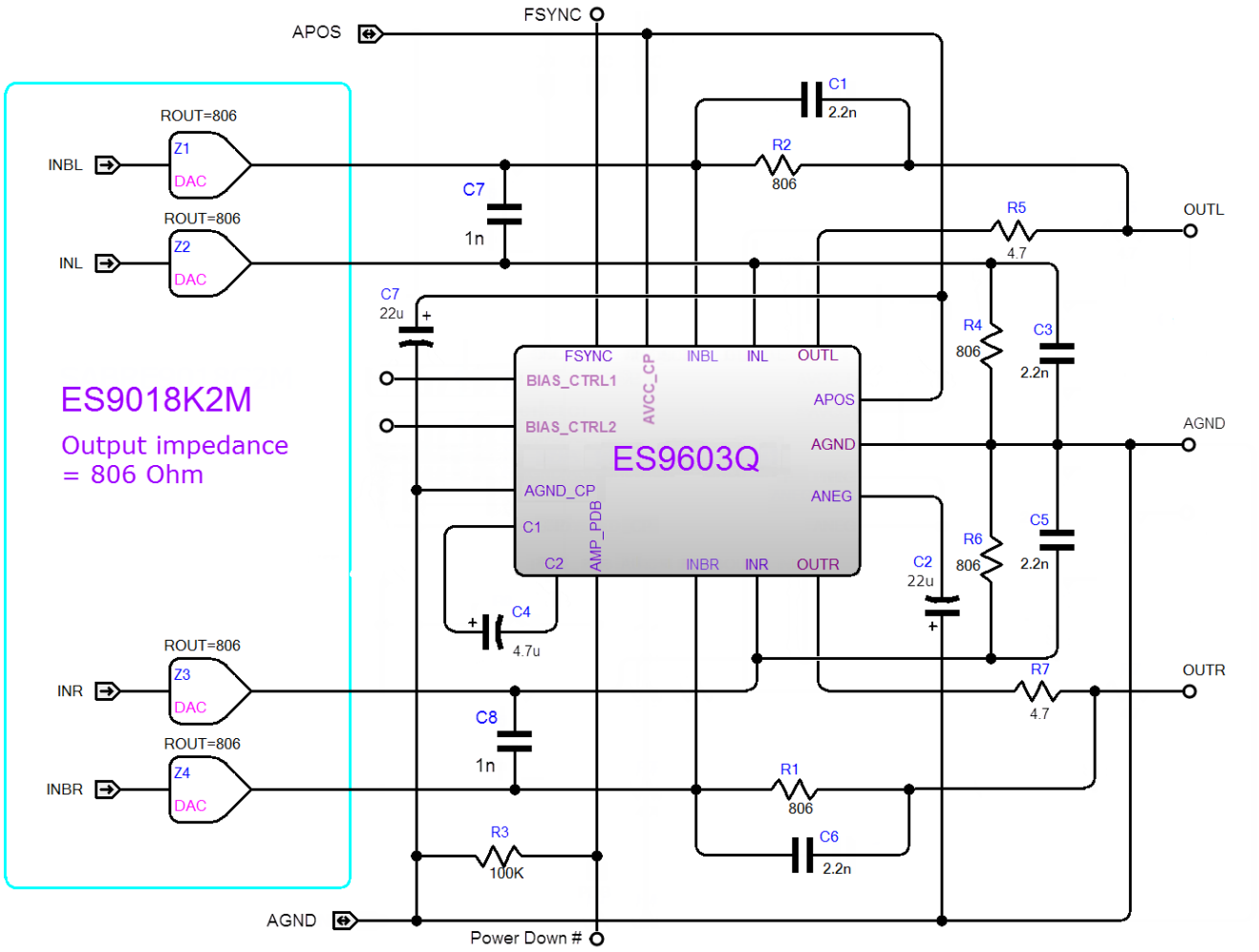


Figure 2. Simplified ES9603Q Application Circuit.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Positive Supply Voltage (APOS, AVCC_CP)	+3.7V
Storage temperature	–65°C to +105°C
Voltage range for control pins AMP_PDB, BIAS_CTRL1 and BIAS_CTRL2	–0.3V to APOS+ 0.3V
Voltage range for control pin FSYNC	–0.3V to AVCC_CP + 0.3V
ESD Protection Human Body Model (HBM) Machine Model (MM) Charge Device Model (CDM)	 2000V 200V 500V

WARNING: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature	T_A	–20°C to +70°C

Power Supply	**Symbol**	**Voltage**	**Quiescent Current (Note 1)**	**Standby Current (Note 2)**
Power supply voltage	AVCC_CP APOS	+3.3V ± 5%	7mA typical in Normal Mode	< 5µA
Power Supply	**Symbol**	**Load Resistance**	**Supply Current (Normal power, Note 3)**	**Output Voltage (Note 4)**
Power Supply current at +3.3V	I_{SY}	32Ω	50mA typical	800mVrms @ 1kHz

Notes

1) Input idling, output unloaded, internal oscillator, all external supply voltages at nominal center values
2) With AMP_PDB held low
3) Supply current is with both outputs loaded and driven at 800mVrms
4) 800mVrms sine wave across a 32Ω load produces a 20mW output

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Minimum	Maximum	Unit
VIH	High-level input voltage	1.4		V
VIL	Low-level input voltage		0.4	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current	I_B	INL, INBL, INR, INBR inputs	–1.0	0.1	+1.0	nA
Output Offset Voltage	V_{OS}	OUTL to AGND & OUTR to AGND, no input signal	–2.0	0.1	+2.0	mV

ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

T_A = 25ºC, APOS = AVCC_CP = +3.3V, 1kHz signal, C2 = 22µF, C4 = 4.7µF, FSYNC = open (Figure 2 configuration), Normal mode

1. SNR/DNR: A-weighted over 20Hz-20kHz in averaging mode
2. THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	VOUT = 2.0Vrms, A-weighted, RL = 600Ω		122		dB
Total Harmonic Distortion plus Noise	THD+N	VOUT = 2.0Vrms, RL = 100kΩ		–123		dB
		VOUT = 2.0Vrms, RL = 600Ω		–117		dB
		POUT = 49mW into 32Ω load		–102		dB
Power Supply Rejection	PSR	fin = 217Hz, 200mVp-p ripple		–89		dB
		fin = 1kHz, 200mVp-p ripple		–89		dB
		fin = 10kHz, 200mVp-p ripple		–82		dB
Common-Mode Rejection	CMR	5mV Input, RL = 600Ω		-139		dB
Output Swing		RL = 100kΩ		APOS-0.2		V
Open-Loop Gain				139		dB

TYPICAL PERFORMANCE CURVES

The following typical performance curves are generated using ESS' evaluation board as shown in Figure 11. The internal charge pump is used to supply the negative rail. Measurements are taken using an Audio Precision Audio Analyzer. Note that all measurements in the graphs include errors due to the test equipment plus those of the ES9018K2M DAC on the evaluation board. Although these errors are very low, they are significant when measuring a state-of-the-art headphone amplifier like the ES9603Q. Therefore the parametric values shown in the characteristic curves are slightly degraded compared to the values in the tables as the latter are calculated from measurements in near-ideal conditions.

TYPICAL PERFORMANCE CURVES

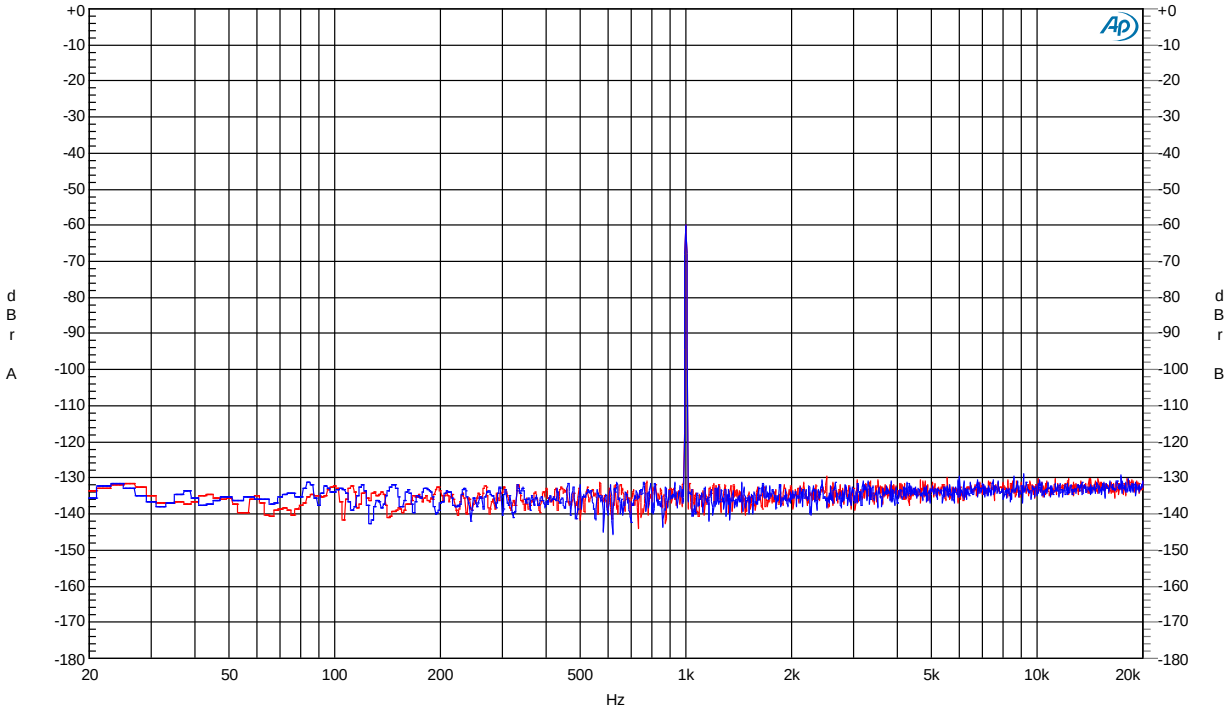


Figure 3. DNR FFT, 1kHz @ –60dB, Single-Ended, 32Ω Load

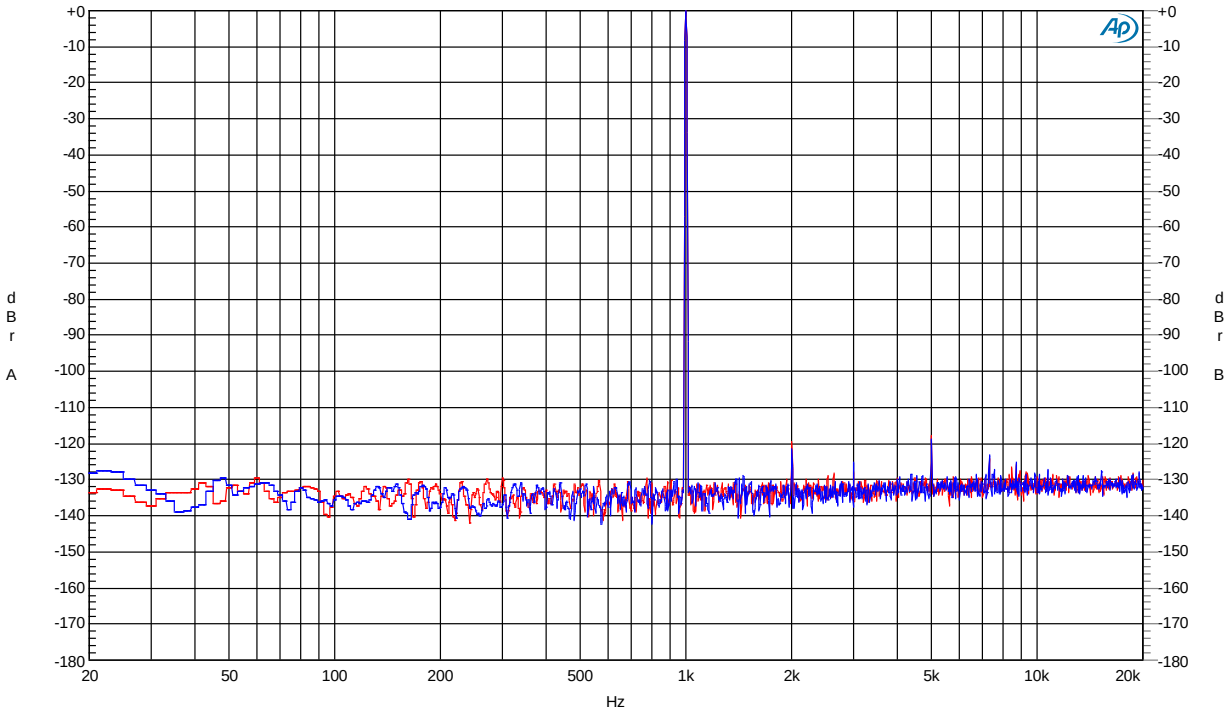


Figure 4. THD+N FFT, 1kHz @ –6dB, Single-Ended, 32Ω Load (normal power)

TYPICAL PERFORMANCE CURVES

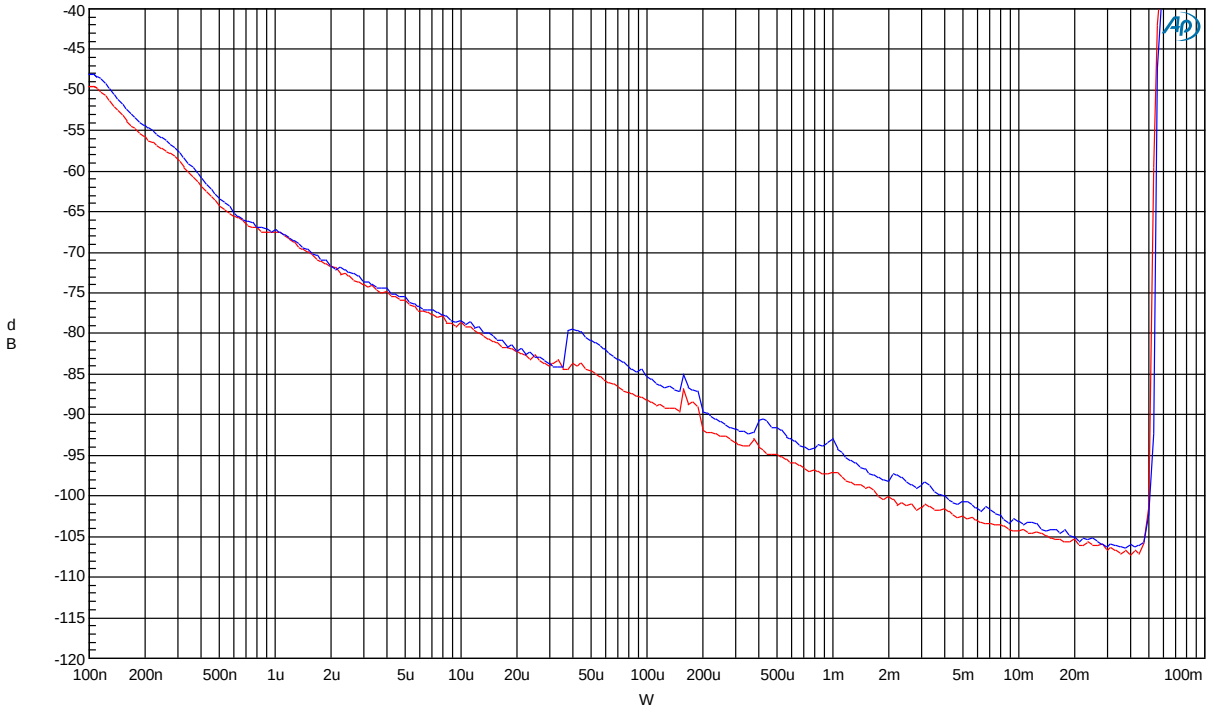


Figure 5. THD+N Un-weighted vs. Output Power, Dual Channel Drive, Single Ended, 32Ω Load (normal power)

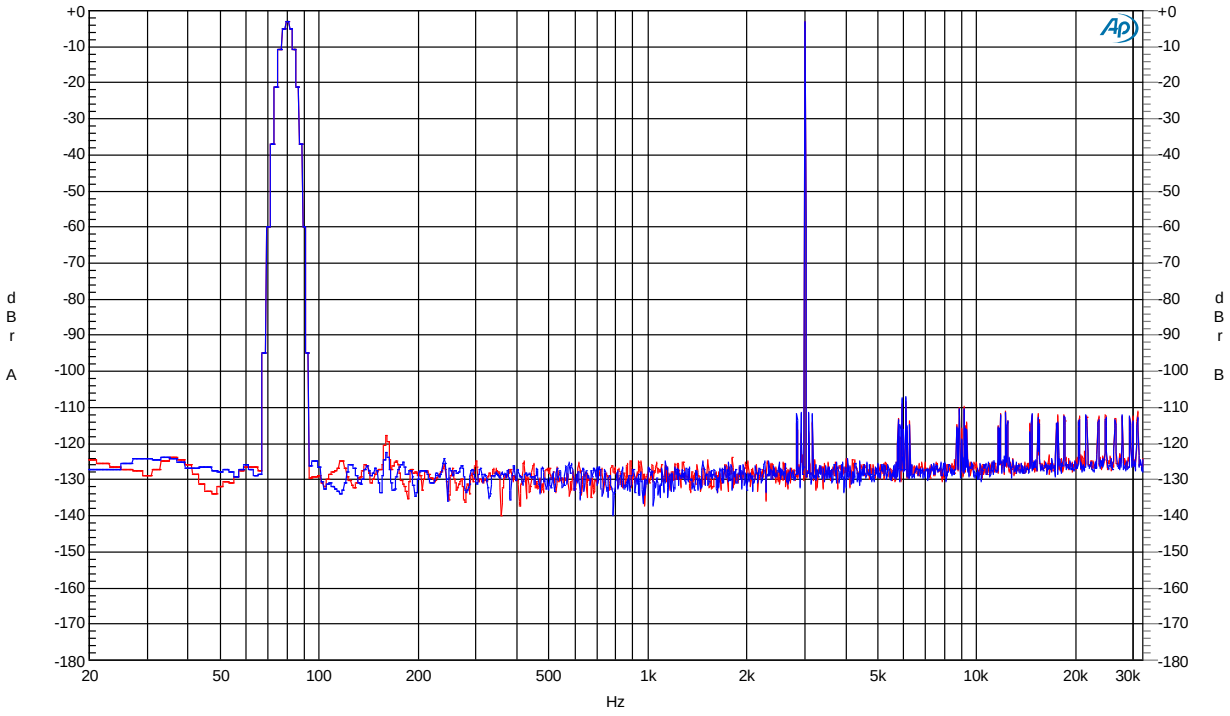


Figure 6. IMD FFT, 3kHz & 80Hz @ SMPTE 1:1, Single Ended, 32Ω Load (normal power)

TYPICAL PERFORMANCE CURVES

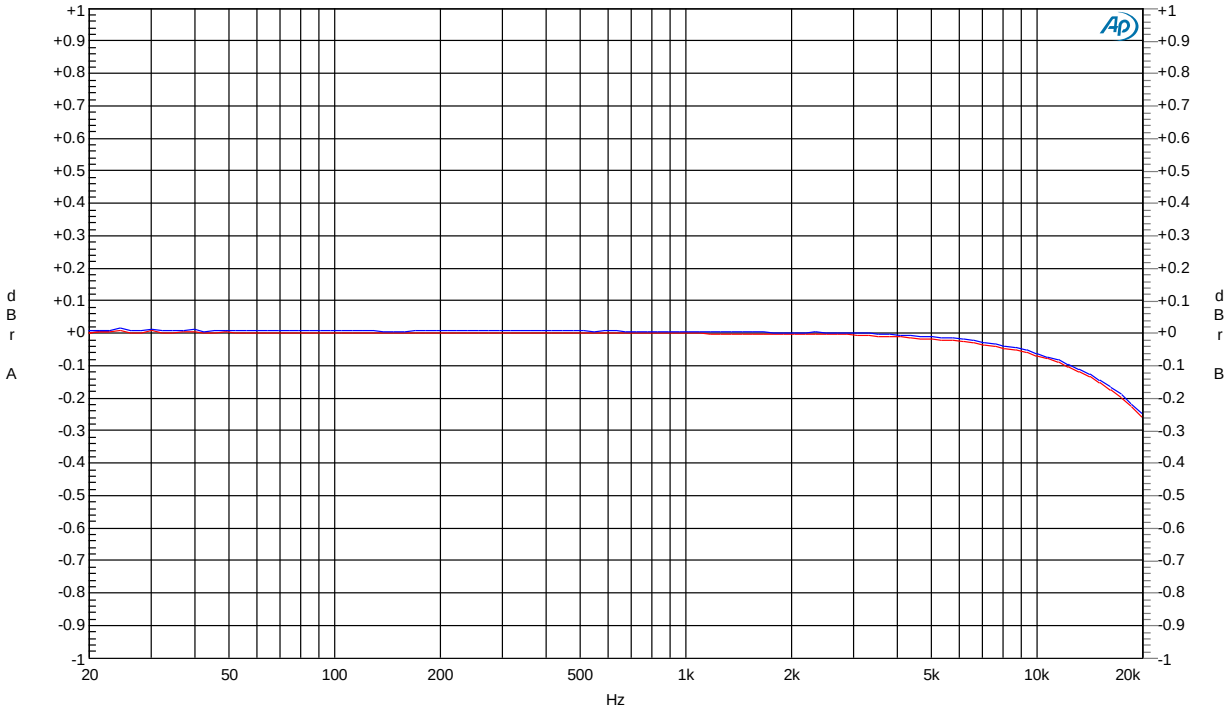


Figure 7. Frequency Response, 20Hz to 22kHz @ 0dB, Log Scale, Single Ended, 32Ω Load (normal power)

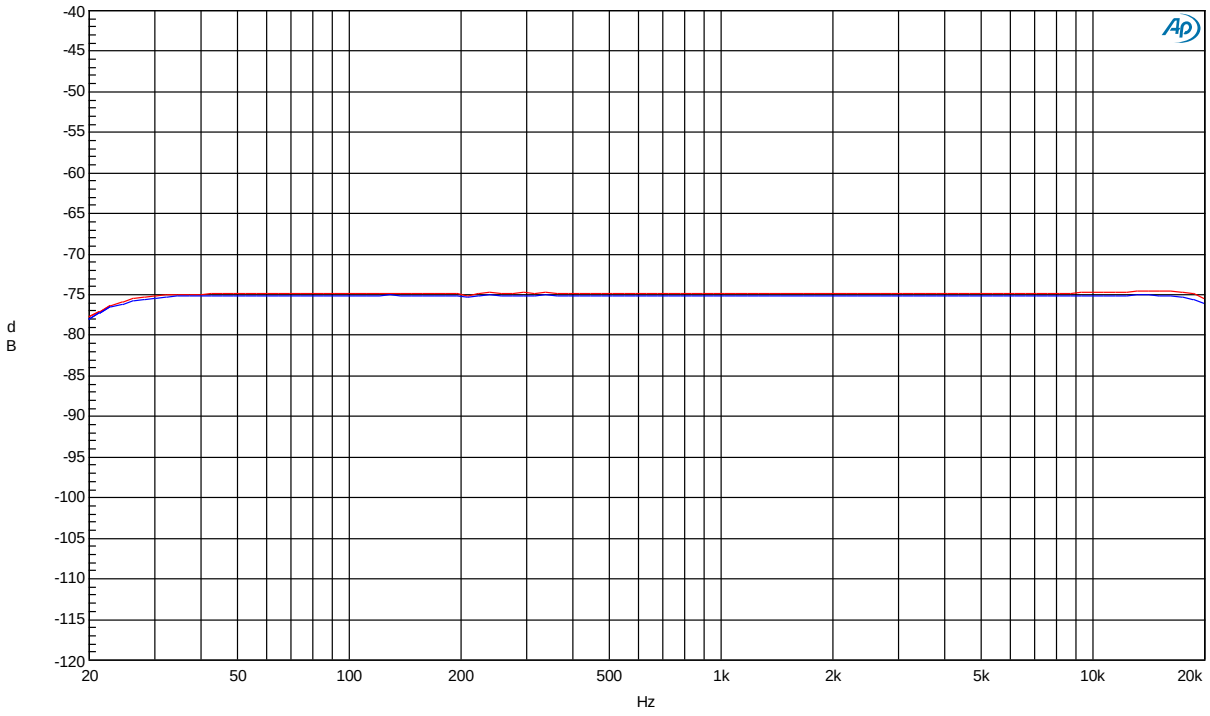


Figure 8. Crosstalk vs. Frequency, Single Ended, 32Ω Load (normal power)

TYPICAL PERFORMANCE CURVES

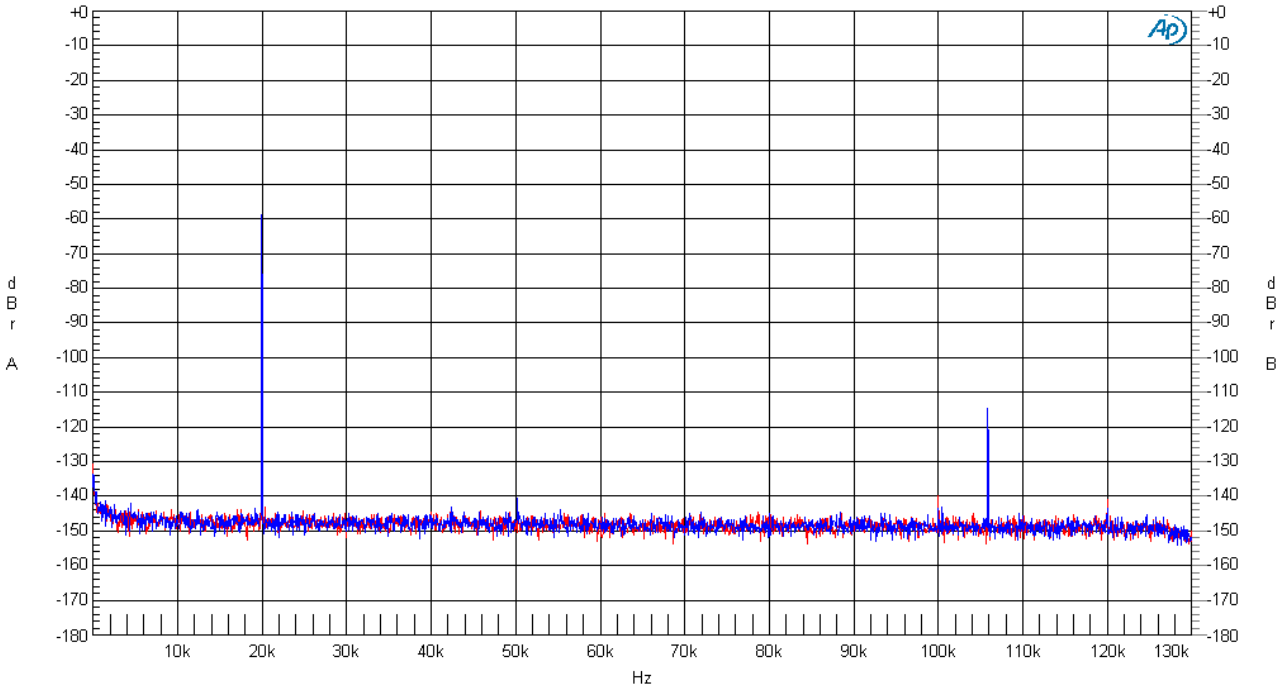


Figure 9. Wideband FFT, 20kHz @ –60dB, Single Ended, 32Ω Load (normal power)

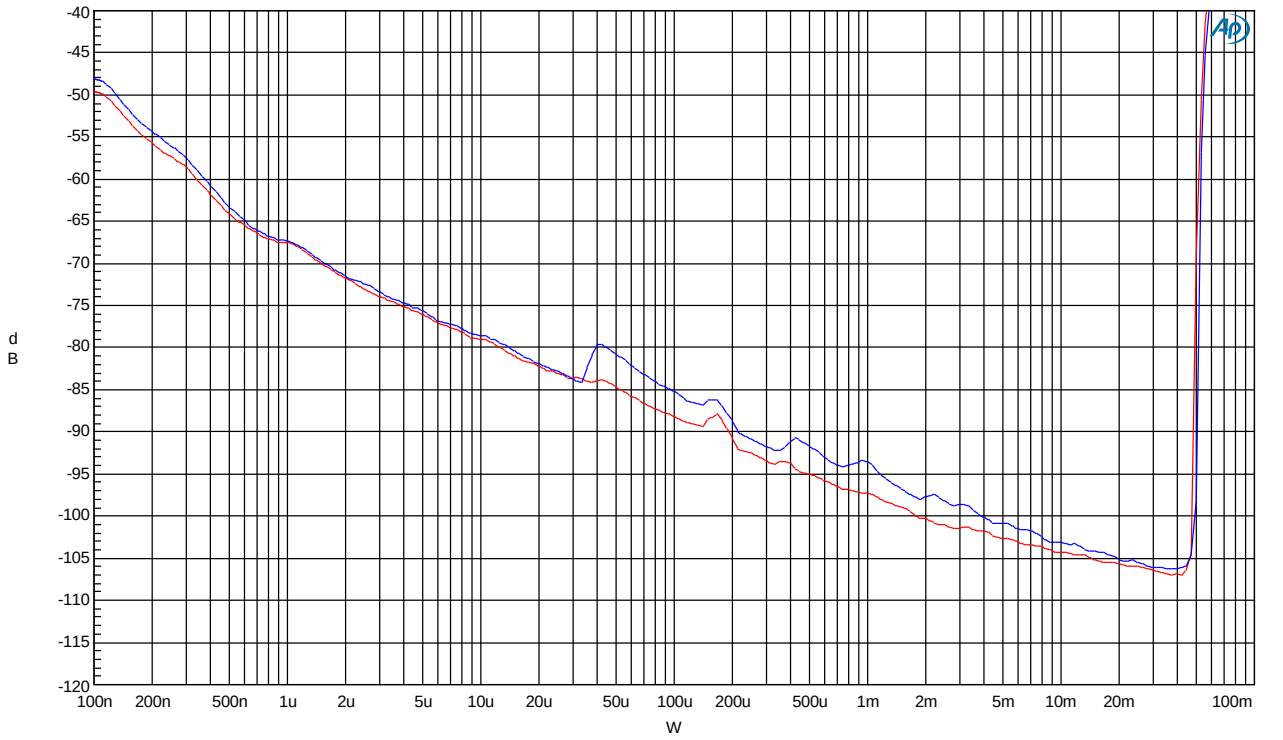
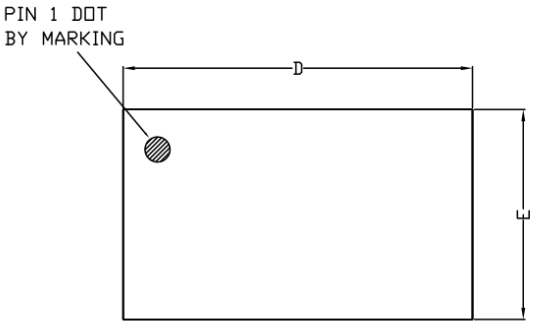
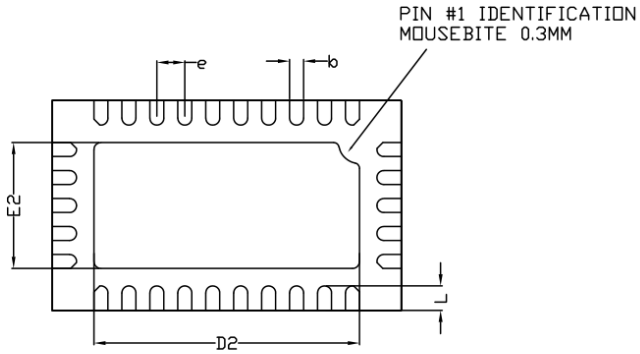


Figure 10. THD+N Un-weighted vs. Output Power, Dual Channel Drive, Single Ended, 16Ω Load, ext. –3.3V supply (normal power)

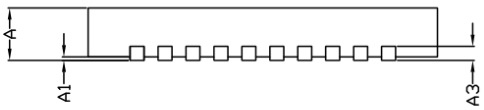
30-Pin QFN Mechanical Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Lead finish : NiPdAu

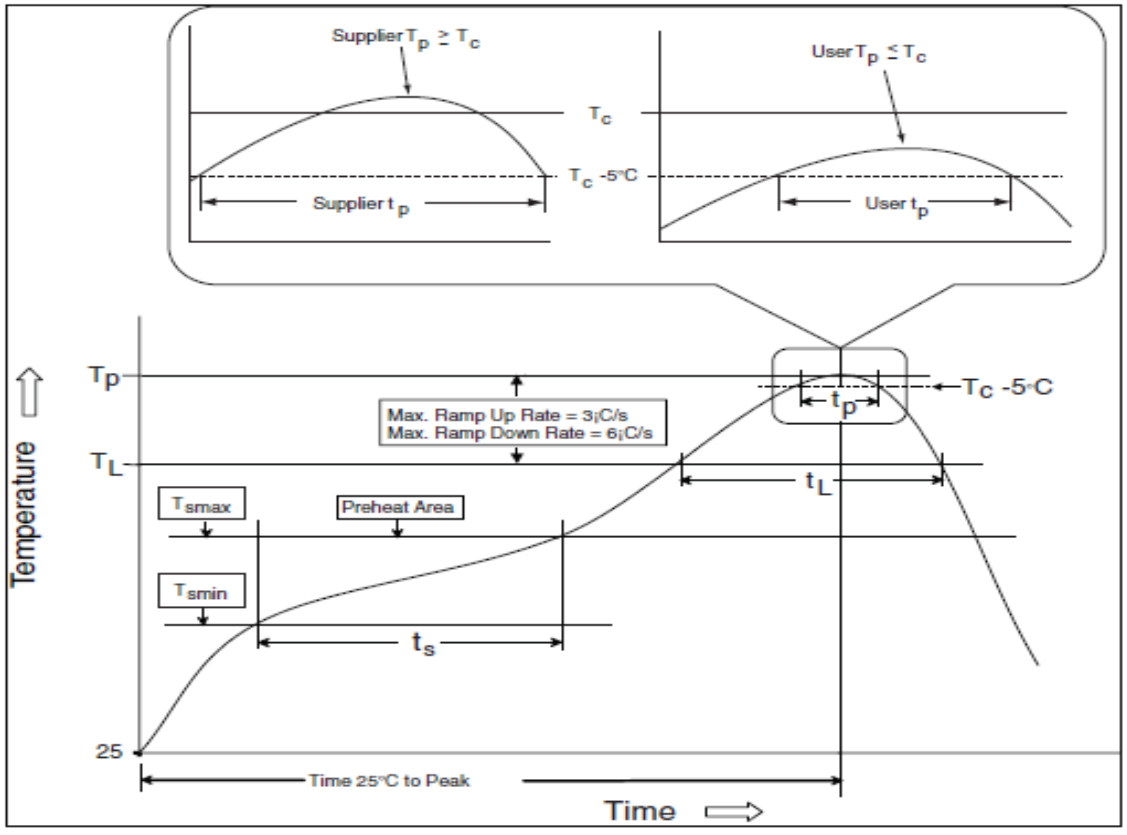
COMMON DIMENSIONS(MM)			
PKG.	W:VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.2 REF.		
D	4.95	5.00	5.05
E	2.95	3.00	3.05
b	0.15	0.20	0.25
L	0.25	0.35	0.45
D2	3.75	3.80	3.85
E2	1.75	1.80	1.85
e	0.40 BSC		

Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10°C to 20°C.
The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.
Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)



Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual Soldering:
Allowed up to 2 times with maximum temperature of 350 degrees no longer than 3 seconds.

Table RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	6°C / second max.
Time 25°C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.
For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Table RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

ORDERING INFORMATION

Part Number	Description	Package
ES9603Q	Sabre Headphone Amp with Programmable Current	30-pin QFN

The letter Q identifies the package type QFN.

Revision History

Current Version: 0.4.1

Rev.	Date	Notes
0.1	July 27, 2015	Initial release
0.2	September 9, 2015	• Added C7 and C8 to the recommended application circuit of figure 2. • Added ESD rating for Charge Device Model (CDM) • Added supply voltage limits to the Absolute Maximum Ratings table • Added specifications to the Analog Performance Table
0.3	November 28, 2017	• Remove ESS logo from pin diagram • Remove 30-Pin QFN example land pattern heading
0.4.1	August 29, 2022	• Updated programming quiescent current table • Updated formatting • Updated Company address

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