Analog Reinvented

ES9027PRO
32-bit High-Performance 8-Channel DAC
Product Datasheet

The ESS Sabre® ES9027PRO is a 32-bit 8 Channel digital-to-analog converters (DAC) that target high end consumer devices, professional audio applications such as recording systems, mixer consoles and digital audio workstations (DAW), test equipment, instruments, audio processors applications. It was designed to create the new generation of the world's highest performing audio DAC series.

The ES9027PRO has 8 integrated DACs which use ESS' patented Hyperstream® IV DAC Architecture. Using the Dual modulator architecture, it delivers incredible audio sound quality and specifications, including +124dB DNR, -114dB THD+N per channel.

The ES9027PRO SABRE® DAC improves on previous designs to include:

- TDM & SPI support for more options in connectively
- Lower power consumption than previous generations, including the Hyperstream IV DAC modulator
- New Hardware mode for simplified programming.

TDM, DSD, DoP, and I2S, LJ, master/slave interfaces as well as synchronous S/PDIF are supported.

The ES9027PRO has 7 built-in pre-programmed digital filters which allows the most discerning user to tune the SABRE sound to their own personal sound signature.

FEATURE	DESCRIPTION
Patented 32-bit HyperStream® IV Architecture DAC Technology	32-bit audio DAC with high dynamic range & ultra-low distortion
+124dB DNR per channel -114dB THD+N per channel	Unprecedented dynamic range and ultra-low distortion
High Sample Rates	Up to PCM 768kHz & native DSD1024
Customizable filter characteristics	7 predefined digital filters optimized for latency or sound color for each channel to allow for a unique sound signature
Multiple Input formats are available	I2S, LJ, RJ, TDM, DSD, DoP and S/PDIF
I2C, SPI, and Hardware interface control	Configured by microcontroller or other I2C/SPI source, or pins through Hardware Mode
Lower Power Consumption than Previous Gen.	Simplifies power supply design
Standardized Packaging	7mm x 7mm, 48 pin QFP/QFN for reduced PCB board space

APPLICATIONS

- Professional digital audio workstations (DAW) Audio Playback
- A/V Receivers
- Personal Audio Devices & Media Streamers
- High End Audiophile Equipment
- Any equipment that requires the very best audio digital to analog conversion

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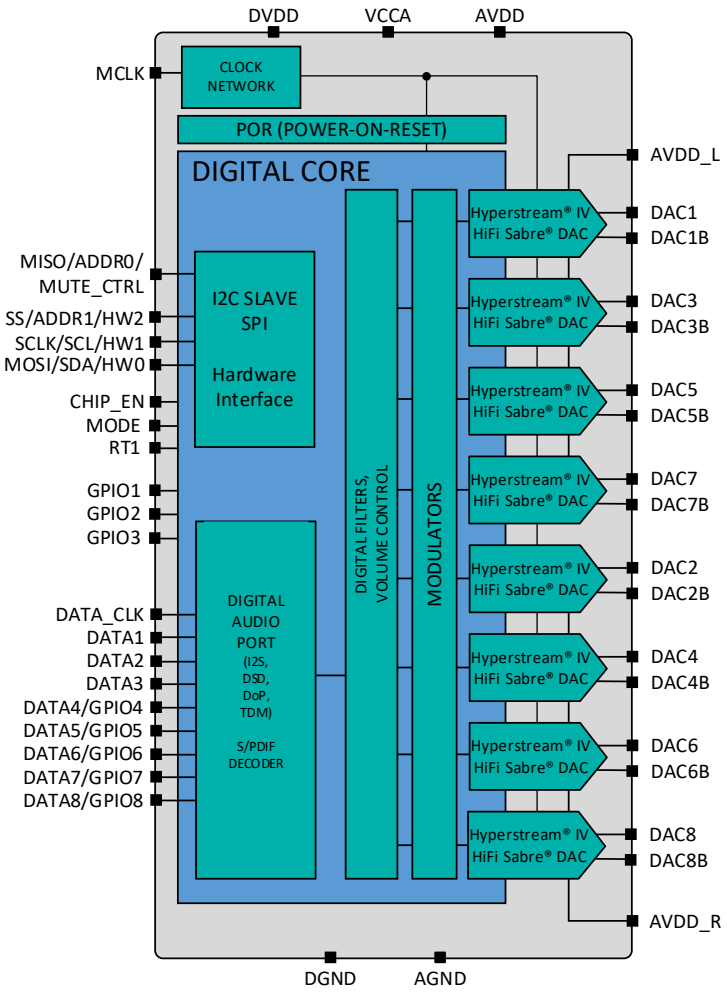
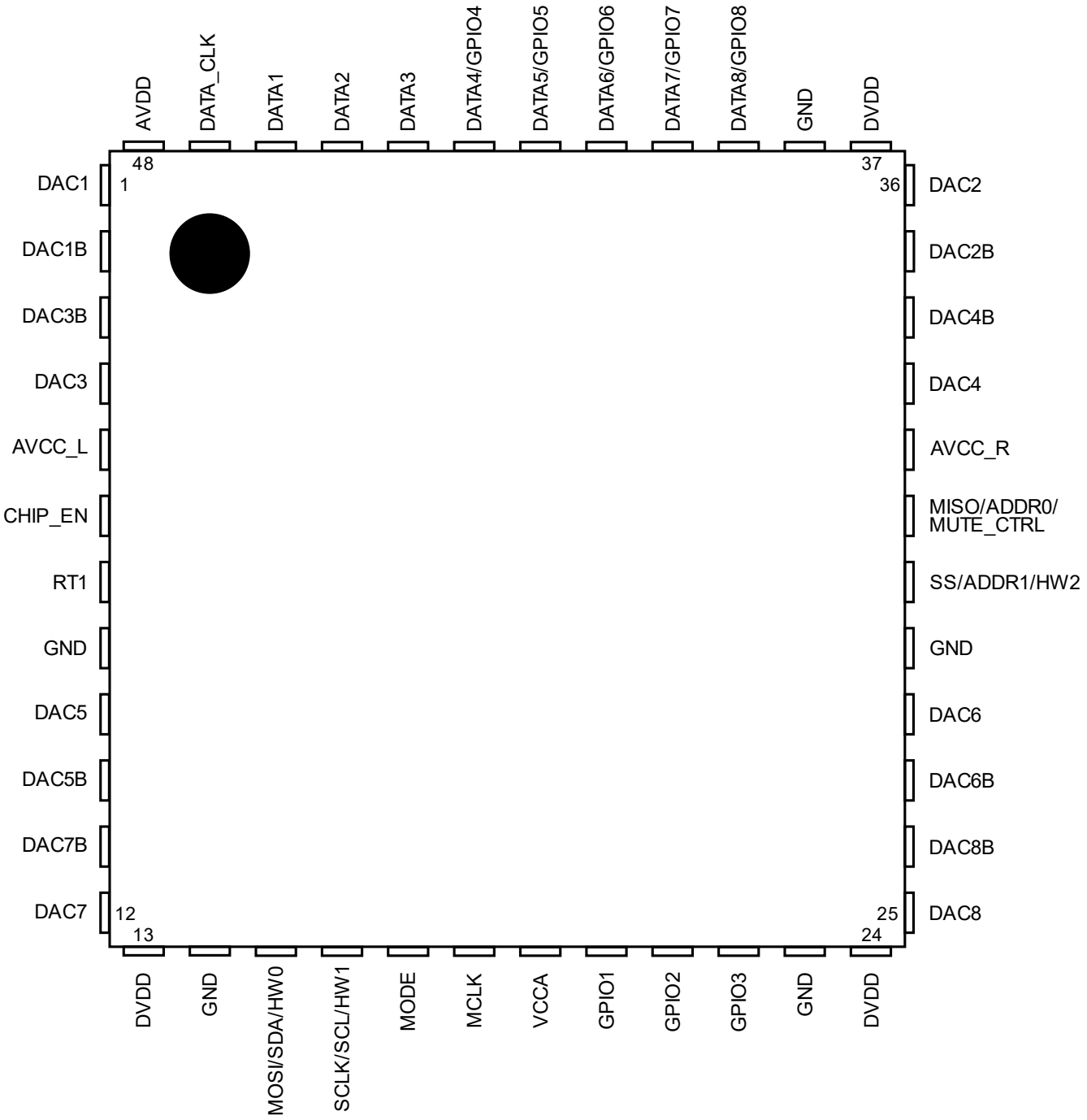


Figure 1 - ES9027PRO Block Diagram

ES9027PRO Pinout

48 QFN/QFP Pinout



ES9027PRO*
(Top View)

*Note: ES9027QPRO have exposed pad (pin 49) that should be connected to ground.

48 QFP/QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	DAC1	AO	Ground	Differential Positive Output for Channel 1
2	DAC1B	AO	Ground	Differential Negative Output for Channel 1
3	DAC3B	AO	Ground	Differential Negative Output for Channel 3
4	DAC3	AO	Ground	Differential Positive Output for Channel 3
5	AVCC_L	Power	Power	3.3V DAC analog output stage reference supply for the Left side
6	CHIP_EN	I	HiZ	Active-high Chip Enable
7	RT1	I	HiZ	Reserved. Must be connected to GND for normal operation.
8	GND	Ground	Ground	Ground
9	DAC5	AO	Ground	Differential Positive Output for Channel 5
10	DAC5B	AO	Ground	Differential Negative Output for Channel 5
11	DAC7B	AO	Ground	Differential Negative Output for Channel 7
12	DAC7	AO	Ground	Differential Positive Output for Channel 7
13	DVDD	Power	Power	Digital Core Supply, 1.2V
14	GND	Ground	Ground	Ground
15	MOSI/SDA/HW0	I	HiZ	Serial communication for SPI/I2C & HW0 interface pin, controlled by MODE
16	SCLK/SCL/HW1	I	HiZ	Serial Clock for SCLK (SPI), SCL (I2C), also HW1 controlled by MODE pin
17	MODE	I	HiZ	I2C/SPI Control selection or HW mode
18	MCLK	I	HiZ	Oscillator input
19	VCCA	Power	Power	Analog Supply, 3.3V
20	GPIO1	I/O	HiZ	General I/O w/extended functions
21	GPIO2	I/O	HiZ	General I/O w/extended functions
22	GPIO3	I/O	HiZ	General I/O w/extended functions
23	GND	Ground	Ground	Ground
24	DVDD	Power	Power	Digital Supply, 1.2V
25	DAC8	AO	Ground	Differential Positive Output for Channel 8
26	DAC8B	AO	Ground	Differential Negative Output for Channel 8
27	DAC6B	AO	Ground	Differential Negative Output for Channel 6
28	DAC6	AO	Ground	Differential Positive Output for Channel 6
29	GND	Ground	Ground	Ground
30	SS/ADDR1/HW2	I	HiZ	Serial communication for SPI/I2C & HW2 interface pin, controlled by MODE pin
31	MISO/ADDR0/ MUTE_CTRL	I	HiZ	Serial communication for SPI/I2C & MUTE_CTRL interface pin, controlled by MODE pin
32	AVCC_R	Power	Power	3.3V DAC analog output stage reference supply for the Right side
33	DAC4	AO	Ground	Differential Positive Output for Channel 4
34	DAC4B	AO	Ground	Differential Negative Output for Channel 4
35	DAC2B	AO	Ground	Differential Negative Output for Channel 2
36	DAC2	AO	Ground	Differential Positive Output for Channel 2
37	DVDD	Power	Power	Digital Supply, 1.2V
38	GND	Ground	Ground	Ground
39	DATA8/GPIO8	I/O	HiZ	Serial DATA8, General I/O 8
40	DATA7/GPIO7	I/O	HiZ	Serial DATA7, General I/O 7
41	DATA6/GPIO6	I/O	HiZ	Serial DATA6, General I/O 6
42	DATA5/GPIO5	I/O	HiZ	Serial DATA5, General I/O 5
43	DATA4/GPIO4	I/O	HiZ	Serial DATA4, General I/O 4
44	DATA3	I	HiZ	Serial DATA3 pin
45	DATA2	I	HiZ	Serial DATA2 pin
46	DATA1	I	HiZ	Serial DATA1 pin
47	DATA_CLK	I	HiZ	Serial Data Clock pin
48	AVDD	Power	Power	3.3V I/O Supply
49	Package Pad (QFN package only)	-	-	Connect to ground

* Note: AO = Analog Output, I = Digital Input, I/O = Digital Input/Output

Feature List

The ES9027PRO is a SABRE 8 channel high performance digital to analog converter (DAC) with features and performance including the new Hyperstream IV modulator that produces a device that is well suited for all Audiophile and PRO Audio applications.

These features include TDM & SPI support as well as a Hardware (HW) mode for simplifying configuration of the ES9027PRO.

TDM / I2S / LJ / RJ / DSD / DoP & S/PDIF interfaces are supported.

Sample rates up to 768kHz with PCM data and DSD rates up to DSD1024 are supported. 7 selectable build-in digital filters are also available.

Configuration Modes

The ES9027PRO has 4 control programming modes. They are controlled by the state of the MODE (pin 17):

MODE PIN	Configuration
0	I²C interface
Pull Low	HW control mode (see Hardware Mode Table)
Pull High	HW control mode (see Hardware Mode Table)
1	SPI interface

Software Mode

ES9027PRO supports both I²C or SPI serial communication to configure the registers. There are two types of registers, read/write registers and read-only registers.

See below for the pin connection for each one:

I²C

- MODE (Pin 17) – ***GND***
- Connect per I²C standard
  - SDA (Pin 15)
  - SCL (Pin 16)
  - ADDR0 (Pin 31)
  - ADDR1 (Pin 30)

Table 1 - I2C address configurations

I2C Address	ADDR1	ADDR0
0x90	***GND***	***GND***
0x92	***GND***	***AVDD***
0x94	***AVDD***	***GND***
0x96	***AVDD***	***AVDD***

SPI

- Mode (Pin 17) – **AVDD**
- Connect per SPI standard
  - MOSI (Pin 15)
  - SCLK (Pin 16)
  - SS (Pin 30)
  - MISO (Pin 31)

Table 2 - SPI commands

SPI command	First byte
Write	***3***
Read	***1***

Hardware Mode

The ES9027PRO has 32 pre-configured modes that can be set with external pin configuration. These modes configure the DAC for different input serial data rates and set the DAC muting.

These modes are set with pins:

- MODE (Pin 17)
- HW0 (Pin 15)
- HW1 (Pin 16)
- HW2 (Pin 30)
- MUTE_CTRL (Pin 31)

Each hardware mode pin has 4 states:

- 0 – Pin directly connected to GND
- 1 – Pin directly connected to AVDD
- Pull 0 – Pin pulled to GND through 47kΩ resistor
- Pull 1 – Pin pulled to AVDD through 47kΩ resistor

Design Information

Each hardware mode pin can be configured with either a pull-up or pull-down resistor. Therefore, it is important that the pin is configured to allow for the desired hardware modes. Some guidelines include the following:

- The HW0 and HW1 pins never require a pull up or pull-down resistor.

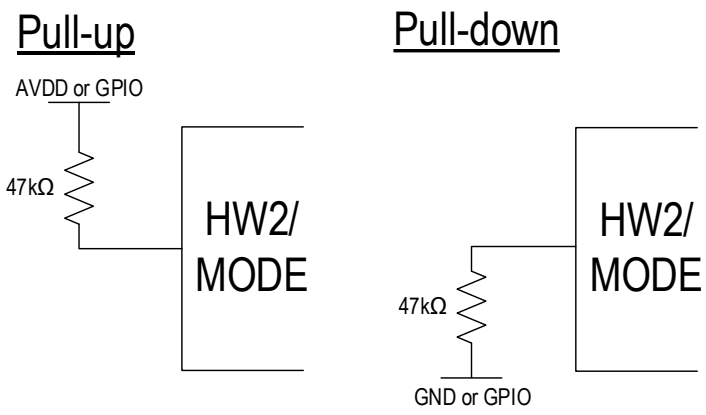


Figure 2 – Hardware mode pin configurations

Muting

MUTE_CTRL (Pin 31) is used to control the muting of the output and enabling of the Automute feature while in Hardware Mode:

- 0 – Output Muted, No Automute
- 1 – Output Unmuted, No Automute
- Pull 0 – Output Muted, Automute Enabled
- Pull 1 – Output Unmuted, Automute Enabled

Hardware Mode Pin Configurations

HW Mode	FS (kHz)	BCK (MHz)	MCLK (MHz)	BCK/Channel	MODE	HW2	HW1	HW0
	I2S Master Mode							
0	MCLK / 128	MCLK / 2	5 < MCLK < 50	32	Pull 0	0	0	0
1	MCLK / 256	MCLK / 4	5 < MCLK < 50	32	Pull 0	0	0	1
2	MCLK / 512	MCLK / 8	5 < MCLK < 50	32	Pull 0	0	1	0
3	MCLK / 1024	MCLK / 16	5 < MCLK < 50	32	Pull 0	0	1	1
	LJ Master Mode							
4	MCLK / 128	MCLK / 2	5 < MCLK < 50	32	Pull 0	Pull 0	0	0
5	MCLK / 256	MCLK / 4	5 < MCLK < 50	32	Pull 0	Pull 0	0	1
6	MCLK / 512	MCLK / 8	5 < MCLK < 50	32	Pull 0	Pull 0	1	0
7	MCLK / 1024	MCLK / 16	5 < MCLK < 50	32	Pull 0	Pull 0	1	1
	I2S Slave SYNC, Auto Detect FS & BCK, MCLK/1							
8	Auto (8 < FS < 384)	64FS	128FS < MCLK < 50	32	Pull 0	Pull 1	0	0
	I2S Slave SYNC, Auto Detect FS & BCK, MCLK/2							
9	Auto (8 < FS < 192)	64FS	128FS < MCLK < 50	32	Pull 0	Pull 1	0	1
	I2S Slave SYNC, Auto Detect FS & BCK, MCLK/4							
10	Auto (8 < FS < 96)	64FS	128FS < MCLK < 50	32	Pull 0	Pull 1	1	0
	I2S Slave SYNC, Auto Clock Gear (128FS), Auto Detect FS & BCK							
11	Auto (8 < FS < 384)	64FS	128FS < MCLK < 50	32	Pull 0	Pull 1	1	1
	LJ Slave SYNC, Auto Detect FS & BCK, MCLK/1							
12	Auto (8 < FS < 384)	64FS	128FS < MCLK < 50	32	Pull 0	1	0	0
	LJ Slave SYNC, Auto Detect FS & BCK, MCLK/2							
13	Auto (8 < FS < 192)	64FS	128FS < MCLK < 50	32	Pull 0	1	0	1
	LJ Slave SYNC, Auto Detect FS & BCK, MCLK/4							
14	Auto (8 < FS < 96)	64FS	128FS < MCLK < 50	32	Pull 0	1	1	0
	LJ Slave SYNC, Auto Clock Gear (128FS), Auto Detect FS & BCK							
15	Auto (8 < FS < 384)	64FS	128FS < MCLK < 50	32	Pull 0	1	1	1
	S/PDIF, DoP, or I2S Slave ASYNC, Auto Detect, MCLK/1							
16**	Auto (8 < FS < 384)	64FS	130FS < MCLK < 50	32	Pull 1	0	0	0
	S/PDIF, DoP, or I2S Slave ASYNC, Auto Detect, MCLK/2							
17**	Auto (8 < FS < 192)	64FS	130FS < MCLK < 50	32	Pull 1	0	0	1
	S/PDIF, DoP, or I2S Slave ASYNC, Auto Detect, MCLK/4							
18**	Auto (8 < FS < 96)	64FS	130FS < MCLK < 50	32	Pull 1	0	1	0
	I2S Slave ASYNC, Auto Clock Gear (>130FS), Auto Detect							
19	Auto (8 < FS < 384)	64FS	130FS < MCLK < 50	32	Pull 1	0	1	1
	LJ Slave ASYNC, Auto Detect, MCLK/1							
20	Auto (8 < FS < 384)	64FS	130FS < MCLK < 50	32	Pull 1	Pull 0	0	0

	LJ Slave ASYNC, Auto Detect, MCLK/2							
21	Auto (8 < FS < 192)	64FS	130FS < MCLK < 50	32	Pull 1	Pull 0	0	1
	LJ Slave ASYNC, Auto Detect, MCLK/4							
22	Auto (8 < FS < 96)	64FS	130FS < MCLK < 50	32	Pull 1	Pull 0	1	0
	LJ Slave ASYNC, Auto Clock Gear, Auto Detect							
23	Auto (8 < FS < 384)	64FS	130FS < MCLK < 50	32	Pull 1	Pull 0	1	1
	DSD Slave, SYNC, Auto Detect							
24	64FS	64FS	128FS < MCLK < 50	--	Pull 1	Pull 1	0	0
	DSD Slave, SYNC, Auto Clock Gear, Auto Detect							
25	64FS	64FS	128FS < MCLK < 50	--	Pull 1	Pull 1	0	1
	DSD Slave, ASYNC, Auto FS							
26	64FS	64FS	130FS < MCLK < 50	--	Pull 1	Pull 1	1	0
	DSD Slave, ASYNC, Auto Clock Gear, Auto FS							
27	64FS	64FS	130FS < MCLK < 50	--	Pull 1	Pull 1	1	1
	TDM Left Justified, Slave, SYNC, Auto Detect							
28*	Auto (8 < FS < 192)	Auto (256FS,512FS, 1024FS)	128FS < MCLK < 50	32	Pull 1	1	0	0
29*	Auto (8 < FS < 96)	Auto (512FS, 1024FS)	128FS < MCLK < 50	32	Pull 1	1	0	1
30*	Auto (8 < FS < 48)	Auto (1024FS)	128FS < MCLK < 50	32	Pull 1	1	1	0
31*	Auto (8 < FS < 48)	Auto 1024FS)	128FS < MCLK < 50	32	Pull 1	1	1	1

*Note: Mode 28 = Channel Slots 1 to 8, Mode 29 = Channel Slots 9 to 16, Mode 30 = Channel slots 17 to 24, Mode 31 = Channel slots 25 to 32.
** Note 2 If DoP is required, HW modes 16-18 must be used, see Hardware Mode Input Datatypes Compatibility table

Recommended Hardware Mode Setup Sequence

The hardware mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted.

Note: It is recommended that MUTE_CTRL is set low until the HW mode is finalized and after CHIP_EN is asserted, then asserted last.

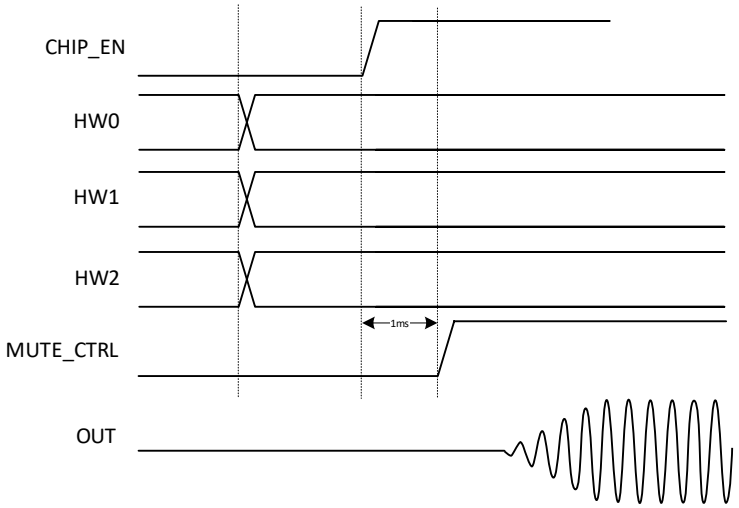


Figure 3 - Hardware mode startup sequence

Hardware Mode Input Datatypes Compatibility

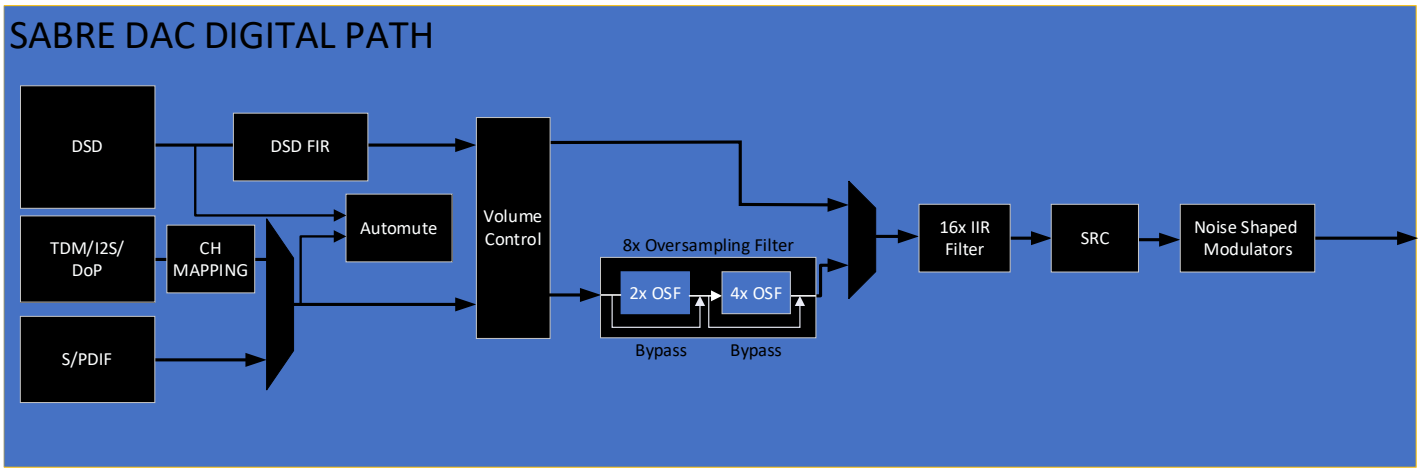
	Input Datatype						
Hardware Modes	I2S	LJ	RJ	TDM	DOP	DSD	S/PDIF
Software Mode	✓	✓	✓	✓	✓	✓	✓
HW 0-3	✓						
HW 4-7		✓					
HW 8-11	✓						
HW 12-15		✓					
HW 16-18	✓				✓		✓
HW 19	✓						
HW 20-23		✓					
HW 24-27						✓	
HW 28-31				✓			

Hardware Mode Features

	Input HW Mode Features				
Hardware Modes	AUTO_FS_DETECT	AUTO_CH_NUM	AUTO_INPUT_SEL	SYNC mode	ASYNC mode
Equivalent Software Mode	Reg 3[7]	Reg 57[7]	Reg57[0]	Reg1[6]	Reg1[6]
HW 0-15	✓			✓	
HW 16-18			✓		✓
HW 19-23					✓
HW 24-25	✓			✓	
HW 26-27					✓
HW 28-31	✓	✓		✓	

Digital Features

Digital Signal Path



Note: Channel Mapping is only available with the TDM/I2S & DoP interface.

GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	Analog Shutdown*	N/A
1	1'b0	Output
2	1'b1	Output
3	CLK_IDAC	Output
4	Interrupt	Output
5	Mute all channel	Input
6	Input Selection	Input
7	Lock status	Output
8	CLK_VALID flag	Output
9	PWM1	Output
10	PWM2	Output
11	PWM3	Output
12	Volume min	Output
13	Automute status	Output
14	Soft Ramp finished	Output
15	Reserved	Output

Table 3 – Standard GPIO Functions

For GPIO_CONFIG 0:

*Analog Shutdown is input disabled, output is tri-stated

GPIOx Default states:

GPIO1: Automute Status

GPIO3-8: Analog Shutdown

GPIO2: GPIO_CONFIG = 7

Audio Input Formats

For configuring PCM, TDM, DSD, or S/PDIF, use Registers 57-71

PCM (subset of TDM interface)

Data is organized as 2 channels per data line. Any channel on any data line can be mapped to any DAC through the TDM_CHx_CONFIG channel mapping Registers 64-71. Data is latched on the positive edge of BCLK.

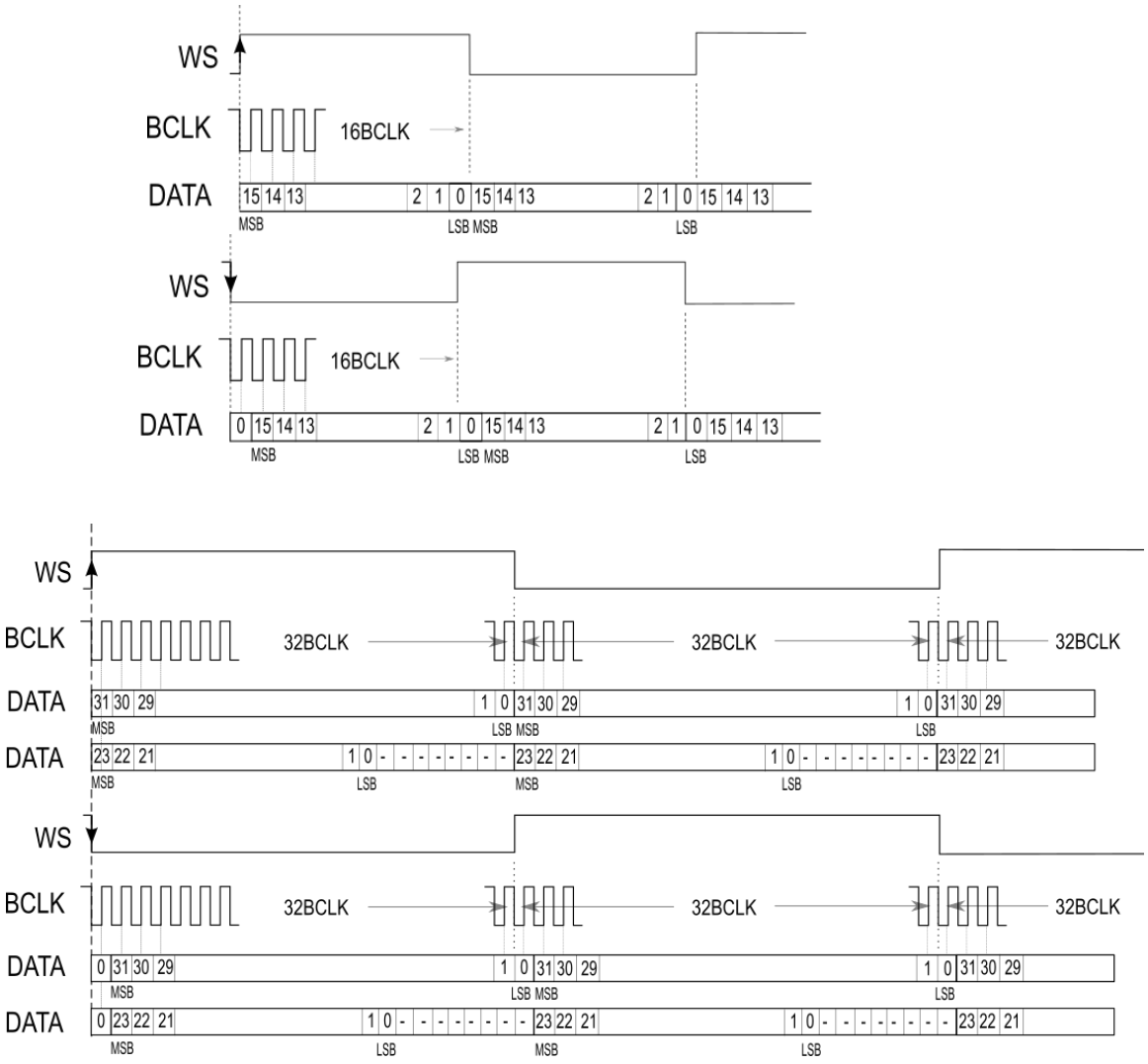


Figure 4 – I2S & LJ Input for 16bit and 32bit word depths

Time-division multiplexing (TDM)

ES9027PRO supports time-division multiplexing (TDM) format, allowing more than 2 channels (or slots) to be transmitted on each data line, up to a maximum of 32 channels per data line. Typical formats are TDM128 (4chx32bit), TDM256 (8chx32bit), TDM512 (16chx32bit) and TDM1024 (32chx32bit). In this mode, the TDM_CHx_CONFIG channel mapping Registers 64-71 can be used to internally map any slot (channel) to any DAC. Data is latched on the positive edge of BCLK.

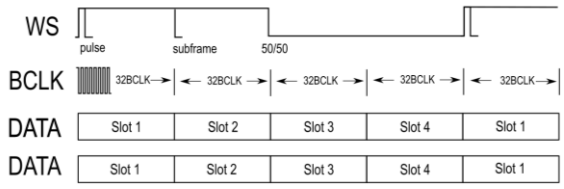


Figure 5 – TDM128 mode

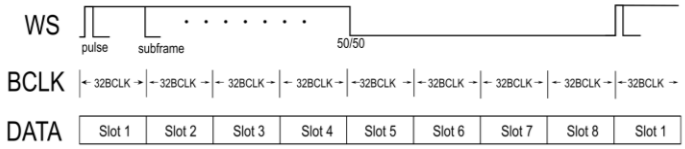


Figure 6 – TDM256 mode

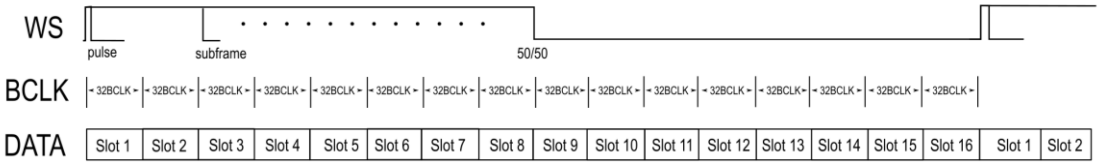


Figure 7 – TDM512 mode

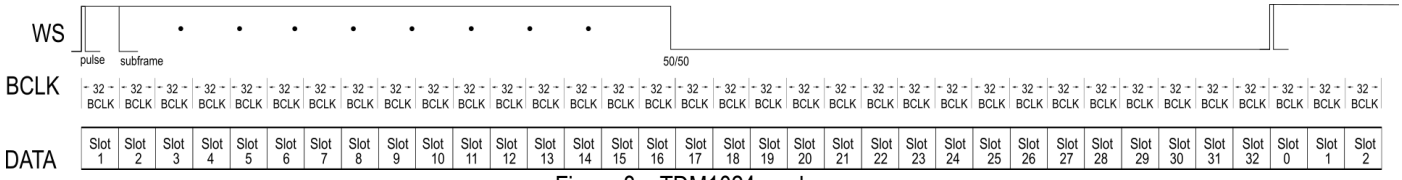


Figure 8 – TDM1024 mode

DSD[1]

In DSD mode, there is a single DSD clock line, and each channel of data is an additional DSD data line. There is no internal channel mapping for DSD input, DSD data input to DATA1 is sent to Ch1, DSD data input to DATA2 is sent to Ch2, etc. For 4 channel and 2 channel applications, the interpolation path data can be copied from DAC1+DAC2 to the other DAC pairs, see Register 0[6:3] for details.

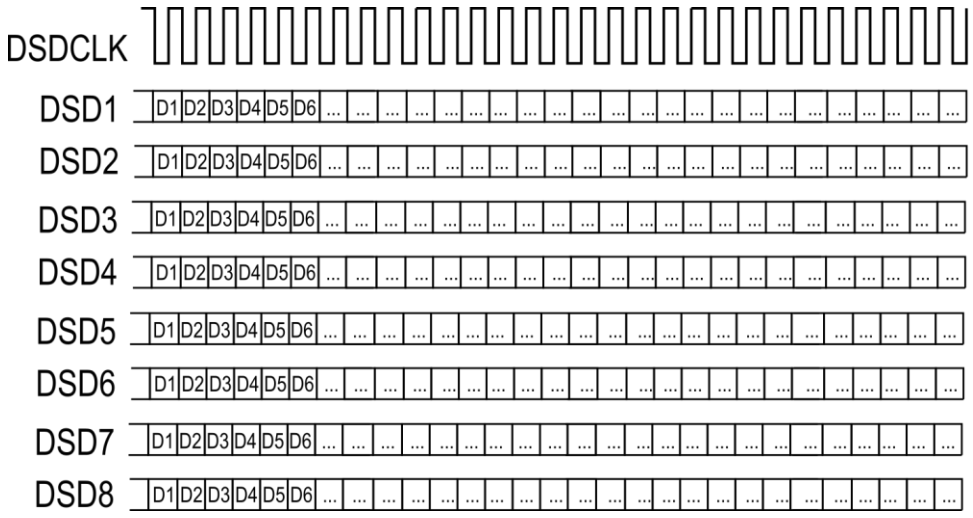


Figure 9 – DSD format, 1bit stream

S/PDIF

S/PDIF is transmitted over a single signal line using dual phase encoded data, which allows for clock extraction from the data signal line. In S/PDIF mode, there is only stereo data input. Channel 1 data will be sent to all odd channel DACs, Channel 2 data will be sent to all even channel DACs.

[1] The Automute Feature is not available when using DSD mode

Pre-Programmed Digital Filters

The ES9027PRO has 7 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 88[2:0] for configuration). The 7 filters are:

- Minimum Phase (default)
- Linear Phase Apodizing
- Linear Phase Fast Roll-off
- Linear Phase Slow Roll-off
- Minimum Phase Fast Roll-off
- Minimum Phase Slow Roll-off
- Minimum Phase Slow Roll-off Low Dispersion

PCM Filter Properties (48kHz Sampling)

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.49 x fs	Hz
Stop band	-97dB	0.55 x fs			Hz
Group Delay		3.29/fs		9.37/fs	s
Flatness (ripple)	0.0004				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.44 x fs	Hz
Stop band	-107dB	0.5 x fs			Hz
Group Delay			33.2/fs		s
Flatness (ripple)	0.0017				dB

Linear Phase Fast Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.49 x fs	Hz
Stop band	-118dB	0.55 x fs			Hz
Group Delay			33.8/fs		s
Flatness (ripple)	0.0023				dB

Linear Phase Slow Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.44 x fs	Hz
Stop band	-84dB	0.74 x fs			Hz
Group Delay			5.62/fs		s
Flatness (ripple)	0.002				dB

Minimum Phase Fast Roll-off					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	–3dB			0.48 x fs	Hz
Stop band	-99dB	0.55 x fs			Hz
Group Delay		3.29/fs		9.51/fs	s
Flatness (ripple)	0.0016				dB

Minimum Phase Slow Roll-off					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	–3dB			0.43 x fs	Hz
Stop band	-84dB	0.79 x fs			Hz
Group Delay		2.5/fs		3/fs	s
Flatness (ripple)	0.0035				dB

Minimum Phase Slow Roll-off Low Dispersion					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	–3dB			0.43 x fs	Hz
Stop band	-84dB	0.79 x fs			Hz
Group Delay		9.7/fs		9.9/fs	s
Flatness (ripple)	0.0053				dB

PCM Filter Latency

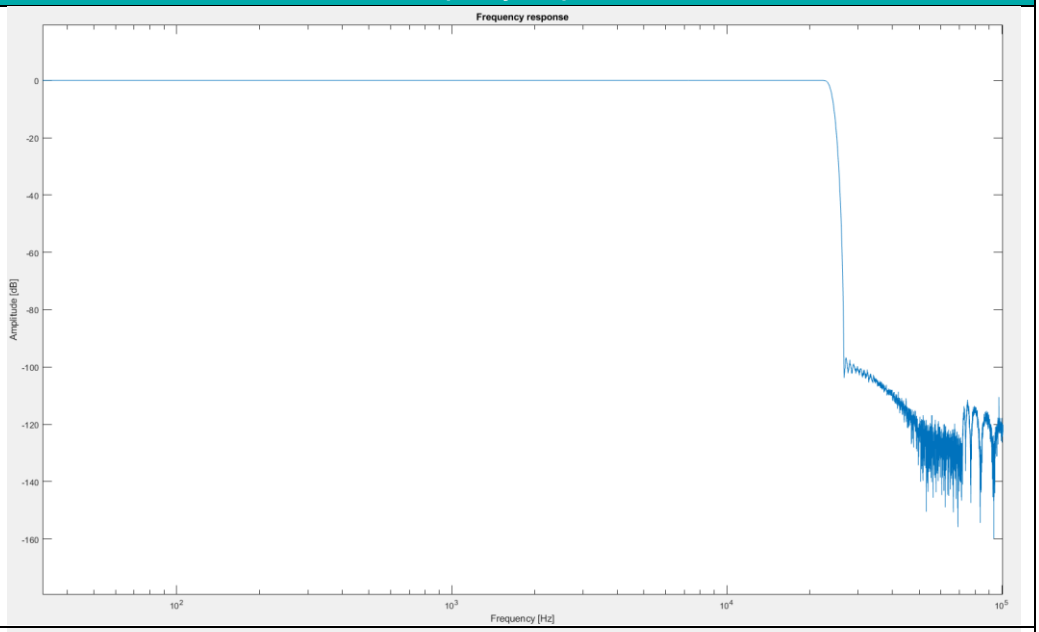
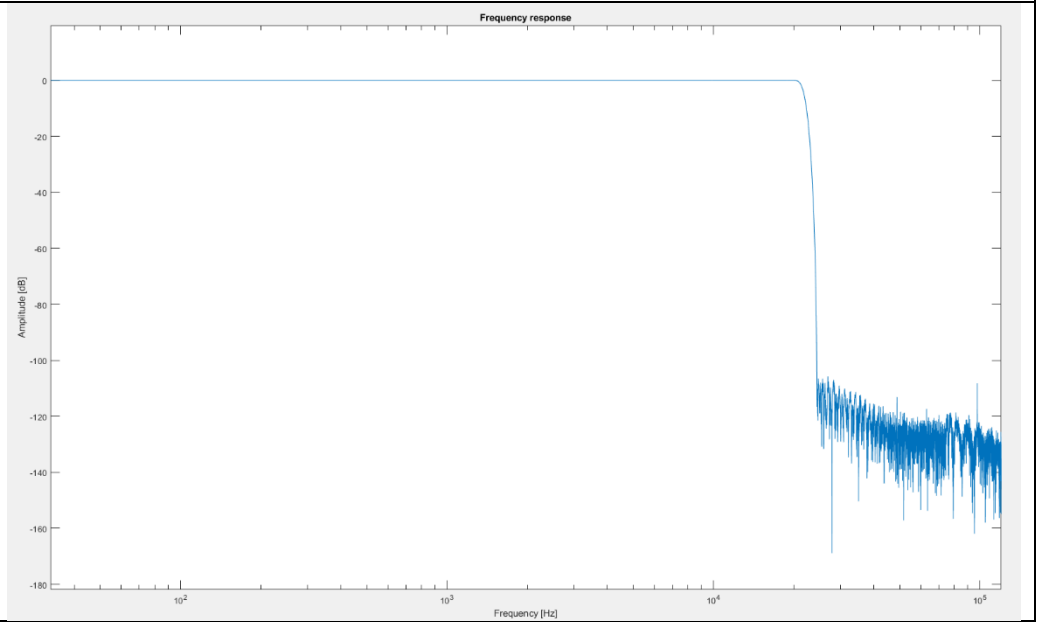
The following table shows the simulated latency of each filter at 48kHz sampling rate. Latency delay will reduce (scale) with sampling rate.

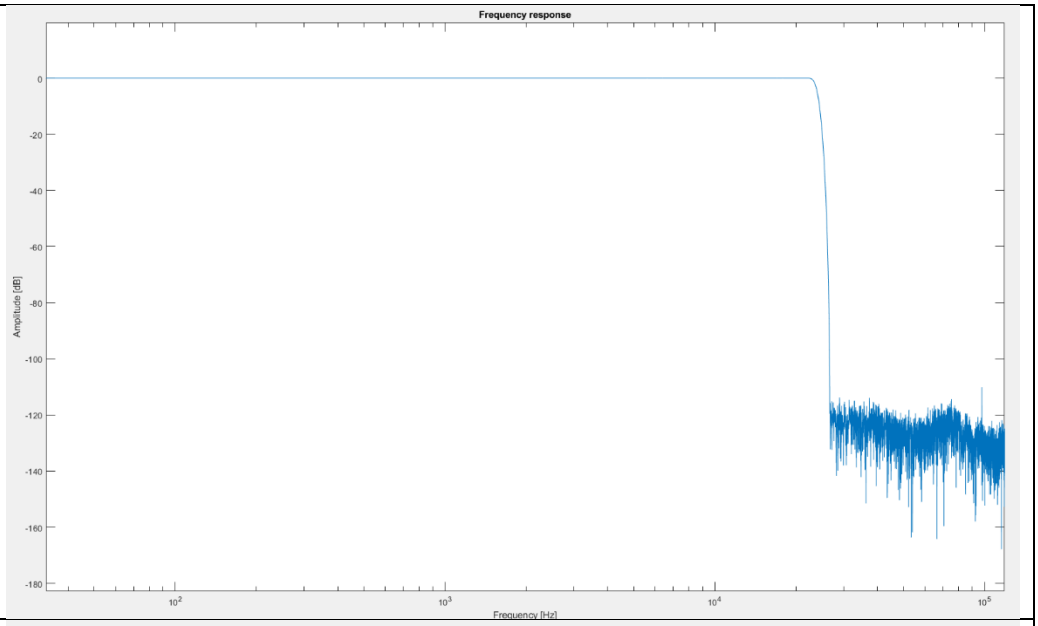
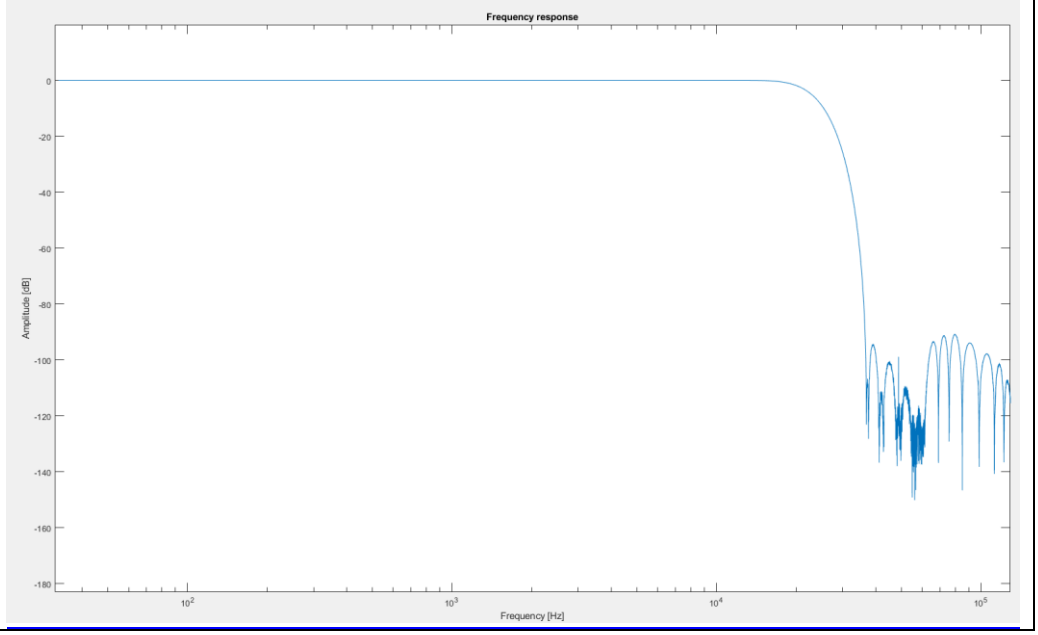
Digital Filter	Delay(us) @ fs=48kHz
Minimum phase (default)	158us
Linear Phase Apodizing	760us
Linear Phase Fast Roll-Off	771us
Linear Phase Slow Roll-Off	208us
Minimum Phase fast roll-off	158us
Minimum Phase slow roll-off	137us
Minimum Phase Slow roll-off low dispersion	282us

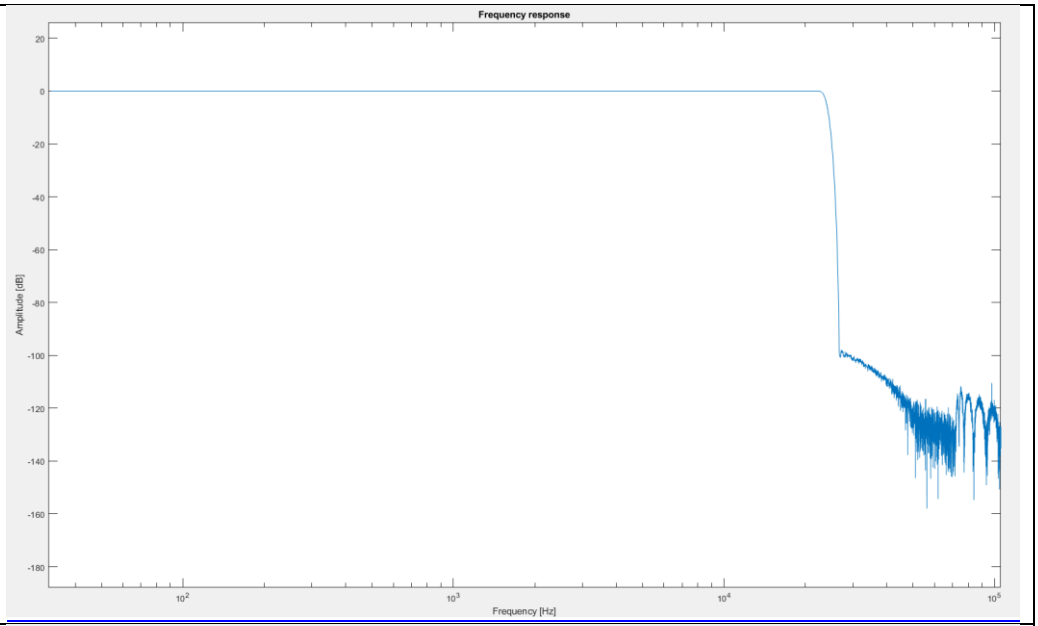
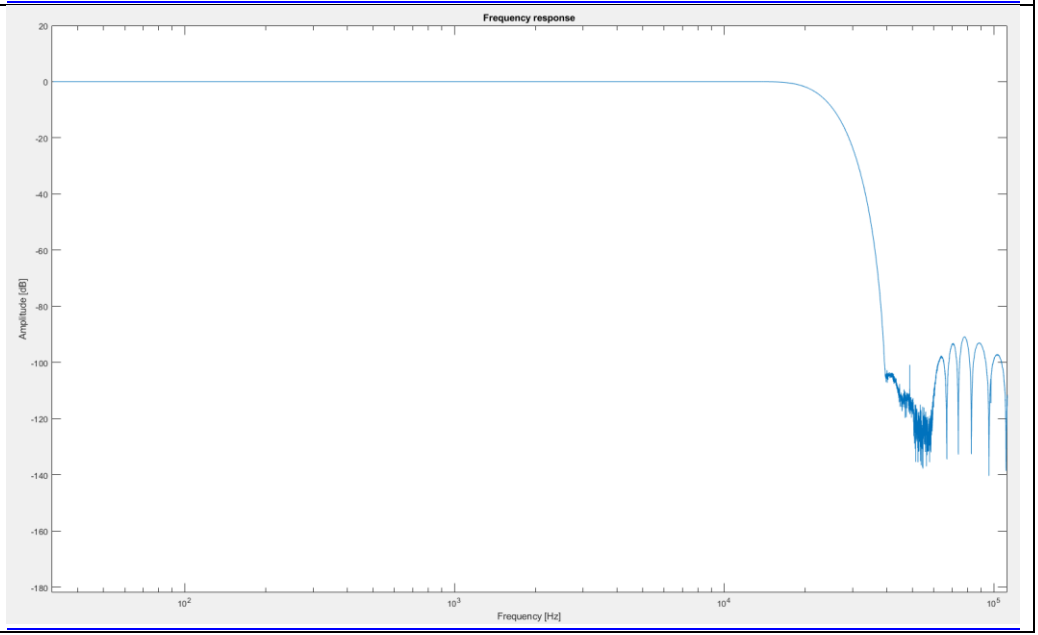
Table 4 – Latency of Pre-Programmed Digital Filters

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 48kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-off	
Linear Phase Slow Roll-off	

Minimum Phase Fast Roll-off	
Minimum Phase Slow Roll-off	

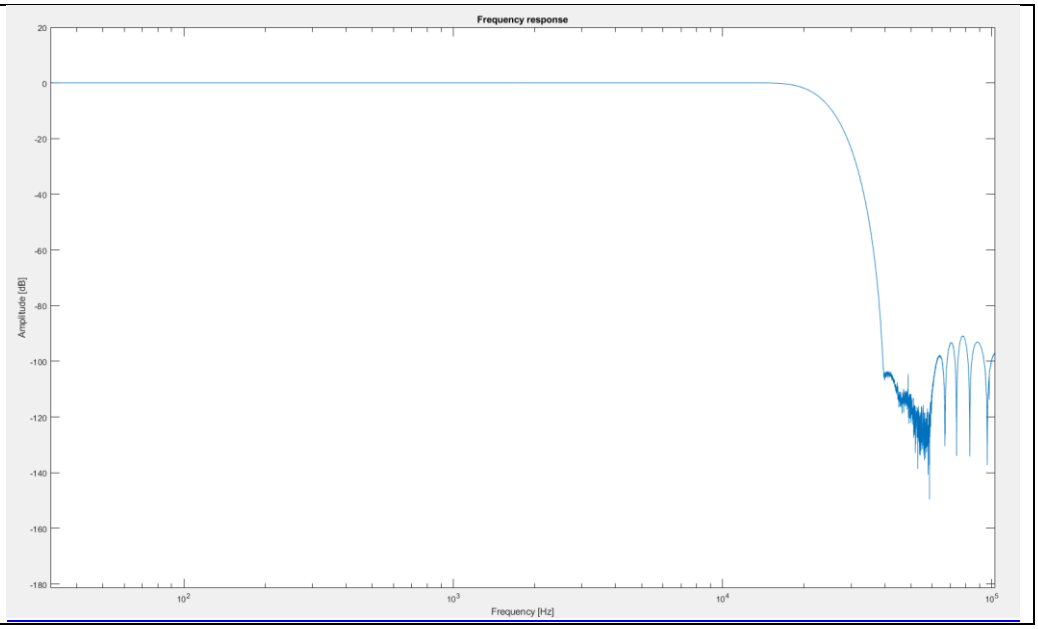
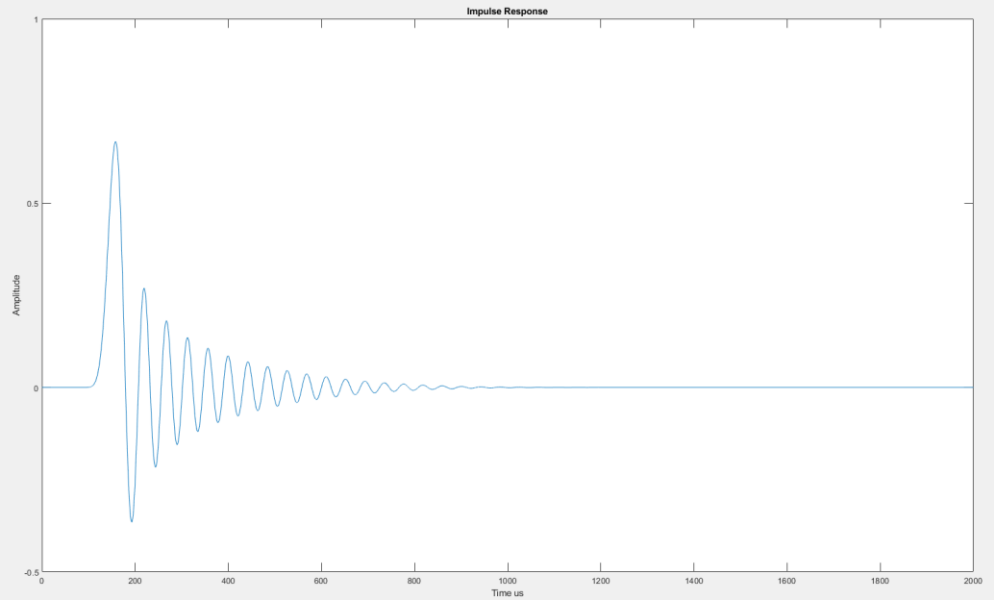
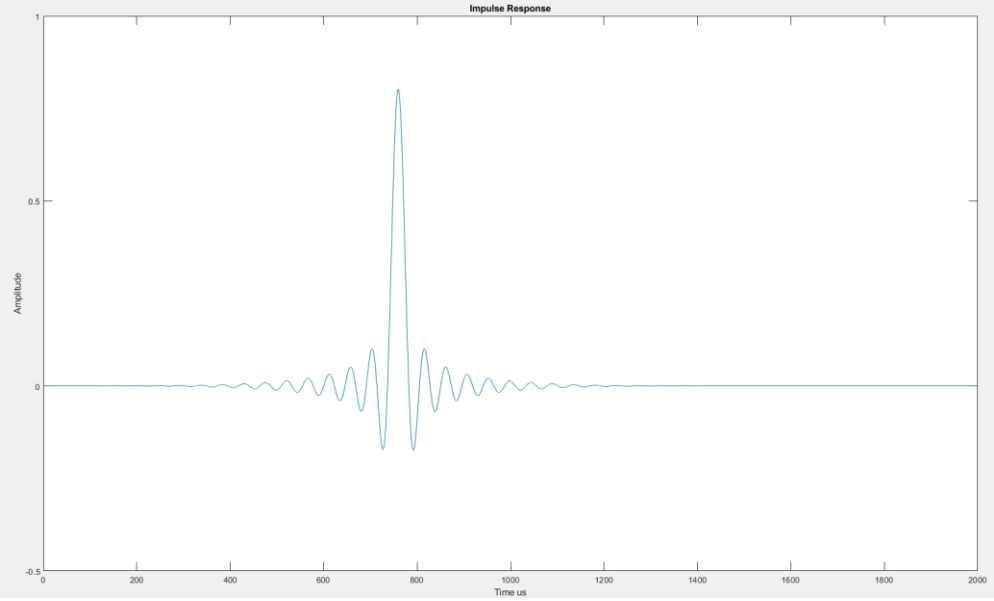
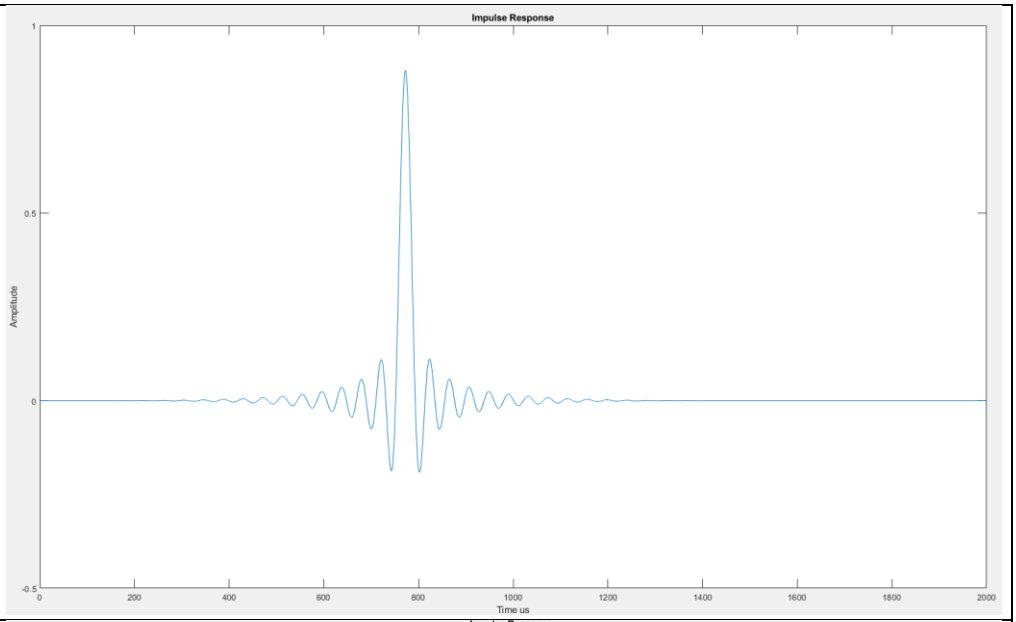
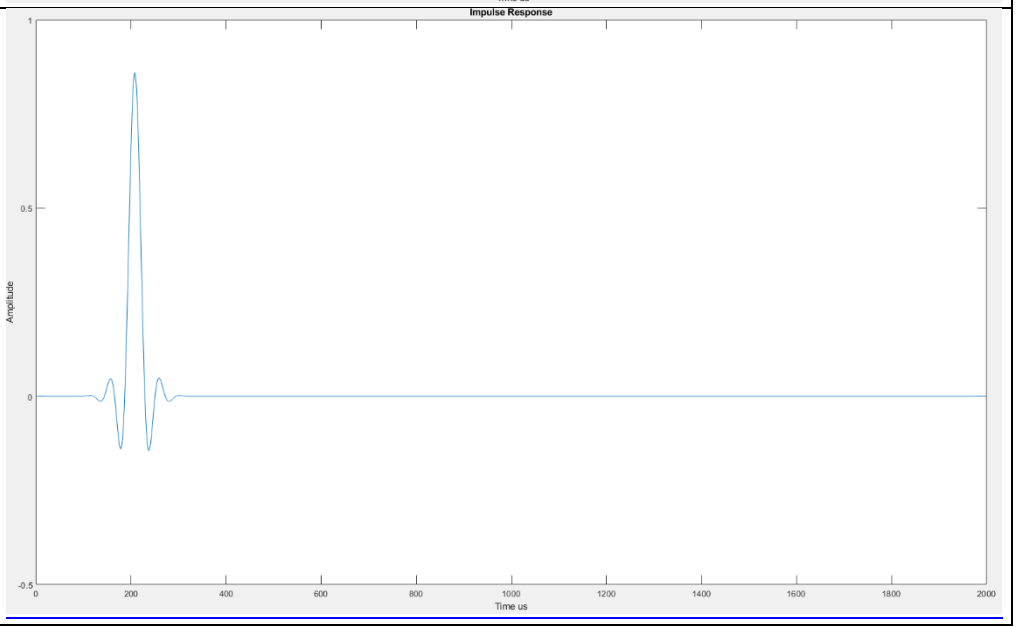
Minimum Phase Slow Roll-off Low Dispersion	

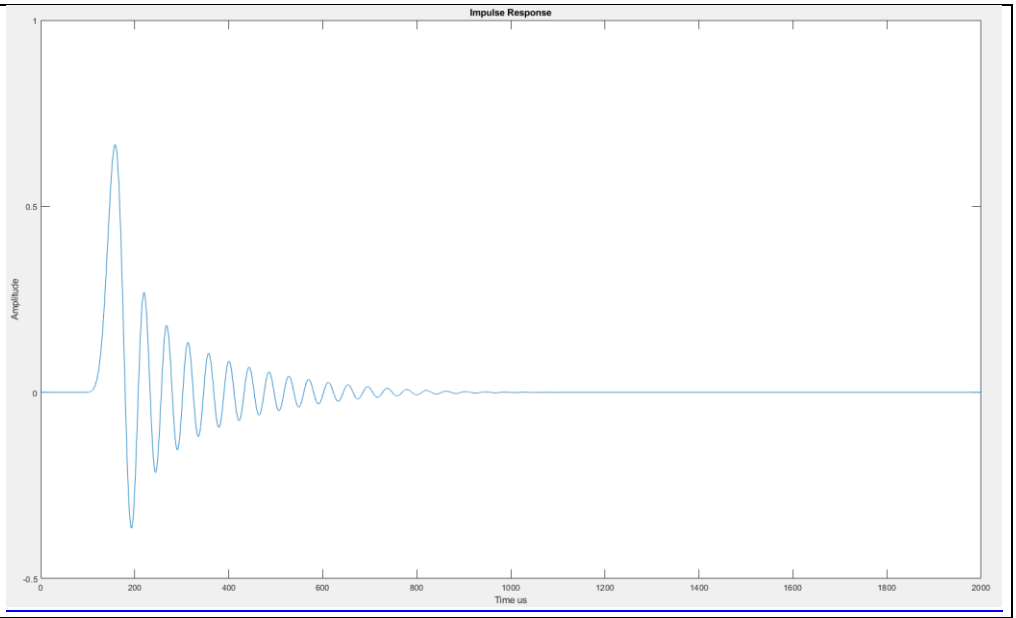
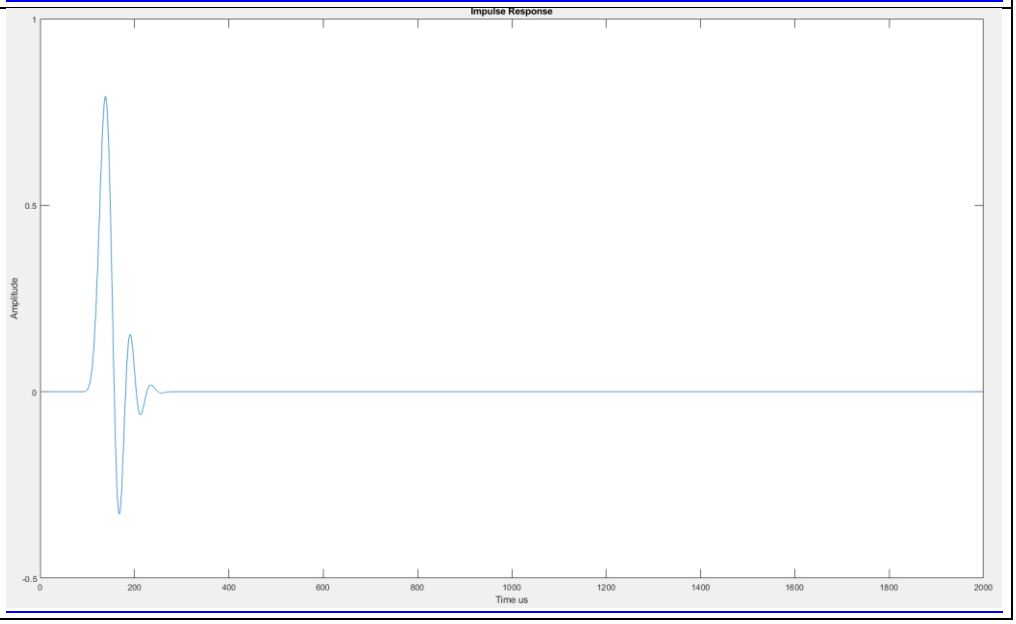
Table 5 - Frequency response of PCM filters

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. Simulation sample rate is 48kHz.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-off	
Linear Phase slow roll-off	

Minimum phase fast roll-off	
Minimum phase slow roll-off	

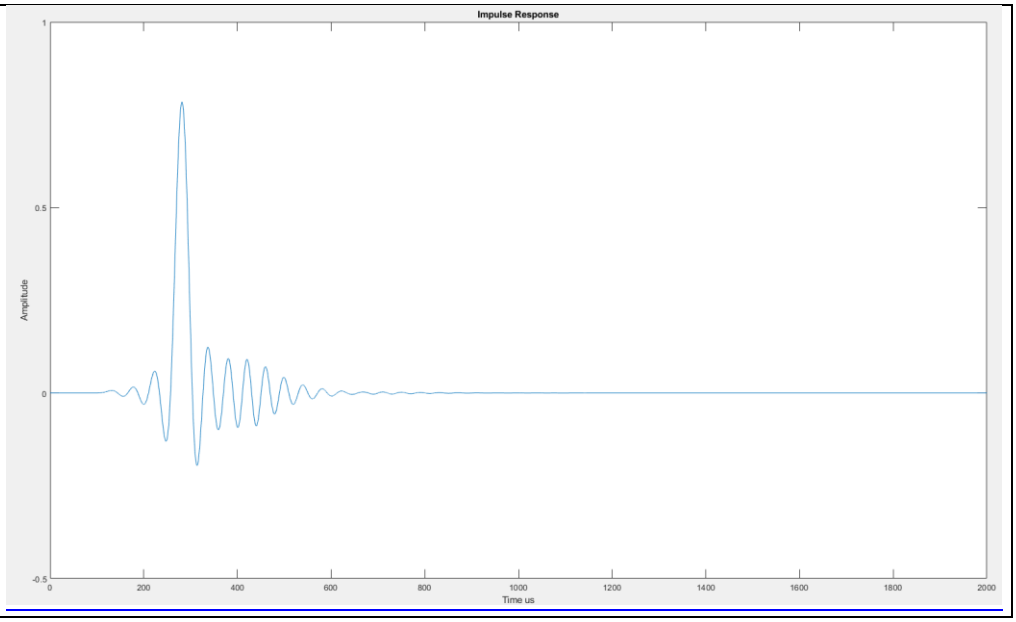
Minimum phase slow roll-off low dispersion	

Table 6 - Impulse response of PCM filters

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_L • AVCC_R • AVDD • VCCA • DVDD	 • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +1.4V with respect to Ground
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD(nom)+0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 TBD TBD

Table 7 – Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	(AVDD / 2) + 0.4		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	AVDD – 0.2		V	
Low-level output voltage	VOL		0.2	V	

Table 8 – IO electrical characteristics

Recommended Operating Conditions

There are the recommended operating conditions for the ES9027PRO

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	–20°C to +85°C
AVCC_L		3.3V
AVCC_R		3.3V
AVDD		3.3V
VCCA		3.3V
DVDD		1.2V

Table 9 – Recommended operating conditions

Power Consumption

Power numbers are given when the device is in slave mode.

Test Condition 0 Standby

Standby (CHIP_EN = 0)					
AVCC			***<1***		uA
AVDD			***<1***		uA
VCCA			***<1***		uA

Test Condition 1 (unless otherwise noted)
T_A = 25°C, AVCC_R = AVCC_L = VCCA = AVDD = **+3.3V**, DVDD= **+1.2V,** fs = **48kHz**, DAC enabled, 1kHz sine full scale

Parameter	Min	Typ	Max	Unit
Hardware Mode: 3 (MCLK = 49.152MHz) MCLK/1				
AVCC_R		22.1		mA
AVCC_L		22.1		mA
VCCA		1.2		mA
AVDD		2.1		mA
DVDD		32.0		mA
Power Consumption		**197**		**mW**
Hardware Mode: 0 (MCLK = 6.144MHz) MCLK/1				
AVCC_R		13.6		mA
AVCC_L		13.6		mA
VCCA		0.2		mA
AVDD		2.1		mA
DVDD		10.3		mA
Power Consumption		**110**		**mW**
Hardware Mode: 19 (MCLK = 50MHz) Auto Clock Gear				
AVCC_R		14.9		mA
AVCC_L		14.9		mA
VCCA		0.5		mA
AVDD		0.3		mA
DVDD		17.9		mA
Power Consumption		**123**		**mW**

Table 10 – Power consumption with test conditions 1

Test Condition 2 (unless otherwise noted)
T_A = 25°C, AVCC_R = AVCC_L = VCCA = AVDD = **+3.3V**, DVDD= **+1.2V**, fs = **48kHz**, DAC enabled, streaming zeros, automute enabled

Parameter	Min	Typ	Max	Unit
Hardware Mode: 3 (MCLK = 49.152MHz) MCLK/1				
AVCC_R		9.2		mA
AVCC_L		9.2		mA
VCCA		1.2		mA
AVDD		2.2		mA
DVDD		18.4		mA
Power Consumption		**95**		**mW**
Hardware Mode: 0 (MCLK = 6.144MHz) MCLK/1				
AVCC_R		1.6		mA
AVCC_L		1.6		mA
VCCA		0.6		mA
AVDD		2.1		mA
DVDD		4.3		mA
Power Consumption		**24**		**mW**
Hardware Mode: 19 (MCLK = 50MHz) Auto Clock Gear				
AVCC_R		2.8		mA
AVCC_L		2.8		mA
VCCA		0.4		mA
AVDD		0.4		mA
DVDD		9.0		mA
Power Consumption		**32**		**mW**

Table 11 – Power consumption with test conditions 2

Performance

Test Conditions 1 (unless otherwise noted)
T_A = 25°C, AVCC_R = AVCC_L = VCCA = AVDD = **+3.3V**, DVDD= **+1.2V**, fs = **48kHz, HW mode 3** (I2S Master Mode), MCLK = 49.152MHz

Note: Performance numbers were measured using the ESS evaluation board v1.0

Parameter		Min	Typ	Max	Unit
Resolution			32		Bit
Max MCLK frequency				50	MHz
THD+N Ratio / THD Ratio @ fs=48kHz (differential)	0dBFS, BW=20Hz-20kHz		-114 / -118		dB
THD+N Ratio / THD Ratio @ fs=96kHz (differential)	0dBFS, BW=20Hz-40kHz		-112 / -118		dB
THD+N Ratio / THD Ratio @ fs=192kHz (differential)	0dBFS, BW=20Hz-80kHz		-110 / -118		dB
THD+N Ratio / THD Ratio @ fs=384kHz (differential)	0dBFS, BW=20Hz-160kHz		-108 / -118		dB
DNR (A-weighted) (8 Channel mode – Single Channel diff)	-60dBFS		124		dB
DNR (A-weighted) (Stereo mode – 4 channel sum diff)			128		dB
DNR (A-weighted) (Mono mode – 8 channel sum diff)			130		dB
Voltage output amplitude	Full-scale out		0.886 x AVCC		Vpp
Voltage output offset	Bipolar zero out		AVCC/2		V
Current output amplitude	Full-scale out		1000 x 0.886 x AVCC / Rdac		mApp
Current output offsets	Bipolar zero out		1000 x (AVCC/2 – Vg) / Rdac		mA
Output Impedance (R_{DAC}) (Per + or – pin of each differential DAC output pair)			760±15%		ohm

Table 12 – Performance data

Timing Requirements

I²C Slave Interface Timing

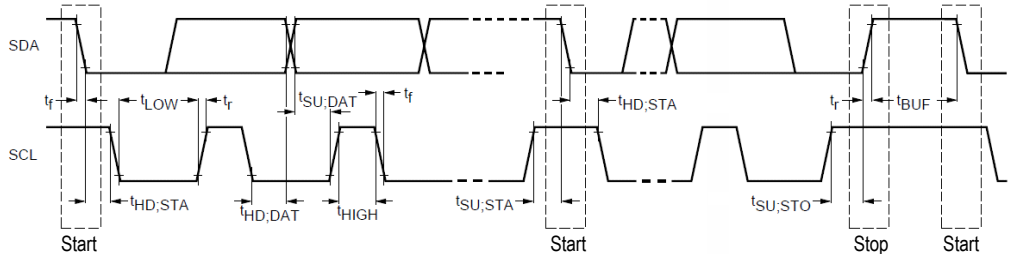


Figure 10 – I²C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 13 – I2C slave/synchronous slave interface timing definitions

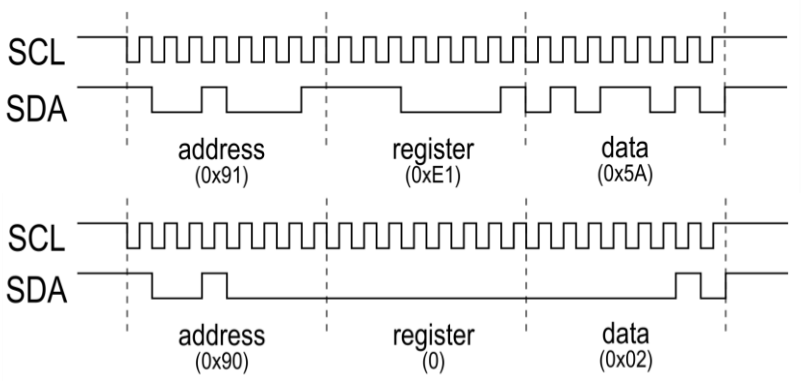


Figure 11 – I²C single byte examples of read and write instructions with I²C

SPI Slave Interface

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data

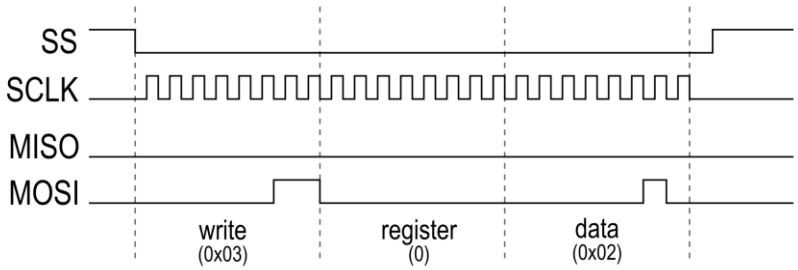


Figure 12 – SPI single byte write

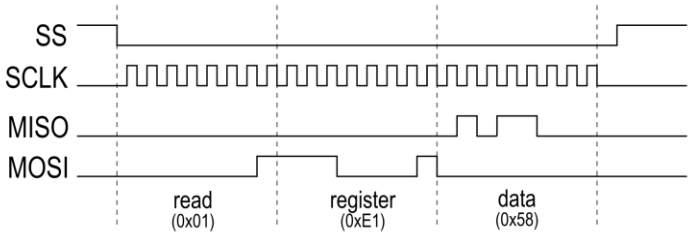


Figure 13 – SPI single byte read

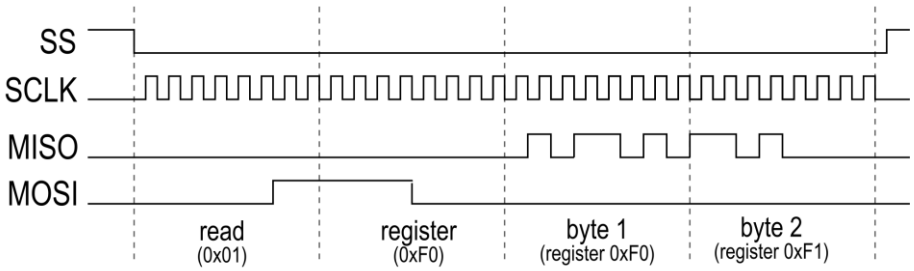


Figure 14 – SPI multi-byte read

Register Overview

ES9027PRO contains read/write and read-only registers. A system clock must be present to access registers.

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Read/Write Register Addresses

Registers 0-141 (0x00 – 0x8D) are read/write registers

Read-only Register Addresses

Register 224-245 (0xE0 – 0xF5) are read registers

Multi-Byte Registers

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.
MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYSTEM CONFIG	SOFT_RESET	ENABLE_64FS_ MODE	CH78_SEL		CH56_SEL	CH34_SEL	DAC_ MODE_REG	RESERVED
0x01	1	SYS MODE CONFIG	ENABLE_DAC	SYNC_MODE	RESERVED		ENABLE_SPDIF _DECODE	ENABLE_DOP_ DECODE	ENABLE_DSD_ DECODE	ENABLE_TDM_ DECODE
0x02	2	RESERVED	RESERVED							
0x03	3	DAC CLOCK CONFIG	AUTO_FS_ DETECT	SELECT_ IDAC_HALF	SELECT_IDAC_NUM					
0x04	4	CLOCK CONFIG	MASTER_BCK_DIV							
0x05	5	CLK GEAR SELECT	RESERVED		SEL_CLK_GEAR		RESERVED	AUTO_ CLK_GEAR	RESERVED	
0x06 - 0x09	6 - 9	RESERVED	RESERVED							
0x0A	10	INTERUPT VOL MIN MASK P	VOL_MIN_CH8_ MASKP	VOL_MIN_CH7_ MASKP	VOL_MIN_CH6_ MASKP	VOL_MIN_CH5_ MASKP	VOL_MIN_CH4_ MASKP	VOL_MIN_CH3_ MASKP	VOL_MIN_CH2_ MASKP	VOL_MIN_CH1_ MASKP
0x0B	11	INTERRUPT AUTOMUTE MASKP	AUTOMUTE_ FLAG_CH8_ MASKP	AUTOMUTE_ FLAG_CH7_ MASKP	AUTOMUTE_ FLAG_CH6_ MASKP	AUTOMUTE_ FLAG_CH5_ MASKP	AUTOMUTE_ FLAG_CH4_ MASKP	AUTOMUTE_ FLAG_CH3_ MASKP	AUTOMUTE_ FLAG_CH2_ MASKP	AUTOMUTE_ FLAG_CH1_ MASKP
0x0C	12	SS FULL RAMP MASKP	SS_FULL_ RAMP_CH8_ MASKP	SS_FULL_ RAMP_CH7_ MASKP	SS_FULL_ RAMP_CH6_ MASKP	SS_FULL_ RAMP_CH5_ MASKP	SS_FULL_ RAMP_CH4_ MASKP	SS_FULL_ RAMP_CH3_ MASKP	SS_FULL_ RAMP_CH2_ MASKP	SS_FULL_ RAMP_CH1_ MASKP
0x0D	13	INTERRUPT MASKP	INPUT_SELECT_OVERRIDE_MASKP		TDM_VALID_ EDGE_MASKP	RESERVED			BCK_WS_FAIL_ MASKP	DOP_VALID_ MASKP
0x0E	14	RESERVED	RESERVED							
0x0F	15	INTERUPT VOL MIN MASKN	VOL_MIN_CH8_ MASKN	VOL_MIN_CH7_ MASKN	VOL_MIN_CH6_ MASKN	VOL_MIN_CH5_ MASKN	VOL_MIN_CH4_ MASKN	VOL_MIN_CH3_ MASKN	VOL_MIN_CH2_ MASKN	VOL_MIN_CH1_ MASKN
0x10	16	INTERRUPT AUTOMUTE MASKN	AUTOMUTE_ FLAG_CH8_ MASKN	AUTOMUTE_ FLAG_CH7_ MASKN	AUTOMUTE_ FLAG_CH6_ MASKN	AUTOMUTE_ FLAG_CH5_ MASKN	AUTOMUTE_ FLAG_CH4_ MASKN	AUTOMUTE_ FLAG_CH3_ MASKN	AUTOMUTE_ FLAG_CH2_ MASKN	AUTOMUTE_ FLAG_CH1_ MASKN
0x11	17	INTERRUPT SS FULL RAMP MASKN	SS_FULL_ RAMP_CH8_ MASKN	SS_FULL_ RAMP_CH7_ MASKN	SS_FULL_ RAMP_CH6_ MASKN	SS_FULL_ RAMP_CH5_ MASKN	SS_FULL_ RAMP_CH4_ MASKN	SS_FULL_ RAMP_CH3_ MASKN	SS_FULL_ RAMP_CH2_ MASKN	SS_FULL_ RAMP_CH1_ MASKN
0x12	18	INTERRUPT MASKN	INPUT_SELECT_OVERRIDE_MASKN		TDM_VALID_ EDGE_MASKN	RESERVED			BCK_WS_FAIL_ MASKN	DOP_VALID_ MASKN
0x13	19	RESERVED	RESERVED							
0x14	20	INTERRUPT VOL MIN CLEAR	VOL_MIN_CH8_ CLEAR	VOL_MIN_CH7_ CLEAR	VOL_MIN_CH6_ CLEAR	VOL_MIN_CH5_ CLEAR	VOL_MIN_CH4_ CLEAR	VOL_MIN_CH3_ CLEAR	VOL_MIN_CH2_ CLEAR	VOL_MIN_CH1_ CLEAR
0x15	21	INTERRUPT AUTOMUTE CLEAR	AUTOMUTE_ FLAG_CH8_ CLEAR	AUTOMUTE_ FLAG_CH7_ CLEAR	AUTOMUTE_ FLAG_CH6_ CLEAR	AUTOMUTE_ FLAG_CH5_ CLEAR	AUTOMUTE_ FLAG_CH4_ CLEAR	AUTOMUTE_ FLAG_CH3_ CLEAR	AUTOMUTE_ FLAG_CH2_ CLEAR	AUTOMUTE_ FLAG_CH1_ CLEAR
0x16	22	INTERRUPT SS FULL RAMP CLEAR	SS_FULL_ RAMP_CH8_ CLEAR	SS_FULL_ RAMP_CH7_ CLEAR	SS_FULL_ RAMP_CH6_ CLEAR	SS_FULL_ RAMP_CH5_ CLEAR	SS_FULL_ RAMP_CH4_ CLEAR	SS_FULL_ RAMP_CH3_ CLEAR	SS_FULL_ RAMP_CH2_ CLEAR	SS_FULL_ RAMP_CH1_ CLEAR
0x17	23	INTERRUPT CLEAR	INPUT_SELECT_OVERRIDE_CLEAR		TDM_VALID_ EDGE_CLEAR	RESERVED			BCK_WS_ FAIL_CLEAR	DOP_VALID_ CLEAR
0x18 - 0x1C	24 - 28	RESERVED	RESERVED							
0x1D	29	DPLL BW	DPLL_BW				RESERVED			
0x1E - 0x28	30 - 36	RESERVED	RESERVED							
0x25	37	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x26	38	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x27	39	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x28	40	GPIO7/8 CONFIG	GPIO8_CFG				GPIO7_CFG			
0x29	41	GPIO OUTPUT ENABLE	GPIO8_OE	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x2A	42	GPIO INPUT	GPIO8_SDB	GPIO7_SDB	GPIO6_SDB	GPIO5_SDB	GPIO4_SDB	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB
0x2B	43	GPIO WK EN	GPIO8_WK_EN	GPIO7_WK_EN	GPIO6_WK_EN	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x2C	44	INVERT GPIO	INVERT_GPIO8	INVERT_GPIO7	INVERT_GPIO6	INVERT_GPIO5	INVERT_GPIO4	INVERT_GPIO3	INVERT_GPIO2	INVERT_GPIO1
0x2D	45	GPIO READ	GPIO8_READ	GPIO7_READ	GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x2E	46	GPIO OUTPUT LOGIC	GPIO_SEL		GPIO_OR_ SS_RAMP	GPIO_OR_ VOL_MIN	GPIO_OR_ AUTOMUTE	GPIO_AND_ SS_RAMP	GPIO_AND_ VOL_MIN	GPIO_AND_ AUTOMUTE
0x2F	47		GPIO_ DAC_MODE	RESERVED						GPIO_SEL
0x30	48	PWM1 COUNT	PWM1_COUNT							
0x31	49	PWM1 FREQUENCY	PWM1_FREQ							
0x32	50		PWM1_FREQ							
0x33	51	PWM2 COUNT	PWM2_COUNT							
0x34	52	PWM2 FREQUENCY	PWM2_FREQ							
0x35	53		PWM2_FREQ							
0x36	54	PWM3 COUNT	PWM3_COUNT							
0x37	55	PWM3 FREQUENCY	PWM3_FREQ							
0x38	56		PWM3_FREQ							
0x39	57	INPUT SELECTION	AUTO_ CH_DETECT	ENABLE_ DSD_FAULT_ DETECTION	DSD_MASTER_ MODE	PCM_MASTER_ MODE	RESERVED	INPUT_SEL		AUTO_ INPUT_SEL
0x3A	58	SERIAL MASTER ENCODER CONFIG	TDM_RESYNC	BCK_INV	RESERVED	MASTER_FRAME_LENGTH		MASTER_WS_ PULSE_MODE	MASTER_ WS_INVERT	MASTER_ BCK_INVERT
0x3B	59	TDM CONFIG	RESERVED		TDM_CH_NUM					
0x3C	60	TDM CONFIG1	TDM_LJ_MODE	TDM_ VALID_EDGE	RESERVED					
0x3D	61	TDM CONFIG2	ENABLE_ ASYNC_LOCK_ MONITOR	TDM_BIT_WIDTH	TDM_DATA_LATCH_ADJ					
0x3E	62	BCK/WS MONITOR CONFIG	DISABLE_	DISABLE_	ENABLE_	ENABLE_	DISABLE_	RESERVED		

			DSD_DC	DSD_MUTE	WS_MONITOR	BCK_MONITOR	PCM_DC			
0x3F	63	RESERVED	RESERVED							
0x40	64	TDM CH1 CONFIG	RESERVED	TDM_CH1_LINE_SEL		TDM_CH1_SLOT_SEL				
0x41	65	TDM CH2 CONFIG	RESERVED	TDM_CH2_LINE_SEL		TDM_CH2_SLOT_SEL				
0x42	66	TDM CH3 CONFIG	RESERVED	TDM_CH3_LINE_SEL		TDM_CH3_SLOT_SEL				
0x43	67	TDM CH4 CONFIG	RESERVED	TDM_CH4_LINE_SEL		TDM_CH4_SLOT_SEL				
0x44	68	TDM CH5 CONFIG	RESERVED	TDM_CH5_LINE_SEL		TDM_CH5_SLOT_SEL				
0x45	69	TDM CH6 CONFIG	RESERVED	TDM_CH6_LINE_SEL		TDM_CH6_SLOT_SEL				
0x46	70	TDM CH7 CONFIG	RESERVED	TDM_CH7_LINE_SEL		TDM_CH7_SLOT_SEL				
0x47	71	TDM CH8 CONFIG	RESERVED	TDM_CH8_LINE_SEL		TDM_CH8_SLOT_SEL				
0x48 - 0x49	72 - 73	RESERVED	RESERVED							
0x4A	74	VOLUME1	VOLUME1							
0x4B	75	VOLUME2	VOLUME2							
0x4C	76	VOLUME3	VOLUME3							
0x4D	77	VOLUME4	VOLUME4							
0x4E	78	VOLUME5	VOLUME5							
0x4F	79	VOLUME6	VOLUME6							
0x50	80	VOLUME7	VOLUME7							
0x51	81	VOLUME8	VOLUME8							
0x52	82	DAC VOL UP RATE	DAC_VOL_RATE_UP							
0x53	83	DAC VOL DOWN RATE	DAC_VOL_RATE_DOWN							
0x54	84	DAC VOL DOWN RATE FAST	DAC_VOL_RATE_FAST							
0x55	85	RESERVED	RESERVED							
0x56	86	DAC MUTE	DAC_MUTE_CH8	DAC_MUTE_CH7	DAC_MUTE_CH6	DAC_MUTE_CH5	DAC_MUTE_CH4	DAC_MUTE_CH3	DAC_MUTE_CH2	DAC_MUTE_CH1
0x57	87	DAC INVERT	DAC_INVERT_CH8	DAC_INVERT_CH7	DAC_INVERT_CH6	DAC_INVERT_CH5	DAC_INVERT_CH4	DAC_INVERT_CH3	DAC_INVERT_CH2	DAC_INVERT_CH1
0x58	88	FILTER SHAPE	RESERVED					FILTER_SHAPE		
0x59	89	IIR BANDWIDTH & S/PDIF SELECT	SPDIF_SEL				VOLUME_HOLD	IIR_BW		
0x5A	90	DAC PATH CONFIG	RESERVED						BYPASS_FIR4X	BYPASS_FIR2X
0x5B - 0x7A	91 - 122	RESERVED	RESERVED							
0x7B	123	AUTOMUTE ENABLE	AUTOMUTE_EN_CH8	AUTOMUTE_EN_CH7	AUTOMUTE_EN_CH6	AUTOMUTE_EN_CH5	AUTOMUTE_EN_CH4	AUTOMUTE_EN_CH3	AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1
0x7C	124	AUTOMUTE TIME	AUTOMUTE_TIME							
0x7D	125		RESERVED				AUTOMUTE_RAMP_TO_GROUND	AUTOMUTE_TIME		
0x7E	126	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x7F	127		AUTOMUTE_LEVEL							
0x80	128	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL							
0x81	129		AUTOMUTE_OFF_LEVEL							
0x82	130	SOFT RAMP CONFIG	RESERVED			SOFT_RAMP_TIME				
0x83 - 0x91	131 - 145	RESERVED	RESERVED							
0xE0	224	SYS READ	RESERVED				MODES		ADDR1	ADDR0
0xE1	225	CHIP ID READ	CHIP_ID							
0xE2 - 0xE4	226 - 228	RESERVED	RESERVED							
0xE5	229	INTERRUPT STATE	VOL_MIN_STATE							
0xE6	230		AUTOMUTE_STATE							
0xE7	231		SS_FULL_RAMP_STATE							
0xE8	232		INPUT_SELECT_OVERRIDE_STATE		TDM_DATA_VALID_STATE	RESERVED			BCK_WS_FAIL_STATE	DOP_VALID_STATE
0xE9	233	RESERVED	RESERVED							
0xEA	234	INTERRUPT SOURCE	VOL_MIN_SOURCE							
0xEB	235		AUTOMUTE_SOURCE							
0xEC	236		SS_FULL_RAMP_SOURCE							
0xED	237		INPUT_SELECT_OVERRIDE_SOURCE		TDM_DATA_VALID_SOURCE	RESERVED			BCK_WS_FAIL_SOURCE	DOP_VALID_SOURCE
0xEE	238	RESERVED	RESERVED							
0xEF	239	RATIO VALID READ	RATIO_VALID	RESERVED						
0xF0	240	GPIO READ	GPIO8_I_READ	GPIO7_I_READ	GPIO6_I_READ	GPIO5_I_READ	GPIO4_I_READ	GPIO3_I_READ	GPIO2_I_READ	GPIO1_I_READ
0xF1	241	VOL MIN READ	VOL_MIN_CH8	VOL_MIN_CH7	VOL_MIN_CH6	VOL_MIN_CH5	VOL_MIN_CH4	VOL_MIN_CH3	VOL_MIN_CH2	VOL_MIN_CH1
0xF2	242	AUTOMUTE READ	AUTOMUTE_CH8	AUTOMUTE_CH7	AUTOMUTE_CH6	AUTOMUTE_CH5	AUTOMUTE_CH4	AUTOMUTE_CH3	AUTOMUTE_CH2	AUTOMUTE_CH1
0xF3	243	SOFT RAMP UP READ	SS_RAMP_UP_CH8	SS_RAMP_UP_CH7	SS_RAMP_UP_CH6	SS_RAMP_UP_CH5	SS_RAMP_UP_CH4	SS_RAMP_UP_CH3	SS_RAMP_UP_CH2	SS_RAMP_UP_CH1
0xF4	244	SOFT RAMP DOWN READ	SS_RAMP_DOWN_CH8	SS_RAMP_DOWN_CH7	SS_RAMP_DOWN_CH6	SS_RAMP_DOWN_CH5	SS_RAMP_DOWN_CH4	SS_RAMP_DOWN_CH3	SS_RAMP_DOWN_CH2	SS_RAMP_DOWN_CH1
0xF5	245	SPDIF, TDM, DOP, AND INPUT READBACK	SPDIF_VALID	TDM_DATA_VALID	DOP_VALID				INPUT_SELECT_OVERRIDE	
0xF6 - 0xFB	246 - 251	RESERVED	RESERVED							

Register Listings

Some reserved registers values might be asserted in default mode. This is normal and does not need to be changed.

System Registers

Register 0: SYSTEM CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	2'b00	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core
[6]	ENABLE_64FS_MODE	Enables 64FS mode for 768kHz sample rate. • 1'b0: 64FS mode disabled (default) • 1'b1: 64FS mode enabled
[5:4]	CH78_SEL	Selects ch7/8 nsmod input. • 2'b00: Input from ch7/8 interpolation path (default) • 2'b01: Input from ch5/6 interpolation path • 2'b10: Input from ch1/2 interpolation path • 2'b11: Reserved
[3]	CH56_SEL	Selects ch5/6 nsmod input. • 1'b0: Input from ch5/6 interpolation path (default) • 1'b1: Input from ch1/2 interpolation path
[2]	CH34_SEL	Selects ch3/4 nsmod input. • 1'b0: Input from ch3/4 interpolation path (default) • 1'b1: Input from ch1/2 interpolation path
[1]	DAC_MODE_REG	Enables DAC data path • 1'b0: DAC disabled • 1'b1: DAC enabled
[0]	RESERVED	NA

Register 1: SYS MODE CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b0	2'b01	1'b0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	ENABLE_DAC	Enables DAC interpolation path clock. • 1'b0: Clock disabled • 1'b1: Clock enabled (default)
[6]	SYNC_MODE	Enables SYNC mode • 1'b0: ASYNC mode enabled (default) • 1'b1: SYNC mode enabled
[5:4]	RESERVED	NA
[3]	ENABLE_SPDIF_DECODE	Enables SPDIF decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_TDM_DECODE	Enables TDM decoding. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 2: RESERVED

Register 3: DAC CLOCK CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b1	1'b0	6'd0

Bits	Mnemonic	Description
[7]	AUTO_FS_DETECT	• 1'b0: Disabled • 1'b1: Auto tune CLK_DAC/CLK_IDAC ratio according to detected FS (default) Note: Cannot be used in ASYNC mode
[6]	SELECT_IDAC_HALF	• 1'b0: Divide by SELECT_IDAC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_IDAC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	SELECT_IDAC_NUM	CLK_IDAC divider. Whole number divide value + 1 for CLK_IDAC (SYS_CLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd1: Whole number divide value + 1 = 2 • 6'd63: Whole number divide value + 1 = 64

Register 4: CLOCK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_BCK_DIV	Master mode clock divider. Whole number divide value + 1 for CLK_Master (SYS_CLK/divide_value).

Register 5: CLK GEAR SELECT

Bits	[7:6]	[5:4]	[3]	[2]	[1:0]
Default	2'b00	2'd0	1'b0	1'b0	2'b00

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	SEL_CLK_GEAR	Clock Gearing • 2'd0: SYS_CLK/1 • 2'd1: SYS_CLK/2 • 2'd2: SYS_CLK/4 • 2'd3: SYS_CLK/8
[3]	RESERVED	NA
[2]	AUTO_CLK_GEAR	• 1'b0: Disable automatic clock gearing. SYS_CLK = SEL_CLK_GEAR • 1'b1: Enable automatic clock gearing. SYS_CLK will increase up to SEL_CLK_GEAR
[1:0]	RESERVED	NA

Register 9-7: RESERVED

Register 10: INTERUPT VOL MIN MASK P

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	VOL_MIN_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	VOL_MIN_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	VOL_MIN_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	VOL_MIN_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	VOL_MIN_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	VOL_MIN_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	VOL_MIN_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 11: INTERRUPT AUTOMUTE MASKP

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_FLAG_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	AUTOMUTE_FLAG_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	AUTOMUTE_FLAG_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	AUTOMUTE_FLAG_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	AUTOMUTE_FLAG_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	AUTOMUTE_FLAG_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	AUTOMUTE_FLAG_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	AUTOMUTE_FLAG_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 12: SS FULL RAMP MASKP

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SS_FULL_RAMP_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	SS_FULL_RAMP_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	SS_FULL_RAMP_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	SS_FULL_RAMP_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	SS_FULL_RAMP_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	SS_FULL_RAMP_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	SS_FULL_RAMP_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	SS_FULL_RAMP_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 13: INTERRUPT MASKP

Bits	[7:6]	[5]	[4:2]	[1]	[0]
Default	2'b00	1'b0	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	INPUT_SELECT_OVERRIDE_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	TDM_VALID_EDGE_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4:2]	RESERVED	NA
[1]	BCK_WS_FAIL_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	DOP_VALID_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 14: RESERVED

Register 15: INTERUPT VOL MIN MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	VOL_MIN_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	VOL_MIN_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	VOL_MIN_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	VOL_MIN_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	VOL_MIN_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	VOL_MIN_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	VOL_MIN_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 16: INTERRUPT AUTOMUTE MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_FLAG_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	AUTOMUTE_FLAG_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	AUTOMUTE_FLAG_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	AUTOMUTE_FLAG_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	AUTOMUTE_FLAG_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	AUTOMUTE_FLAG_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	AUTOMUTE_FLAG_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	AUTOMUTE_FLAG_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 17: INTERRUPT SS FULL RAMP MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SS_FULL_RAMP_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	SS_FULL_RAMP_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	SS_FULL_RAMP_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	SS_FULL_RAMP_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	SS_FULL_RAMP_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	SS_FULL_RAMP_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	SS_FULL_RAMP_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	SS_FULL_RAMP_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 18: INTERRUPT MASKN

Bits	[7:6]	[5]	[4:2]	[1]	[0]
Default	2'b00	1'b0	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	INPUT_SELECT_OVERRIDE_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	TDM_VALID_EDGE_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4:2]	RESERVED	NA
[1]	BCK_WS_FAIL_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	DOP_VALID_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 19: RESERVED

Register 20: INTERRUPT VOL MIN CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_CLEAR	Write a 1'b1 to clear the interrupt
[6]	VOL_MIN_CH7_CLEAR	Write a 1'b1 to clear the interrupt
[5]	VOL_MIN_CH6_CLEAR	Write a 1'b1 to clear the interrupt
[4]	VOL_MIN_CH5_CLEAR	Write a 1'b1 to clear the interrupt
[3]	VOL_MIN_CH4_CLEAR	Write a 1'b1 to clear the interrupt
[2]	VOL_MIN_CH3_CLEAR	Write a 1'b1 to clear the interrupt
[1]	VOL_MIN_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[0]	VOL_MIN_CH1_CLEAR	Write a 1'b1 to clear the interrupt

Register 21: INTERRUPT AUTOMUTE CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_FLAG_CH8_CLEAR	Write a 1'b1 to clear the interrupt
[6]	AUTOMUTE_FLAG_CH7_CLEAR	Write a 1'b1 to clear the interrupt
[5]	AUTOMUTE_FLAG_CH6_CLEAR	Write a 1'b1 to clear the interrupt
[4]	AUTOMUTE_FLAG_CH5_CLEAR	Write a 1'b1 to clear the interrupt
[3]	AUTOMUTE_FLAG_CH4_CLEAR	Write a 1'b1 to clear the interrupt
[2]	AUTOMUTE_FLAG_CH3_CLEAR	Write a 1'b1 to clear the interrupt
[1]	AUTOMUTE_FLAG_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[0]	AUTOMUTE_FLAG_CH1_CLEAR	Write a 1'b1 to clear the interrupt

Register 22: INTERRUPT SS FULL RAMP CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SS_FULL_RAMP_CH8_CLEAR	Write a 1'b1 to clear the interrupt
[6]	SS_FULL_RAMP_CH7_CLEAR	Write a 1'b1 to clear the interrupt
[5]	SS_FULL_RAMP_CH6_CLEAR	Write a 1'b1 to clear the interrupt
[4]	SS_FULL_RAMP_CH5_CLEAR	Write a 1'b1 to clear the interrupt
[3]	SS_FULL_RAMP_CH4_CLEAR	Write a 1'b1 to clear the interrupt
[2]	SS_FULL_RAMP_CH3_CLEAR	Write a 1'b1 to clear the interrupt
[1]	SS_FULL_RAMP_CH2_CLEAR	Write a 1'b1 to clear the interrupt
[0]	SS_FULL_RAMP_CH1_CLEAR	Write a 1'b1 to clear the interrupt

Register 23: INTERRUPT CLEAR

Bits	[7:6]	[5]	[4:2]	[1]	[0]
Default	2'b00	1'b0	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	INPUT_SELECT_OVERRIDE_CLEAR	Write a 1'b1 to clear the interrupt
[5]	TDM_VALID_EDGE_CLEAR	Write a 1'b1 to clear the interrupt
[4:2]	RESERVED	NA
[1]	BCK_WS_FAIL_CLEAR	Write a 1'b1 to clear the interrupt
[0]	DOP_VALID_CLEAR	Write a 1'b1 to clear the interrupt

Register 28-24: RESERVED

Register 29: DPLL BW

Bits	[7:4]	[3:0]
Default	4'd4	4'd0

Bits	Mnemonic	Description
[7:4]	DPLL_BW	Sets the bandwidth of the DPLL. • 4'd0: Reserved • 4'd1: Lowest Bandwidth • 4'd15: Highest Bandwidth
[3:0]	RESERVED	NA

Register 36-30: RESERVED

GPIO Registers

Register 37: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd7	4'd13

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configures GPIO2 • 4'd0: analog shutdown - shutdown • 4'd1: output 0 – output • 4'd2: output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: interrupt – output • 4'd5: mute all channel - input • 4'd6: input selection - input • 4'd7: LOCK_STATUS – output (default) • 4'd8: CLKEN_1FS – output • 4'd9: output PWM1 – output • 4'd10: output PWM2 – output • 4'd11: output PWM3 – output • 4'd12: volume minimum – output • 4'd13: automute status – output • 4'd14: soft ramp done – output • 4'd15: Reserved
[3:0]	GPIO1_CFG	Configures GPIO1 • 4'd0: analog shutdown - shutdown • 4'd1: output 0 – output • 4'd2: output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: interrupt – output • 4'd5: mute all channel - input • 4'd6: input selection - input • 4'd7: LOCK_STATUS – output • 4'd8: CLKEN_1FS – output • 4'd9: output PWM1 – output • 4'd10: output PWM2 – output • 4'd11: output PWM3 – output • 4'd12: volume minimum – output • 4'd13: automute status – output (default) • 4'd14: soft ramp done – output • 4'd15: Reserved

Register 38: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configures GPIO4 • 4'd0: analog shutdown - shutdown • 4'd1: output 0 – output • 4'd2: output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: interrupt – output • 4'd5: mute all channel - input • 4'd6: input selection - input • 4'd7: LOCK_STATUS – output • 4'd8: CLKEN_1FS – output • 4'd9: output PWM1 – output • 4'd10: output PWM2 – output • 4'd11: output PWM3 – output • 4'd12: volume minimum – output • 4'd13: automute status – output • 4'd14: soft ramp done – output • 4'd15: Reserved
[3:0]	GPIO3_CFG	Configures GPIO3 • 4'd0: analog shutdown - shutdown • 4'd1: output 0 – output • 4'd2: output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: interrupt – output • 4'd5: mute all channel - input • 4'd6: input selection - input • 4'd7: LOCK_STATUS – output • 4'd8: CLKEN_1FS – output • 4'd9: output PWM1 – output • 4'd10: output PWM2 – output • 4'd11: output PWM3 – output • 4'd12: volume minimum – output • 4'd13: automute status – output • 4'd14: soft ramp done – output • 4'd15: Reserved

Register 39: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configures GPIO6 • 4'd0: analog shutdown - shutdown • 4'd1: output 0 – output • 4'd2: output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: interrupt – output • 4'd5: mute all channel - input • 4'd6: input selection - input • 4'd7: LOCK_STATUS – output • 4'd8: CLKEN_1FS – output • 4'd9: output PWM1 – output • 4'd10: output PWM2 – output • 4'd11: output PWM3 – output • 4'd12: volume minimum – output • 4'd13: automute status – output • 4'd14: soft ramp done – output • 4'd15: Reserved
[3:0]	GPIO5_CFG	Configures GPIO5 • 4'd0: analog shutdown - shutdown • 4'd1: output 0 – output • 4'd2: output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: interrupt – output • 4'd5: mute all channel - input • 4'd6: input selection - input • 4'd7: LOCK_STATUS – output • 4'd8: CLKEN_1FS – output • 4'd9: output PWM1 – output • 4'd10: output PWM2 – output • 4'd11: output PWM3 – output • 4'd12: volume minimum – output • 4'd13: automute status – output • 4'd14: soft ramp done – output • 4'd15: Reserved

Register 40: GPIO7/8 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO8_CFG	Configures GPIO8 • 4'd0: analog shutdown - shutdown • 4'd1: output 0 – output • 4'd2: output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: interrupt – output • 4'd5: mute all channel - input • 4'd6: input selection - input • 4'd7: LOCK_STATUS – output • 4'd8: CLKEN_1FS – output • 4'd9: output PWM1 – output • 4'd10: output PWM2 – output • 4'd11: output PWM3 – output • 4'd12: volume minimum – output • 4'd13: automute status – output • 4'd14: soft ramp done – output • 4'd15: Reserved
[3:0]	GPIO7_CFG	Configures GPIO7 • 4'd0: analog shutdown - shutdown • 4'd1: output 0 – output • 4'd2: output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: interrupt – output • 4'd5: mute all channel - input • 4'd6: input selection - input • 4'd7: LOCK_STATUS – output • 4'd8: CLKEN_1FS – output • 4'd9: output PWM1 – output • 4'd10: output PWM2 – output • 4'd11: output PWM3 – output • 4'd12: volume minimum – output • 4'd13: automute status – output • 4'd14: soft ramp done – output • 4'd15: Reserved

Register 41: GPIO OUTPUT ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1

Bits	Mnemonic	Description
[7]	GPIO8_OE	• 1'b0: Tristate GPIO8 (default) • 1'b1: GPIO8 Output Enable
[6]	GPIO7_OE	• 1'b0: Tristate GPIO7 (default) • 1'b1: GPIO7 Output Enable
[5]	GPIO6_OE	• 1'b0: Tristate GPIO6 (default) • 1'b1: GPIO6 Output Enable
[4]	GPIO5_OE	• 1'b0: Tristate GPIO5 (default) • 1'b1: GPIO5 Output Enable
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 (default) • 1'b1: GPIO4 Output Enable
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 (default) • 1'b1: GPIO3 Output Enable
[1]	GPIO2_OE	• 1'b0: Tristate GPIO2 • 1'b1: GPIO2 Output Enable (default)
[0]	GPIO1_OE	• 1'b0: Tristate GPIO1 • 1'b1: GPIO1 Output Enable (default)

Register 42: GPIO INPUT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'b1	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_SDB	• 1'b0: Disables GPIO8 input (default) • 1'b1: Enables GPIO8 input
[6]	GPIO7_SDB	• 1'b0: Disables GPIO7 input (default) • 1'b1: Enables GPIO7 input
[5]	GPIO6_SDB	• 1'b0: Disables GPIO6 input (default) • 1'b1: Enables GPIO6 input
[4]	GPIO5_SDB	• 1'b0: Disables GPIO5 input (default) • 1'b1: Enables GPIO5 input
[3]	GPIO4_SDB	• 1'b0: Disables GPIO4 input (default) • 1'b1: Enables GPIO4 input
[2]	GPIO3_SDB	• 1'b0: Disables GPIO3 input (default) • 1'b1: Enables GPIO3 input
[1]	GPIO2_SDB	• 1'b0: Disables GPIO2 input (default) • 1'b1: Enables GPIO2 input
[0]	GPIO1_SDB	• 1'b0: Disables GPIO1 input (default) • 1'b1: Enables GPIO1 input

Register 43: GPIO WK EN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_WK_EN	• 1'b0: GPIO8 weak keeper disabled (default) • 1'b1: GPIO8 weak keeper enabled
[6]	GPIO7_WK_EN	• 1'b0: GPIO7 weak keeper disabled (default) • 1'b1: GPIO7 weak keeper enabled
[5]	GPIO6_WK_EN	• 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled
[4]	GPIO5_WK_EN	• 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[3]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[2]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[1]	GPIO2_WK_EN	• 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[0]	GPIO1_WK_EN	• 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled

Register 44: INVERT GPIO

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	INVERT_GPIO8	• 1'b1: Inverts GPIO8 output.
[6]	INVERT_GPIO7	• 1'b1: Inverts GPIO7 output.
[5]	INVERT_GPIO6	• 1'b1: Inverts GPIO6 output.
[4]	INVERT_GPIO5	• 1'b1: Inverts GPIO5 output.
[3]	INVERT_GPIO4	• 1'b1: Inverts GPIO4 output.
[2]	INVERT_GPIO3	• 1'b1: Inverts GPIO3 output.
[1]	INVERT_GPIO2	• 1'b1: Inverts GPIO2 output.
[0]	INVERT_GPIO1	• 1'b1: Inverts GPIO1 output.

Register 45: GPIO READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_READ	• 1'b0: GPIO8 Readback disabled (default) • 1'b1: Allow readback of GPIO8_I
[6]	GPIO7_READ	• 1'b0: GPIO7 Readback disabled (default) • 1'b1: Allow readback of GPIO7_I
[5]	GPIO6_READ	• 1'b0: GPIO6 Readback disabled (default) • 1'b1: Allow readback of GPIO6_I
[4]	GPIO5_READ	• 1'b0: GPIO5 Readback disabled (default) • 1'b1: Allow readback of GPIO5_I
[3]	GPIO4_READ	• 1'b0: GPIO4 Readback disabled (default) • 1'b1: Allow readback of GPIO4_I
[2]	GPIO3_READ	• 1'b0: GPIO3 Readback disabled (default) • 1'b1: Allow readback of GPIO3_I
[1]	GPIO2_READ	• 1'b0: GPIO2 Readback disabled (default) • 1'b1: Allow readback of GPIO2_I
[0]	GPIO1_READ	• 1'b0: GPIO1 Readback disabled (default) • 1'b1: Allow readback of GPIO1_I

Register 47-46: GPIO OUTPUT LOGIC

Bits	[15]	[14:9]	[8:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	6'd0	3'd0	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[15]	GPIO_DAC_MODE	When any GPIOx_CFG = 6 (input system mode control): • 1'b0: Power down when GPIO input is 1 • 1'b1: HIFI when GPIO input is 1 (when GPIO input is 0, system mode is determined by register DAC_MODE_REG (register 0, bit[1]))
[14:9]	RESERVED	NA
[8:6]	GPIO_SEL	When GPIOx_CFG = 12, 13 or 14, and the corresponding GPIO_AND and GPIO_OR are not set: • 3'd0: Outputs status/flag from ch1 • 3'd1: Outputs status/flag from ch2 • 3'd2: Outputs status/flag from ch3 • 3'd3: Outputs status/flag from ch4 • 3'd4: Outputs status/flag from ch5 • 3'd5: Outputs status/flag from ch6 • 3'd6: Outputs status/flag from ch7 • 3'd7: Outputs status/flag from ch8
[5]	GPIO_OR_SS_RAMP	When GPIOx_CFG = 14 (output soft ramp done flag): • 1'b0: The soft ramp done flag is determined by GPIO_AND_SS_RAMP and GPIO_SEL (default) • 1'b1: The soft ramp done flag is the "OR" of all 8ch soft ramp done flags
[4]	GPIO_OR_VOL_MIN	When GPIOx_CFG = 12 (output vol_min flag): • 1'b0: The vol_min flag is determined by GPIO_AND_VOL_MIN and GPIO_SEL (default) • 1'b1: The vol_min flag is the "OR" of all 8ch vol_min flags
[3]	GPIO_OR_AUTOMUTE	When GPIOx_CFG = 13 (output automute status): • 1'b0: The automute status is determined by GPIO_AND_AUTOMUTE and GPIO_SEL (default) • 1'b1: The automute status is the "OR" of all 8ch automute status
[2]	GPIO_AND_SS_RAMP	When GPIOx_CFG = 14 (output soft ramp done flag) and GPIO_OR_SS_RAMP is not set: • 1'b0: The soft ramp done flag is from a single channel selected by GPIO_SEL • 1'b1: The soft ramp done flag is the "AND" of all 8ch soft ramp done flags (default)
[1]	GPIO_AND_VOL_MIN	When GPIOx_CFG = 12 (output vol_min flag) and GPIO_OR_VOL_MIN is not set: • 1'b0: The vol_min flag is from a single channel selected by GPIO_SEL • 1'b1: The vol_min flag is the "AND" of all 8ch vol_min flags (default)
[0]	GPIO_AND_AUTOMUTE	When GPIOx_CFG = 13 (output automute status) and GPIO_OR_AUTOMUTE is not set: • 1'b0: The automute status is from a single channel selected by GPIO_SEL • 1'b1: The automute status is the "AND" of all 8ch automute status (default)

Register 48: PWM1 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM1_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. Valid from 8'd0 to 8'd255

Register 50-49: PWM1 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM1_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. Valid from 16'h0000 to 16'hFFFF $$frequency\ (Hz) = \frac{SYS\_CLK}{PWM1\_FREQ + 1}$$ $$Duty\ Cycle\ (\%) = \left(1 - \frac{(PWM1\_FREQ + 1) - PWM1\_COUNT}{PWM1\_FREQ + 1}\right) \times 100$$

Register 51: PWM2 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM2_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. Valid from 8'd0 to 8'd255

Register 53-52: PWM2 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM2_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. Valid from 16'h0000 to 16'hFFFF $$frequency\ (Hz) = \frac{SYS\_CLK}{PWM2\_FREQ + 1}$$ $$Duty\ Cycle\ (\%) = \left(1 - \frac{(PWM2\_FREQ + 1) - PWM2\_COUNT}{PWM2\_FREQ + 1}\right) \times 100$$

Register 54: PWM3 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM3_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. Valid from 8'd0 to 8'd255

Register 56-55: PWM3 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. Valid from 16'h0000 to 16'hFFFF $$frequency\ (Hz) = \frac{SYS\_CLK}{PWM3\_FREQ + 1}$$ $$Duty\ Cycle\ (\%) = \left(1 - \frac{(PWM3\_FREQ + 1) - PWM3\_COUNT}{PWM3\_FREQ + 1}\right) \times 100$$

DAC Registers

Register 57: INPUT SELECTION

Bits	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Default	1'b0	1'b1	1'b0	1'b0	1'b0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Auto detect BCK/FRAME ratio to determine the number of TDM channels • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_DSD_FAULT_DETECTION	• 1'b0: Disabled • 1'b1: Enabled (default)
[5]	DSD_MASTER_MODE	DSD master mode config. • 1'b0: DSD slave mode (default) • 1'b1: DSD master mode. DSD_CLK outputs from DATA_CLK
[4]	PCM_MASTER_MODE	PCM master mode config. • 1'b0: PCM slave mode (default) • 1'b1: PCM master mode enabled. Master BCK and WS output from DATA_CLK and DATA1
[3]	RESERVED	NA
[2:1]	INPUT_SEL	Selects input data format when AUTO_INPUT_SELECT is disabled. • 2'd0: TDM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: SPDIF
[0]	AUTO_INPUT_SEL	Automatic input data selection config. • 1'b0: Disables auto input select. Input data format is set by INPUT_SEL (default) • 1'b1: Automatically determine the input data format.

Register 58: SERIAL MASTER ENCODER CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM decoder to resync. • 1'b0: Let decoder sync (default) • 1'b1: Force decoder not sync
[6]	BCK_INV	Invert the slave BCK • 1'b0: Normal operation • 1'b1: Invert slave BCK
[5]	RESERVED	NA
[4:3]	MASTER_FRAME_LENGTH	Selects the bit length in each TDM channel in master mode. • 2'd0: 32-bit (default) • 2'd1: 24-bit • 2'd2: 16-bit • 2'd3: Reserved
[2]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	MASTER_BCK_INVERT	Inverts master BCK or DSD_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)

Register 59: TDM CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:0]	TDM_CH_NUM	Total number of TDM slots per frame = TDM_CH_NUM + 1.

Register 60: TDM CONFIG1

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd0

Bits	Mnemonic	Description
[7]	TDM_LJ_MODE	TDM LJ mode. • 1'b0: Standard I2S (default) • 1'b1: LJ mode
[6]	TDM_VALID_EDGE	TDM WS valid edge. • 1'b0: negative edge (default) • 1'b1: positive edge
[5:0]	RESERVED	NA

Register 61: TDM CONFIG2

Bits	[7]	[6:5]	[4:0]
Default	1'b1	2'b00	5'd0

Bits	Mnemonic	Description
[7]	ENABLE_ASYNC_LOCK_MONITOR	Monitors the lock status of the SRC, when in ASYNC mode. Sets BCK_WS_FAIL on unlock. • 1'b0: Disabled • 1'b1: Enabled (default)
[6:5]	TDM_BIT_WIDTH	Bit width of each TDM slot. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit • 2'b11: Reserved
[4:0]	TDM_DATA_LATCH_ADJ	Sets the position of the start bit within each TDM slot. Can be moved by TDM_DATA_LATCH_ADJ clock cycles. • 5'd0: Normal position • 5'd1-31: Number of clock cycles to wait

Register 62: BCK/WS MONITOR CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2:0]
Default	1'b0	1'b0	1'b1	1'b1	1'b0	3'd0

Bits	Mnemonic	Description
[7]	DISABLE_DSD_DC	• 1'b0: DSD DC can trigger an automute if automute is enabled (default) • 1'b1: DSD DC is ignored.
[6]	DISABLE_DSD_MUTE	• 1'b0: DSD mute pattern can trigger an automute is auotmute is enabled (default) • 1'b1: DSD mute pattern is ignored.
[5]	ENABLE_WS_MONITOR	Enable WS monitor. • 1'b0: Disable • 1'b1: Enable (default)
[4]	ENABLE_BCK_MONITOR	Enable BCK monitor. • 1'b0: Disable (default) • 1'b1: Enable
[3]	DISABLE_PCM_DC	• 1'b0: PCM DC signal can trigger an automute if automute is enabled. • 1'b1: PCM DC is ignored.
[2:0]	RESERVED	NA

Register 63: RESERVED

Register 64: TDM CH1 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH1_LINE_SEL	CH1 data line selection. CH1 receives data from Nth line. N = TDM_CH1_LINE_SEL + 1. Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH1_SLOT_SEL	CH1 data slot selection. CH1 receives data from Mth slot. M = TDM_CH1_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 65: TDM CH2 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH2_LINE_SEL	CH2 data line selection. CH2 receives data from Nth line. N = TDM_CH2_LINE_SEL + 1. Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH2_SLOT_SEL	CH2 data slot selection. CH2 receives data from Mth slot. M = TDM_CH2_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 66: TDM CH3 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH3_LINE_SEL	CH3 data line selection. CH3 receives data from Nth line. N = TDM_CH3_LINE_SEL + 1. Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH3_SLOT_SEL	CH3 data slot selection. CH3 receives data from Mth slot. M = TDM_CH3_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 67: TDM CH4 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH4_LINE_SEL	CH4 data line selection. CH4 receives data from Nth line. N = TDM_CH4_LINE_SEL + 1. Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH4_SLOT_SEL	CH4 data slot selection. CH4 receives data from Mth slot. M = TDM_CH4_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 68: TDM CH5 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH5_LINE_SEL	CH5 data line selection. CH5 receives data from Nth line. N = TDM_CH5_LINE_SEL + 1. Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH5_SLOT_SEL	CH5 data slot selection. CH5 receives data from Mth slot. M = TDM_CH5_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 69: TDM CH6 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH6_LINE_SEL	CH6 data line selection. CH6 receives data from Nth line. N = TDM_CH6_LINE_SEL + 1. Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH6_SLOT_SEL	CH6 data slot selection. CH6 receives data from Mth slot. M = TDM_CH6_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 70: TDM CH7 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH7_LINE_SEL	CH7 data line selection. CH7 receives data from Nth line. N = TDM_CH7_LINE_SEL + 1. Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH7_SLOT_SEL	CH7 data slot selection. CH7 receives data from Mth slot. M = TDM_CH7_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 71: TDM CH8 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH8_LINE_SEL	CH8 data line selection. CH8 receives data from Nth line. N = TDM_CH8_LINE_SEL + 1. Note: Valid for TDM, PCM and DoP.
[4:0]	TDM_CH8_SLOT_SEL	CH8 data slot selection. CH8 receives data from Mth slot. M = TDM_CH8_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 73-72: RESERVED

Register 74: VOLUME1

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME1	DAC ch1 volume. -0dB to -127.5dB, 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 75: VOLUME2

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME2	DAC ch2 volume. -0dB to -127.5dB, 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 76: VOLUME3

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME3	DAC ch3 volume. -0dB to -127.5dB, 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 77: VOLUME4

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME4	DAC ch4 volume. -0dB to -127.5dB, 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 78: VOLUME5

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME5	DAC ch5 volume. -0dB to -127.5dB, 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 79: VOLUME6

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME6	DAC ch6 volume. -0dB to -127.5dB, 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 80: VOLUME7

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME7	DAC ch7 volume. -0dB to -127.5dB, 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 81: VOLUME8

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME8	DAC ch8 volume. -0dB to -127.5dB, 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 82: DAC VOL UP RATE

Bits	[7:0]
Default	8'd4

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_UP	Value by which the old VOLUME value is incremented to reach the new VOLUME value Valid from 8'd0 (instant) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value • 8'd0: Instant change • 8'd4: Default • 8'd255: Fastest change $ramp\_rate\ [s] = \frac{2^{15}}{DAC\_VOL\_RATE\_UP\ *\ FS}$

Register 83: DAC VOL DOWN RATE

Bits	[7:0]
Default	8'd4

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_DOWN	Value by which the old VOLUME value is incremented to reach the new VOLUME value Valid from 8'd0 (instant) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value • 8'd0: Instant change • 8'd4: Default • 8'd255: Fastest change $ramp\_rate\ [s] = \frac{2^{15}}{DAC\_VOL\_RATE\_DOWN\ *\ FS}$

Register 84: DAC VOL DOWN RATE FAST

Bits	[7:0]
Default	8'd255

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_FAST	Value by which the old VOLUME value is incremented to reach the new VOLUME value Valid from 8'd0 (instant) to 8'd255 (fastest), where 8'd0 instantly changes the VOLUME value Only used during abnormal mute (PLL unlock or BCK_WS ratio failed) • 8'd0: Instant change • 8'd255: Fastest change (default) $ramp\_rate\ [s] = \frac{2^{15}}{DAC\_VOL\_RATE\_FAST\ *\ FS}$

Register 85: RESERVED

Register 86: DAC MUTE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_MUTE_CH8	• 1'b0: Normal operation (default) • 1'b1: Mute ch8
[6]	DAC_MUTE_CH7	• 1'b0: Normal operation (default) • 1'b1: Mute ch7
[5]	DAC_MUTE_CH6	• 1'b0: Normal operation (default) • 1'b1: Mute ch6
[4]	DAC_MUTE_CH5	• 1'b0: Normal operation (default) • 1'b1: Mute ch5
[3]	DAC_MUTE_CH4	• 1'b0: Normal operation (default) • 1'b1: Mute ch4
[2]	DAC_MUTE_CH3	• 1'b0: Normal operation (default) • 1'b1: Mute ch3
[1]	DAC_MUTE_CH2	• 1'b0: Normal operation (default) • 1'b1: Mute ch2
[0]	DAC_MUTE_CH1	• 1'b0: Normal operation (default) • 1'b1: Mute ch1

Register 87: DAC INVERT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_INVERT_CH8	Invert the output on Ch8 at the input to the NSMOD
[6]	DAC_INVERT_CH7	Invert the output on Ch7 at the input to the NSMOD
[5]	DAC_INVERT_CH6	Invert the output on Ch6 at the input to the NSMOD
[4]	DAC_INVERT_CH5	Invert the output on Ch5 at the input to the NSMOD
[3]	DAC_INVERT_CH4	Invert the output on Ch4 at the input to the NSMOD
[2]	DAC_INVERT_CH3	Invert the output on Ch3 at the input to the NSMOD
[1]	DAC_INVERT_CH2	Invert the output on Ch2 at the input to the NSMOD
[0]	DAC_INVERT_CH1	Invert the output on Ch1 at the input to the NSMOD

Register 88: FILTER SHAPE

Bits	[7:3]	[2:0]
Default	5'd12	3'd0

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2:0]	FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing • 3'd2: Linear phase fast roll-off • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion

Register 89: IIR BANDWIDTH & S/PDIF SELECT

Bits	[7:4]	[3]	[2:0]
Default	4'd0	1'b0	3'd4

Bits	Mnemonic	Description
[7:4]	SPDIF_SEL	Selects the SPDIF data input pin • 4'd0: Disabled (default) • 4'd1: GPIO1 • 4'd2: GPIO2 • 4'd3: GPIO3 • 4'd4: DATA1 • 4'd5: DATA2 • 4'd6: DATA3 • 4'd7: DATA4/GPIO4 • 4'd8: DATA5/GPIO5 • 4'd9: DATA6/GPIO6 • 4'd10: DATA7/GPIO7 • 4'd11: DATA8/GPIO8 • Others: Reserved • Note: GPIO pins also require the GPIO input to be enabled
[3]	VOLUME_HOLD	Hold volume coefficients to allow for all channels to update at same time.
[2:0]	IIR_BW	Controls the IIR bandwidth in the digital datapath. • 3'd0: Invalid • 3'd1: BW * 8 • 3'd2: BW * 4 • 3'd3: BW * 2 • 3'd4: Default BW • 3'd5: BW / 2 • 3'd6: BW / 4 • 3'd7: BW / 8

Register 90: DAC PATH CONFIG

Bits	[7:2]	[1]	[0]
Default	6'b00000	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	BYPASS_FIR4X	• 1'b0: Non-bypass IFir_4x (default) • 1'b1: Bypass IFir_4x
[0]	BYPASS_FIR2X	• 1'b0: Non-bypass IFir_2x (default) • 1'b1: Bypass IFir_2x

Register 122-98: RESERVED

Register 123: AUTOMUTE ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	AUTOMUTE_EN_CH8	• 1'b0: Disables ch8 automute • 1'b1: Enables ch8 automute (default) Note: Automute is available for PCM only
[6]	AUTOMUTE_EN_CH7	• 1'b0: Disables ch7 automute • 1'b1: Enables ch7 automute (default) Note: Automute is available for PCM only
[5]	AUTOMUTE_EN_CH6	• 1'b0: Disables ch6 automute • 1'b1: Enables ch6 automute (default) Note: Automute is available for PCM only
[4]	AUTOMUTE_EN_CH5	• 1'b0: Disables ch5 automute • 1'b1: Enables ch5 automute (default) Note: Automute is available for PCM only
[3]	AUTOMUTE_EN_CH4	• 1'b0: Disables ch4 automute • 1'b1: Enables ch4 automute (default) Note: Automute is available for PCM only
[2]	AUTOMUTE_EN_CH3	• 1'b0: Disables ch3 automute • 1'b1: Enables ch3 automute (default) Note: Automute is available for PCM only
[1]	AUTOMUTE_EN_CH2	• 1'b0: Disables ch2 automute • 1'b1: Enables ch2 automute (default) Note: Automute is available for PCM only
[0]	AUTOMUTE_EN_CH1	• 1'b0: Disables ch1 automute • 1'b1: Enables ch1 automute (default) Note: Automute is available for PCM only

Register 125-124: AUTOMUTE TIME

Bits	[15:12]	[11]	[10:0]
Default	4'd0	1'b1	11'd15

Bits	Mnemonic	Description
[15:12]	RESERVED	NA
[11]	AUTOMUTE_RAMP_TO_GROUND	• 1'b0: When ramped to min volume during normal mute, do not soft ramp to ground • 1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default) normal mute includes: automute, mute by register, mute by GPIO
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. Valid from 0 (disabled) to 11'h7FF (fastest), where 11'h001 is the slowest $Time\ [s] = \frac{2^{18}}{AUTOMUTE\_TIME * FS}$

Register 127-126: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'0008

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	Configures the threshold which the audio must be below before an automute condition is flagged. Valid from: 16'hFFFF (-42dB) to 16'h0001 (-132dB) Shift right 1 bit corresponds to -6dB Note: this register works in tandem with AUTOMUTE_TIME to create the automute condition

Register 129-128: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'000A

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	Configures the threshold which the audio must be above before the automute condition is cleared (cleared immediately). Valid from: 16'hFFFF (-42dB) to 16'h0001 (-132dB) Shift right 1 bit corresponds to -6dB

Register 130: SOFT RAMP CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd3

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. Valid from 0 to 20 (inclusive). $Time\ [s] = 4096 * \frac{2^{SOFT\_RAMP\_TIME+1}}{CLK_{IDAC[Hz]}}$

Register 145-131: RESERVED

Readback Registers

Register 224: SYS READ

Bits	[7:4]	[3:2]	[1]	[0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3:2]	MODES	Chip mode readback. Based off MODE Pin (Pin 3) • 2'b00: I2C • 2'b11: SPI Note: All other values are invalid.
[1]	ADDR1	I2C address select bit1.
[0]	ADDR0	I2C address select bit0.

Register 225: CHIP ID READ

Bits	[7:0]
Default	0x58 (ES9027PRO)

Bits	Mnemonic	Description
[7:0]	CHIP_ID	Chip ID.

Register 228-227: RESERVED

Register 232-229: INTERRUPT STATE

Bits	[31:30]	[29]	[28:26]	[25]	[24]	[23:16]	[15:8]	[7:0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[31:30]	INPUT_SELECT_OVERRIDE_STATE	State of the INPUT_SELECT_OVERRIDE interrupt. Note: Interrupt clear bits are required to reset value.
[29]	TDM_DATA_VALID_STATE	State of the TDM_DATA_VALID interrupt. Note: Interrupt clear bit is required to reset value.
[28:26]	RESERVED	NA
[25]	BCK_WS_FAIL_STATE	State of the BCK_WS_FAIL interrupt. Note: Interrupt clear bit is required to reset value.
[24]	DOP_VALID_STATE	State of the DOP_VALID interrupt. Note: Interrupt clear bit is required to reset value.
[23:16]	SS_FULL_RAMP_STATE	State of each channel's SS_FULL_RAMP interrupt. Note: Interrupt clear bit is required to reset value.
[15:8]	AUTOMUTE_STATE	State of each channel's AUTOMUTE_STATE interrupt. Note: Interrupt clear bit is required to reset value.
[7:0]	VOL_MIN_STATE	State of each channel's VOL_MIN_STATE interrupt. Note: Interrupt clear bit is required to reset value.

Register 233: RESERVED

Register 237-234: INTERRUPT SOURCE

Bits	[31:30]	[29]	[28:26]	[25]	[24]	[23:16]	[15:8]	[7:0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[31:30]	INPUT_SELECT_OVERRIDE_SOURCE	Output of the AUTO_INPUT_SELECT logic.
[29]	TDM_DATA_VALID_SOURCE	TDM data valid flag.
[28:26]	RESERVED	NA
[25]	BCK_WS_FAIL_SOURCE	Validity of BCK, WS, and ASYNC_LOCK flag. Requires respective monitor bits to be set.
[24]	DOP_VALID_SOURCE	Valid DoP flag for Channels 1 and 2.
[23:16]	SS_FULL_RAMP_SOURCE	Channel flag for whether it is fully ramped up or down.
[15:8]	AUTOMUTE_SOURCE	Channel flag for whether it is automute is active.
[7:0]	VOL_MIN_SOURCE	Channel flag for whether the corresponding volume register = 0x00

Register 238: RESERVED

Register 239: RATIO VALID READ

Bits	[7]	[6:0]
Default	-	-

Bits	Mnemonic	Description
[7]	RATIO_VALID	Indicates validity of the CLK_DAC/CLK_IDAC ratio • 1'b0: Invalid • 1'b1: Valid
[6:0]	RESERVED	NA

Register 240: GPIO READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	GPIO8_I_READ	GPIO8 Readback
[6]	GPIO7_I_READ	GPIO7 Readback
[5]	GPIO6_I_READ	GPIO6 Readback
[4]	GPIO5_I_READ	GPIO5 Readback
[3]	GPIO4_I_READ	GPIO4 Readback
[2]	GPIO3_I_READ	GPIO3 Readback
[1]	GPIO2_I_READ	GPIO2 Readback
[0]	GPIO1_I_READ	GPIO1 Readback

Register 241: VOL MIN READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8	Volume min flag ch8
[6]	VOL_MIN_CH7	Volume min flag ch7
[5]	VOL_MIN_CH6	Volume min flag ch6
[4]	VOL_MIN_CH5	Volume min flag ch5
[3]	VOL_MIN_CH4	Volume min flag ch4
[2]	VOL_MIN_CH3	Volume min flag ch3
[1]	VOL_MIN_CH2	Volume min flag ch2
[0]	VOL_MIN_CH1	Volume min flag ch1

Register 242: AUTOMUTE READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	AUTOMUTE_CH8	Automute status ch8
[6]	AUTOMUTE_CH7	Automute status ch7
[5]	AUTOMUTE_CH6	Automute status ch6
[4]	AUTOMUTE_CH5	Automute status ch5
[3]	AUTOMUTE_CH4	Automute status ch4
[2]	AUTOMUTE_CH3	Automute status ch3
[1]	AUTOMUTE_CH2	Automute status ch2
[0]	AUTOMUTE_CH1	Automute status ch1

Register 243: SOFT RAMP UP READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_UP_CH8	Soft ramped up flag ch8
[6]	SS_RAMP_UP_CH7	Soft ramped up flag ch7
[5]	SS_RAMP_UP_CH6	Soft ramped up flag ch6
[4]	SS_RAMP_UP_CH5	Soft ramped up flag ch5
[3]	SS_RAMP_UP_CH4	Soft ramped up flag ch4
[2]	SS_RAMP_UP_CH3	Soft ramped up flag ch3
[1]	SS_RAMP_UP_CH2	Soft ramped up flag ch2
[0]	SS_RAMP_UP_CH1	Soft ramped up flag ch1

Register 244: SOFT RAMP DOWN READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_DOWN_CH8	Soft ramped down flag ch8
[6]	SS_RAMP_DOWN_CH7	Soft ramped down flag ch7
[5]	SS_RAMP_DOWN_CH6	Soft ramped down flag ch6
[4]	SS_RAMP_DOWN_CH5	Soft ramped down flag ch5
[3]	SS_RAMP_DOWN_CH4	Soft ramped down flag ch4
[2]	SS_RAMP_DOWN_CH3	Soft ramped down flag ch3
[1]	SS_RAMP_DOWN_CH2	Soft ramped down flag ch2
[0]	SS_RAMP_DOWN_CH1	Soft ramped down flag ch1

Register 245: S/PDIF, TDM, DOP, AND INPUT READBACK

Bits	[7]	[6]	[5:2]	[1:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	SPDIF_VALID	SPDIF valid flag
[6]	TDM_DATA_VALID	TDM valid data flag
[5:2]	DOP_VALID	DoP valid flag
[1:0]	INPUT_SELECT_OVERRIDE	AUTO_INPUT_SEL value

Register 251-248: RESERVED

ES9027PRO Reference Schematic

Hardware Mode

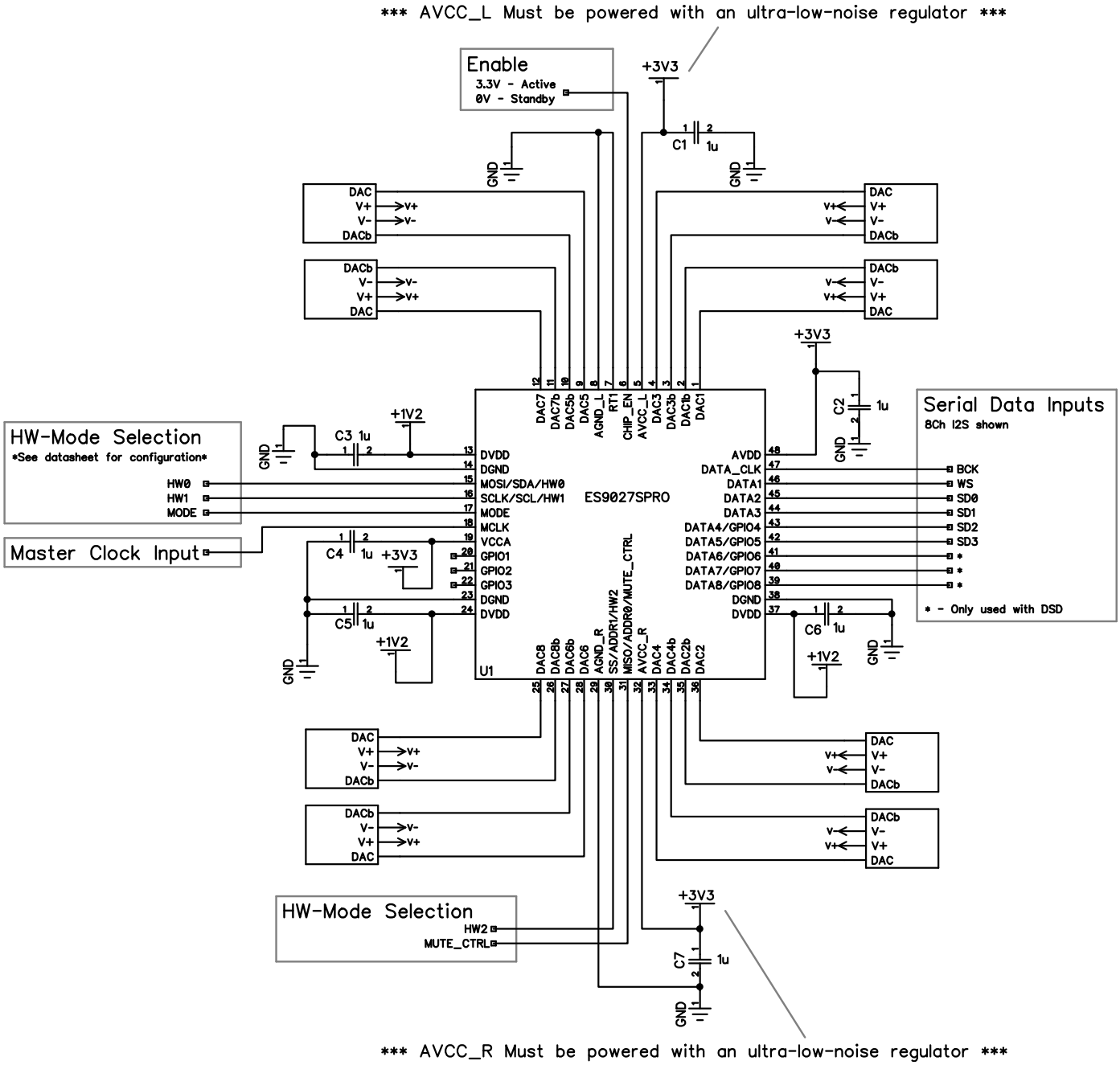


Figure 15 – ES9027SPRO Hardware mode reference schematic

*Note: The ES9027QPRO QFN package has an exposed pad (pin 49) that should be connected to ground.

Software Mode

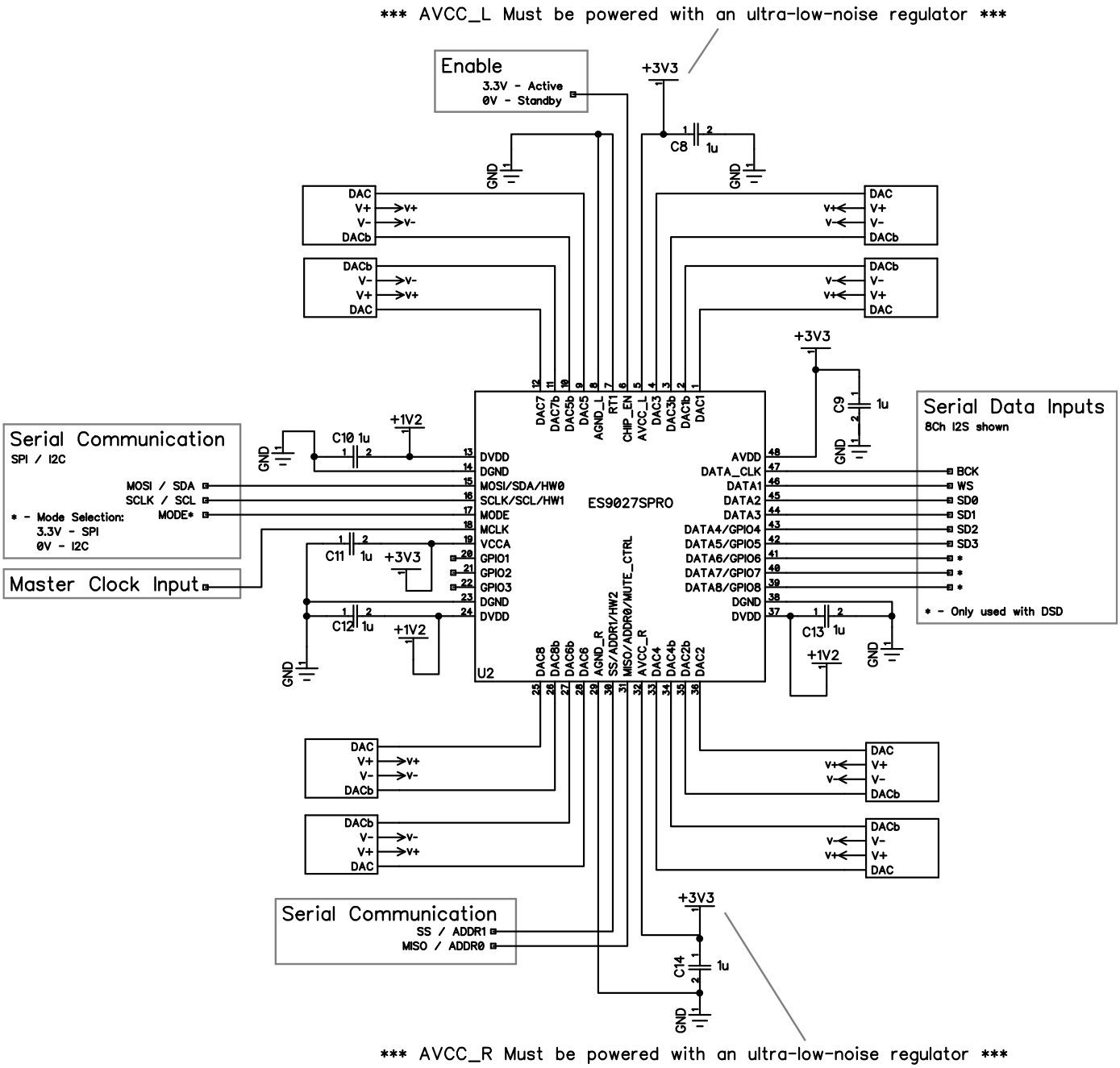


Figure 16 – ES9027SPRO Software mode reference schematic

*Note: The ES9027QPRO QFN package has an exposed pad (pin 49) that should be connected to ground.

Reference Output Stage

This output stage is used on the ES9027PRO 1v1 evaluation boards to achieve the performance on this datasheet.

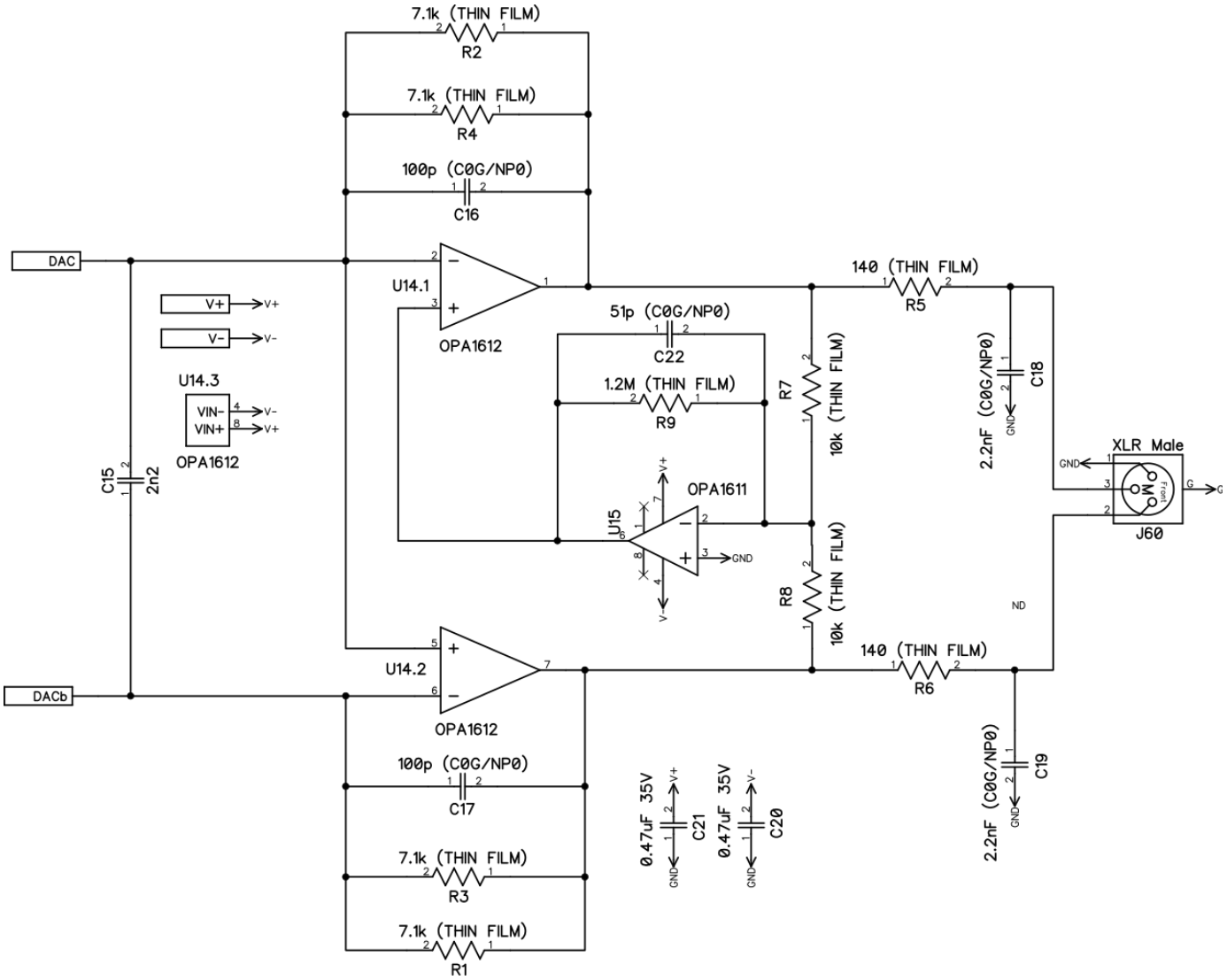
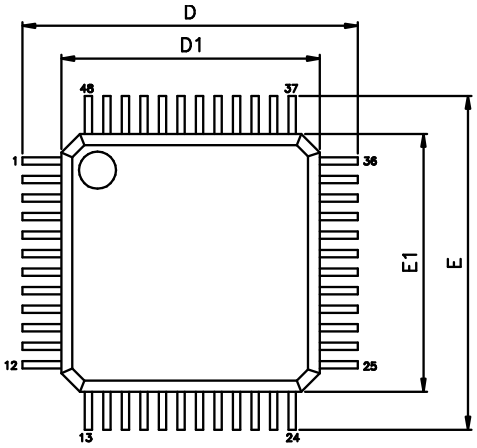


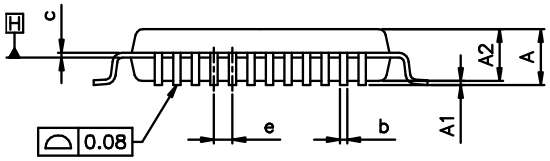
Figure 17 – Output stage reference schematic

48 QFP Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



NOTES:
1. JEDEC OUTLINE : MS-026 BBC
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

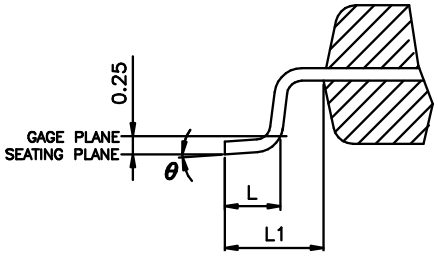
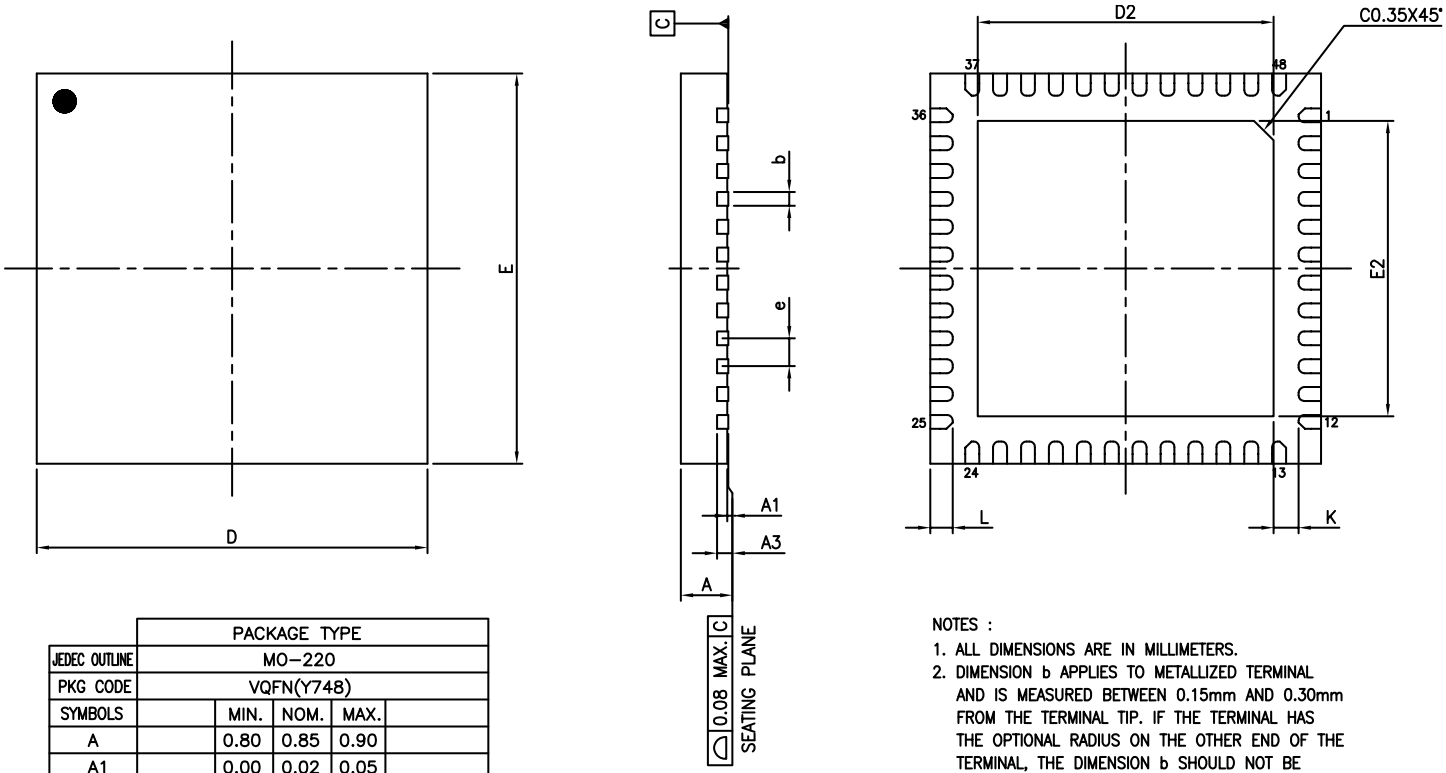


Figure 18 – ES9027SPRO 48 QFP package dimensions

48 QFN Package Dimensions



	PACKAGE TYPE				
JEDEC OUTLINE	MO-220				
PKG CODE	VQFN(Y748)				
SYMBOLS		MIN.	NOM.	MAX.	
A		0.80	0.85	0.90	
A1		0.00	0.02	0.05	
A3		0.203 REF.			
b		0.20	0.25	0.30	
D		7.00 BSC			
E		7.00 BSC			
e		0.50 BSC			
L		0.35	0.40	0.45	
K		0.20	–	–	

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
224X224 MIL	5.25	5.30	5.35	5.25	5.30	5.35	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 19 – ES9027QPRO 48 QFN package dimensions

48 QFP Top View Marking

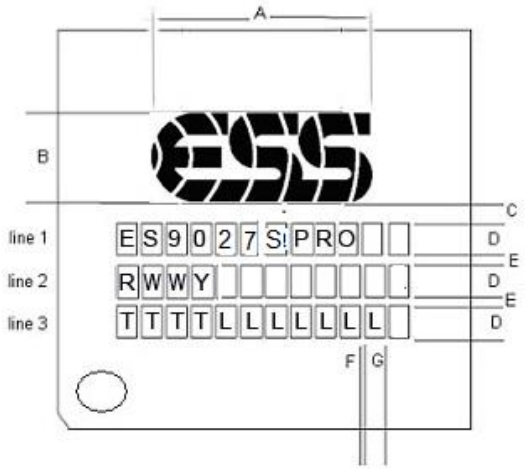


Figure 20 – ES9027SPRO Marking

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
48 LQFP 7mm x 7mm	5.0	2.0	0.3	0.56	0.2	0.08	0.33

T	*Tracking number*
W	*Work week*
Y	*Last digit of year*
L	*Lot number*
R	*Silicon Revision*

48 QFN Top View Marking

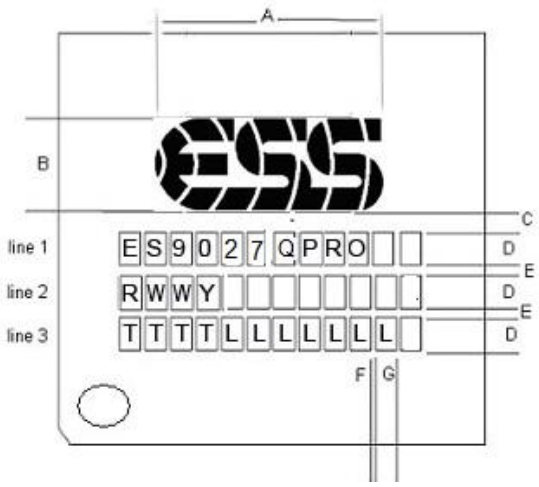


Figure 21 – ES9027QPRO Marking

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
48 QFN 7mm x 7mm	5.0	2.0	0.3	0.56	0.2	0.08	0.33

T	*Tracking number*
W	*Work week*
Y	*Last digit of year*
L	*Lot number*
R	*Silicon Revision*

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process – Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.
The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used. Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

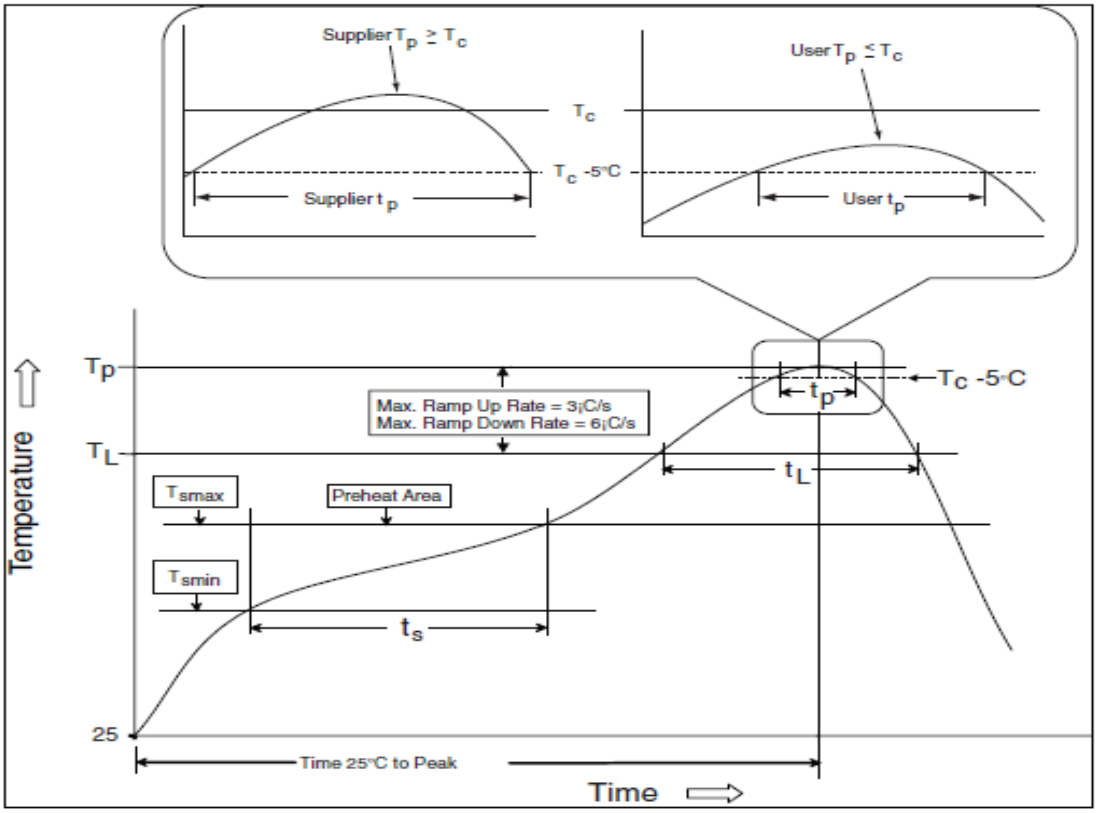


Figure 22 – IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 14 – RPC-1 Classification reflow profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 15 – RPC-2 Pb free classification temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9027SPRO	SABRE PRO 32-bit 8 Channel DAC	7mm x 7mm 48 QFP
ES9027QPRO • Inquire for availability	SABRE PRO 32-bit 8 Channel DAC	7mm x 7mm 48 QFN

Revision History

Current Version 0.4.1

Rev.	Date	Notes
0.1	March 25th, 2022	Initial release
0.2	June 5th, 2022	• Added Digital Signal path diagram • Updated the feature list & functional block diagram • Added QFN package dimensions & markings • Updated Hardware Mode Setup Sequence • Updated ordering information • Updated register listings including MQA Config register • Updated Hardware mode pin configuration table • Updated Performance table
0.3.1	August 11th, 2022	• Added Digital Filter characteristics and latency table • Updated Registers 1[6],5,58[4:3],64-71,82-84,130, and others • Updated Feature list • Updated HW mode table & added HW feature tables • Updated digital signal path diagram • Updated performance data • Updated output stage reference schematic
0.4.1	November 17, 2022	• Added correct register listing defaults for TDM_CHx_CONFIG reigsters • Clarified description of data lines for TDM_CHx_LINE_SEL • Updated Audio Input Formats • Added missing SPI commands to SPI section • Changed labeling of MSB Justified to Left Justified • Added Timing Requirements section, I2C Slave Timing section title • Changed Output stage (for Reference) to Recommended output stage • Removed ES9027MPRO device, device not available • Reserved Register 90[2] • Updated Digital Signal Path figure • Revised I2C, SPI drawings • Added note on DoP (HW modes 16-18) usage in HW mode to Hardware Mode Pin Configurations • Unreserved Register 89[2:0] IIR_BW • Updated some register descriptions for clarity

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