GPX2-EVA-KIT

TDC-GPX2 Evaluation Kit

SC-001264-UG User Guide

GPX2-EVA-Kit User Guide

Revision: 5

Release Date: 2021-01-25

Content Guide

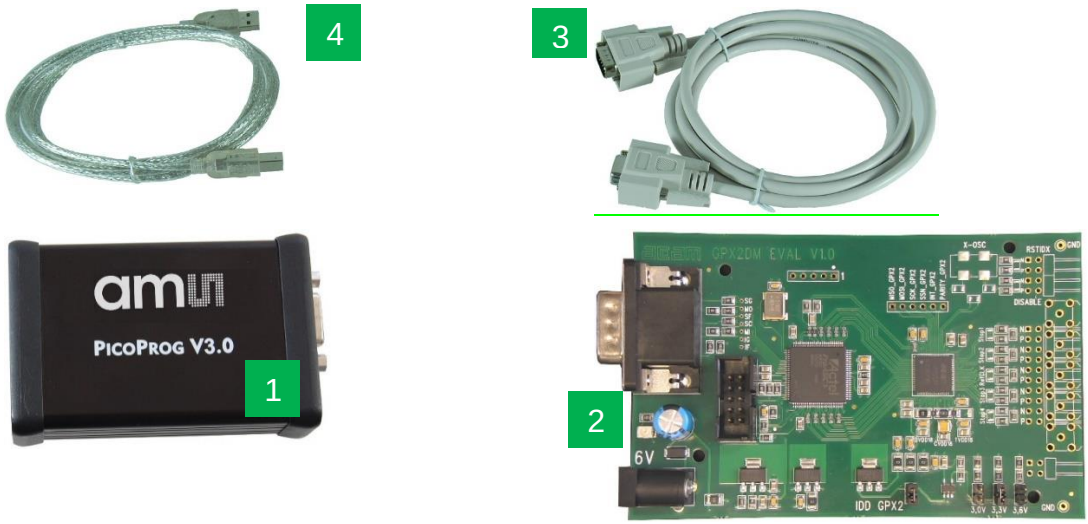
1 Introduction

The GPX2-EVA-KIT evaluation system is designed as a platform for a quick and easy start of evaluation of the TDC-GPX2 time-to-digital converter. The kit offers a graphical user interface for user-friendly configuration and extensive testing of the TDC-GPX2. For a proper use of the evaluation system, we strongly recommended to refer to the latest TDC-GPX2 datasheet.

Features are:

- PC supported system with USB communication interface
- Easy to use evaluation and measurement software
- Different power options, selectable by jumpers
- Three reference clock sources for alternate clock options
- Data collection to ASCII text files
- Visualization of measurement results

Figure 1: Kit Content



Pos.	Item	Comment
1	PICOPROG V3.0	Programmer and interface
2	GPX2-EVA BOARD	Based on TDC-GPX2, V1.0
3	High density DSUB15 cable	Connecting Evaluation board to programmer
4	USB cable	Connects PicoProg V3.0 to PC

1.1 Ordering Information

Ordering Code	Part Number	Description
GPX2-EVA-KIT	220310001	TDC-GPX2 Eval Kit for QFN40 version including PICOPROG and cables
GPX2-EVA-BOARD	220310003	TDC-GPX2 evaluation board for QFN64

2 Quick Start Guide

This section describes how to set up the GPX2-EVA-KIT, establish basic operation and make measurements quickly.

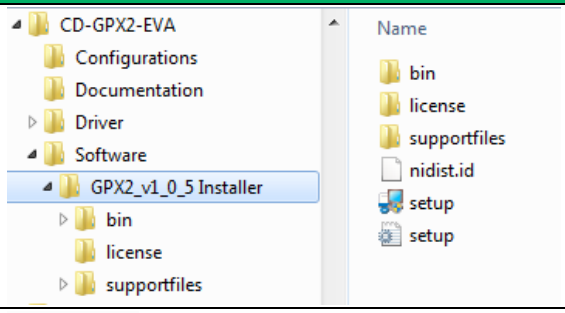
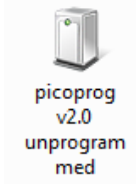
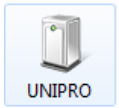
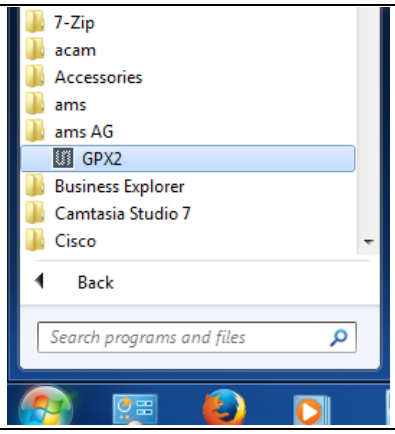
2.1 Install the Software

Please download the latest software for the kit from:

Link: https://downloads.sciosense.com/tdc-gpx2/

It is crucial to install the software before connecting the evaluation kit to your computer. A default driver loading of your OS may interfere with correct installation.

Figure 2: Installation steps

Step	Screen
Download the latest software installation package to the desired directory. Unzip the package to the desired directory. Open “setup.exe” from the unzipped directory. Follow the instructions on the screen.	
When connecting the PicoProg to the USB port it will be listed first as “picoprog v2.0 un-programmed” device. This is true also for PicoProg V3.0.	
Starting the software will download a special firmware into the PICOPROG, picoprog_gpx2_v005.hex or higher, and the device will now be listed as “UNIPRO”:	
St Open the START Menu and open the software from C:\Program files\…\GPX2\GPX2 Frontpanel	

2.2 Install the Hardware:

- Make sure software is installed correctly before proceeding with this step!
- Connect your computer with the PicoProg V3.0 using USB cable.
- Connect PicoProg V3.0 and the evaluation kit motherboard using the DB15 interfaces or directly.
- Connect the power supply. Make sure it is set to 6 V supply voltage.
- The green LED on the evaluation kit should be on.
- Connect your signal source.

2.3 Software

- Execute the GPX2 Frontpanel Software. The communication status should be green
- The software starts with an initial configuration, that can be opened the default configuration file config_default.cfg.
- Press “Power On Reset! – “Write Config” – “Init Reset”
- Press “Start Measurement”

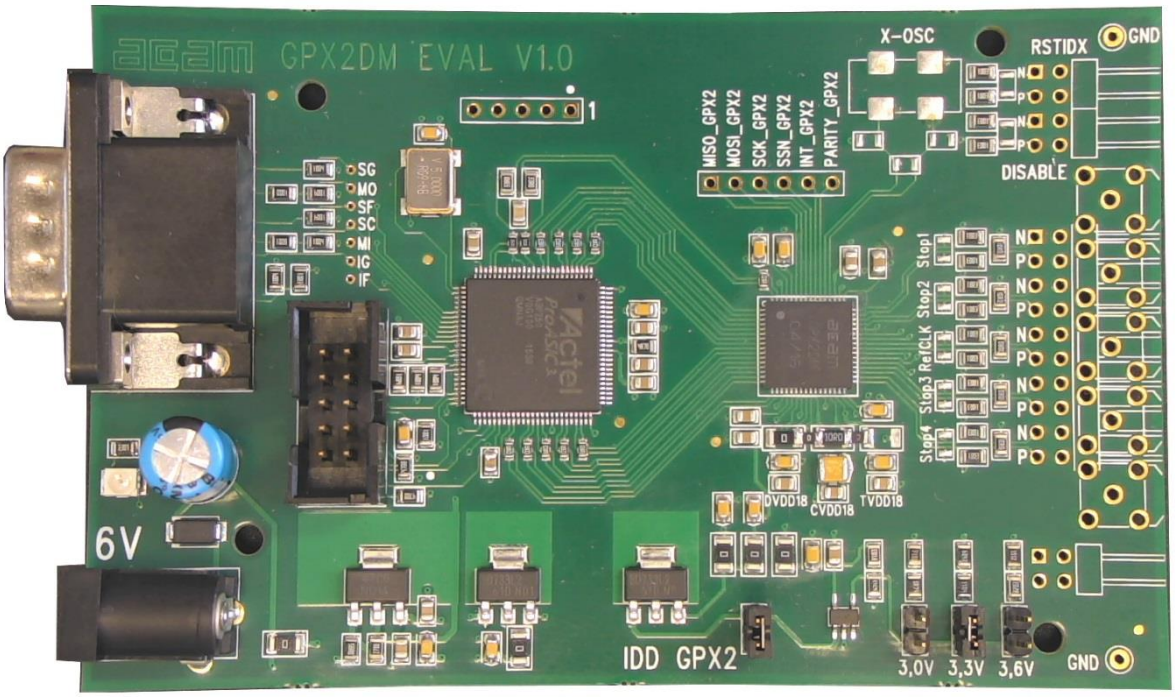
The measurement should run and results should be displayed now.

3 Hardware Description

3.1 Introduction

An on-board FPGA [1] manages the communication to the TDC-GPX [2]. It writes the configuration into the chip via the SPI interface and can use the same to read data. In addition, the FPGA manages the readout from the serial LVDS outputs of the TDC-GPX2. The SPI signals are available via additional pads [3]. A jumper selects the supply voltage as 3.0 V, 3.3 V or 3.6 V [4]. A separate jumper allows measuring the current into the TDC-GPX2 [5].

Figure 3: GPX2-EVA-BOARD



Solder pads are prepared to apply an external oscillator. This may be used as a reference instead of the RefClk input. [6]

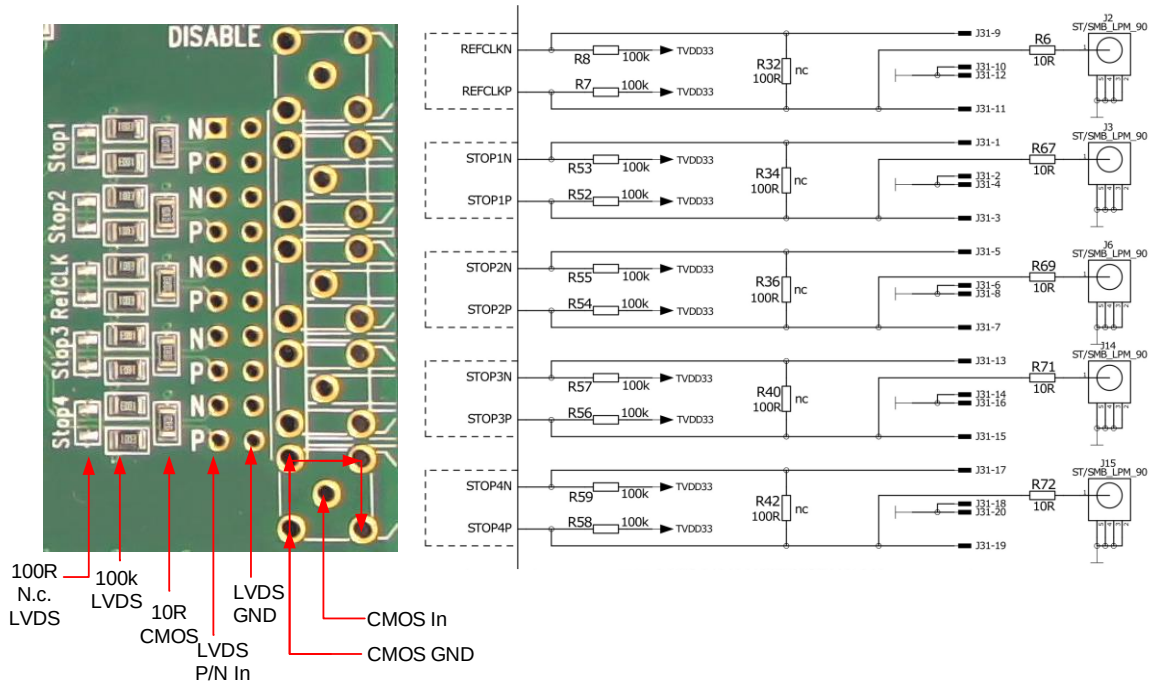
Further, solder pads are available to connect the signal lines. Here the user may solder cables directly, apply pin connectors, or in case of CMOS signals pads for SMB connectors are prepared.

Note: The FPGA manages the SPI communication and blocks the lines. Therefore, if you want to communicate directly with TDC-GPX2 via SPI [3] then remove 0Ohm resistors R75, R76 and R77 first [7].

3.2 Input Signals lines

The board is prepared to connect directly CMOS input signals or LVDS signals.

Figure 4: Input section



3.2.1 CMOS Inputs

On the board there is a 10 Ohm series resistor.

3.2.2 LVDS Inputs

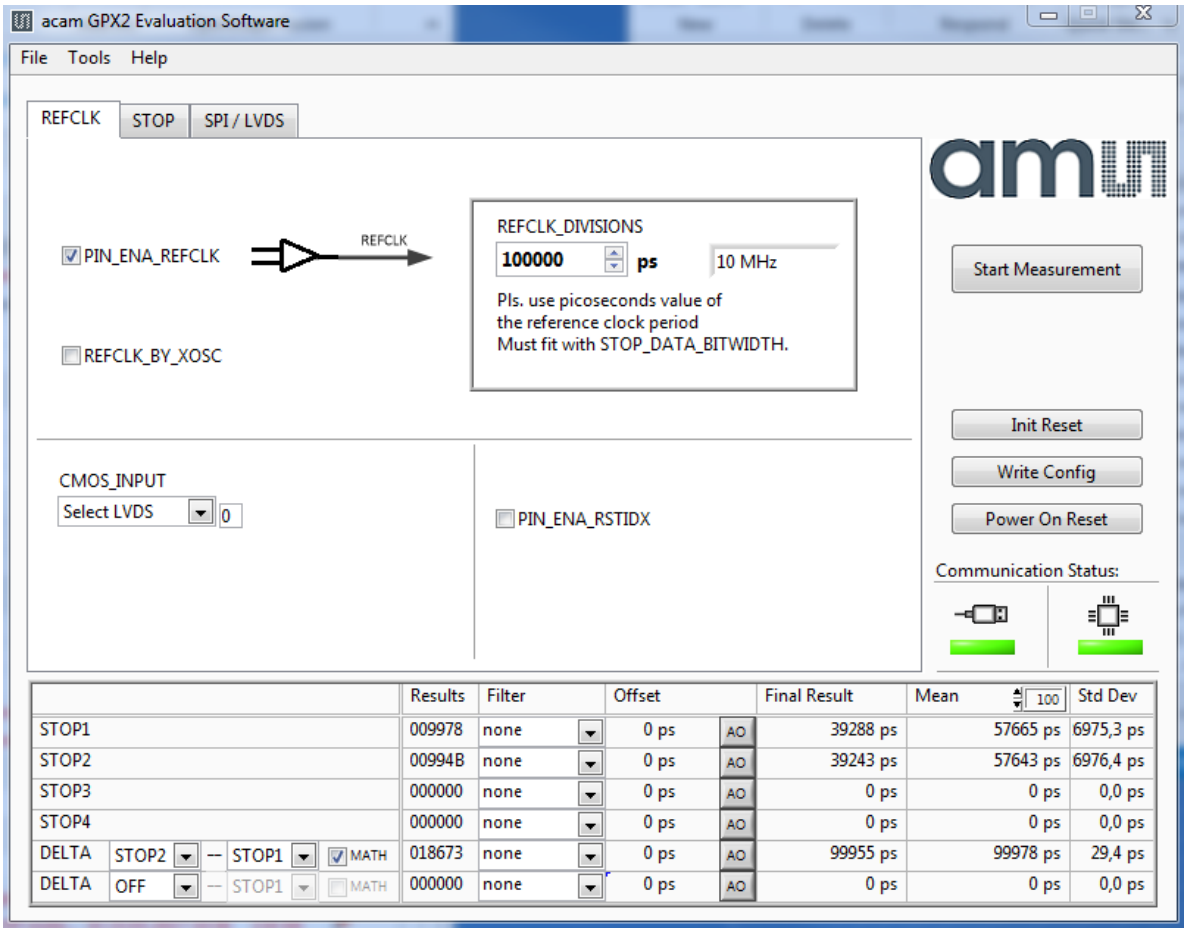
On the board there are 100kOhm pull-up resistors to TVDD33. The resistors interconnecting P and N inputs are not assembled.

4 Software Description

4.1 Main Window, REFCLK Page

The software will start with the following main window:

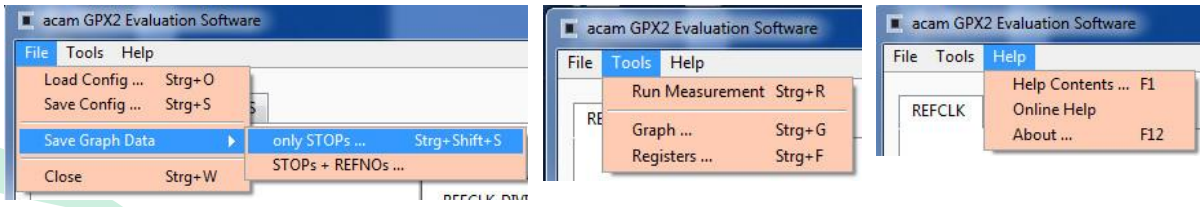
Figure 5: GPX2 evaluation software main window



The main menu offers the typical functions to load and save configurations, to run a measurement, to open the graph and register windows as well as a help.

The two figures on the right indicate the communication status. Both bar indicators should be green.

Figure 6: Menu selections



As a first step we recommend to load the standard configuration config_default.cfg, then press “Power On Reset”, “Write Config” and “Init Reset”.

The first page, “REFCLK”, allows the user to select the reference input as well as the definition of the LSB. REFCLK_DIVISIONS defines the LSB at the output interface as fraction of the reference

clock period. The most convenient way is applying an LSB of 1ps by configuring REFCLK_DIVISIONS to the picosecond value of the reference clock period.

In the middle section the user selects between CMOS and LVDS.

At the bottom, visible on all tabulators, is the numerical display of the measurement results STOP1 to STOP2. In addition, the software allows to calculate the difference between two stop results. The select box “Math” defines the formula:

Calculation Formula:

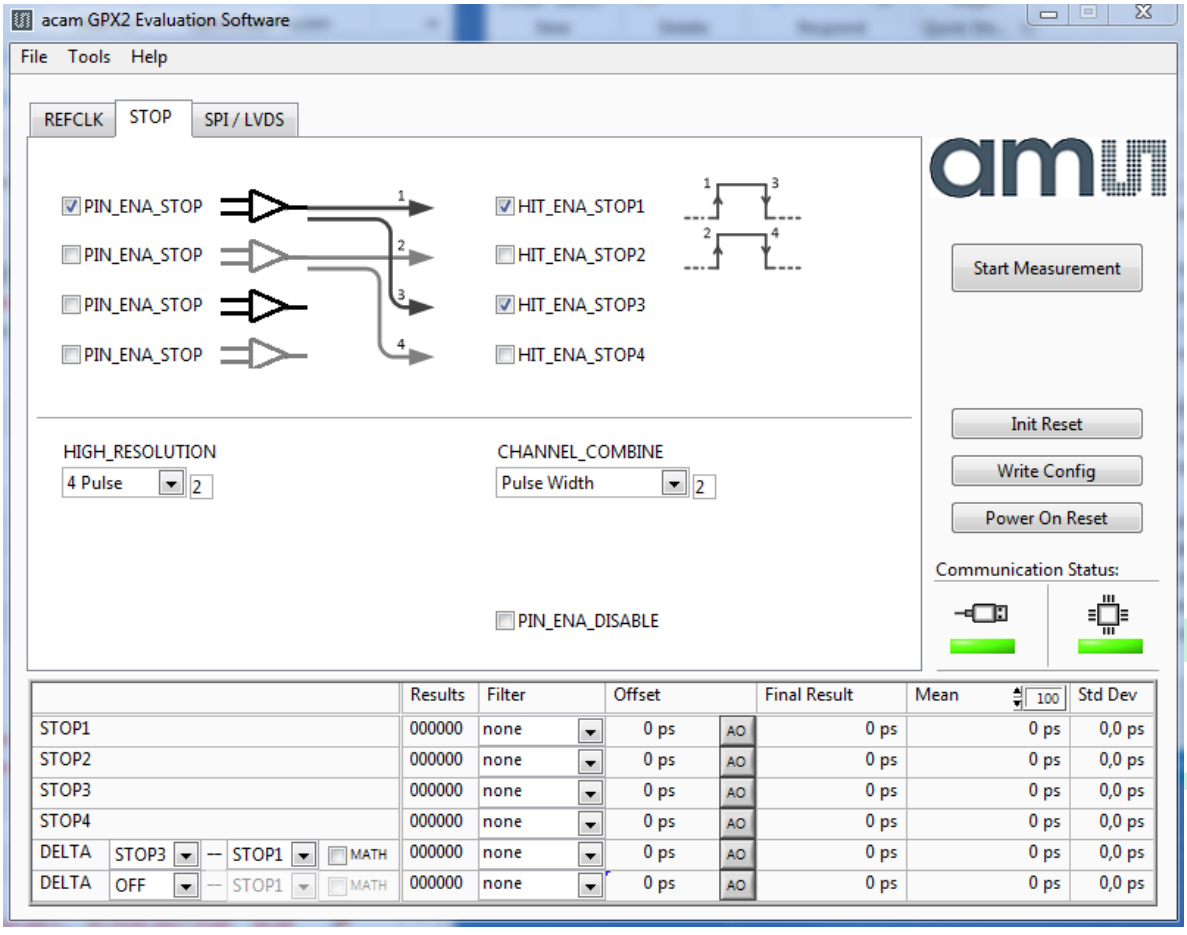
- On: [STOP1 - STOP2]
- Off: [REFNO1 - REFNO2] * REFCLK_DIVISIONS + [STOP1 - STOP2]

Various software filters, sinc or median, can be applied.

4.2 STOP Page

This page is for the PIN and HIT enable selection as well as the high resolution and combined channel settings.

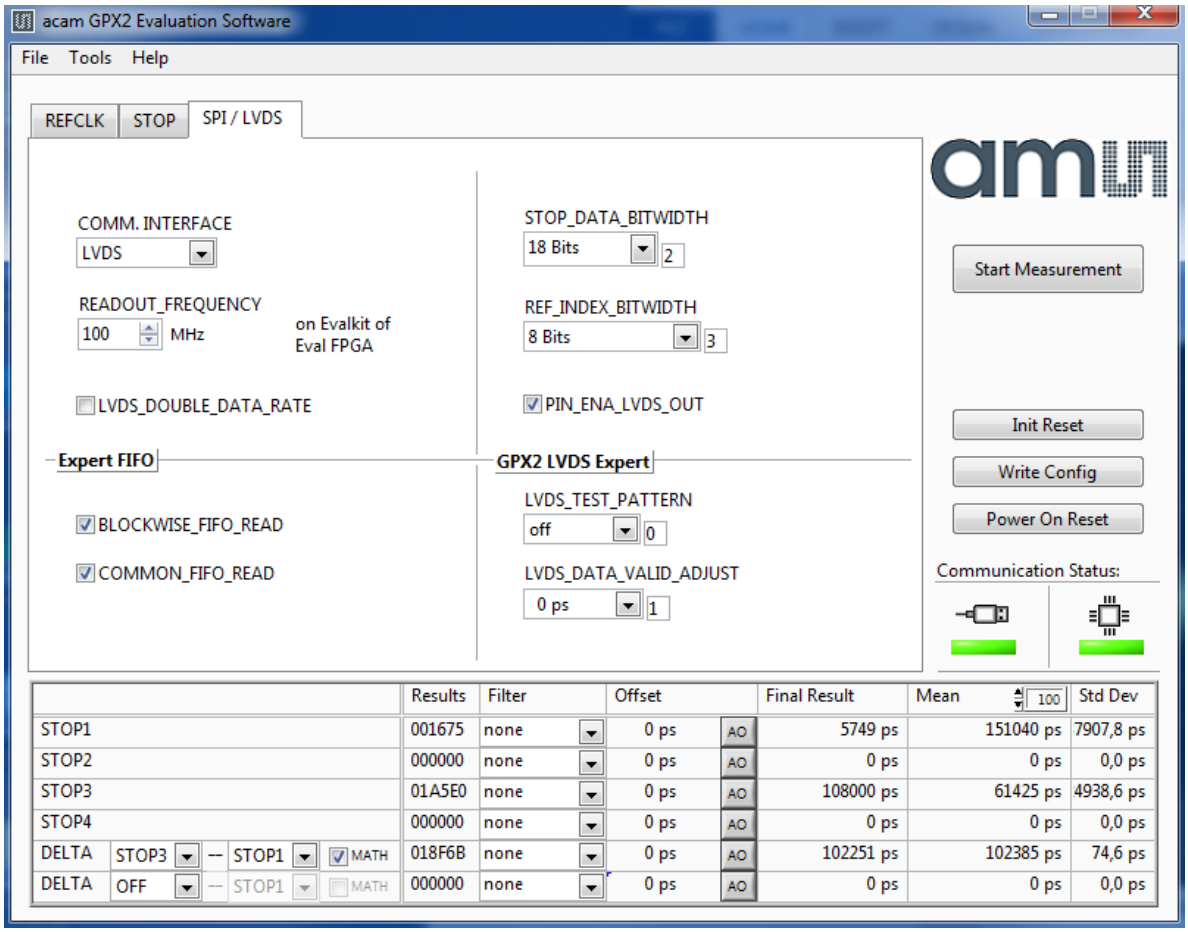
Figure 7: STOP page



4.3 Interface Page

On this page the communication as well as the output data format is defined. In any case, on the evaluation kit all communication is done via the on-board FPGA.

Figure 8: Interface page



Note: The read out speed of the evaluation software is much less than the TDC sample rate. Therefore, in most cases BLOCKWISE_FIFO_READ will give more reasonable display. In addition, often the difference between channels is of interest only and DELTA should be used for display. To have this calculated correctly, Math should be enabled.

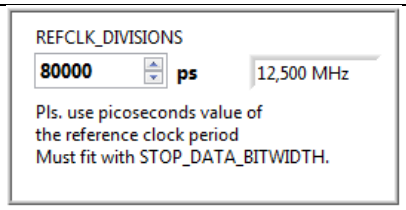
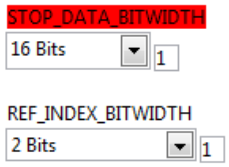
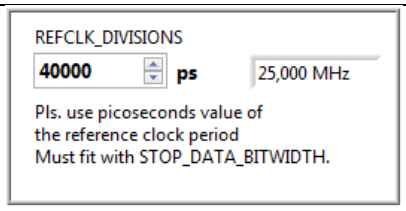
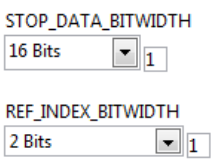
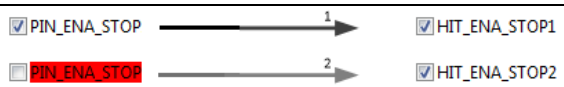
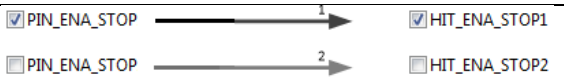
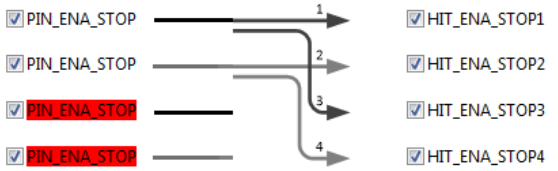
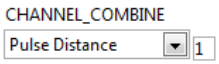
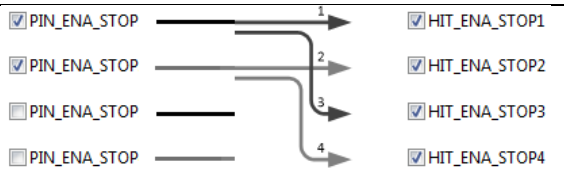
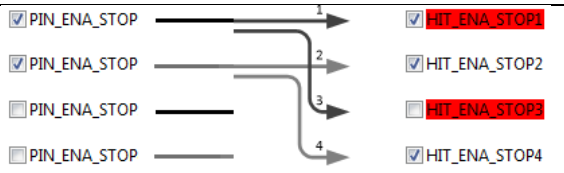
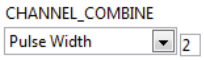
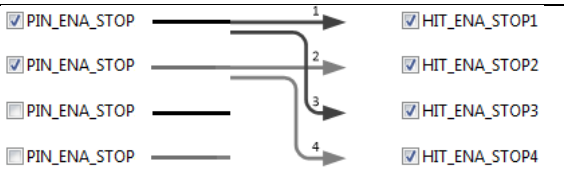
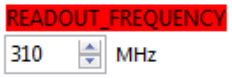
COMMOM_FIFO_READ helps if the same number of data from several channels is expected.

4.4 Avoiding Configuration Conflicts

Some combinations of parameter settings can prohibit operation or cause erroneous results. Some of these combinations are indicated with a red bar. User should avoid such configurations since the results may be difficult to interpret or faulty at all.

Some examples of configuration conflicts:

Figure 9: Avoiding conflicts

A	Bad		
	Good		
B	Bad		
	Good		
C	Bad		
	Good		
D	Bad		
	Good		
E		The LVDS readout frequency is recommended up to 360MHz in SDR mode only. Nevertheless 400 MHz is possible to configure and operate	

4.5 Register Content

A separate window shows the register content in the GUI and the TDC-GPX2. Separate pages display configuration data and result data. Changing the hexadecimal values will change the configuration in the GUI accordingly. With “Write Config” the updated configuration is downloaded into the chip.

Figure 10: Registers Window: Configuration

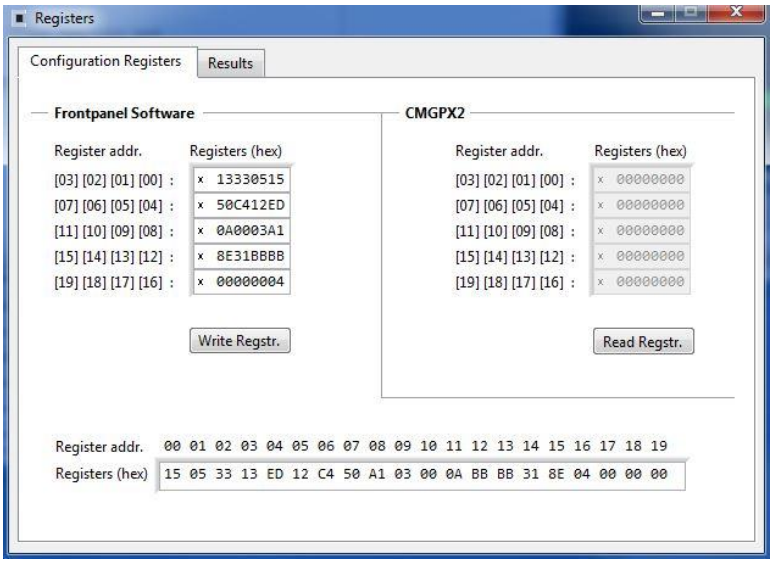
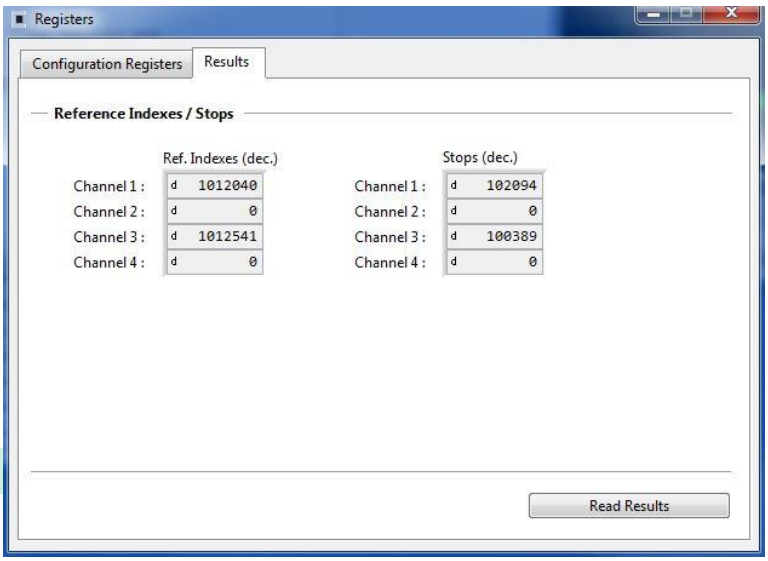


Figure 11: Registers Window: Results

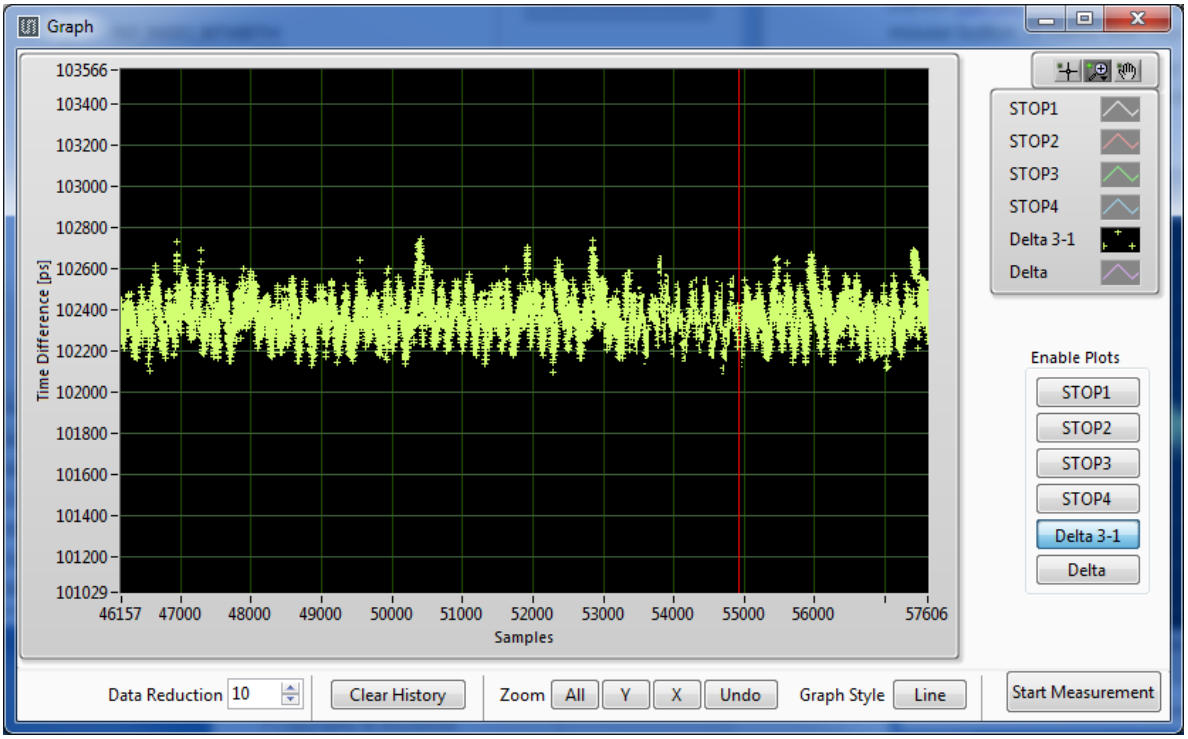


4.6 Graph Window

The graphical display allows to select which data shall be displayed. The shape of the individual curves can be modified individually. Move the mouse over the line symbol and press the right mouse button. A menu with many options will pop up.

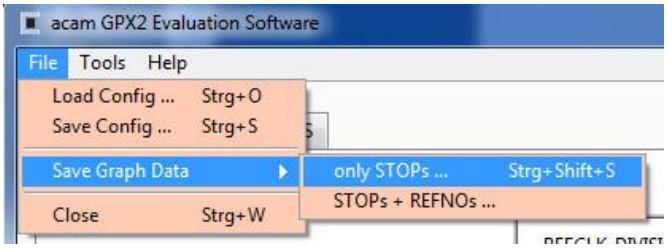
There are dedicated buttons for zoom to all or zoom in X or Y only. In addition, the standard Labview zoom functions are available (see the icons on the top right).

Figure 12: Graph Window



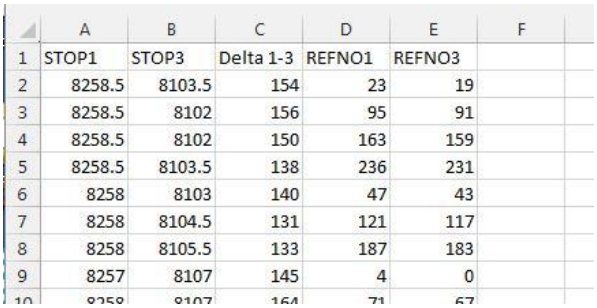
The displayed data can be exported into a text file. The maximum is 128,000 data sets.

Figure 13: Save data menu



The text file can then be analyzed with a table calculation program.

Figure 14: Exported data format



	A	B	C	D	E	F
1	STOP1	STOP3	Delta 1-3	REFNO1	REFNO3	
2	8258.5	8103.5	154	23	19	
3	8258.5	8102	156	95	91	
4	8258.5	8102	150	163	159	
5	8258.5	8103.5	138	236	231	
6	8258	8103	140	47	43	
7	8258	8104.5	131	121	117	
8	8258	8105.5	133	187	183	
9	8257	8107	145	4	0	
10	8258	8107	164	71	67	

4.7 Known Errors

- Software Hang-up
    - Occasionally, typically during tests in the temperature chamber, it may happen that the software hangs up. This is most likely to erroneous reading from the FIFO and related in the FPGA. The error will be removed in the next revision of the FPGA.

5 Schematics, Layers and BOM

Figure 15: GPX2-EVA BOARD Schematics 1

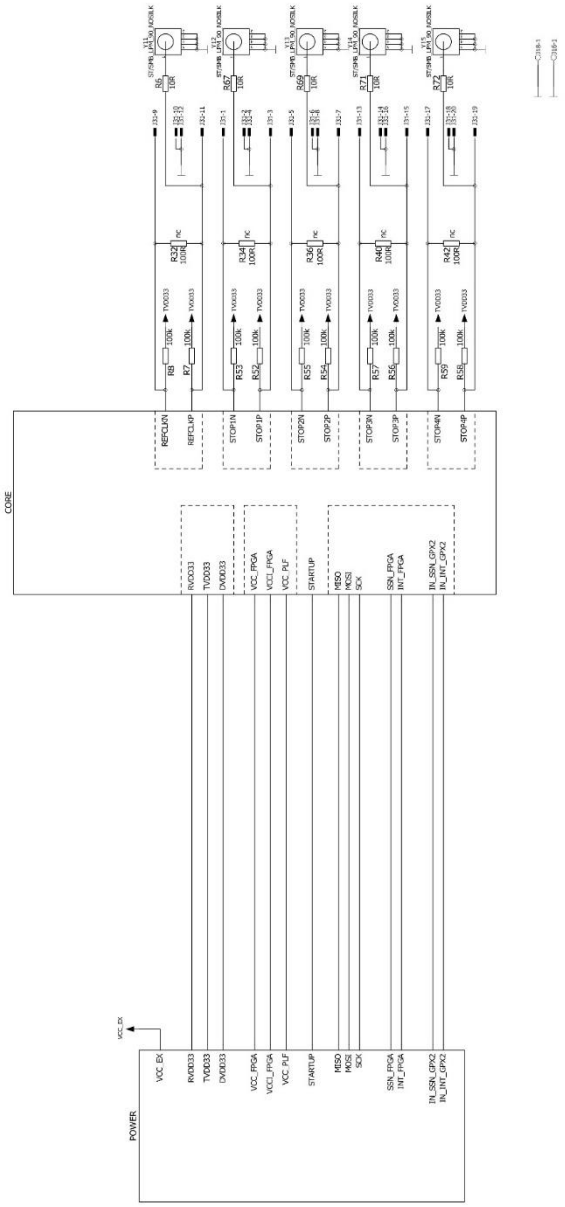


Figure 16: GPX2-EVA BOARD Schematics 2

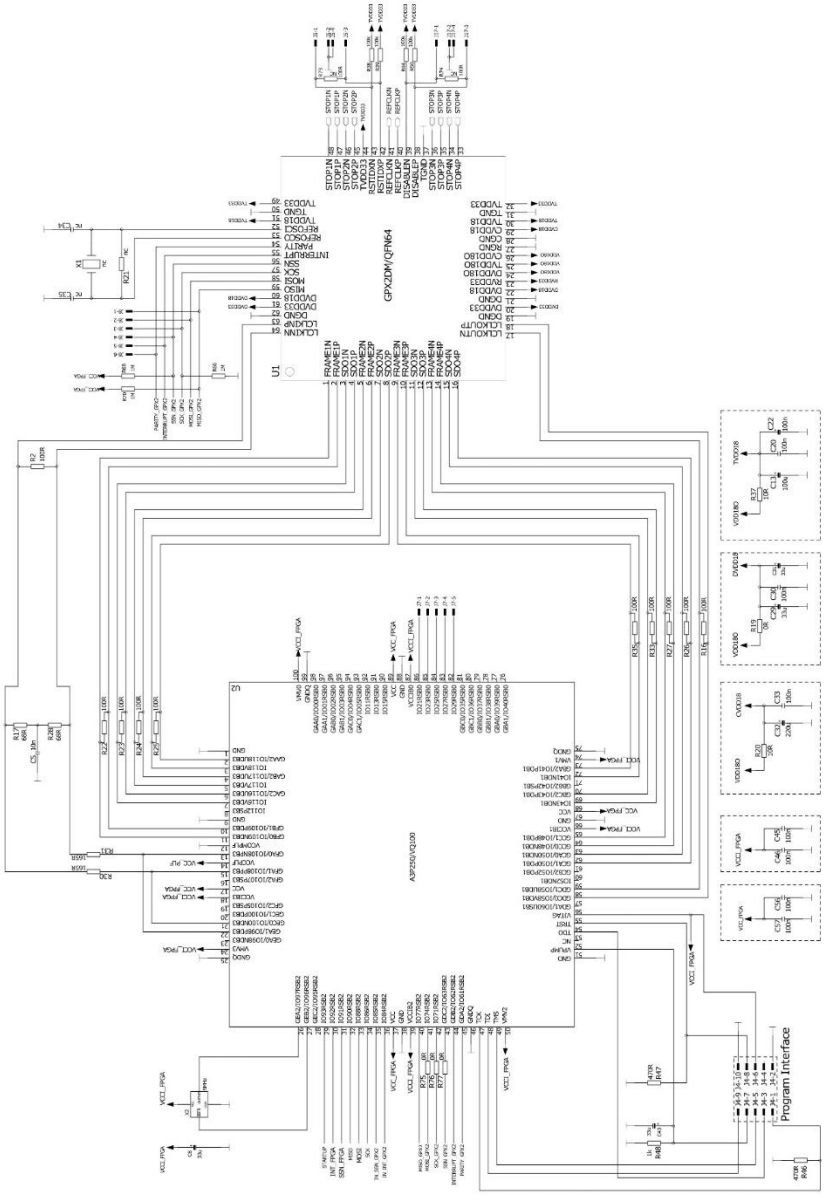


Figure 17: GPX2-EVA BOARD Schematics 3

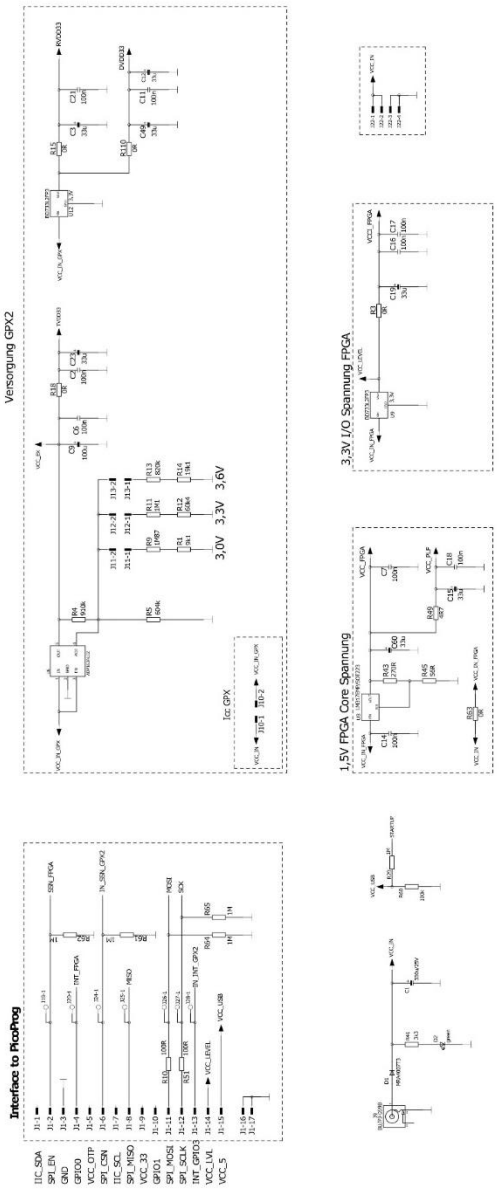


Figure 18: GPX2-EVA BOARD Layout: Top layer

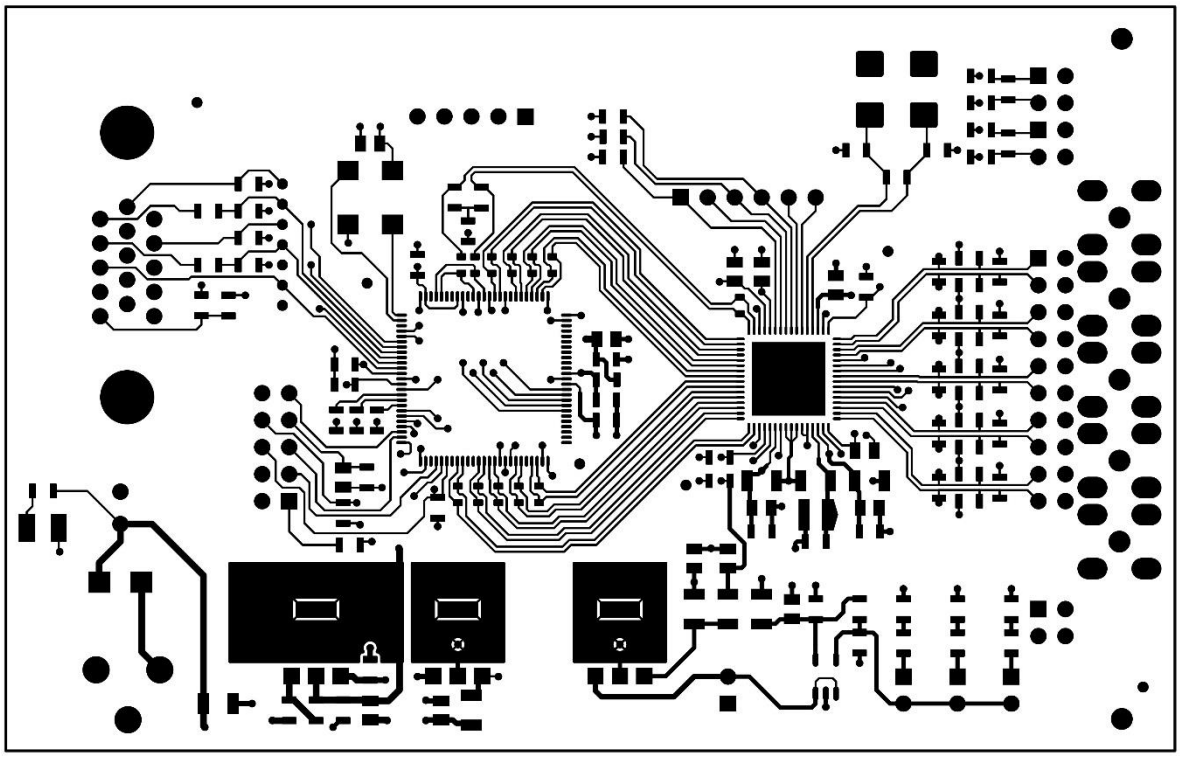


Figure 19: GPX2-EVA BOARD Layout: GND Layer

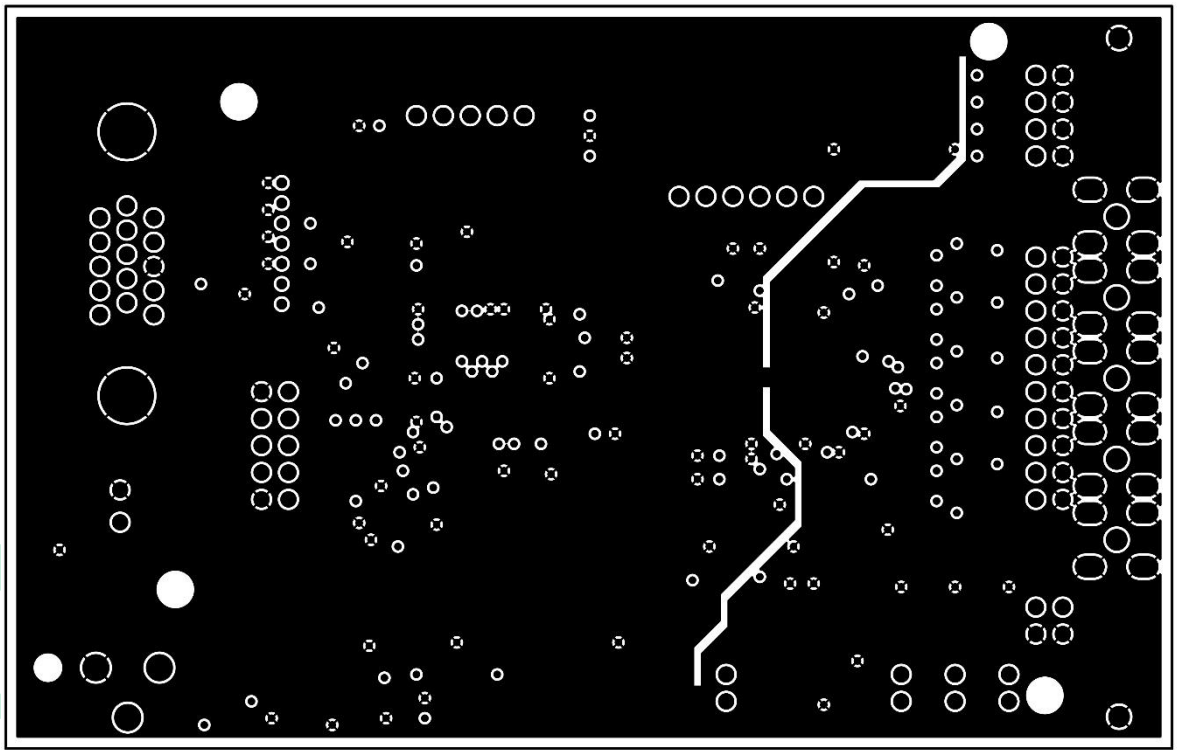


Figure 20: GPX2-EVA BOARD Layout: VDD Layer

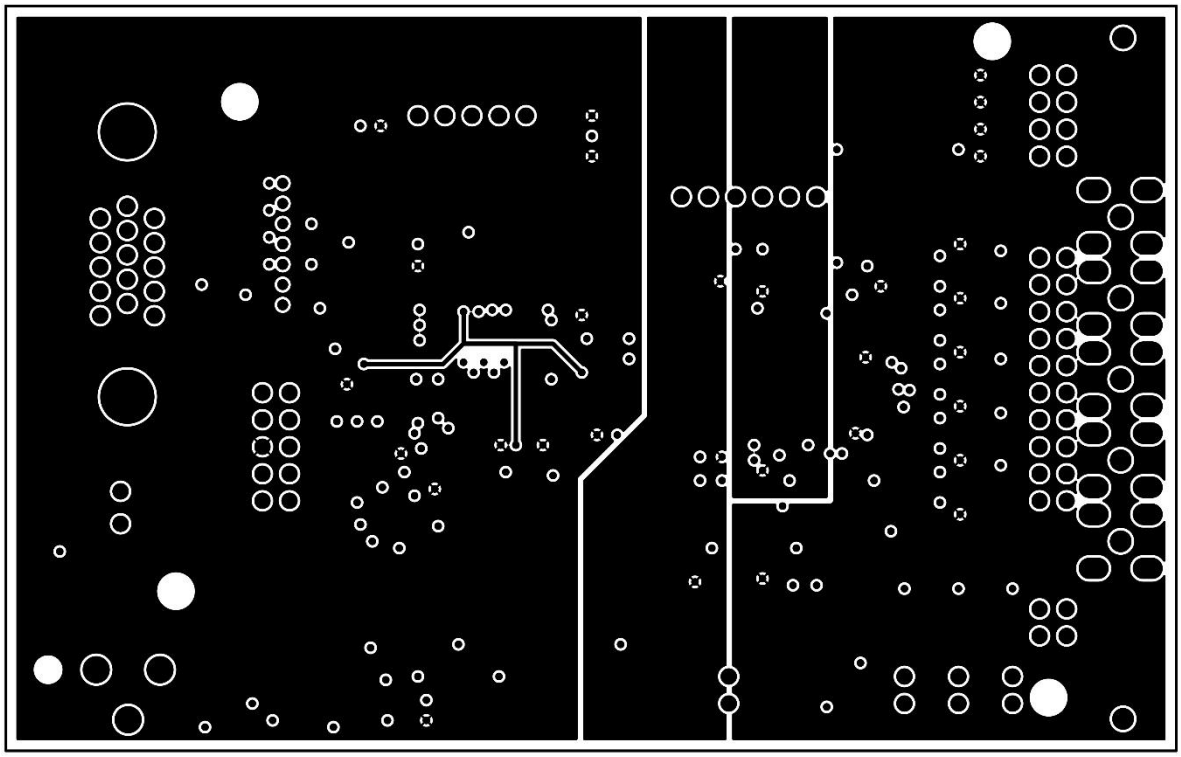


Figure 21: GPX2-EVA BOARD Layout: Bottom layer

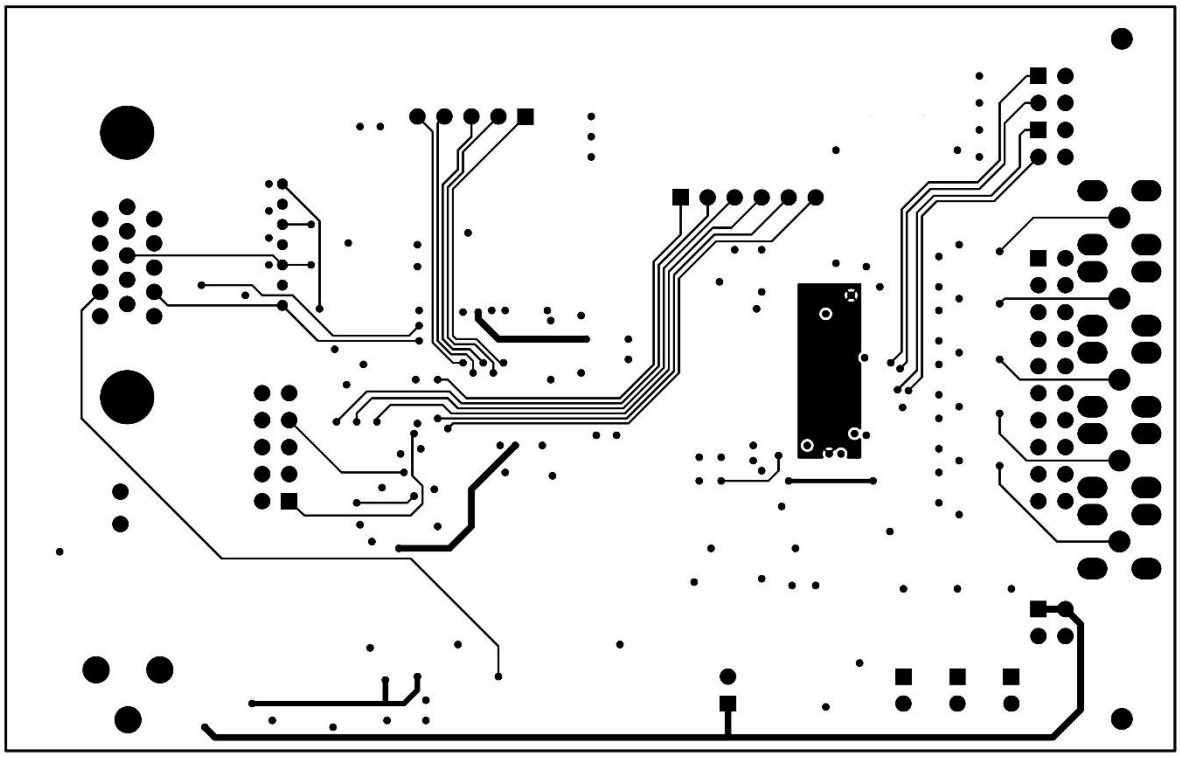


Figure 22: GPX2-EVA BOARD Layout: Assembly layer

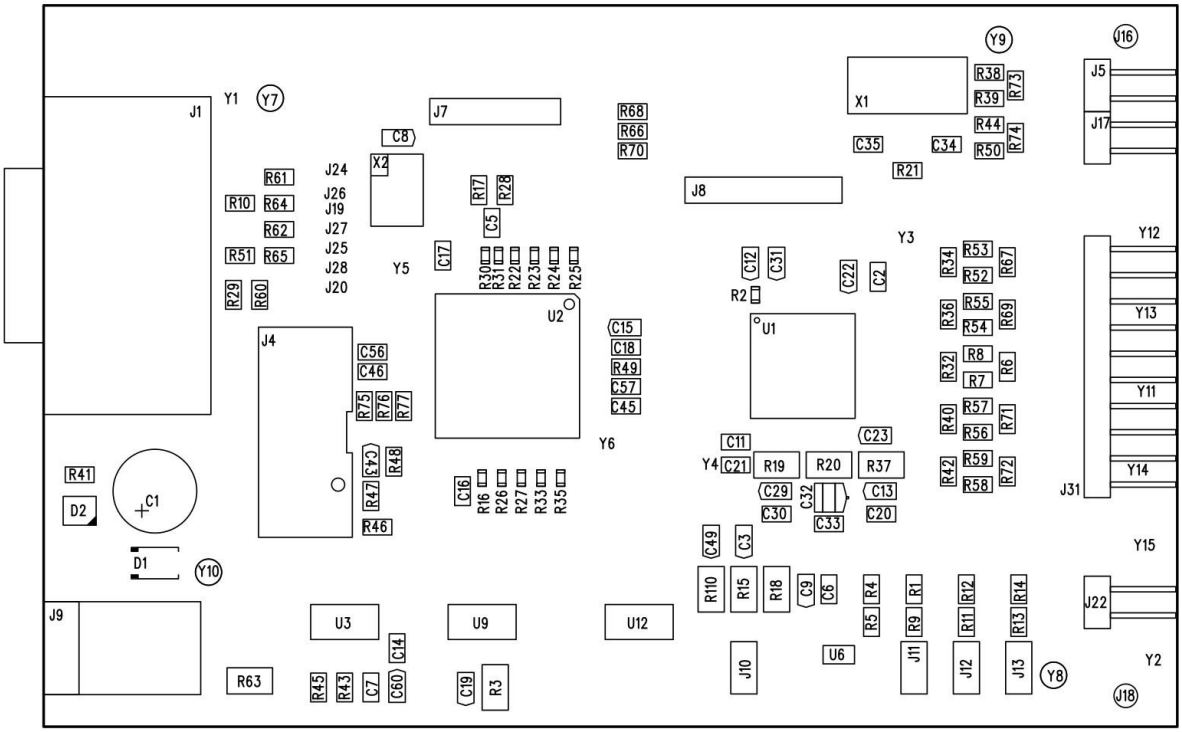


Figure 23: Bill of Materials for GPX2-EVA BOARD

QTY	DESIGNATOR	VALUE	PART DESC	TYPE
1	C5	10n	CHIP-CAPACITOR 0805	
17	C2 C6 C7 C11 C14 C16 C17 C18 C20 C21 C22 C30 C33 C45 C46 C56 C57	100n	CHIP-CAPACITOR 0805	
11	C3 C8 C12 C15 C19 C23 C29 C31 C43 C49 C60	33u	TANTAL	F950J336MPAAQ2
2	C9 C13	100u	TANTAL	F950J107MPAAQ2
1	C32	220u	TANTAL	F950J227MBAAM1Q2
1	C1	330u/25V	ELECTROLYTIC CAPASITOR	Radial 8mm Raster 2,5mm
10	R2 R16 R22 R23 R24 R25 R26 R27 R33 R35	100R	CHIP-RESISTOR 0603	
2	R30 R31	165R	CHIP-RESISTOR 0603	
3	R75 R76 R77	0R	CHIP-RESISTOR 0805	
1	R49	4R7	CHIP-RESISTOR 0805	
5	R6 R67 R69 R71 R72	10R	CHIP-RESISTOR 0805	
1	R45	56R	CHIP-RESISTOR 0805	
2	R17 R28	68R	CHIP-RESISTOR 0805	
2	R10 R51	100R	CHIP-RESISTOR 0805	

1	R43	270R	CHIP-RESISTOR 0805	
2	R46 R47	470R	CHIP-RESISTOR 0805	
1	R48	1k	CHIP-RESISTOR 0805	
1	R41	3k3	CHIP-RESISTOR 0805	
1	R1	9k1	CHIP-RESISTOR 0805	
1	R14	19k1	CHIP-RESISTOR 0805	
1	R12	60k4	CHIP-RESISTOR 0805	
15	R7 R8 R38 R39 R44 R50 R52 R53 R54 R55 R56 R57 R58 R59 R60	100k	CHIP-RESISTOR 0805	
1	R5	604k	CHIP-RESISTOR 0805	
1	R13	820k	CHIP-RESISTOR 0805	
1	R4	910k	CHIP-RESISTOR 0805	
8	R29 R61 R62 R64 R65 R66 R68 R70	1M	CHIP-RESISTOR 0805	
1	R11	1M1	CHIP-RESISTOR 0805	
1	R9	1M87	CHIP-RESISTOR 0805	
6	R3 R15 R18 R19 R63 R110	0R	CHIP-RESISTOR 1206	
6	R20 R37	10R	CHIP-RESISTOR 1206	
1	D1		Recovery Power Rectifier	MRA4007T3
1	D2	green	Surface Mount LED PLCC2	SMTL2-PGC
1	X2	5MHz	Crystal Oscillator	KXO-V97
1	U1		GPX2	
1	U2		ProASIC3 Flash Family FPGA	A3P250VQG100
1	U3		Linear Voltage Regulator	LM317EMP
1	U6		Linear Voltage Regulator	ADP163AUJZ-R7
2	U9 U12		Linear Voltage Regulator 3,3V	BD733L2FP3-CE2
1	J1		Male Connector DSUB15HD 90°	618015330923
1	J4		Box Header Straight 10pin	1-1634688-0
1	J9		DC Power Jack	PJ-059B
4	J10 J11 J12 J13		Male Connector 2x1x180° 2,54	

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7 Document Status

Figure 24: Document Status

Document Status	Product Status	Definition
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ScioSense B.V. standard warranty as given in the General Terms of Trade.
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8 Revision Information

Figure 25: Revision History

Revision	Date	Comment	Page
4	2018-Oct-18	Update of download links for evaluation software package Jump in revision number from 1-03 to 4-00 to fit to a new document management system	
5	2021-01-25	Transfer to ScioSense format Download links updated	All

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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