

PJX8601

Complementary Enhancement Mode MOSFET – ESD Protected

Voltage

20 / -20V

Current

0.5A / -0.5A

Features

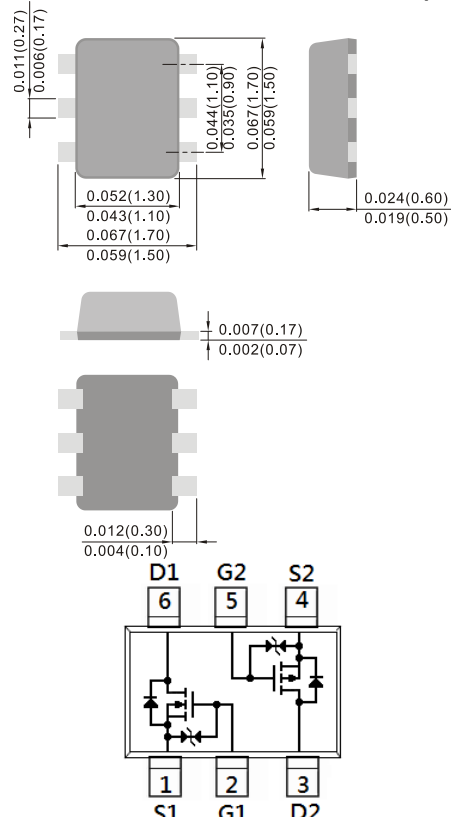
- Low Voltage Drive (1.2V)
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- ESD Protected
- Lead free in compliance with EU RoHS2.0 (2011/65/EU & 2015/865/EU directive)
- Green molding compound as per IEC61249 Std.. (Halogen Free)

Mechanical Data

- Case: SOT-563 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.00009 ounces, 0.026 grams

SOT-563

Unit: inch(mm)



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	N-Ch LIMIT	P-Ch LIMIT	UNITS
Drain-Source Voltage		V _{DS}	20	-20	V
Gate-Source Voltage		V _{GS}	±10	±10	V
Continuous Drain Current		I _D	0.5	-0.5	A
Pulsed Drain Current (Note 4)		I _{DM}	1.0	-1.0	A
Power Dissipation	T _a =25°C	P _D	300		mW
	Derate above 25°C		2.4		mW/°C
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55~150		°C
Typical Thermal Resistance - Junction to Ambient (Note 3)		R _{θJA}	417		°C/W



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N-Channel Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D = 250uA	20	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D = 250uA	0.3	0.64	0.9	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 4.5V, I _D = 500mA	-	0.31	0.4	Ω
		V _{GS} = 2.5V, I _D = 200mA	-	0.36	0.65	
		V _{GS} = 1.8V, I _D = 100mA	-	0.43	0.8	
		V _{GS} = 1.5V, I _D = 50mA	-	0.51	1.2	
		V _{GS} = 1.2V, I _D = 20mA	-	0.71	3.0	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V	-	±0.5	±10	uA
Dynamic (Note 5)						
Total Gate Charge	Q _g	V _{DS} =10V, I _D =500mA, V _{GS} =4.5V	-	1.4	-	nC
Gate-Source Charge	Q _{gs}		-	0.22	-	
Gate-Drain Charge	Q _{gd}		-	0.21	-	
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V, f=1.0MHZ	-	67	-	pF
Output Capacitance	C _{oss}		-	19	-	
Reverse Transfer Capacitance	C _{rss}		-	6	-	
Turn-On Delay Time	td _(on)	V _{DD} =10V, I _D =150mA, V _{GS} =4V, R _G =10Ω (Note 1,2)	-	2.8	-	ns
Turn-On Rise Time	tr		-	20	-	
Turn-Off Delay Time	td _(off)		-	23	-	
Turn-Off Fall Time	tf		-	23	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	500	mA
Diode Forward Voltage	V _{SD}	I _S = 500mA, V _{GS} =0V	-	0.87	1.3	V



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P-Channel Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-20	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.3	-0.6	-1.0	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-500mA	-	0.9	1.2	Ω
		V _{GS} =-2.5V, I _D =-200mA	-	1.07	1.5	
		V _{GS} =-1.8V, I _D =-100mA	-	1.25	2.2	
		V _{GS} =-1.5V, I _D =-40mA	-	1.42	3.6	
		V _{GS} =-1.2V, I _D =-10mA	-	1.7	6.0	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-16V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V	-	±2	±10	uA
Dynamic (Note 5)						
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-500mA, V _{GS} =-4.5V	-	1.4	-	nC
Gate-Source Charge	Q _{gs}		-	0.19	-	
Gate-Drain Charge	Q _{gd}		-	0.2	-	
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1.0MHZ	-	38	-	pF
Output Capacitance	C _{oss}		-	15	-	
Reverse Transfer Capacitance	C _{rss}		-	9	-	
Turn-On Delay Time	td _(on)	V _{DD} =-10V, I _D =-500mA, V _{GS} =-4.5V, R _G =6Ω (Note 1,2)	-	7.2	-	ns
Turn-On Rise Time	tr		-	21	-	
Turn-Off Delay Time	td _(off)		-	85	-	
Turn-Off Fall Time	tf		-	116	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	-500	mA
Diode Forward Voltage	V _{SD}	I _S =-500mA, V _{GS} =0V	-	-0.9	-1.3	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.

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N-Channel TYPICAL CHARACTERISTIC CURVES

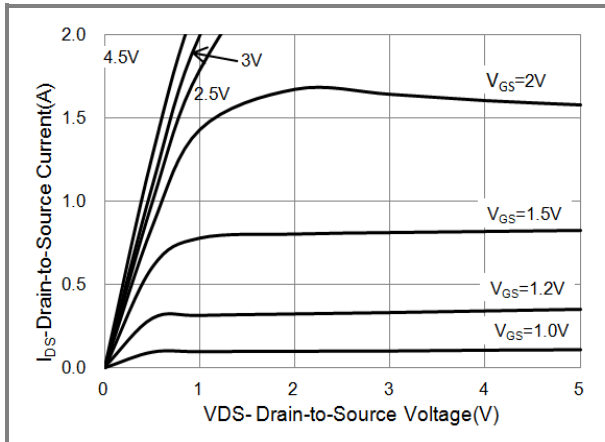


Fig.1 On-Region Characteristics

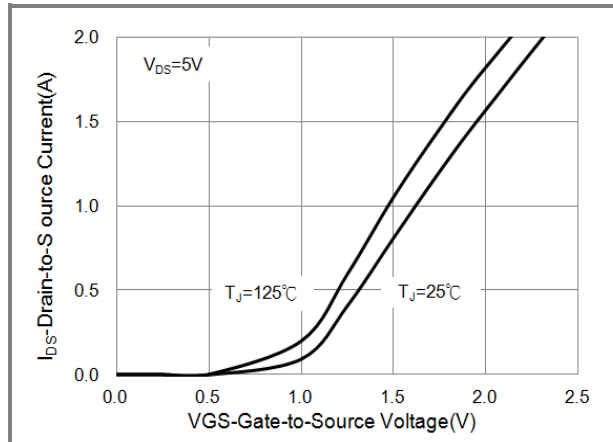


Fig.2 Transfer Characteristics

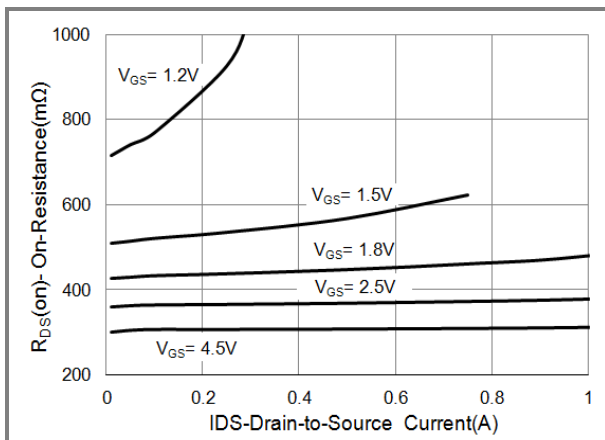


Fig.3 On-Resistance vs. Drain Current

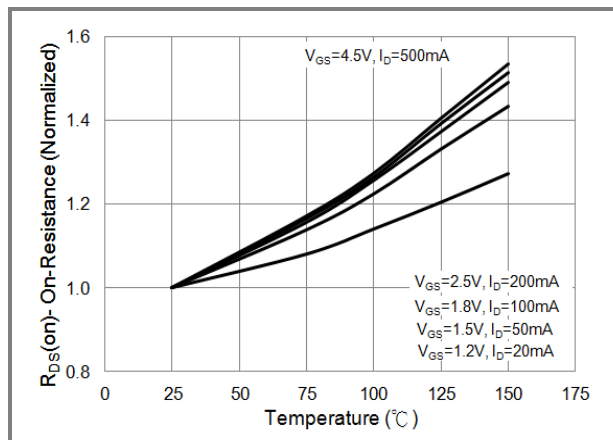


Fig.4 On-Resistance vs. Junction temperature

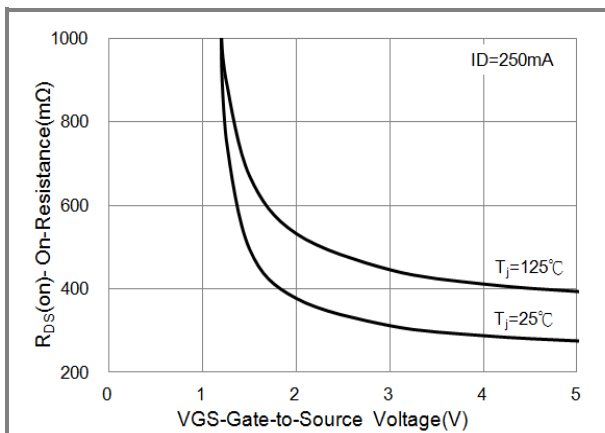


Fig.5 On-Resistance Variation with VGS.

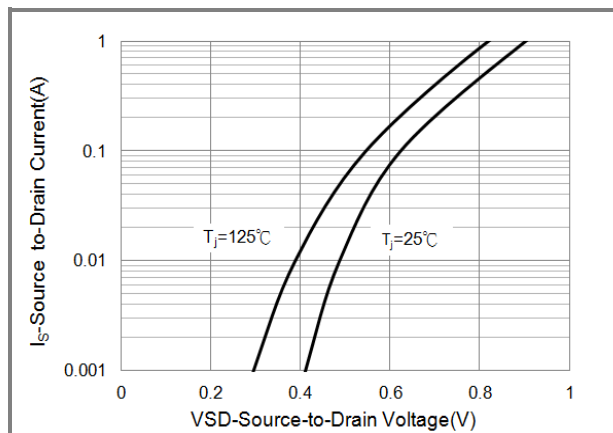


Fig.6 Body Diode Characteristics



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N-Channel TYPICAL CHARACTERISTIC CURVES

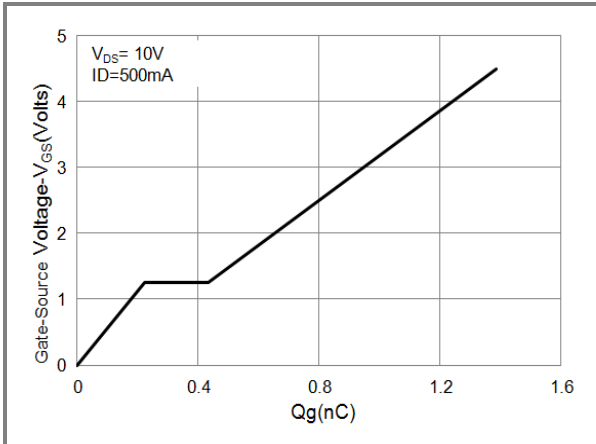


Fig.7 Gate-Charge Characteristics

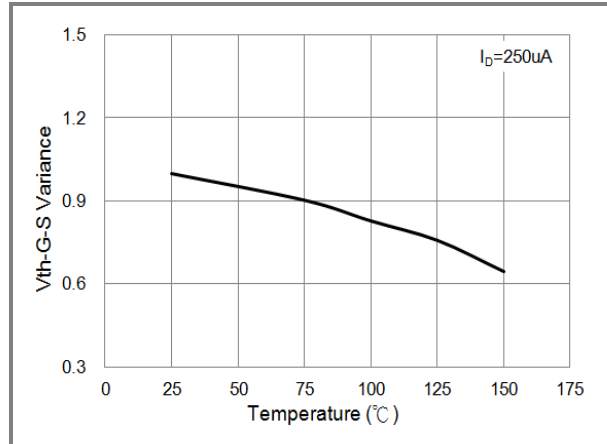


Fig.8 Threshold Voltage Variation with Temperature.

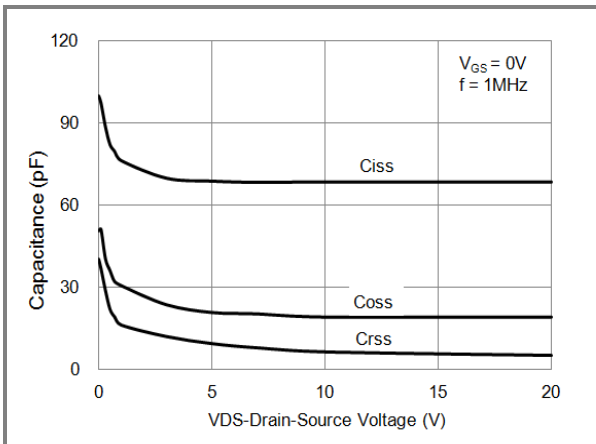


Fig.9 Capacitance vs. Drain-Source Voltage.

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P-Channel TYPICAL CHARACTERISTIC CURVES

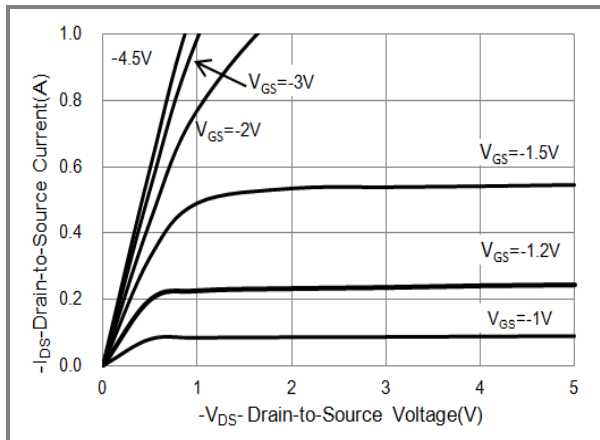


Fig.1 On-Region Characteristics

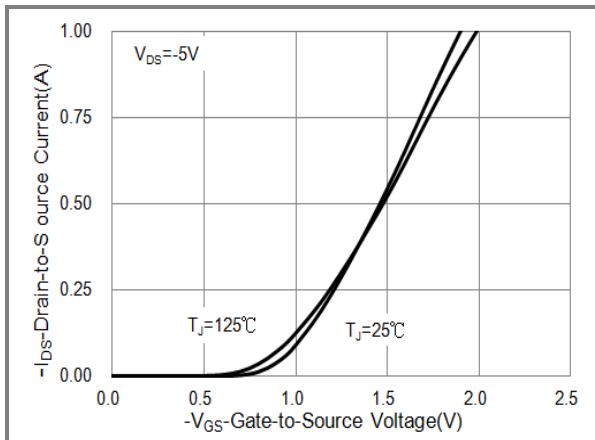


Fig.2 Transfer Characteristics

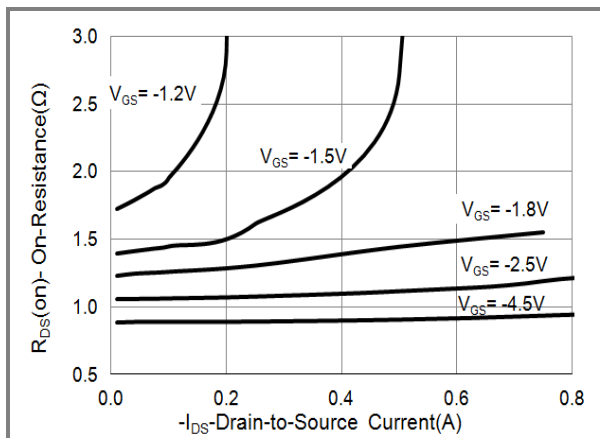


Fig.3 On-Resistance vs. Drain Current

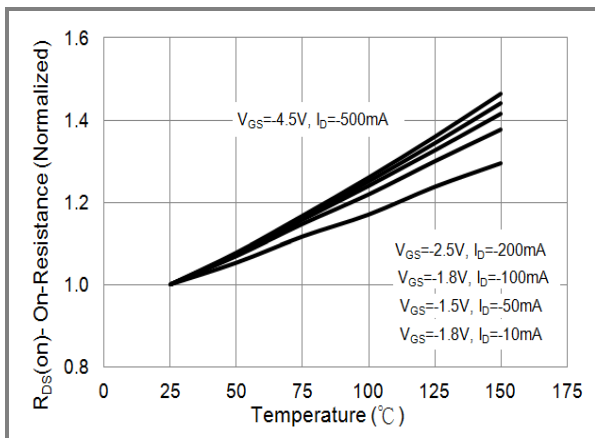


Fig.4 On-Resistance vs. Junction temperature

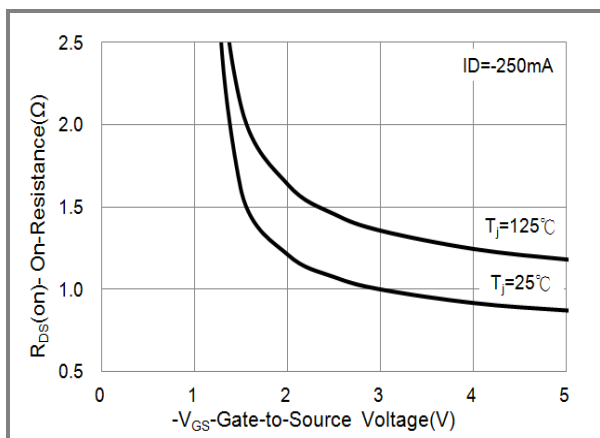


Fig.5 On-Resistance Variation with V_GS.

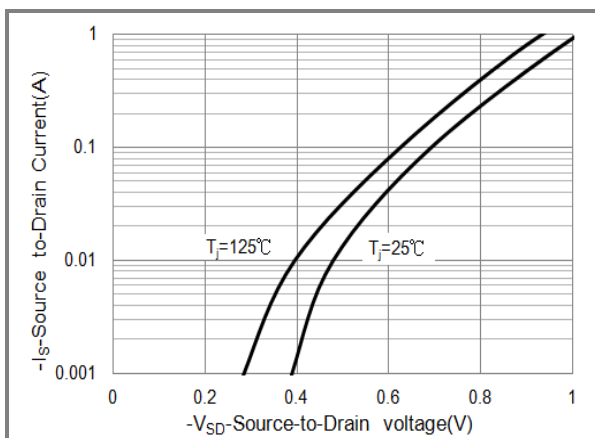


Fig.6 Body Diode Characteristics

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P-Channel TYPICAL CHARACTERISTIC CURVES

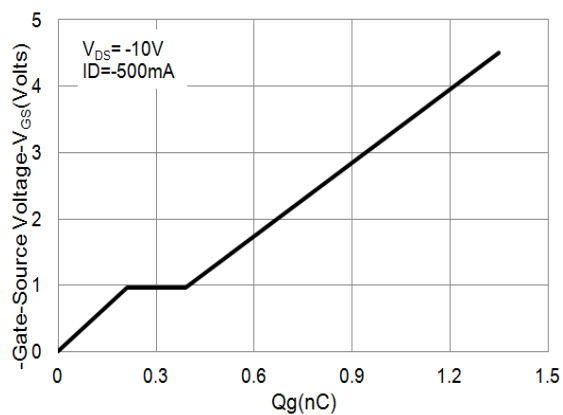


Fig.7 Gate-Charge Characteristics

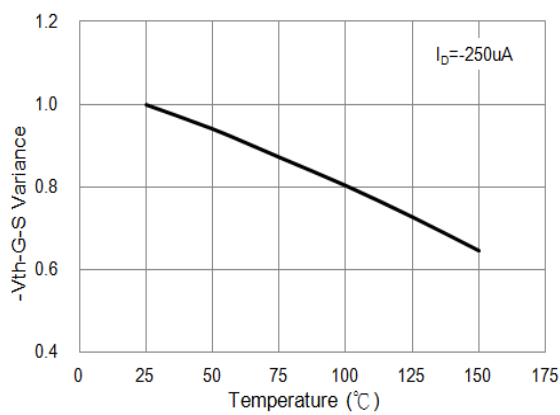


Fig.8 Threshold Voltage Variation with Temperature.

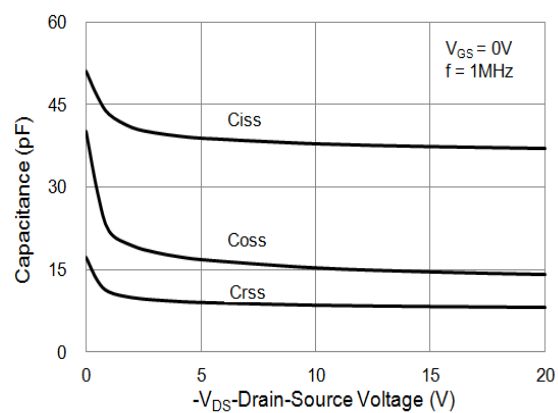


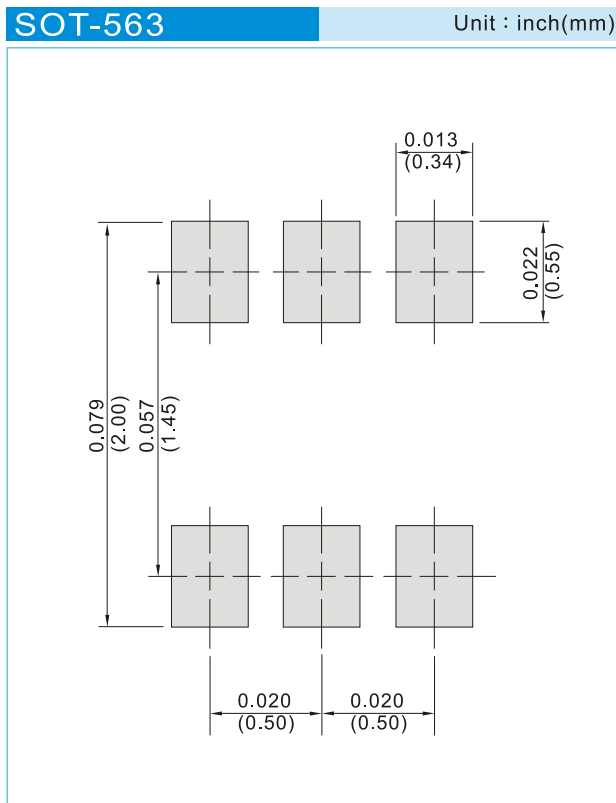
Fig.9 Threshold Voltage Variation with Temperature.

PJX8601

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJX8601_R1_00001	SOT-563	4K pcs / 7" reel	X61	Halogen free

MOUNTING PAD LAYOUT





PJX8601

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