

# PJQ5462A-AU

## 60V N-Channel Enhancement Mode MOSFET

**Voltage**

**60 V**

**Current**

**42 A**

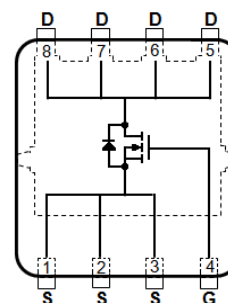
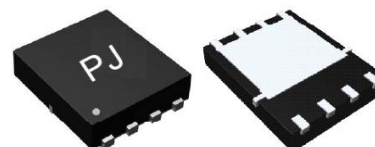
### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@20A<12m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@10A<15m\Omega$
- High switching speed
- Low reverse transfer capacitance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0028 ounces, 0.08 grams

DFN5060-8L



## Maximum Ratings and Thermal Characteristics ( $T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current (Note 4)	$T_C=25^{\circ}C$	$I_D$	42	A
	$T_C=100^{\circ}C$		26	
Pulsed Drain Current (Note 1)	$T_C=25^{\circ}C$	$I_{DM}$	84	
Power Dissipation	$T_C=25^{\circ}C$	$P_D$	71.4	W
	$T_C=100^{\circ}C$		35.7	
Continuous Drain Current (Note 4)	$T_A=25^{\circ}C$	$I_D$	8.5	A
	$T_A=70^{\circ}C$		6.8	
Power Dissipation	$T_A=25^{\circ}C$	$P_D$	2.4	W
	$T_A=70^{\circ}C$		1.6	
Single Pulse Avalanche Energy (Note 6)		$E_{AS}$	72	mJ
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~175	$^{\circ}C$
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	2.1	$^{\circ}C/W$
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature



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## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	1.7	2.5	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V ,I <sub>D</sub> =20A	-	10	12	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	-	11	15	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Dynamic (Note 7)						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V (Note 2,3)	-	40	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	6.0	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	7.2	-	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHZ	-	2142	-	pF
Output Capacitance	C <sub>oss</sub>		-	149	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	86	-	
Turn-On Delay Time	td(on)	V <sub>DD</sub> =15V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V, R <sub>G</sub> =6Ω (Note 2,3)	-	14	-	ns
Turn-On Rise Time	t <sub>r</sub>		-	25	-	
Turn-Off Delay Time	td(off)		-	58	-	
Turn-Off Fall Time	t <sub>f</sub>		-	18	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>	---	-	-	42	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V	-	0.67	1	V

### NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub> = 25°C.
4. The maximum current rating is package limited.
5. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
6. The test condition is L=0.5mH, I<sub>AS</sub>=17A, V<sub>DD</sub>=25V, V<sub>GS</sub>=10V
7. Guaranteed by design, not subject to production testing.

# PJQ5462A-AU

## TYPICAL CHARACTERISTIC CURVES

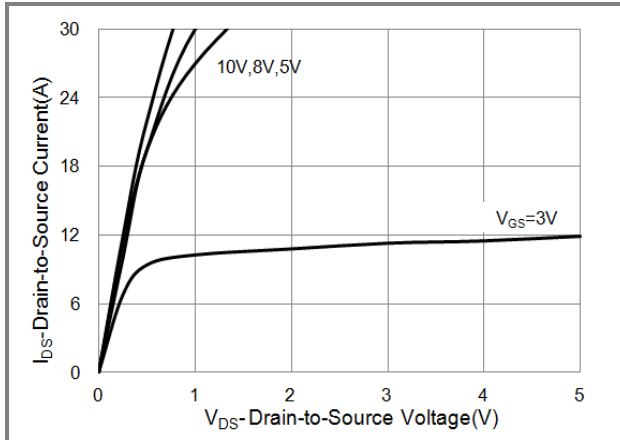


Fig.1 Output Characteristics

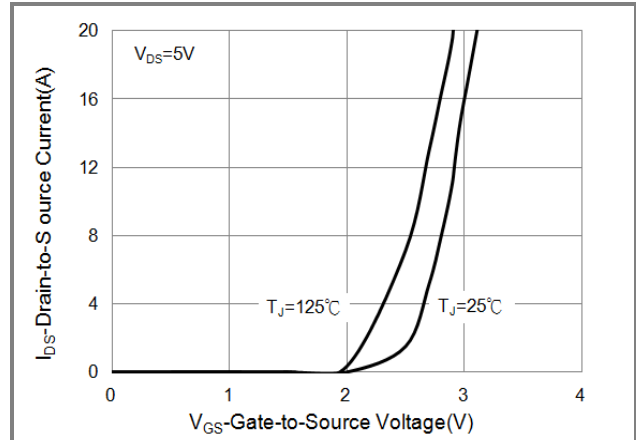


Fig.2 Transfer Characteristics

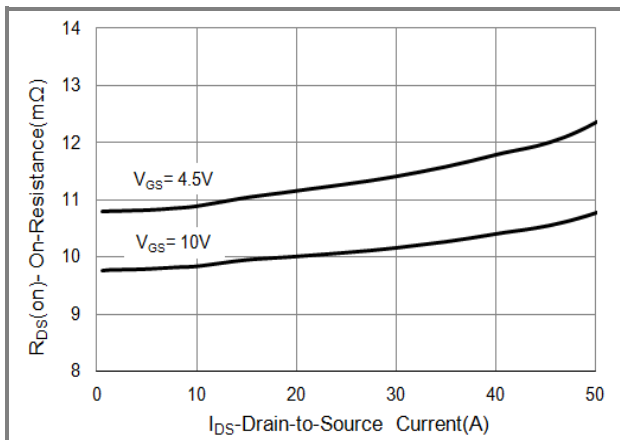


Fig.3 On-Resistance vs. Drain Current

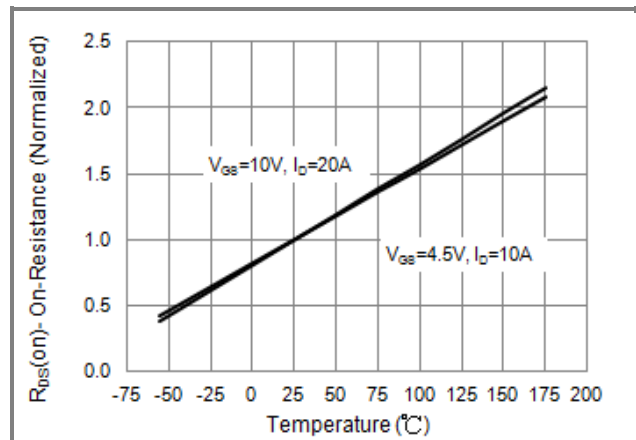


Fig.4 On-Resistance vs. Junction temperature

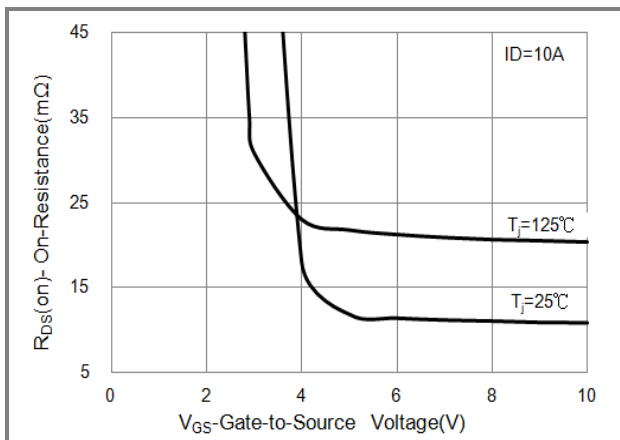


Fig.5 On-Resistance Variation with  $V_{GS}$

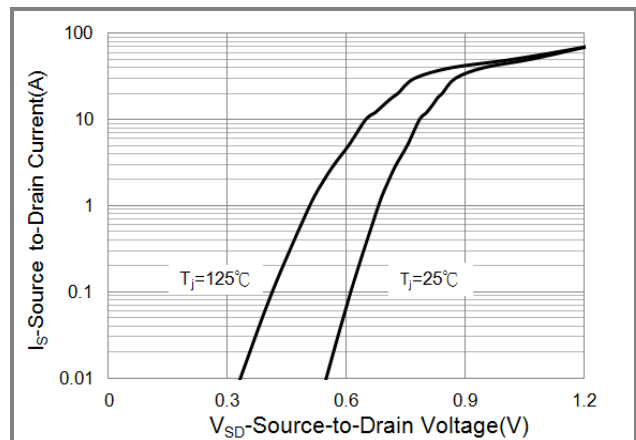


Fig.6 Source-Drain Diode Forward Voltage



## PJQ5462A-AU

### TYPICAL CHARACTERISTIC CURVES

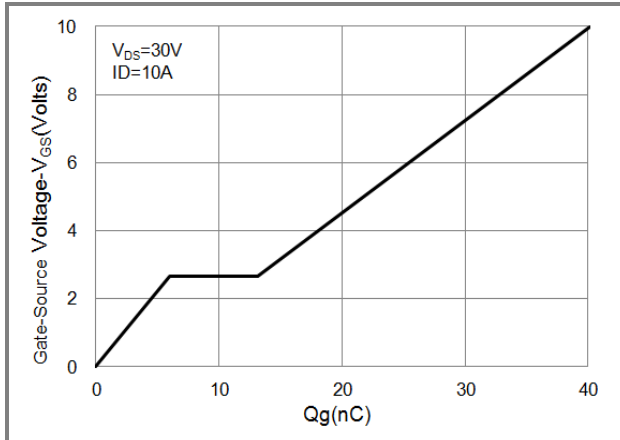


Fig.7 Gate-Charge Characteristics

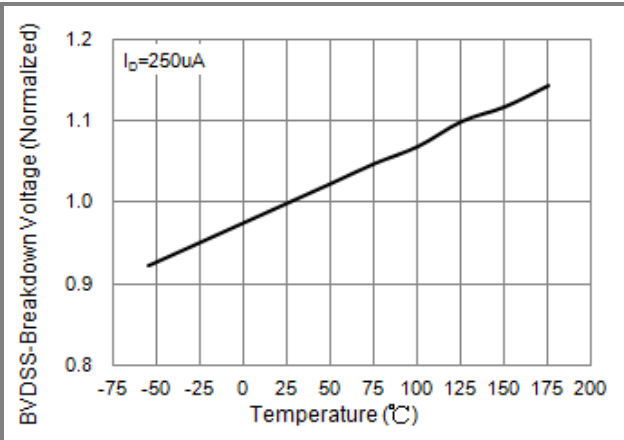


Fig.8 Breakdown Voltage Variation vs. Temperature

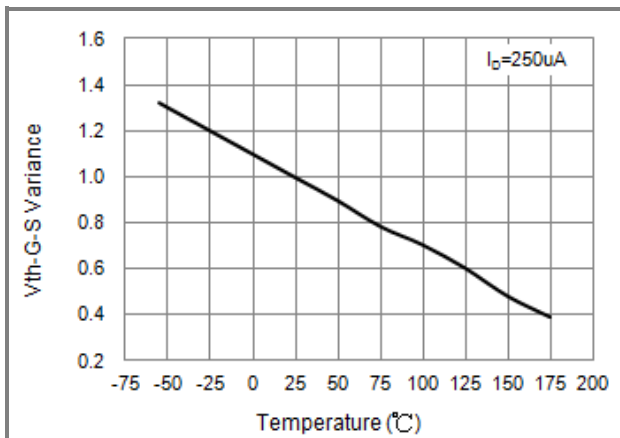


Fig.9 Threshold Voltage Variation with Temperature

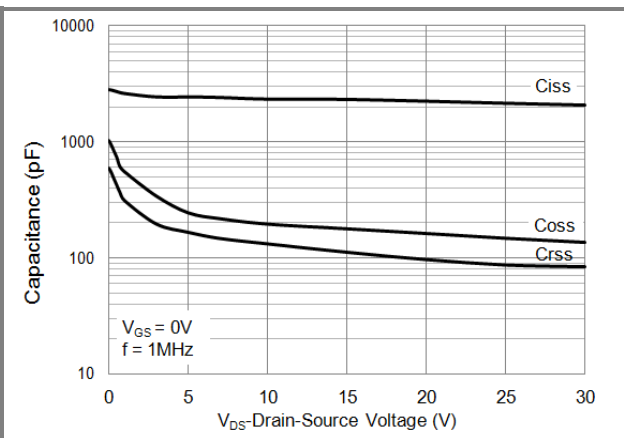


Fig.10 Capacitance vs. Drain-Source Voltage

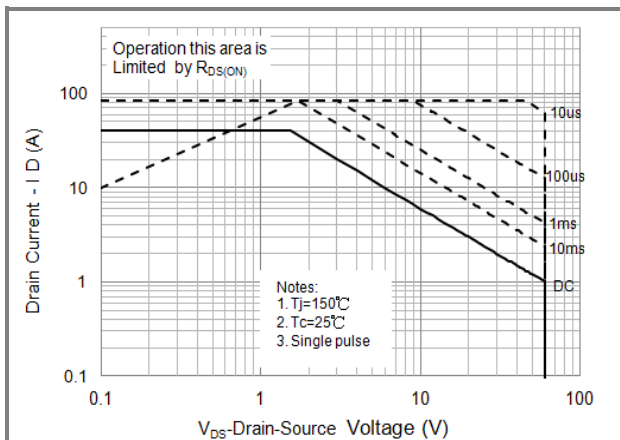


Fig.11 Maximum Safe Operating Area



## PJQ5462A-AU

### TYPICAL CHARACTERISTIC CURVES

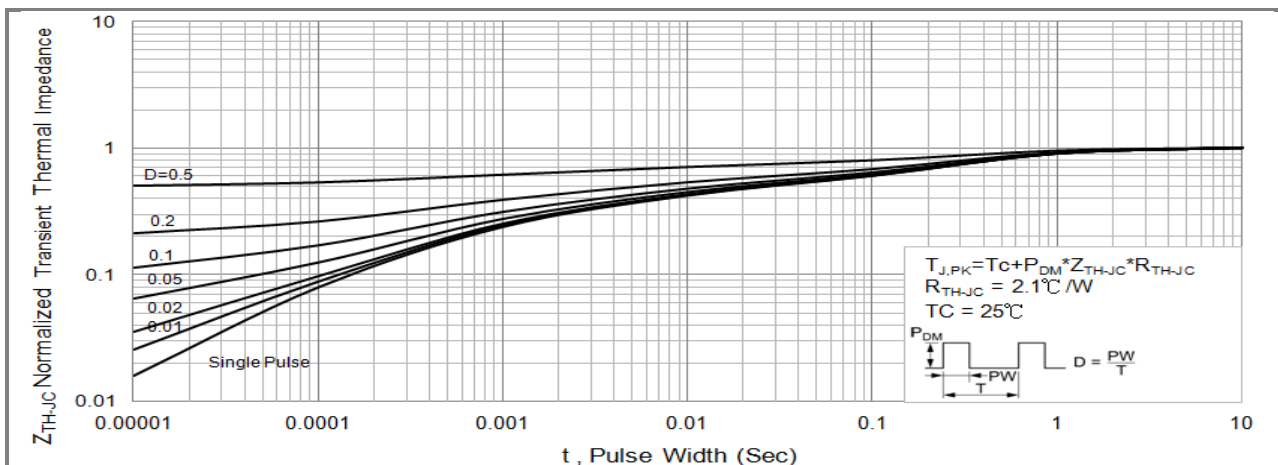


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width

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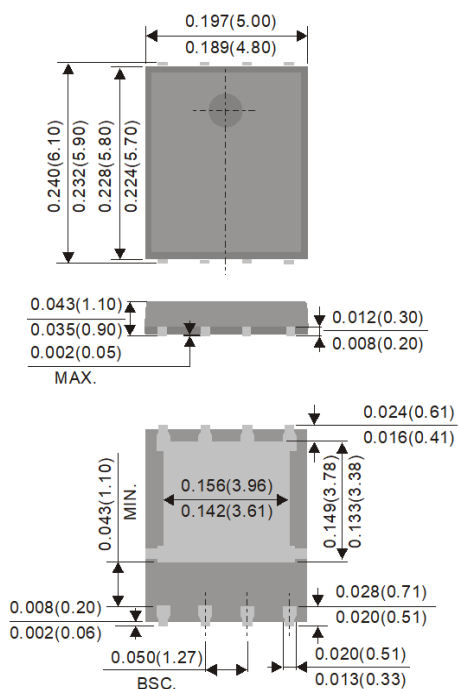
## Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJQ5462A-AU_R2_000A1	DFN5060-8L	3000pcs / 13" reel	Q5462A	Halogen free

## Packaging Information & Mounting Pad Layout

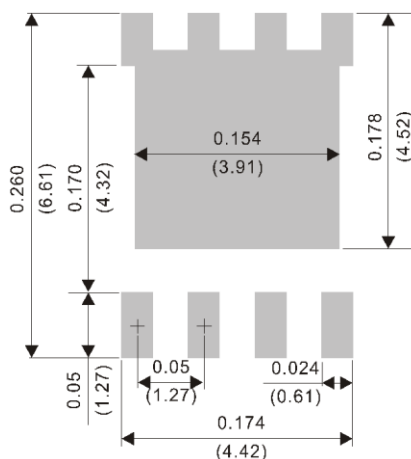
DFN5060-8L Dimension

Unit: inch(mm)



DFN5060-8L Pad Layout

Unit: inch(mm)





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