

100V N-Channel Enhancement Mode MOSFET

Voltage

Current 35 A

DFN3333-8L

Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@15A<25m\Omega$
- R_{DS(ON)}, V_{GS}@4.5V, I_D@10A<28.5mΩ

100 V

- High switching speed
- Improved dv/dt capability
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS	
Drain-Source Voltage		V _{DS}	100		
Gate-Source Voltage		V _{GS}	<u>+</u> 20	V	
Continuous Drain Current ^(Note 4)	Tc=25°C		35	A	
	Tc=100°C	ID	22		
Pulsed Drain Current ^(Note 1)	Tc=25°C	I _{DM}	140		
Power Dissipation	Tc=25°C		62	W	
	Tc=100°C	Po	25		
Continuous Drain Current ^(Note 4)	T _A =25°C		6.3		
	T _A =70°C	lo	5	A	
Power Dissipation	T _A =25°C	D	2.0	W	
	T _A =70°C	Po	1.3		
Single Pulse Avalanche Energy ^(Note 6)		E _{AS}	54	mJ	
Operating Junction and Storage Temperature Range		T _J ,T _{STG}	-55~150	٥C	
Typical Thermal Resistance ^(Note 4,5)	Junction to Case	Rejc	2	°C/W	
	Junction to Ambient	R _{θJA}	62.5		



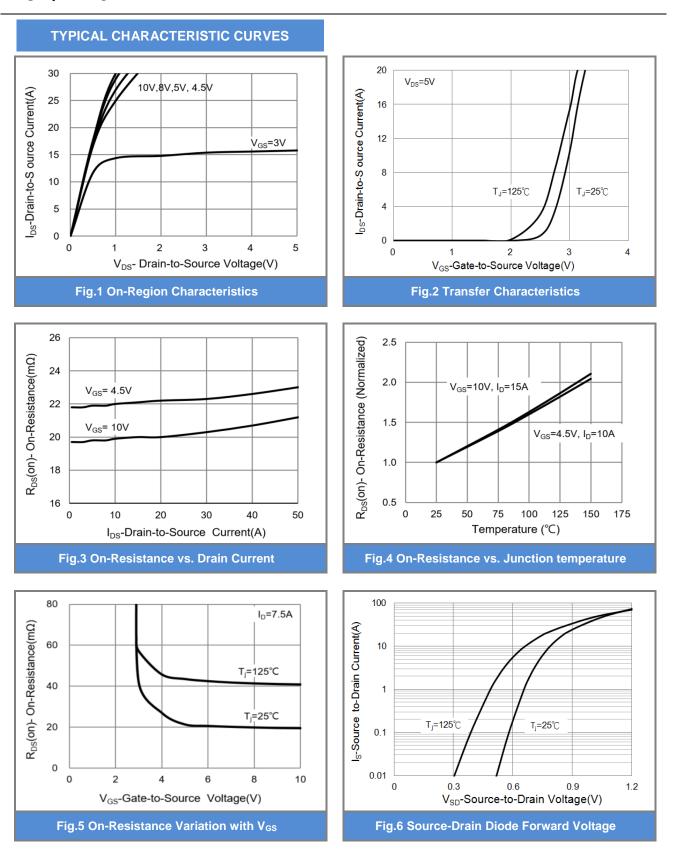
Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	100	-	-	v
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1	1.73	2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =15A	-	20	25	mΩ
		V _{GS} =4.5V, I _D =10A	-	22	28.5	
Zero Gate Voltage Drain Current	IDSS	V _{DS} =80V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	lgss	V _{GS} = <u>+</u> 20V, V _{DS} =0V	-	-	<u>+</u> 100	nA
Dynamic ^(Note 5)		·				
Total Gate Charge	Qg	V _{DS} =50V, I _D =10A, V _{GS} =10V ^(Note 2,3)	-	31	-	nC
Gate-Source Charge	Q _{gs}		-	5.1	-	
Gate-Drain Charge	Q_{gd}		-	7.3	-	
Input Capacitance	Ciss	V _{DS} =30V, V _{GS} =0V,	-	1519	-	pF
Output Capacitance	Coss		-	132	-	
Reverse Transfer Capacitance	Crss	f=1MHZ	-	66	-	
Turn-On Delay Time	td _(on)	V _{DD} =50V, I _D =10A, V _{GS} =10V,	-	11	-	ns
Turn-On Rise Time	tr		-	42	-	
Turn-Off Delay Time	td _(off)		-	40	-	
Turn-Off Fall Time	t _f	$R_G=3\Omega^{(Note 2,3)}$	-	19	-	
Drain-Source Diode						
Maximum Continuous Drain-Source			-	-	35	А
Diode Forward Current	I _S					
Reverse Recovery Time	V_{SD}	Is=1A, V _{GS} =0V	-	0.68	1.2	V

NOTES :

- 1. Pulse width <300us, Duty cycle <2%.
- 2. Essentially independent of operating temperature typical characteristics.
- 3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150$ °C. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25$ °C.
- 4. The maximum current rating is package limited.
- 5. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 6. The test condition is L=3mH, I_{AS} =6A, V_{DD} =50V, V_{GS} =10V, Starting T_J=25°C.
- 7. Guaranteed by design, not subject to production testing.







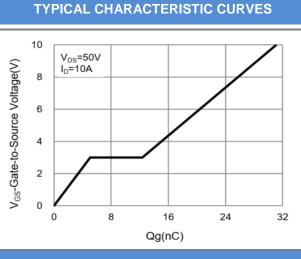
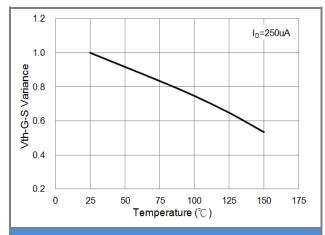
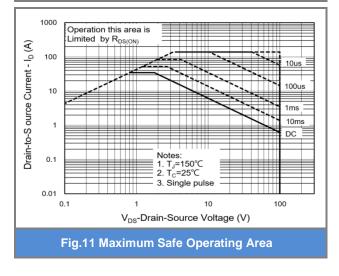
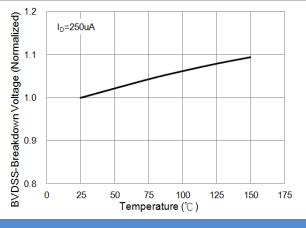


Fig.7 Gate-Charge Characteristics

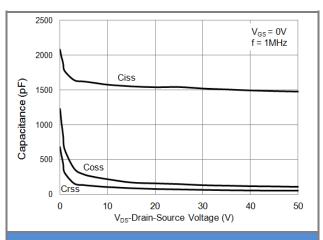


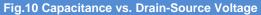


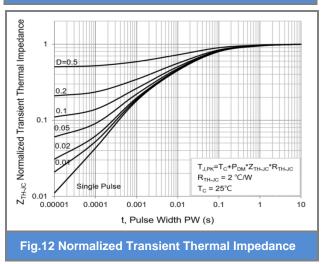










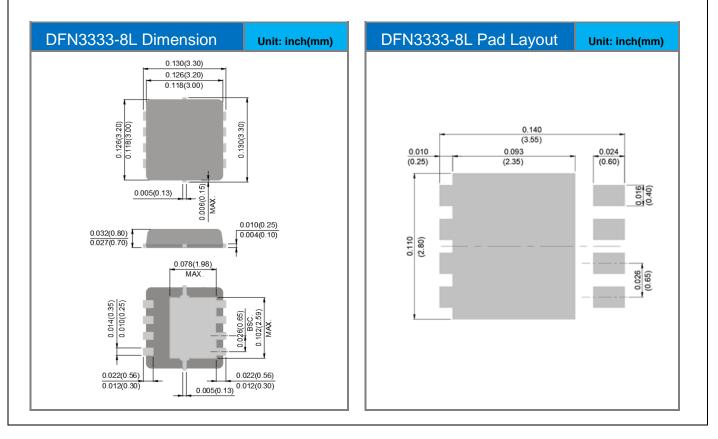




Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJQ4476AP_R2_00001	DFN3333-8L	5K pcs / 13" reel	4476	Halogen free RoHS compliant

Packaging Information & Mounting Pad Layout





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