

PJQ4460AP-AU

60V N-Channel Enhancement Mode MOSFET

Voltage

60 V

Current

11 A

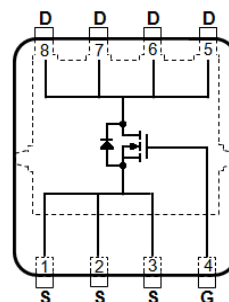
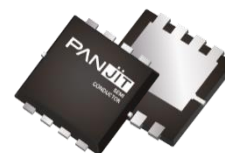
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@6A<72m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@3A<88m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams

DFN3333-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 4)	$T_C=25^\circ\text{C}$	I_D	11	A
	$T_C=100^\circ\text{C}$		7	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	44	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	23.8	W
	$T_C=100^\circ\text{C}$		11.9	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ\text{C}$	I_D	3.7	A
	$T_A=70^\circ\text{C}$		2.9	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.4	W
	$T_A=70^\circ\text{C}$		1.6	
Single Pulse Avalanche Energy ^(Note 6)		E_{AS}	25	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ\text{C}$
Typical Thermal Resistance ^(Note 4,5)	Junction to Case	$R_{\theta JC}$	6.3	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	60	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1	1.8	2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =6A	-	53	72	mΩ
		V _{GS} =4.5V, I _D =3A	-	61	88	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic ^(Note 7)						
Total Gate Charge	Q _g	V _{DS} =48V, I _D =6A, V _{GS} =10V ^(Note 1,2)	-	9.3	-	nC
Gate-Source Charge	Q _{gs}		-	2.2	-	
Gate-Drain Charge	Q _{gd}		-	1.9	-	
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ	-	509	-	pF
Output Capacitance	C _{oss}		-	47	-	
Reverse Transfer Capacitance	C _{rss}		-	23	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} =30V, I _D =1A, V _{GS} =10V, R _G =3.3Ω ^(Note 1,2)	-	3.2	-	ns
Turn-On Rise Time	t _r		-	9.7	-	
Turn-Off Delay Time	t _{d(off)}		-	18.5	-	
Turn-Off Fall Time	t _f		-	6.4	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	11	A
Reverse Recovery Time	V _{SD}	I _S =1A, V _{GS} =0V	-	0.75	1	V

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
4. The maximum current rating is package limited.
5. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. The test condition is L=1mH, I_{AS}=7A, V_{DD}=25V, V_{GS}=10V, Starting T_J=25°C.
7. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

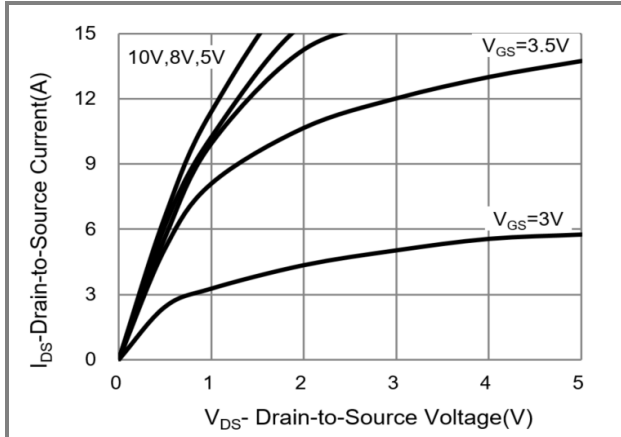


Fig.1 On-Region Characteristics

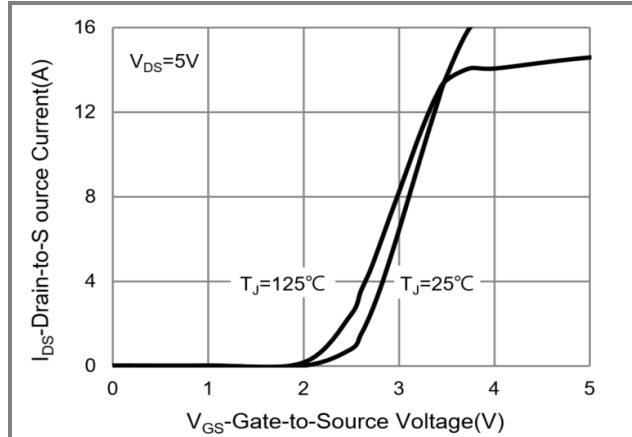


Fig.2 Transfer Characteristics

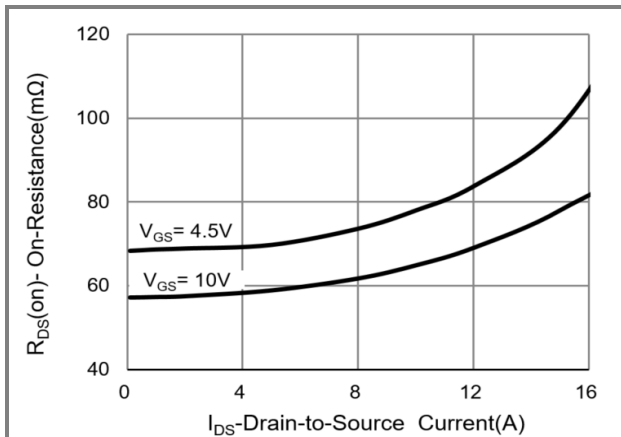


Fig.3 On-Resistance vs. Drain Current

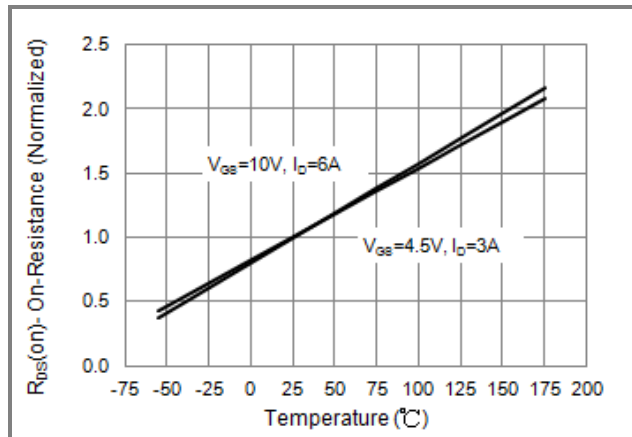


Fig.4 On-Resistance vs. Junction temperature

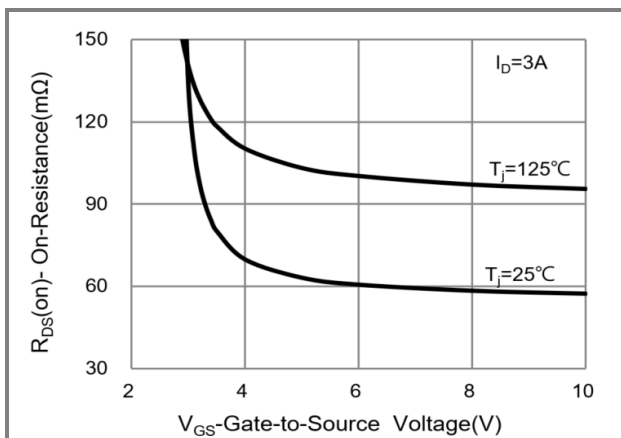


Fig.5 On-Resistance Variation with V_{GS}

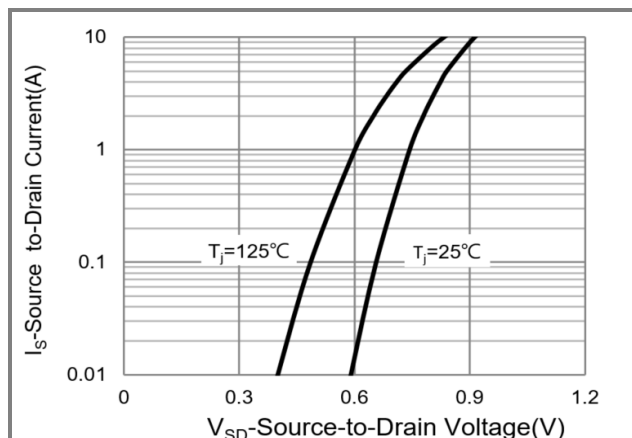


Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

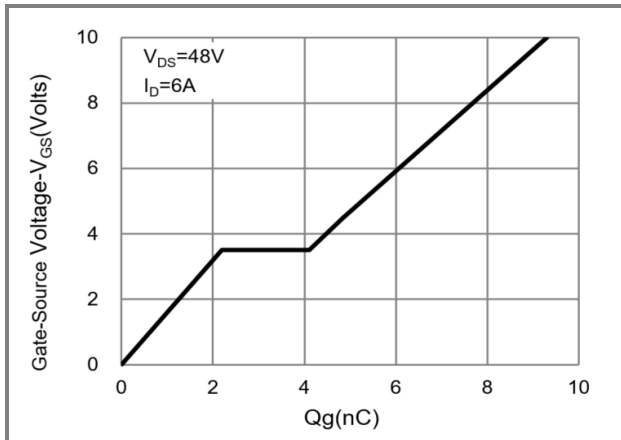


Fig.7 Gate-Charge Characteristics

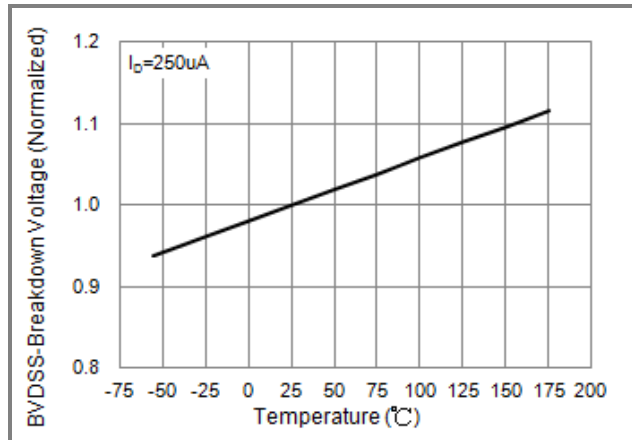


Fig.8 Breakdown Voltage Variation vs. Temperature

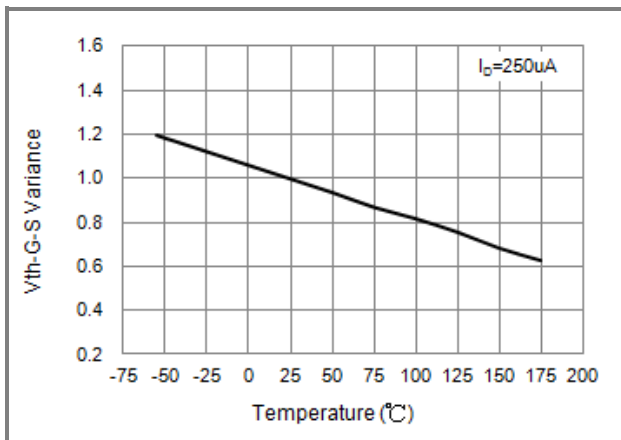


Fig.9 Threshold Voltage Variation with Temperature

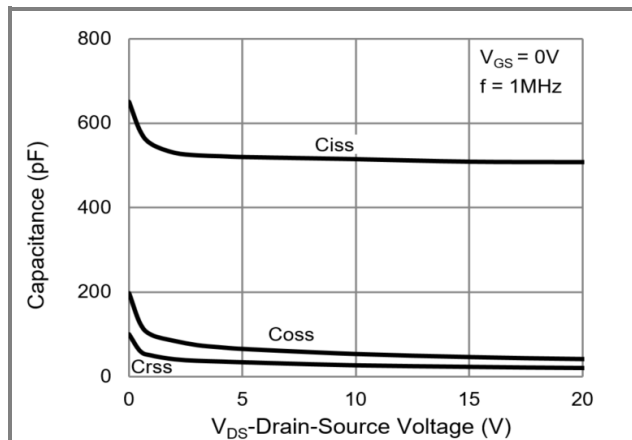


Fig.10 Capacitance vs. Drain-Source Voltage

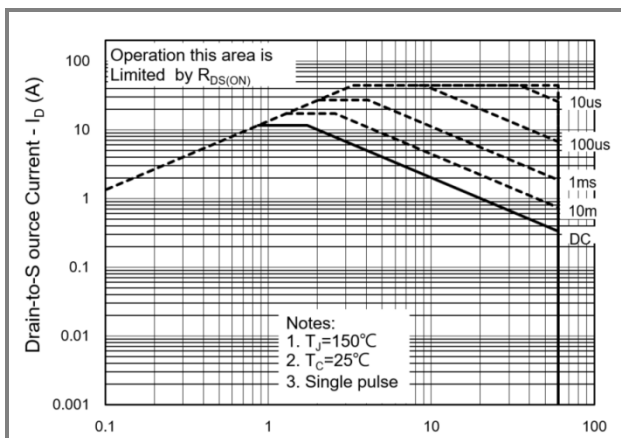


Fig.11 Maximum Safe Operating Area

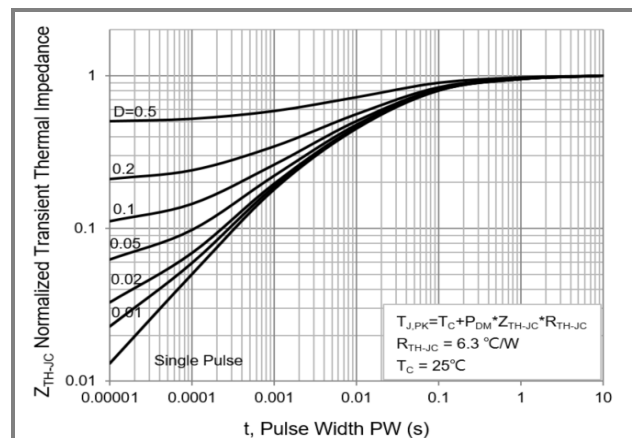


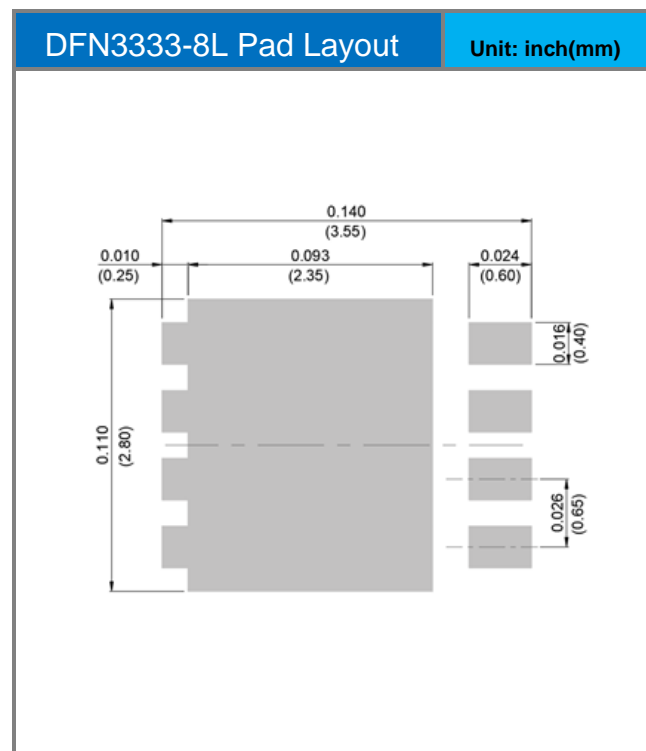
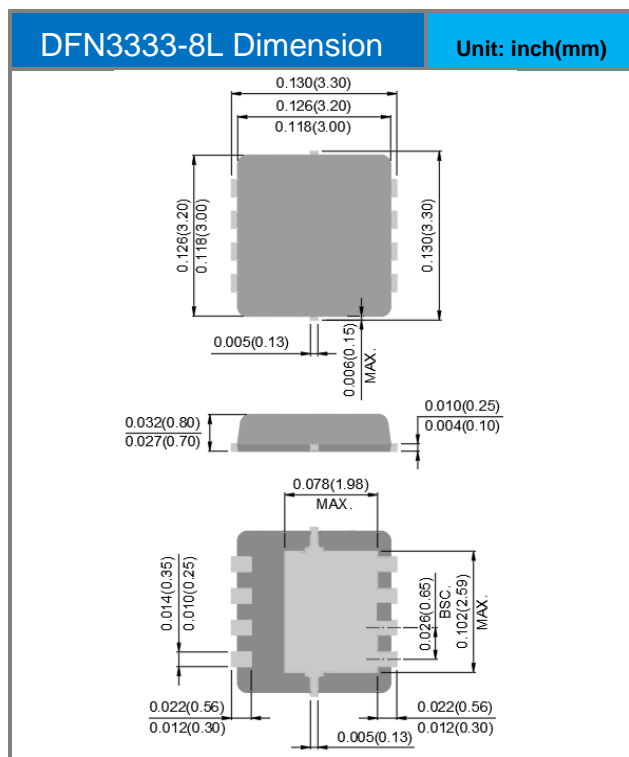
Fig.12 Normalized Transient Thermal Impedance

PJQ4460AP-AU

Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJQ4460AP-AU_R2_000A1	DFN3333-8L	5K pcs / 13" reel	4460	Halogen free RoHS compliant

Packaging Information & Mounting Pad Layout



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