

PJQ4443P-AU

40V P-Channel Enhancement Mode MOSFET

Voltage

-40 V

Current

-46 A

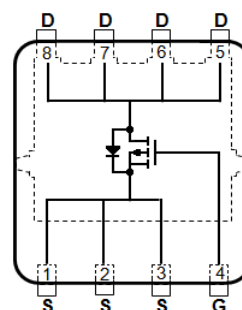
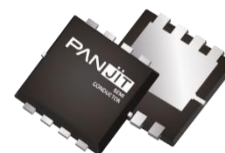
Features

- $R_{DS(ON)}$, $V_{GS}@-10V$, $I_D@-10A<12m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-8A<17.5m\Omega$
- High switching speed
- Improved dv/dt capability
- Low gate charge
- Low reverse transfer capacitance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams

DFN3333-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 4)	$T_C=25^{\circ}C$	I_D	-46	A
	$T_C=100^{\circ}C$		-29	
Pulsed Drain Current ^(Note 1)	$T_C=25^{\circ}C$	I_{DM}	-166	
Power Dissipation	$T_C=25^{\circ}C$	P_D	59.5	W
	$T_C=100^{\circ}C$		23	
Continuous Drain Current ^(Note 4)	$T_A=25^{\circ}C$	I_D	-8.8	A
	$T_A=70^{\circ}C$		-7.1	
Power Dissipation	$T_A=25^{\circ}C$	P_D	2.1	W
	$T_A=70^{\circ}C$		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^{\circ}C$
Typical Thermal Resistance ^(Note 4,5)	Junction to Case	$R_{\theta JC}$	2.1	$^{\circ}C/W$
	Junction to Ambient	$R_{\theta JA}$	59.5	

- Limited only By Maximum Junction Temperature

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-40	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1	-1.52	-2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-10A	-	10	12	mΩ
		V _{GS} =-4.5V, I _D =-8A	-	13.5	17.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic ^(Note 6)						
Total Gate Charge	Q _g	V _{DS} =-32V, I _D =-10A, V _{GS} =-4.5V ^(Note 2,3)	-	23	-	nC
Gate-Source Charge	Q _{gs}		-	8.5	-	
Gate-Drain Charge	Q _{gd}		-	9	-	
Input Capacitance	C _{iss}	V _{DS} =-25V, V _{GS} =0V, f=1MHZ	-	2767	-	pF
Output Capacitance	C _{oss}		-	247	-	
Reverse Transfer Capacitance	C _{rss}		-	139	-	
Turn-On Delay Time	t _{d(on)}	V _{DS} =-20V, I _D =-1A, V _{GS} =-10V, R _G =6Ω ^(Note 2,3)	-	23	-	ns
Turn-On Rise Time	t _r		-	10	-	
Turn-Off Delay Time	t _{d(off)}		-	135	-	
Turn-Off Fall Time	t _f		-	50	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	-46	A
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V	-	-0.7	-1	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
4. The maximum current rating is package limited.
5. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

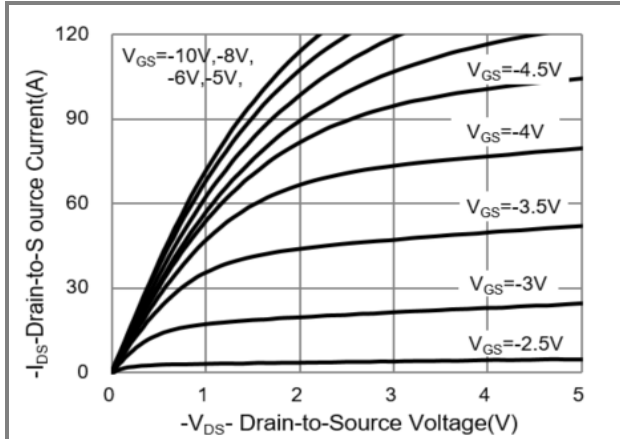


Fig.1 On-Region Characteristics

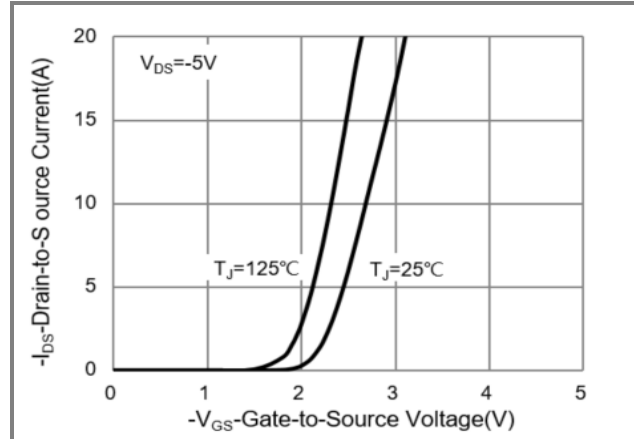


Fig.2 Transfer Characteristics

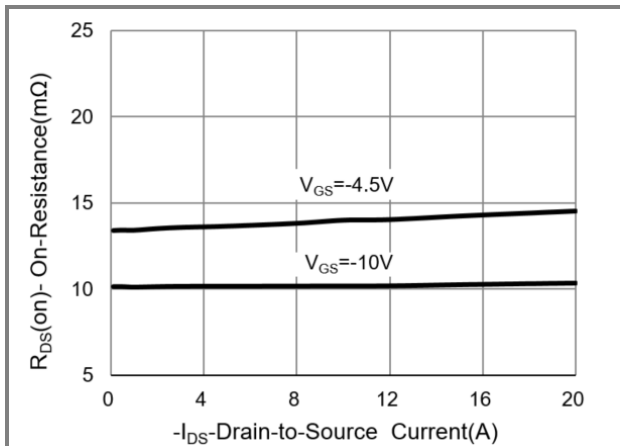


Fig.3 On-Resistance vs. Drain Current

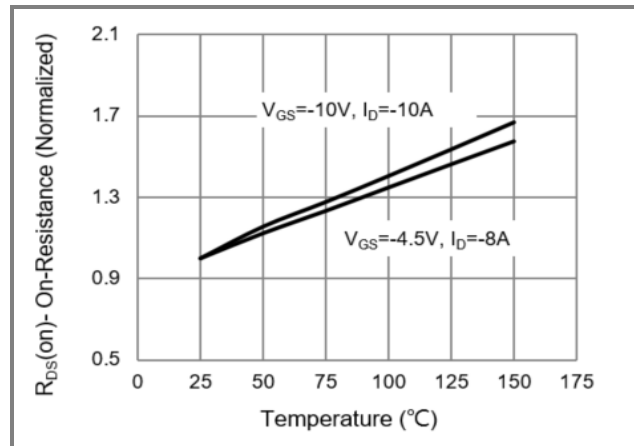


Fig.4 On-Resistance vs. Junction temperature

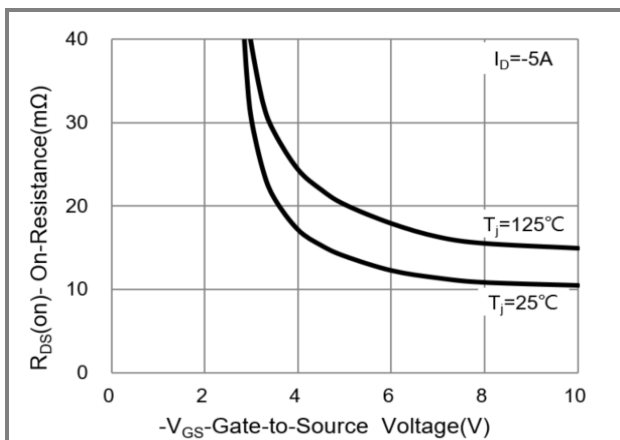


Fig.5 On-Resistance Variation with V_{GS}

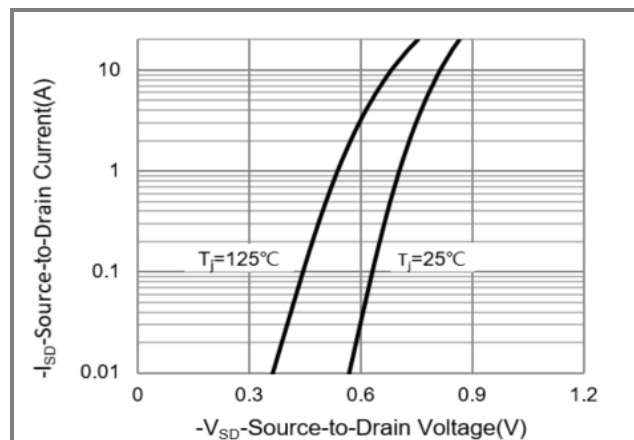
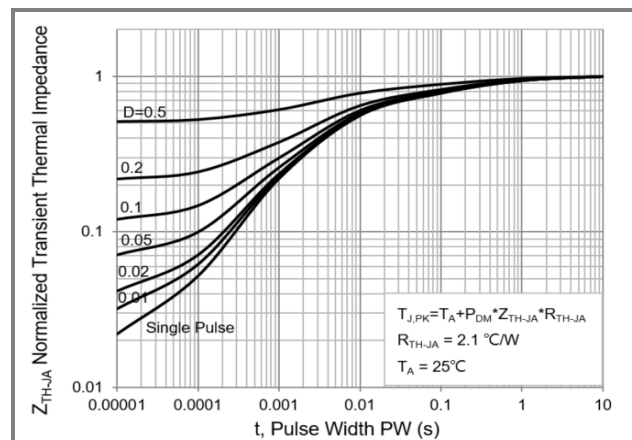
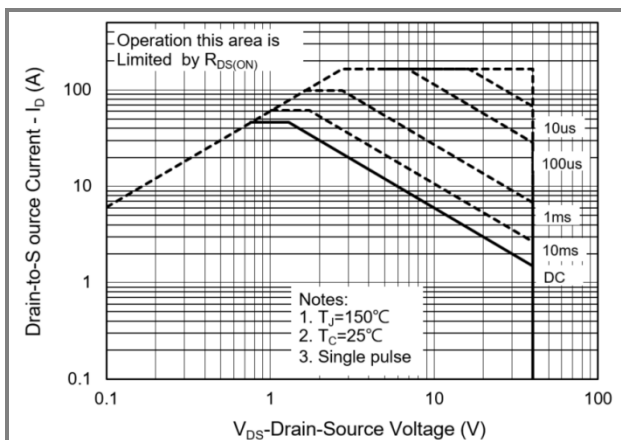
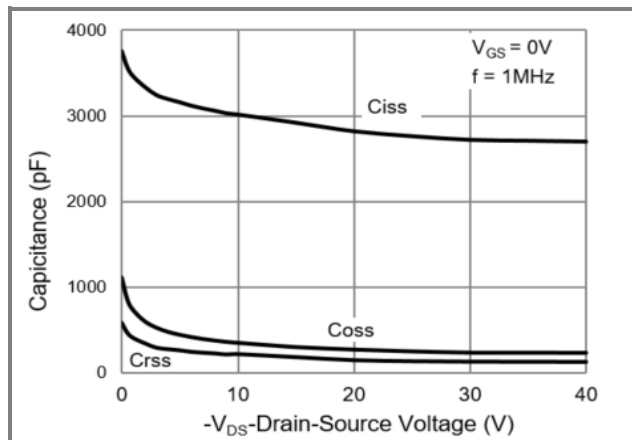
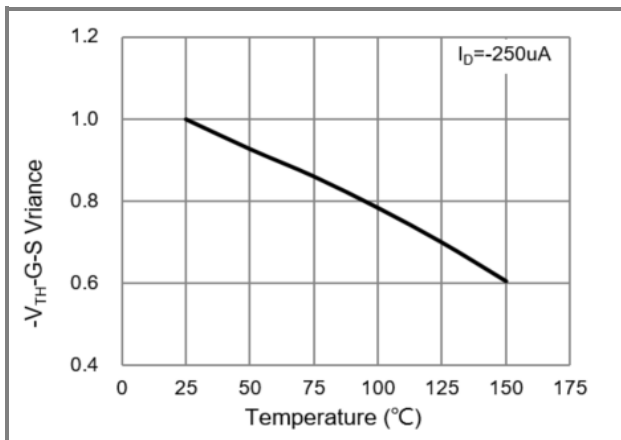
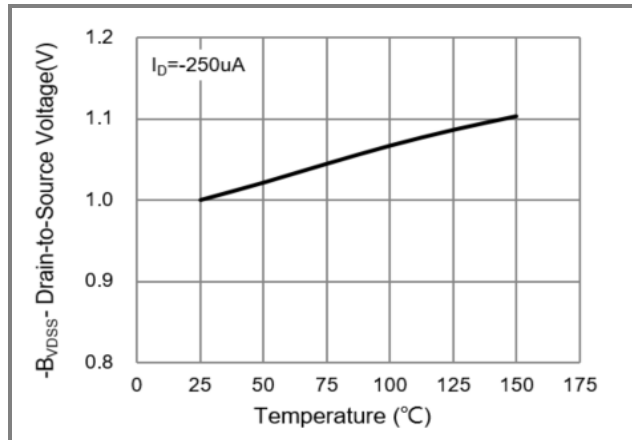
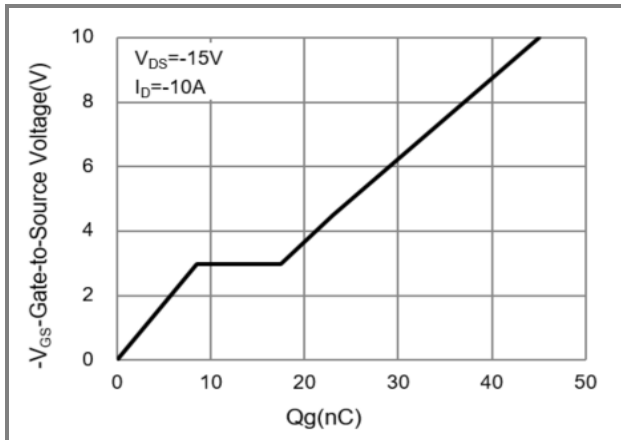


Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

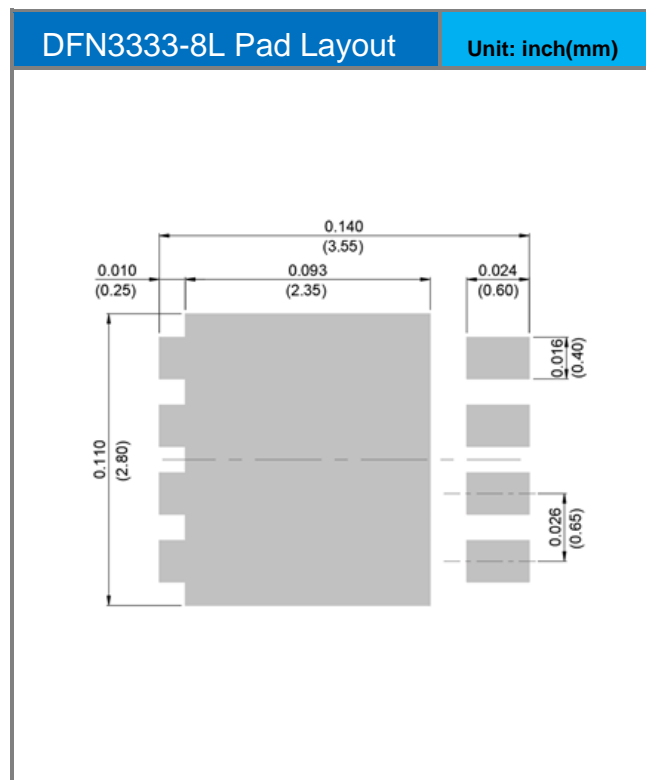
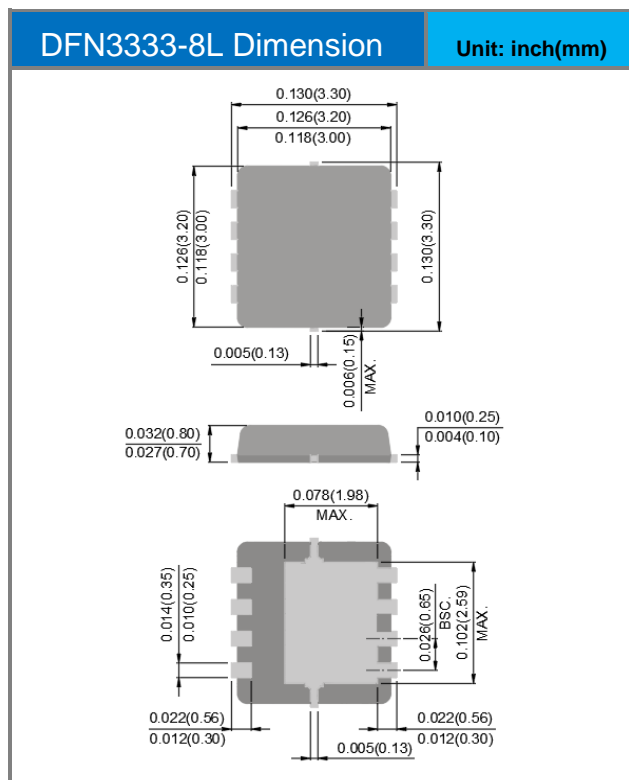


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Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJQ4443P-AU_R2_000A1	DFN3333-8L	5K pcs / 13" reel	4443	Halogen free RoHS compliant

Packaging Information & Mounting Pad Layout



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